Z87300

CMOS Z8
CONSUMER CONTROLLER PROCESSOR

FEATURES

Device	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z87300	4	237	12, 16

Note: *General-Purpose

- 28-Pin DIP, 28-Pin SOIC Packages
- 3.0V to 5.5V Operating Range
- Low-Power Consumption
- 0°C to -70°C Operating Range
- Expanded Register File (ERF)
- 24 Input/Output Lines
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer/Power-On Reset
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z87300 Consumer Controller Processors (CCP) are members of the single-chip Z8® MCU family with enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. These enhancements result in a more efficient, cost effective design and provide the user with increased design flexibility over the standard Z8 microprocessor core. This low-power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z87300 features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available support this wide range of configurations: Program Memory, Register File, Data Memory, and ERF. The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The ERF consists of three control registers.

For applications demanding powerful I/O capabilities, the Z87300's provides 24 pins dedicated to input and output. These lines are configurable under software control to provide timing, status signals, or parallel I/O.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z87300 offers two on-chip counter/timers with a large number of user-selectable modes.

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

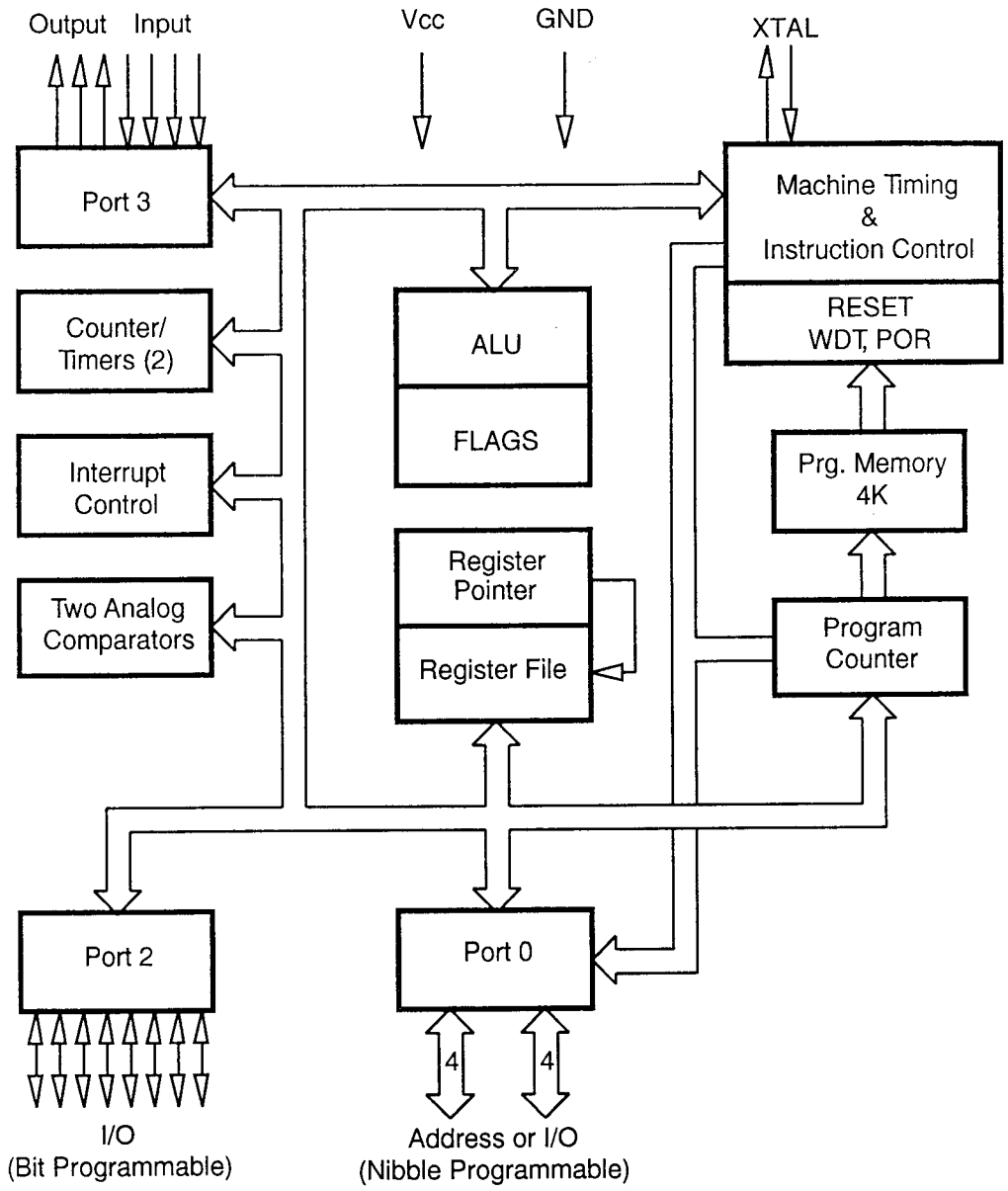

Figure 1. Functional Block Diagram

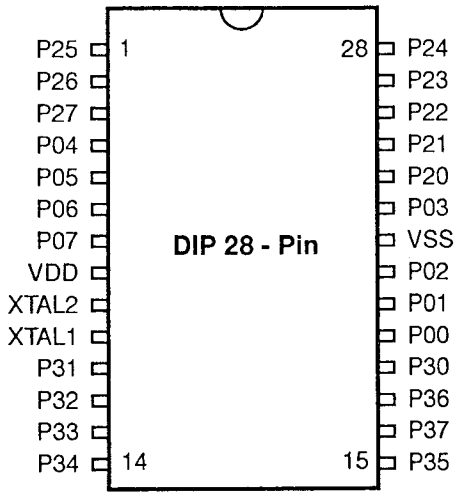

Figure 2. 28-Pin DIP Pin Configuration

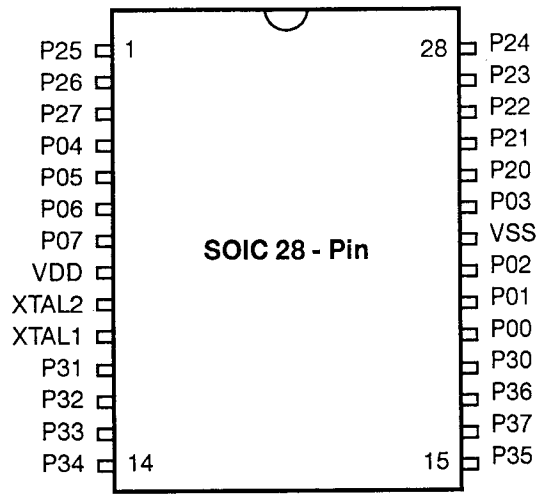

Figure 3. 28-Pin SOIC Pin Configuration

Table 1. 28-Pin DIP/SOIC/PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-3	P27-25	Port 2, Pins 5,6,7	In/Output
4-7	P07-04	Port 0, Pins 4,5,6,7	In/Output
8	V_{DD}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P33-31	Port 3, Pins 1,2,3	Fixed Input
14-15	P35-4	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P02-00	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P24-20	Port 2, Pins 0,1,2,3,4	In/Output

ABSOLUTE MAXIMUM RATINGS

Sym	Description	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp			C
	Power Dissipation		2.2	W

Note: *Voltage on all pins with respect to GND.
See ordering information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 4).

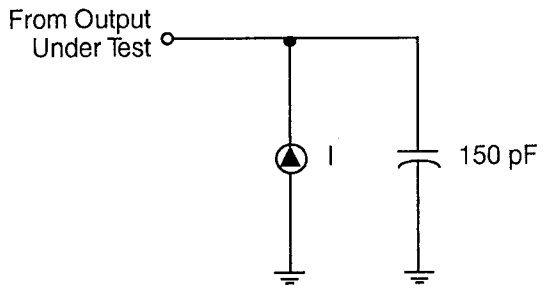

Figure 4. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
	Max Input Voltage	3.0V		7		V	I_{IN} <250µA	
		5.5V		7			I_{IN} <250µA	
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.8	V	Driven by External Clock	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.6	V	Generator Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	1.2	V	Driven by External Clock	
		5.5V	GND-0.3	0.2 V_{CC}	2.1	V	Generator Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.6	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V_{CC}	1.6	V		
V_{OH1}	Output High Voltage	3.0V	V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I_{OL} = +4.0 mA	8
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.0V		1.2	0.3	V	I_{OL} = +6 mA	8
		5.5V		1.2	0.4	V	I_{OL} = +12 mA	8
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	1.8	V		13
		5.5V	.8 V_{CC}	V_{CC}	2.6	V		13
V_{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	1.1	V		13
		5.5V	GND-0.3	0.2 V_{CC}	1.6	V		13
V_{OLR}	Reset Output Low Voltage	3.0V		0.6	0.3	V	I_{OL} = +1.0 mA	13
		5.5V		0.6	0.3	V	I_{OL} = +1.0 mA	13
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25	10	mV		10
		5.5V		25	10	mV		10
I_{IL}	Input Leakage	3.0V	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	-1	1	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	0.004	µA	V_{IN} = 0V, V_{CC}	
IIR	Reset Input Current	3.0V	-20	-130	-60	µA		
		5.5V	-20	-180	-85	µA		
I_{CC}	Supply Current	3.0V		20	7	mA	@ 16 MHz	4
		5.5V		25	20	mA	@ 16 MHz	4
		3.0V		15	5	mA	@ 12 MHz	4
		5.5V		20	15	mA	@ 12 MHz	4

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	6,11
		5.5V		10	4	µA	V_{IN} = 0V, V_{CC} WDT is not Running	6, 11
		3.0V		500	310	µA	V_{IN} = 0V, V_{CC} WDT is t Running	6, 11, 14
		5.5V		800	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	6, 11, 14
V_{ICR}	Input Common Mode Voltage Range	3.0V	0	V_{CC}-1.0V		V		10
		5.5V	0	V_{CC}-1.0V		V		10
I_{ALL}	Auto Latch Low Current	3.0V	0.7	8	3	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	1.4	15	5	µA	$0V < V_{IN} < V_{CC}$	9
I_{ALH}	Auto Latch High Current	3.0V	-0.6	-5	-3	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	-1.0	-8	-6	µA	$0V < V_{IN} < V_{CC}$	9
V_{LV}	V_{CC} Low Voltage				2.8	V	4 MHz max Int. CLK Freq.	7,14
	Protection Voltage		2.2	3.1	2.8		6 MHz max Int. CLK Freq.	7,15
V_{OH}	Output High Voltage (Low EMI Mode)	3.0V	V_{CC}-0.4		3.1	V	I_{OH} = -0.5 mA	
		5.0V	V_{CC}-0.4		4.8	V	I_{OH} = -0.5 mA	
V_{OL}	Output Low Voltage (Low EMI Mode)	3.0V		0.6	0.0.1	V	I_{OL} = 1.0 mA	
		5.0V		0.4		V	I_{OL} = 1.0 mA	

Notes:

1. Typicals are at V_{CC} = 5.0V and 3.3V.
2. GND = 0V
3. All outputs unloaded, I/O pins floating, inputs at rail.
4. CL1 = CL2 = 10 pF.
5. Same as note [4] except inputs at V_{CC}.
6. The V_{LV} voltage increases as the temperature decreases and will overlap lower V_{CC} operating region.
7. Standard Mode (not Low EMI).
8. Auto Latch (Mask Option) selected.
9. For analog comparator, inputs when analog comparators are enabled.
10. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
11. Excludes clock pins.
12. Typicals are at V_{CC} = 5.0V.
13. Internal RC selected

External I/O or Memory Read and Write Timing Table (C43 Only)

(SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	Note [3]	T_A=–0°C to 70°C 12 MHz		16 MHz		Units	Notes
			V_{CC}	Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS Rise Delay	3.0	35		25		ns	2
			5.5	35		25		ns	
2	TdAS(A)	/AS Rise to Address Float Delay	3.0	45		35		ns	2
			5.5	45		35		ns	
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	3.0		250		180	ns	1,2
			5.5		250		180	ns	
4	TwAS	/AS Low Width	3.0	55		40		ns	2
			5.5	55		40		ns	
5	TdAS(DS)	Address Float to /DS Fall	3.0	0		0		ns	
			5.5	0		0		ns	
6	TwDSR	/DS (Read) Low Width	3.0	200		135		ns	1,2
			5.5	200		135		ns	
7	TwDSW	/DS (Write) Low Width	3.0	110		80		ns	1,2
			5.5	110		80		ns	
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	3.0		150		75	ns	1,2
			5.5		150		75	ns	
9	ThDR(DS)	Read Data to /DS Rise Hold Time	3.0	0		0		ns	2
			5.5	0		0		ns	
10	TdDS(A)	/DS Rise to Address Active Delay	3.0	45		50		ns	2
			5.5	55		50		ns	
11	TdDS(AS)	/DS Rise to /AS Fall Delay	3.0	30		35		ns	2
			5.5	45		35		ns	
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	3.0	45		25		ns	2
			5.5	45		25		ns	
13	TdDS(R/W)	/DS Rise to R//W Not Valid	3.0	45		35		ns	2
			5.5	45		35		ns	
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	3.0	55		25		ns	2
			5.5	55		25		ns	
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	3.0	45		35		ns	[2
			5.5	45		35		ns	
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.0		310		230	ns	1,2
			5.5		310		230	ns	
17	TdAS(DS)	/AS Rise to /DS Fall Delay	3.0	65		45		ns	2
			5.5	65		45		ns	
18	TdDM(AS)	/DM Valid to /AS Fall Delay	3.0	35		30		ns	2
			5.5	35		30		ns	
			5.5	45		35		ns	
20	ThDS(AS)	/DS Valid to Address Valid Hold Time	3.0	45		35		ns	
			5.5	45		35		ns	

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

AC CHARACTERISTICS

Additional Timing Diagram

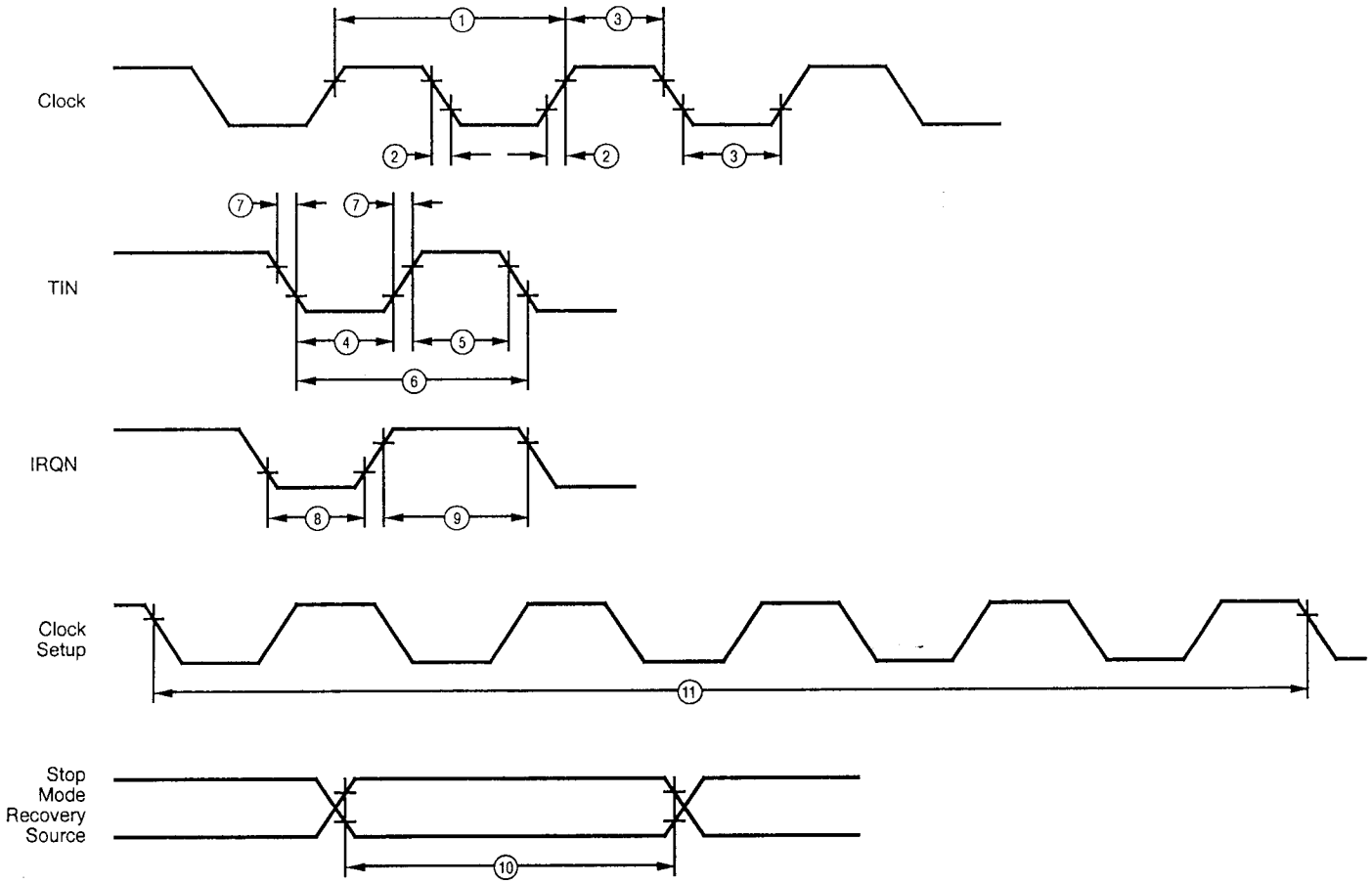

Figure 5. Additional Timing

Additional Timing Table (SCLK/TCLK = XTAL/2)

				T_A = 0°C to +70°C					
			V_{CC}	12 MHz		16 MHz			
No	Symbol	Parameter	Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	ns	1,7
			5.5V	83	DC	62.5	DC	ns	1,7
			3.0V	250	DC	250	DC	ns	1,8
			5.5V	250	DC	250	DC	ns	1,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		15		15	ns	1
			5.5V		15		15	ns	1
3	TwC	Input Clock Width	3.0V	41		31		ns	1
			5.5V	41		31		ns	1
			3.0V	125		125		ns	1,8
			5.5V	125		125		ns	1,8
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin,	Timer Input Rise & Fall Timer	3.0V		100		100	ns	1
			5.5V		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC			1,3
			5.5V	5TpC		5TpC			1,3
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC			1,2
			5.5V	5TpC		5TpC			1,2
10	Twsm	STOP Mode Recovery Width Spec	3.0V	12		12		ns	
			5.5V	12		12		ns	
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		4
			5.5V		5TpC		5TpC		4
									D1, D0
12	Twdt	Watch-Dog Timer Delay Time before time-out	3.0V	7		7		ms	0, 0 [5]
			5.5V	3.5		3.5		ms	0, 0 [5]
			3.0V	14		14		ms	0, 0 [5]
			5.5V	7		7		ms	0, 0 [5]
			3.0V	28		28		ms	0, 0 [5]
			5.5V	14		14		ms	0, 0 [5]
			3.0V	112		112		ms	0, 0 [5]
			5.5V	56		56		ms	0, 0 [5]]
13	TPOR	Power-On Reset Delay	3.0V	3	24	3	24	ms	
			5.5v	1.5	13	1.5	13	ms	

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 0.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. Standard Oscillator mode, Pcon RegD7=1.
8. Maximum frequency for external XTAL Clock is 4MHz when using low EMI oscillator mode, Pcon Reg D7=0.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = XTAL)

				T_A = 0°C to +70°C 8 MHz			
			V_{CC}				
No	Symbol	Parameter	Note [6]	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	ns	1,7,8
			5.5V	250	DC	ns	1,7,8
			3.0v	125	DC	ns	1,7
			5.5V	125	DC	ns	1,7
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		25	ns	1,7
			5.5V		25	ns	1,7
3	TwC	Input Clock Width	3.0V	125		ns	1,7
			5.5V	125		ns	1,7
			3.0v	62	DC	ns	1,7
			5.5V	62	DC	ns	1,7
4	TwTinL	Timer Input Low Width	3.0V	100		ns	1,7
			5.5V	70		ns	1,7
5	TwTinH	Timer Input High Width	3.0V	3TpC			1,7
			5.5V	3TpC			1,7
6	TpTin	Timer Input Period	3.0V	4TpC			1,7
			5.5V	4TpC			1,7
7	TrTin,	Timer Input Rise & Fall Timer	3.0V		100	ns	1,7
			5.5V		100	ns	1,7
8A	TwIL	Int. Request Low Time	3.0V	100		ns	1,2,7
			5.5V	70		ns	1,2,7
8B	TwIL	Int. Request Low Time	3.0V	3TpC			1,3,7
			5.5V	3TpC			1,3,7
9	TwIH	Int. Request Input High Time	3.0V	3TpC			1,2,7
			5.5V	3TpC			1,2,7
10	Twsm	STOP Mode Recovery Width Spec	3.0V	12		ns	4
			5.5V	12		ns	4
11	Tost	Oscillator Start-up Time	3.0V		5TpC		4,9
			5.5V		5TpC		4,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. SMR D1 = 0.
8. Maximum frequency for external xtal clock is 4 MHz when using low EMI Oscillator mode Pcon Reg.D7=0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note [1]	T_A= 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Direction Data
1	TsDI(DAV)	Data In Setup Time	3.0V	0		0		IN
			5.5V	0		0		IN
2	ThDI(RDY)	Data In Hold Time	3.0V	0		0		IN
			5.5V	0		0		IN
3	TwDAV	Data Available Width	3.0V	155		155		IN
			5.5V	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	3.0V		0		0	IN
			5.5V		0		0	IN
5	TdDAVId(RDY)	DAV Out to DAV Fall Delay	3.0v		120		120	IN
			5.5V		80		80	IN
6	RDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V	0		0		IN
			5.5V	0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay	3.0V	42		31		OUT
			5.5V	42		31		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	3.0V	0		0		OUT
			5.5V	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	3.0V		160		160	OUT
			5.5V		115		115	OUT
10	TwRDY	RDY Width	3.0V	110		110		OUT
			5.5V	80		80		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V		110		110	

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com