Z86C03/C06

8-BIT CMOS Z8® MCU

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Speed
Z86C03	512 KB	60	14	8 MHz
Z86C06	1 KB	124	14	12 MHz

Note: *General-Purpose

- 18-Pin Package (DIP, SOIC)
- 3.0 - 5.5 V Operating Range
- Operating Temperature: –40°C to +105°C
- Fast Instruction Pointer: 1.5 µs @ 8 MHz (C03); 1.0 µs @ 12 MHz (C06)
- Multiple Expanded Register File Control Registers and Two SPI Registers (Z86C06 Only)
- One/Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Software-Enabled Watch-Dog Timer
- Power-On Reset Timer
- Two Standby Modes: STOP and HALT
- Two Comparators with Programmable Interrupt Polarity
- 14 Input/Output Lines (Two with Comparator Inputs)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.
- Serial Peripheral Interface (SPI) (Z86C06 Only)
- Software Programmable Low EMI Mode
- ROM Protect Option
- Auto Latches

GENERAL DESCRIPTION

The Z86C03/C06 CCP™ (Consumer Controller Processors) are members of the Z8® MCU single-chip family with enhanced wake-up circuitry, programmable watch-dog timers, and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 512 and 1KB of ROM and 60 and 124 bytes of general-purpose RAM, respectively, these low-cost, low-power consumption CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C03/C06 CCP™ architecture is characterized by Zilog's 8-bit microcontroller core with the addition of an Expanded Register File to allow easy access to register mapped peripheral and I/O circuits. The Z86C03/C06 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, and industrial applications.

For applications demanding powerful I/O capabilities, the Z86C03/C06 provides 14 pins dedicated to input and output. These lines are grouped into two ports and are configurable under software control to provide timing, status signals, or parallel I/O.

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File. The Register File is composed of 61/125 bytes of General-Purpose Registers, two

GENERAL DESCRIPTION (Continued)

I/O Port registers, and 12/14 Control and Status registers. The Expanded Register File consists of three control registers in the Z86C03, and four control registers, a SPI Receive Buffer, and a SPI compare register in the Z86C06.

With powerful peripheral features such, as on-board comparators, counter/timer(s), Watch-Dog Timer (WDT), and Serial Peripheral Interface (SPI) (C06 only), the Z86C03/C06 meets the needs of a variety of sophisticated controller applications (Figure 1).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

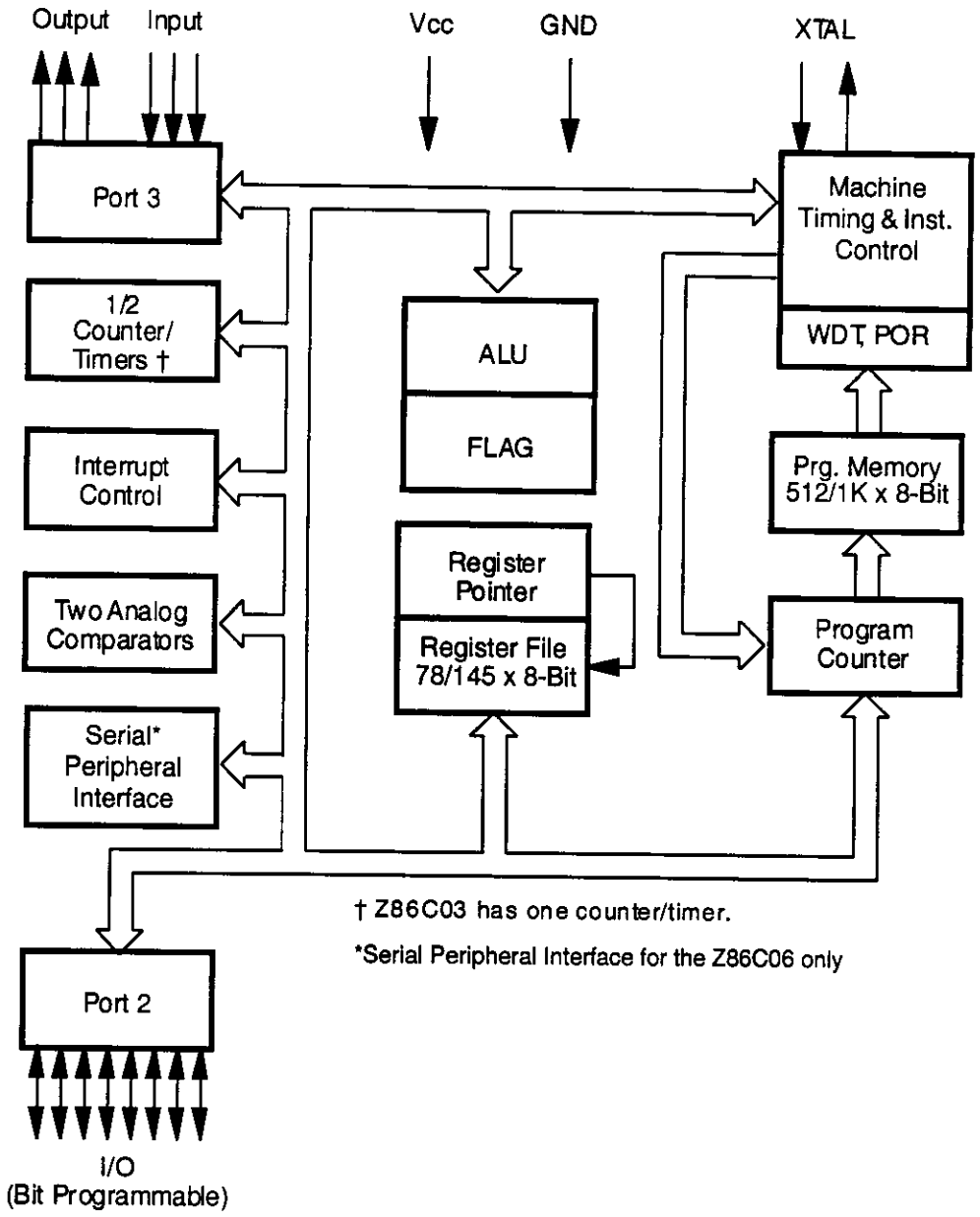


Figure 1. Z86C03/C06 Functional Block Diagram

PIN DESCRIPTION

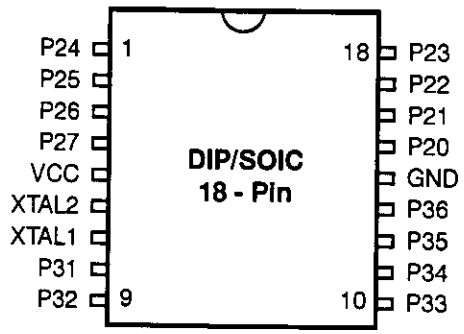


Figure 2. 18-Pin DIP and SOIC Pin Configuration

Table 1. 18-Pin DIP and SOIC Pin Identification

No	Symbol	Function	Direction
1-4	P24-27	Port 2, pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-33	Port 3, pins 1, 2, 3	Fixed Input
11-13	P34-36	Port 3, pins 4, 5, 6	Fixed Output
14	GND	Ground	
15-18	P20-23	Port 2, pins 0, 1, 2, 3	In/Output

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
V_{IHM}	Max Input Voltage**		12	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp	†		°C

Notes:
*Voltage on all pins with respect to GND.
**Applies to Port pins only and must limit current going into or out of Port pins to 250 µA maximum.
†See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin.

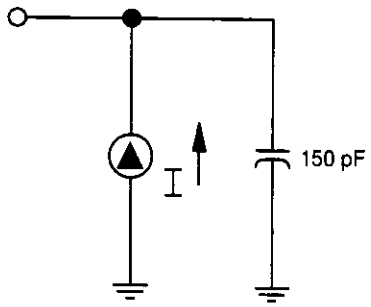


Figure 3. Test Load Configuration

CAPACITANCE

T_A = 25° C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input Capacitance	0	12 pF
Output Capacitance	0	20 pF
I/O Capacitance	0	25 pF

V_{CC} SPECIFICATION

V_{CC} = 3.0V to 5.5V

DC ELECTRICAL CHARACTERISTICS

Z86C03/C06

Symbol	Parameter	V_{CC} Note [3]	T_A=0°C to +70°C Min	Max	T_A=–40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	3.3V		7		7		V	$I_{IN} \le 250\ \mu A$	7
		5.0V		7		7		V	$I_{IN} \le 250\ \mu A$	7
V_{CH}	Clock Input High Voltage	3.3V	0.9 V_{CC}	V_{CC}+0.3	0.9 V_{CC}	V_{CC}+0.3	2.4	V	Driven by External Clock Generator	
		5.0V	0.9 V_{CC}	V_{CC}+0.3	0.9 V_{CC}	V_{CC}+0.3	3.9	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.3V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.6	V	Driven by External Clock Generator	
		5.0V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	2.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	3.3V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.0	V		
		5.0V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage (Low EMI Mode)	3.3V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH}= -500 µA	
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH}= -500 µA	
V_{OL}	Output Low Voltage (Low EMI Mode)	3.3V		0.8		0.8	0.35	V	I_{OL}=+1.0 mA	
		5.0V		0.4		0.4	0.18	V	I_{OL}=+1.0 mA	
V_{OH1}	Output High Voltage	3.3V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA	12
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	12
V_{OL1}	Output Low Voltage	3.3V		0.8		0.8	0.2	V	I_{OL} = +4.0 mA	12
		5.0V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	12
V_{OL2}	Output Low Voltage	3.3V		1.0		1.0	0.4	V	I_{OL} = +6 mA, 3 Pin Max	12
		5.0V		1.0		1.0	0.5	V	I_{OL} = +12 mA, 3 Pin Max	12
V_{OFFSET}	Comparator Input Offset Voltage	3.3V		25		25	10	mV		
		5.0V		25		25	10	mV		
I_{IL}	Input Leakage (Input bias current of comparator)	3.3V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	8
		5.0V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	8
I_{OL}	Output Leakage	3.3V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.0V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	3.3V		6		6	3.0	mA	@ 8 MHz	4, 5, 9
		5.0V		11.0		11.0	6.0	mA	@ 8 MHz	4, 5. 9
		3.3V		8.0		8.0	4.5	mA	@ 12 MHz	4, 5, 9
		5.0V		15		15	9.0	mA	@ 12 MHz	4, 5, 9

Symbol	Parameter	V_{CC} Note [3]	T_A=0°C to +70°C Min	Max	T_A=–40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	3.3V		3.0		3.0	0.7	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 8 MHz	4, 5 10
		5.0V		5		5	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 8 MHz	1, 4, 5,10
		3.3V		4.5		4.5	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 12 MHz	4,5,10
		5.0V		7.0		7.0	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 12 MHz	4,5,10
		3.3V		1.4		1.4	0.6	mA	Clock Divide by 16 @ 8 MHz	4,5,10
		5.0V		3.5		3.5	1.3	mA	Clock Divide by 16 @ 8 MHz	4,5,10
		3.3V		2.0		2.0	0.7	mA	Clock Divide by 16 @ 12 MHz	4,5,10
		5.0V		4.5		4.5	1.5	mA	Clock Divide by 16 @ 12 MHz	4,5,10

Symbol	Parameter	V_{CC} Note [3]	T_A=0°C to +70°C Min	Max	T_A=–40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC2}	Standby Current	3.3V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	6,10
		5.0V		10		20	3.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	6,10
		3.3V		350		360	180	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	6,9
		5.0V		865		875	400	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	6,9
I_{ALL}	Auto Latch Low Current	3.3V		7.0		14.0	4.0	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		20.0		30.0	13	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.3V		-4.0		–8.0	-3	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		-9.0		–16.0	-7	µA	$0V < V_{IN} < V_{CC}$	
T_{POR}	Power On Reset	3.3V	7	24	6	25	13	ms		
		5.0V	3	13	2	14	6.5	ms		
V_{LV}	V_{CC} Low Voltage		1.5	2.65	1.2	2.95	2.4	V	2 MHz max Int. CLK Freq.	13
V_{ICR}	Comparator Input Common Mode Voltage Range			V_{CC}-1.0		V_{CC}-1.5		V		

Notes:

1. I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3	5.0	mA	8 MHz
Crystal or Ceramic Resonator	3.0	5.0	mA	8 MHz

2. V_{SS} = 0V = GND
3. 5.0V ± 0.5V, 3.0V ± 0.3V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 47 pF
6. Same as note [4] except inputs at V_{CC}.
7. The input current must be limited to a maximum of 250 µA or less.
8. Input bias current for comparator inputs P31, P32, P33.
9. Internal on-board RC is driving WDT.
10. WDT is not running.
11. System clock is external XTAL frequency divided by 2.
12. Standard mode (not Low EMI Mode).
13. The V_{BO} voltage increases as the temperature decreases.

AC ELECTRICAL CHARACTERISTICS

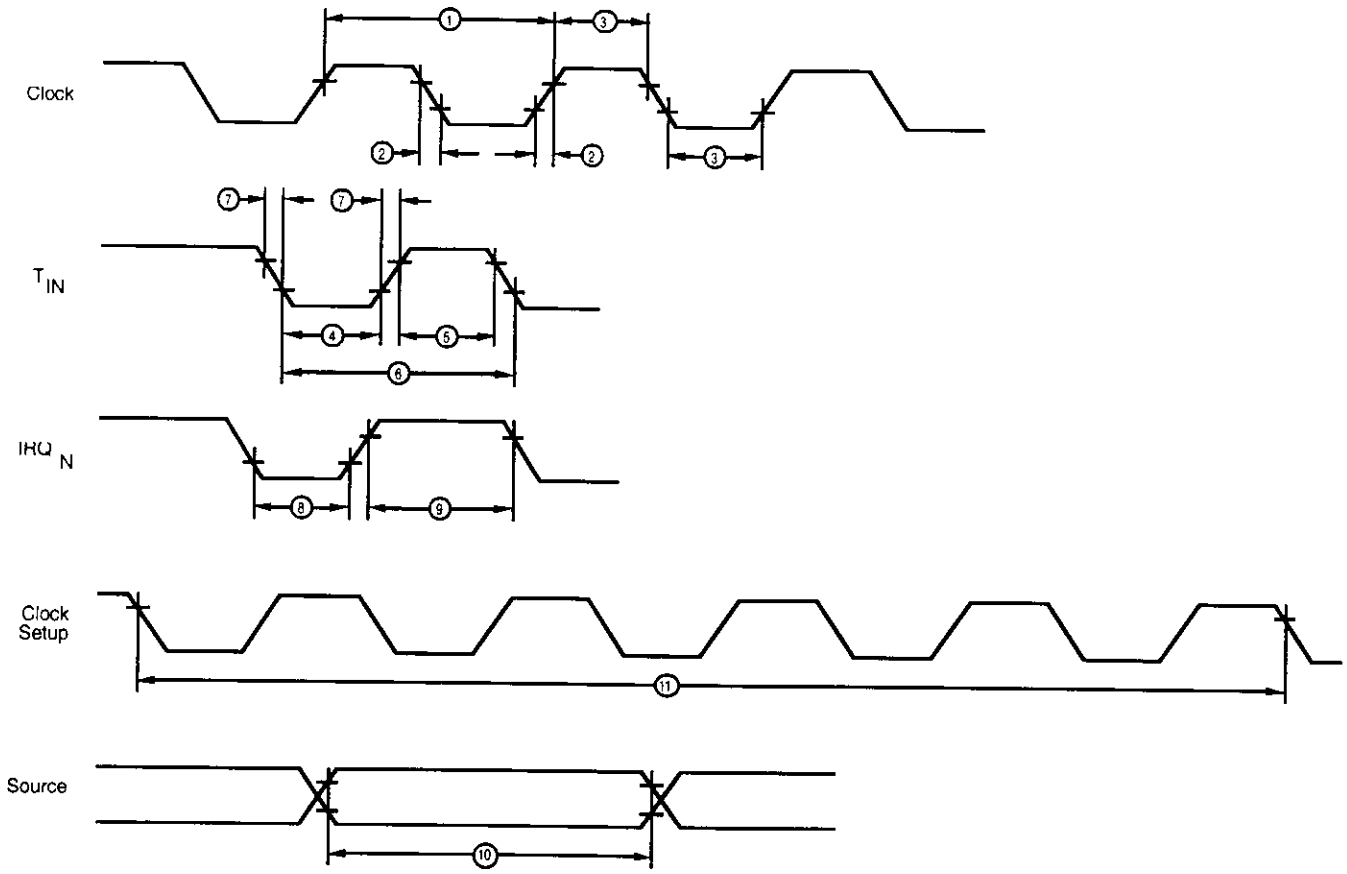


Figure 4. Additional Timing

AC ELECTRICAL CHARACTERISTICS

(SCLK/TCLK = External/2)

				T_A = 0°C To +70°C				T_A = -40°C To +105°C					
			V_{CC}	8 MHz		12 MHz		8 MHz		12 MHz			
No	Sym.	Parameter	Note[3]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.3V	125	DC	83	DC	125	DC	83	DC	ns	1
			5.0V	125	DC	83	DC	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.3V		25		15		25		15	ns	1
			5.0V		25		15		25		15	ns	1
3	TwC	Input Clock Width	3.3V	37		26		37		26		ns	1
			5.0V	37		26		37		26		ns	1
4	TwTinL	Timer Input Low Width	3.3V	100		100		100		100		ns	1
			5.0V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.3V	5TpC		5TpC		5TpC		5TpC			1,7
			5.0V	5TpC		5TpC		5TpC		5TpC			1,7
6	TpTin	Timer Input Period	3.3V	8TpC		8TpC		8TpC		8TpC			1,7
			5.0V	8TpC		8TpC		8TpC		8TpC			1,7
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.3V		100		100		100		100	ns	1
			5.0V		100		100		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.3V	100		100		100		100		ns	1,2
			5.0V	70		70		70		70		ns	1,2
9	TwIH	Int. Request Input High Time	3.3V	5TpC		5TpC		5TpC		5TpC			1,2,7
			5.0V	5TpC		5TpC		5TpC		5TpC			1,2,7
10	Twsm	STOP Mode Recovery Width Spec	3.3V	12		12		12		12		ns	
			5.0V	12		12		12		12		ns	
11	Tost	Oscillator Start-up Time	3.3V		5TpC		5TpC		5TpC		5TpC		Reg. 4
			5.0V		5TpC		5TpC		5TpC		5TpC	ns	
12	Twdt	Watchdog Timer Refresh Time	3.3V	15		15		12		12			5
			5.0V	5		5		3		3		ms	D0=0[6] D1=0[6]
			3.3V	30		30		25		25		ms	D0=1[6]
			5.0V	16		16		12		12		ms	D1=0[6]
			3.3V	60		60		50		50		ms	D1=0[6]
			5.0V	30		30		25		25		ms	D1=1[6]
			3.3V	250		250		200		200		ms	D0=1[6]
			5.0V	120		120		100		100		ms	D1=1[6]

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33)
3. 5.0V ± 0.5V, 3.3V ± 0.3V
4. SMR-D5 = 0 (Stop mode delay off)
5. Reg. WDTMR
6. Internal RC Oscillator only
7. System clock is XTAL frequency divided by 2.

AC ELECTRICAL CHARACTERISTICS (Continued)

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = EXTERNAL)

				T_A = 0°C to +70°C		T_A = -40°C to +105°C			
			V_{CC}	4 MHz		4 MHz			
No	Symbol	Parameter	Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.0V	125		125		ns	1,7,8
			5.5V	125		125		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			1,7,8
			5.5V	3TpC		3TpC			1,7,8
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			1,7,8
			5.5V	4TpC		4TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8	TwIL	Int. Request Low Time	3.0V	100		100		ns	1,2,7,8
			5.5V	70		70		ns	1,7,8
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			1,2,7,8
			5.5V	3TpC		2TpC			1,2,7,8
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		3,8,9
			5.5V		5TpC		5TpC		3,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P33-P31)
3. SMR-D5 = 0
4. SMR-D5 = 1, POR STOP Mode delay is on.
5. Reg. WDTMR
6. V_{CC} = 3.0V to 5.5V
7. SMR D1 = 1
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

PIN FUNCTIONS

XTAL1. Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered and contain Auto Latches. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figures 5, 6 and 7). Low EMI output buffers can be globally programmed by the software. In addition, when the SPI is enabled, P20 functions as data-in (D1), and P27 Functions as data-out (D0) for the SPI (SPI on the Z86C06 only)

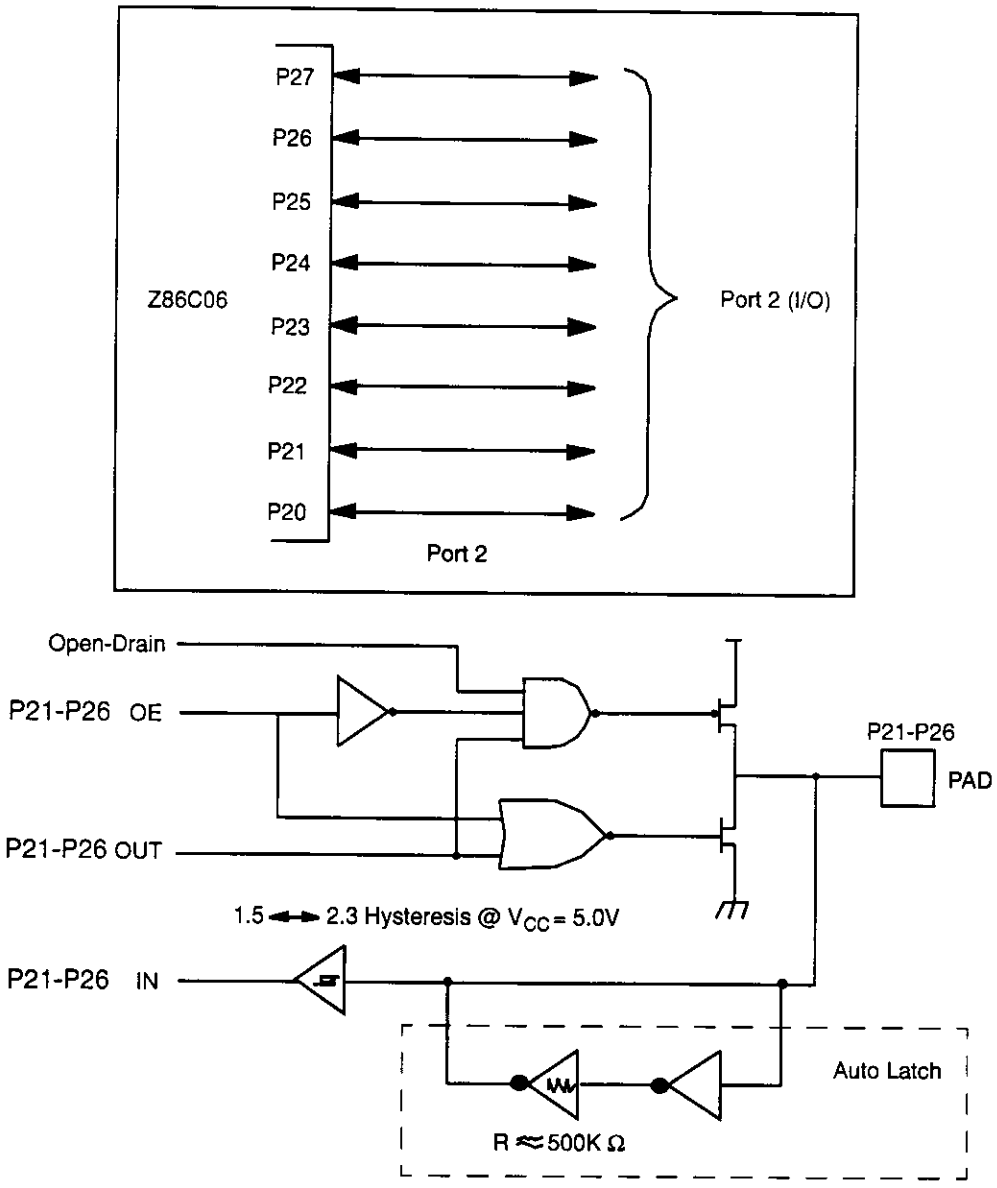


Figure 5. Port 2 Configuration (Z86C06)

PIN FUNCTIONS (Continued)

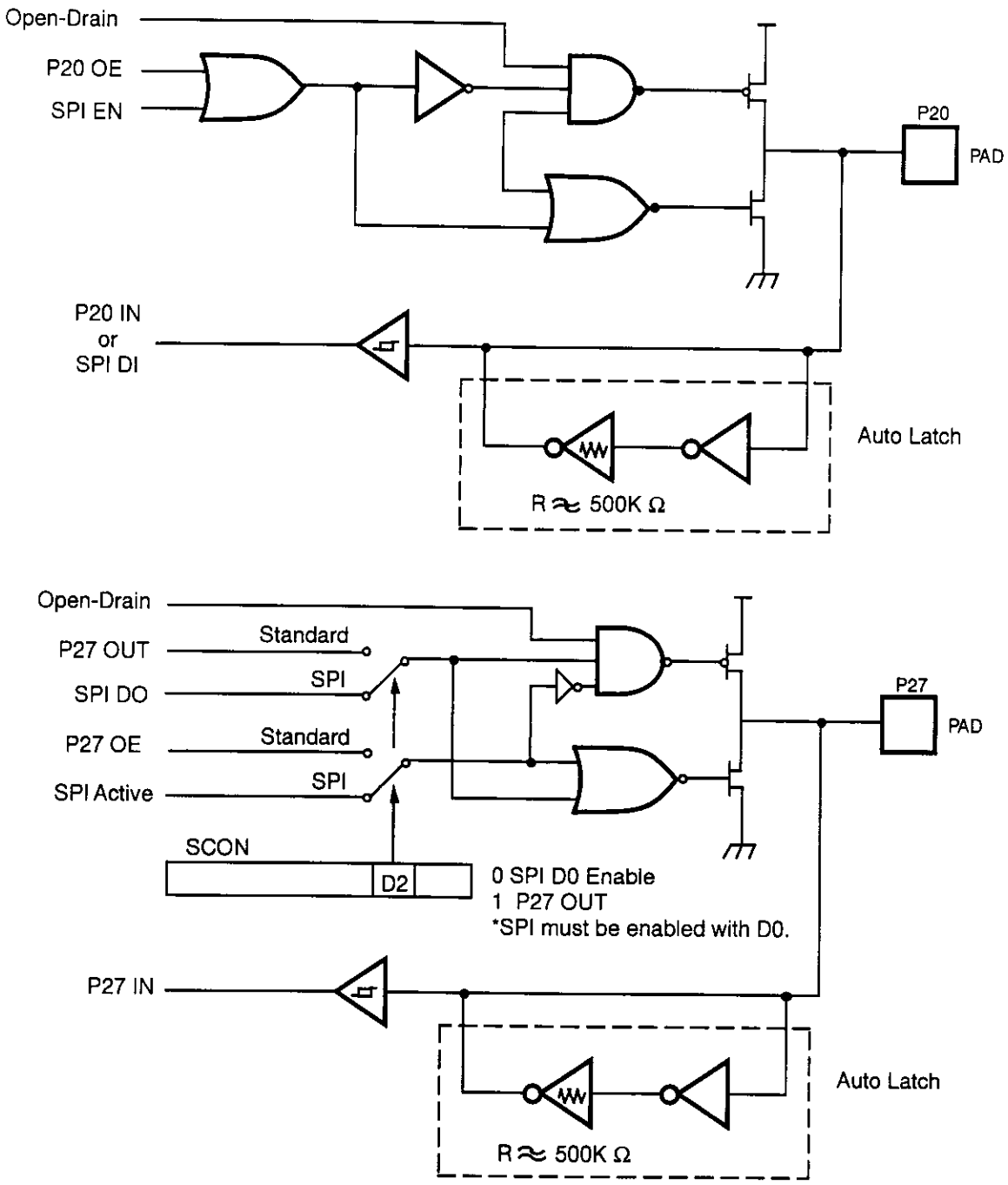


Figure 6. Port 2 Configuration (Z86C06)

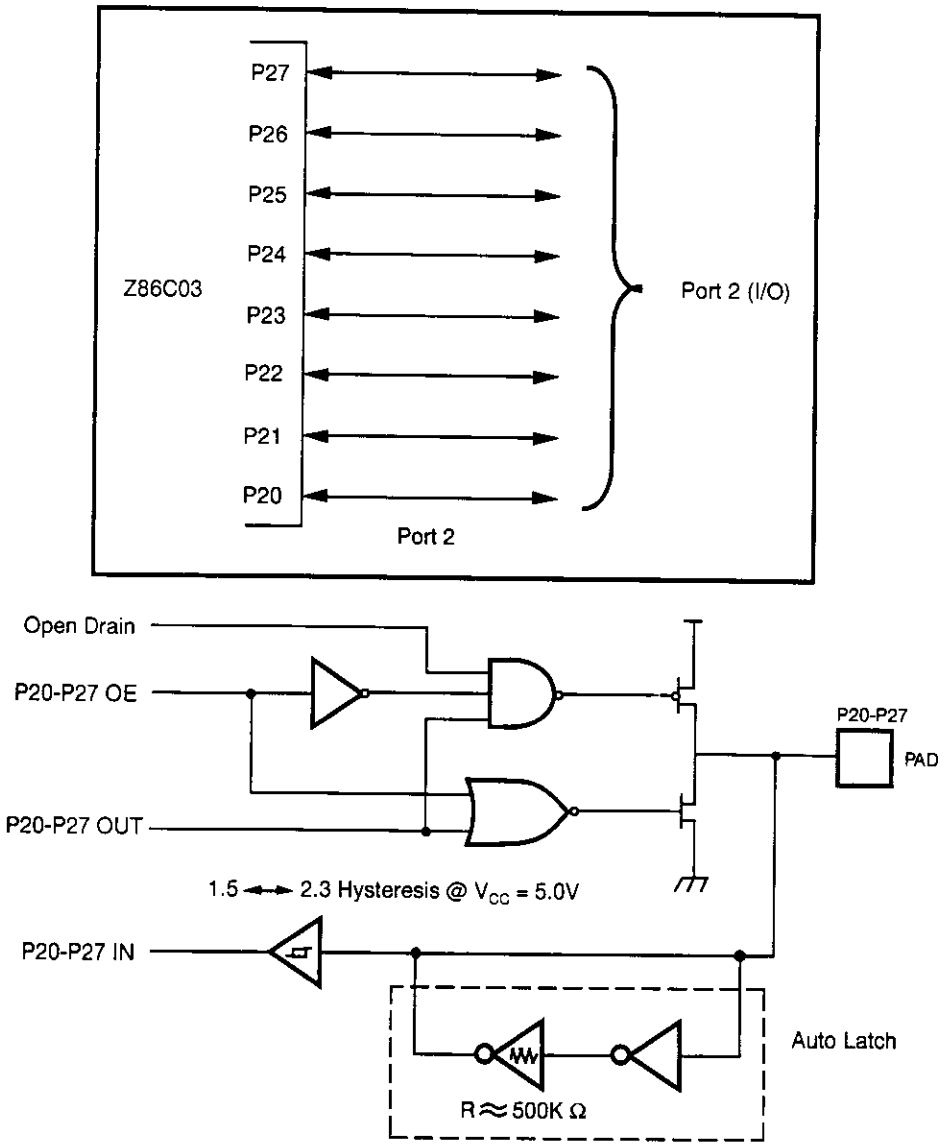


Figure 7. Port 2 Configuration (Z86C03)

PIN FUNCTIONS (Continued)

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Port 3 (P36-P31). Port 3 is a 6-bit, CMOS-compatible port. These six lines consist of three fixed inputs (P31-P33) and three fixed outputs (P34-P36). Pins P31, P32, and P33 are standard CMOS inputs (no auto latches) and pins P34, P35, and P36 are push-pull outputs. Low EMI output buffers can be globally programmed by the software. Two onboard comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M-bit D1). Pins P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input when the analog mode is selected. P33 is a falling edge interrupt input only.

Note: P33 is available as an interrupt input only in the digital mode. P31 and P32 are valid interrupt inputs and P31 is the T_{IN} input when the analog or digital input mode is selected.

The outputs from the analog comparator can be globally programmed to output from P34 and P35 by setting PCON (F) 00 bit D0 = 1.

Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}).

In the Z86C06, pin P34 can also be configured as SPI clock (SK), input and output, and pin P35 can be configured as Slave Select (SS) in slave mode only, when the SPI is enabled (Figures 8 & 9).

Note:

1. Must disable interrupts, switch to analog mode, clear interrupt requests and then enable interrupt when switching from digital to analog mode.
2. When switching from digital to analog mode, it is recommended to wait two NOP delays before sampling the comparator outputs.

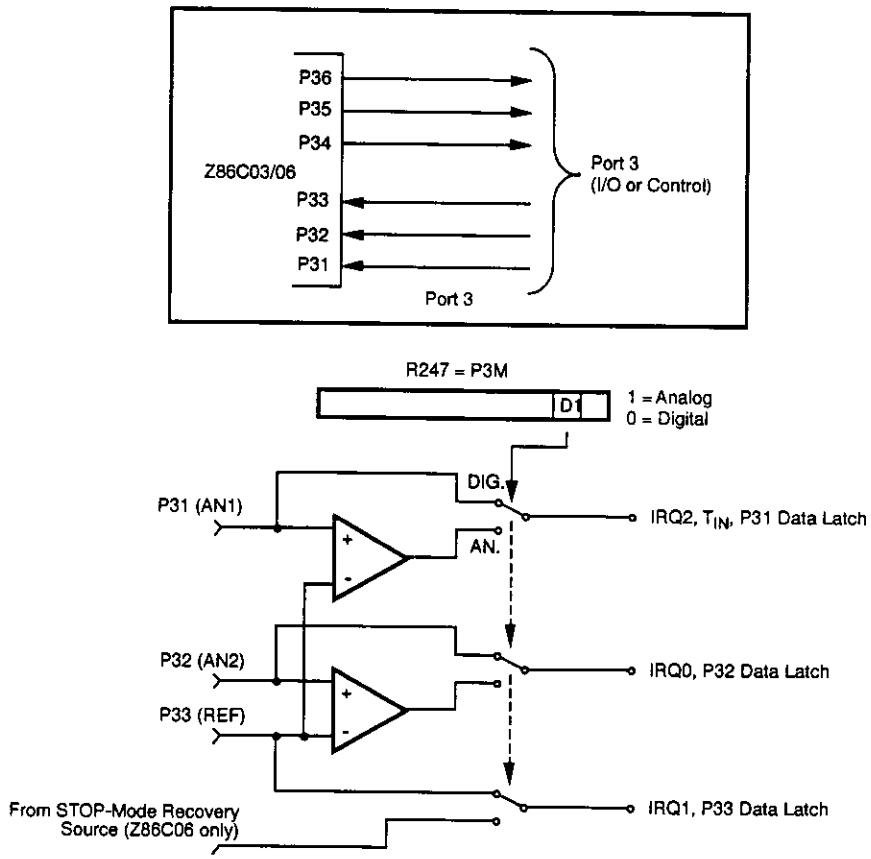


Figure 8. Port 3 Configuration

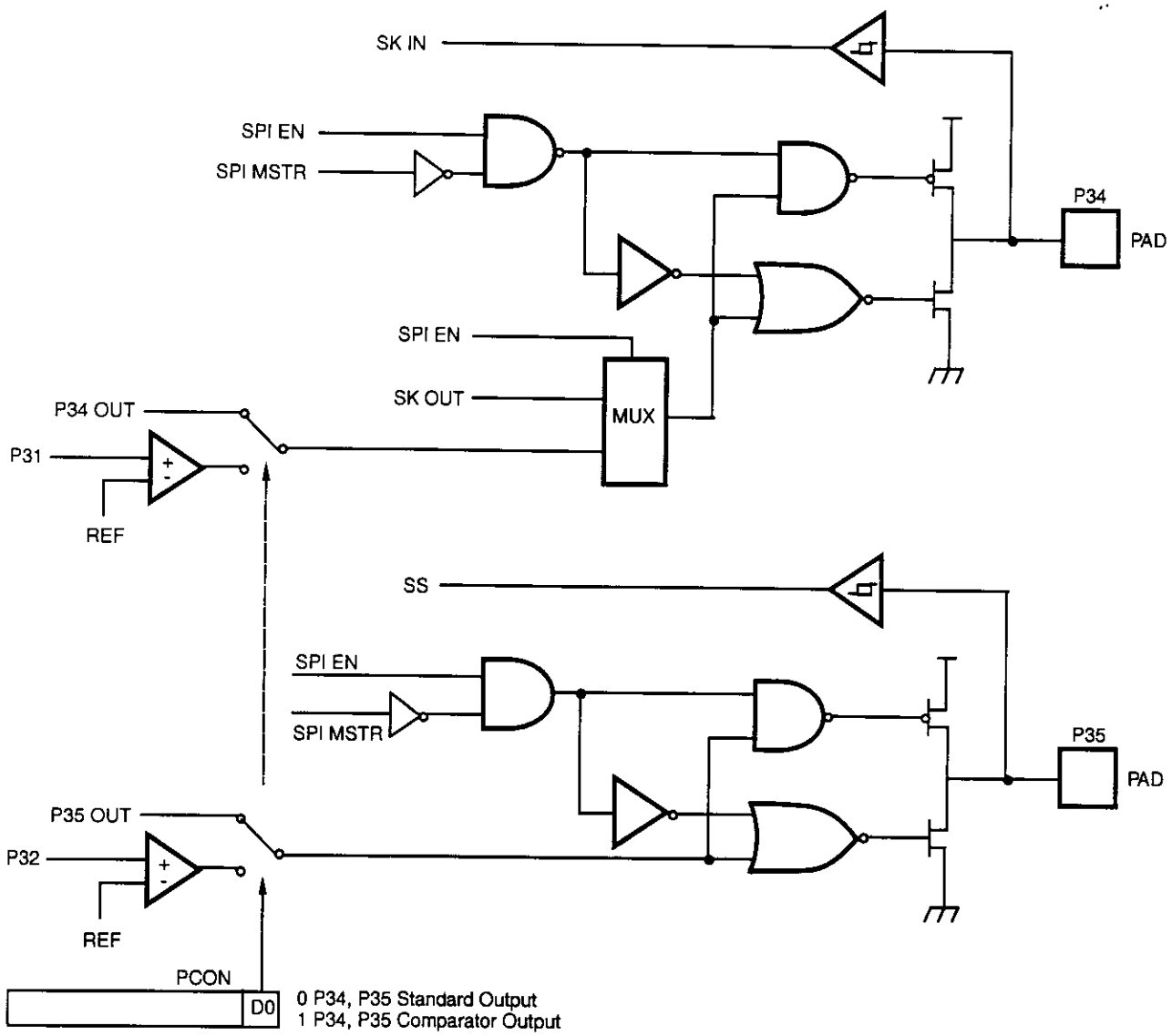


Figure 9. Port 3 Configuration (Z86C06)

Low EMI Emission. The Z86C03/C06 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns (typical).
- Low EMI output drivers resistance of 200 ohms (typical).
- Low EMI oscillator.
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz (250 ns cycle time) when the low EMI oscillator is selected and SCLK = External (SMR Register Bit D1=1).

Comparator Inputs. Port 3 Pin P31 and P32 each have a comparator front end. The comparator reference voltage pin P33 is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In digital mode, Pin P33 can be used as a P33 register input or IRQ1 source.

FUNCTIONAL DESCRIPTION

The following special functions have been added to the Z86C03/C06 CCPs to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of four ways:

1. Power-On Reset
2. Watch-Dog Timer
3. Stop-Mode Recovery Source
4. Low Voltage Protection

Having the Auto Power-On Reset circuitry built-in, the Z86C03/C06 does not require an external reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles.

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a Stop-Mode Recovery operation.

Program Memory. Z86C03/C06 can address up to 512/1 KB of internal program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 511/1023 consists of on-chip, user program mask ROM.

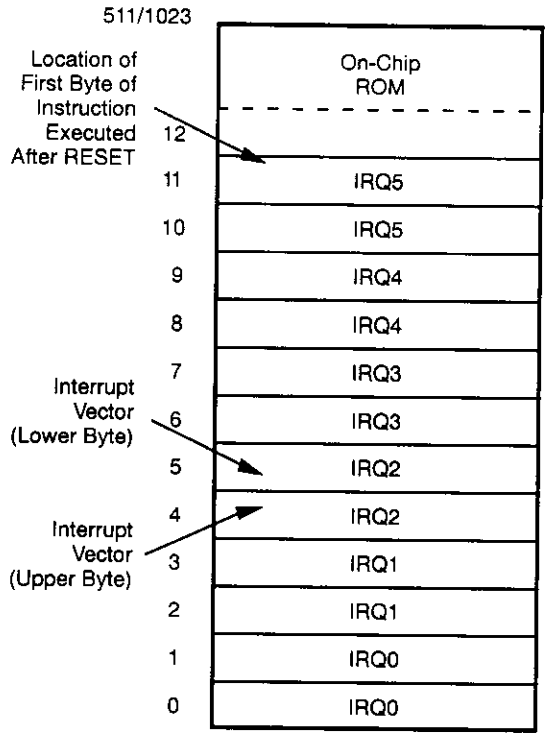
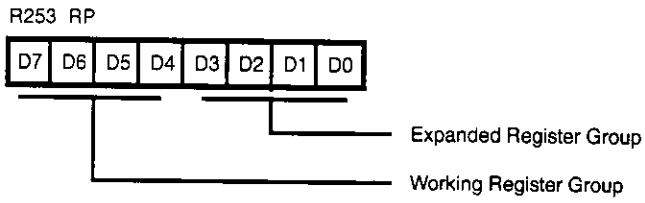


Figure 10. Program Memory Map

ROM Protect. The 512/1K bytes of Program Memory is mask programmable. A ROM protect feature will prevent "dumping" of the ROM contents by inhibiting execution of the LDC and LDCI instructions to program memory in all modes.

ROM protect is mask-programmable. It is selected by the customer when the ROM code is submitted. **Selecting ROM protect disables the LDC and LDCI instructions in all modes. ROM look-up tables are not supported in this mode.**



Note: Default Setting After Reset = 00000000

Figure 11. Register Pointer Register

Register File. The Register File consists of two I/O port registers, 60/124 general-purpose registers, and 13/15 control and status registers. The Z86C03 General-Purpose Register file ranges from address 00 to 3F while the Z86C06 General-Purpose Register file ranges from address 00 to 7F (see Figure 12). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 12). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

Stack. An 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60/124 general-purpose registers.

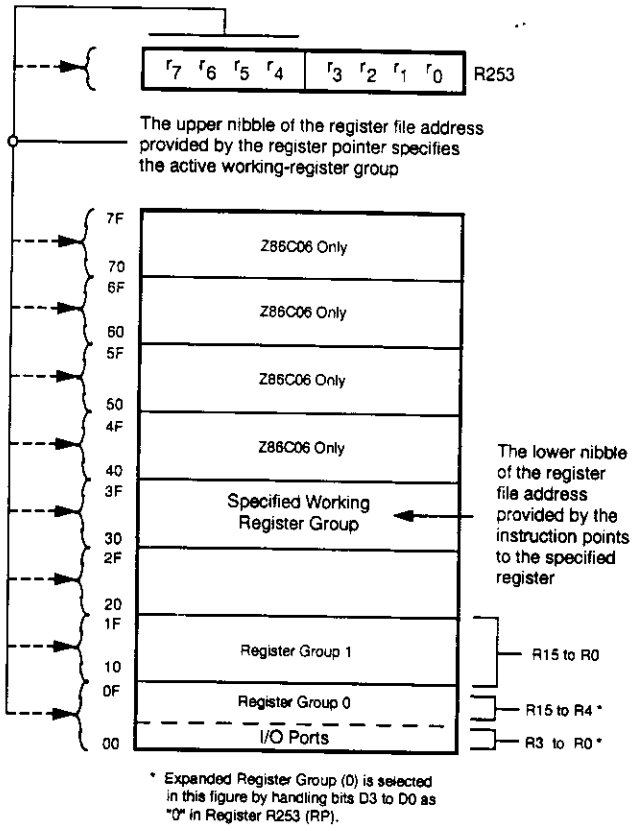


Figure 12. Register Pointer

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figures 13 and 14). These register groups are known as the Expanded Register File (ERF).

Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of register RP select the working register group. For the Z86C03, three system configuration registers reside in the ERF address space Bank F. For the Z86C06, three system configuration registers reside in the ERF address space Bank F, while three SPI registers reside in Bank C. The rest of the ERF address space is not physically implemented and is open for future expansion.

FUNCTIONAL DESCRIPTION (Continued)

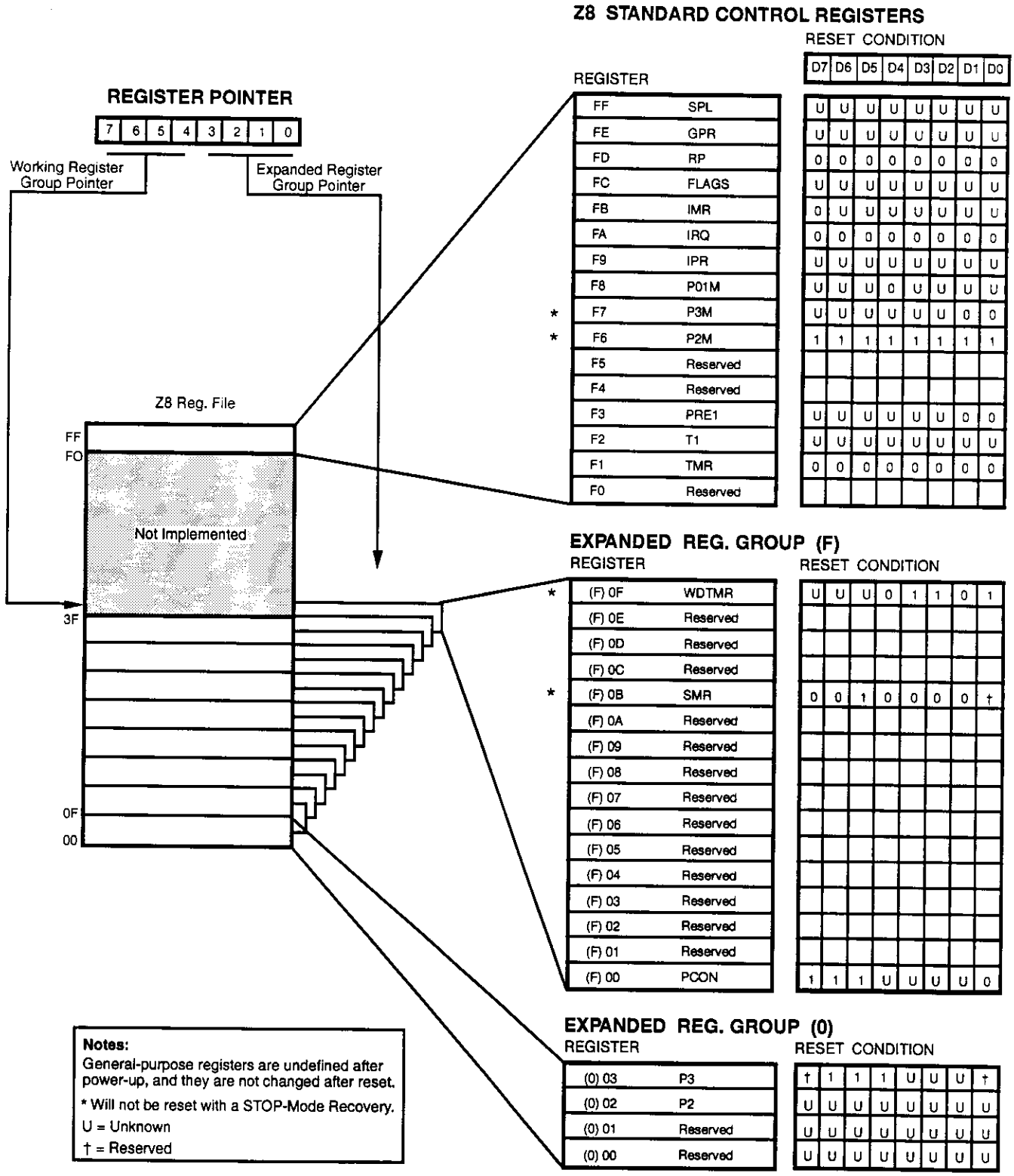


Figure 13. Expanded Register File Architecture (Z86C03)

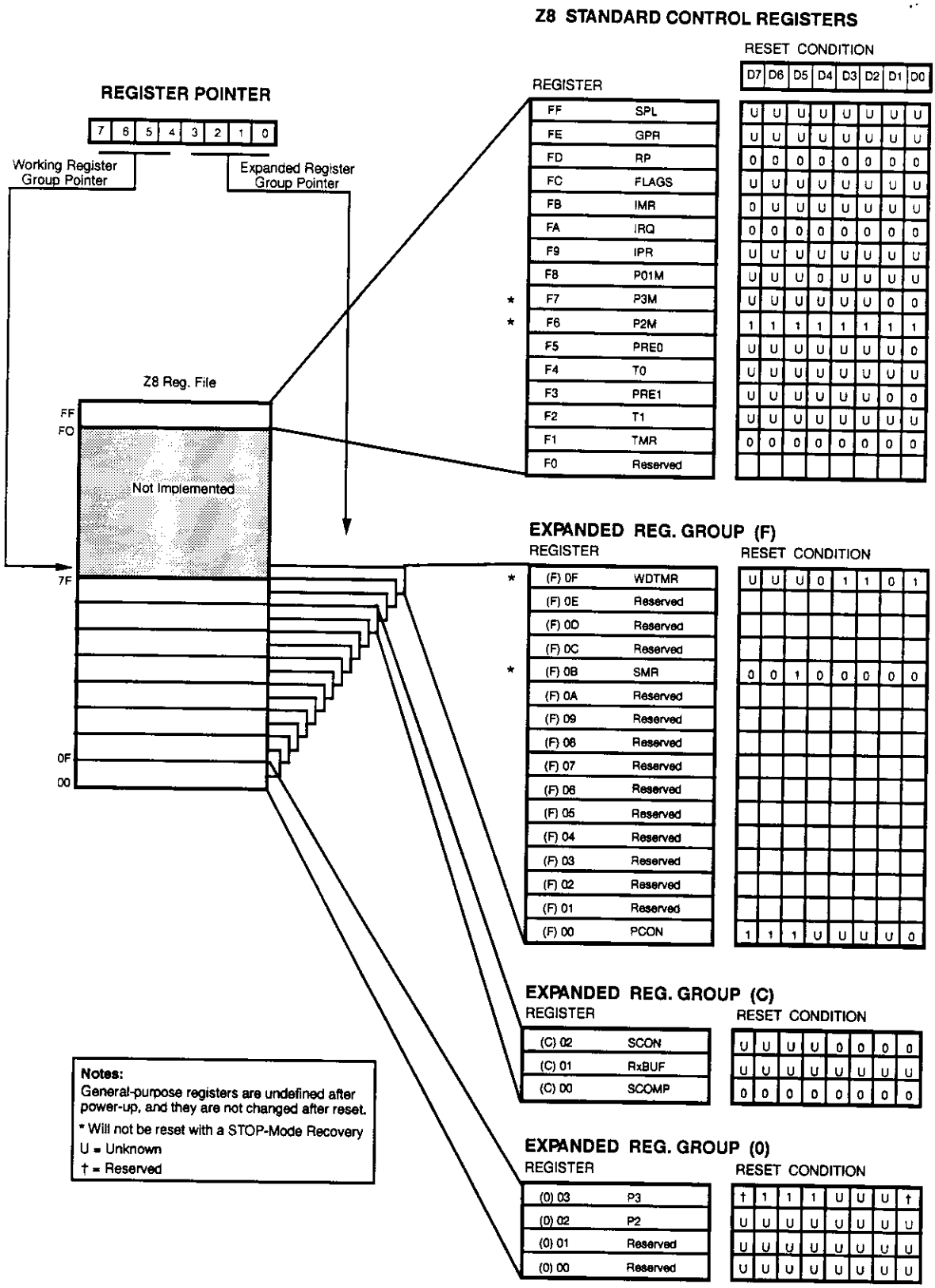


Figure 14. Expanded Register File Architecture (Z86C06)

FUNCTIONAL DESCRIPTION (Continued)

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler (Z86C03 only has T1). The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 15).

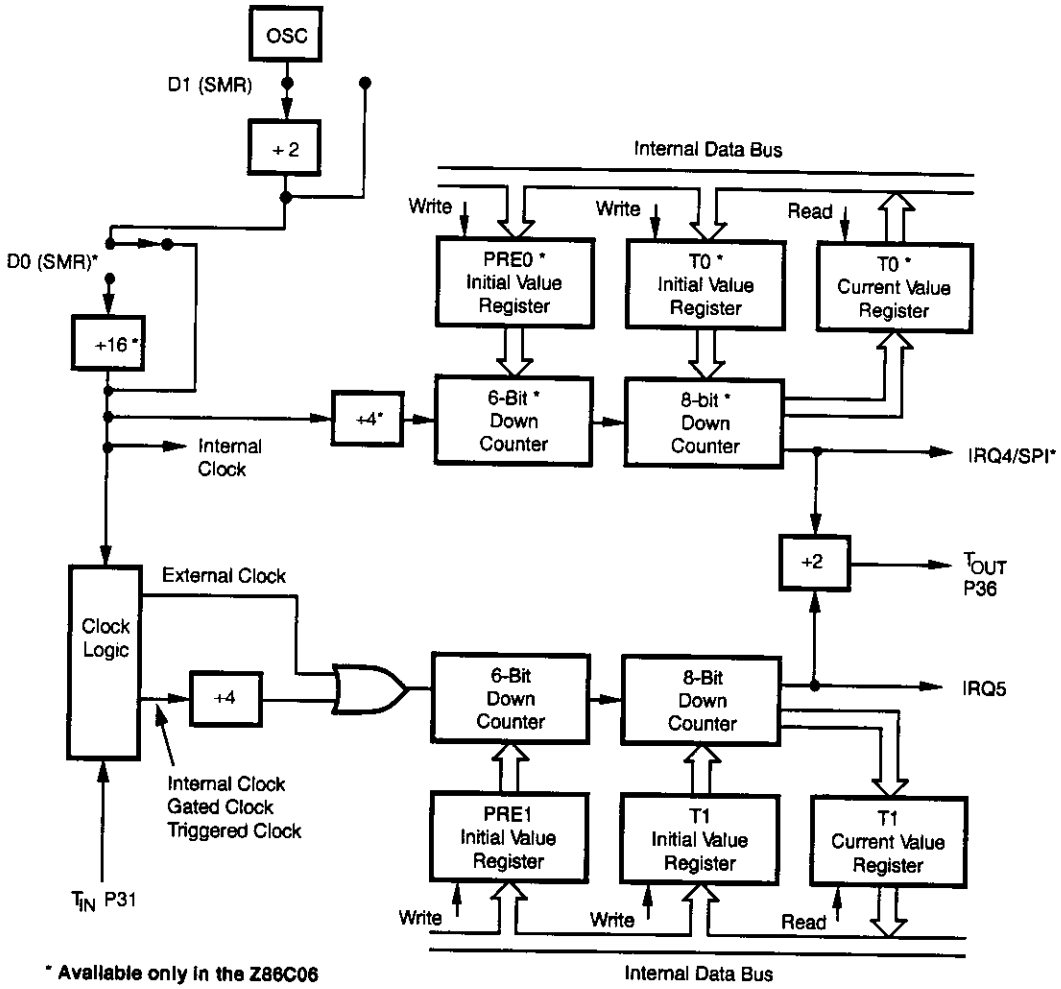


Figure 15. Counter/Timer Block Diagram

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated. Note that IRQ4 is software-generated in the Z86C03.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 serves as a timer output (T_{OUT}) through which T0 (C06

only), T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1 (C06 only). The T_{IN} mode is enabled by setting PRE1 bit D1 (R243) to 0.

Interrupts. The Z86C03/C06 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 16). The six sources are divided as follows; three sources are claimed by Port 3 lines P31-P33, two sources in the counter/timers, and one source for the SPI. The Interrupt Mask Register globally or singularly enables or disables the six interrupt requests (Table 2).

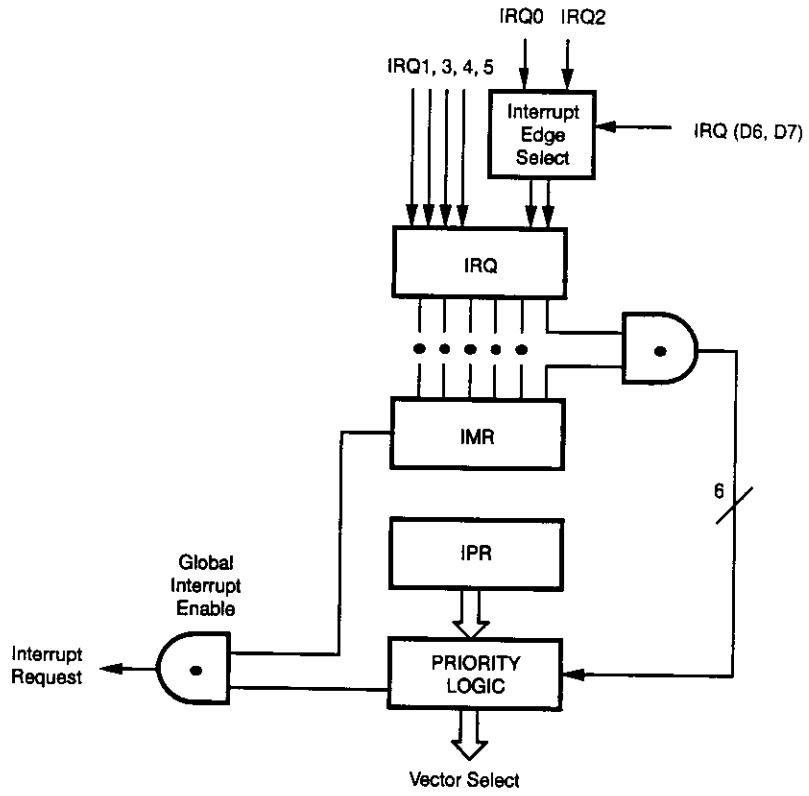


Figure 16. Interrupt Block Diagram

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	IRQ 0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ 1	IRQ 1	2, 3	External (P33), Falling Edge Triggered
IRQ 2	IRQ 2, TIN	4,5	External (P31), Rising/Falling Edge Triggered
IRQ 3*	IRQ 3	6, 7	Software Generated, SPI Receive
IRQ 4	T0/IRQ 4	8, 9	Internal for C06 and Software Generated for C03
IRQ 5	TI	10, 11	Internal

Note: * In the Z86C06, the SPI receive interrupt is mapped to IRQ3 when enabled.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86C03/C06 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to

FUNCTIONAL DESCRIPTION (Continued)

determine which of the interrupt requests need service. In the Z86C06, when the SPI is disabled, IRQ3 has no hardware source but can be invoked by software (write to IRQ3 Register). When the SPI is enabled, an interrupt will be mapped to IRQ3 after a byte of data has been received by the SPI Shift Register.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

The programming bits for the INTERRUPT EDGE SELECT are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

Table 3. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

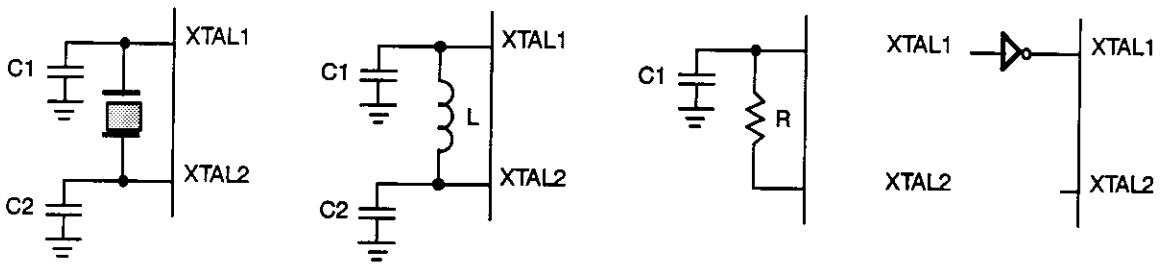
Note:
F = Falling Edge
R = Rising Edge

Clock. The Z86C03/C06 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 8 MHz/12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values (capacitance between 10 pF to 300 pF) from each pin directly to the device ground (pin 14). The layout is important to reduce ground noise injection.

The RC oscillator option is mask-programmable, to be selected by the customer at the time ROM code is submitted. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 17). The RC value vs. Frequency curves are shown in Figures 61 and 62.

In addition, a special feature has been incorporated into the Z86C03/C06; in low EMI noise mode (bit 7 of PCON register=0) with the RC option selected, the oscillator is targeted to consume considerately less I_{CC} current at frequencies of 10 kHz or less.



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC
C1, C2 = 22 pF
L = 130 µH *
F = 3 MHz

RC
@ 5V Vcc (TYP)
C1 = 33pF*
R = 1kΩ*
F = 9.5 MHz

External Clock

* Preliminary Value Including Pin Parasitics

Figure 17. Oscillator Configuration

Power-On Reset. A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the three conditions:

- Power-Fail to Power-OK Status
- Stop-Mode Recovery (If D5 of SMR=1)
- WDT Time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, and RC/LC oscillators with fast start-up time).

HALT. A Halt instructions will turn off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device may be recovered by interrupts either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP mode is terminated by a RESET only, either by WDT time-out, POR, SPI compare; or SMR recovery. This causes the processor to restart the application program at address 000C (HEX). Note, the crystal remains active in STOP mode if bits 3 and 4 of the WDTMR are enabled. In this mode, only the Watch-Dog Timer runs in STOP mode.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP mode
            or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT mode
```

Serial Peripheral Interface (SPI)—Z86C06 Only. The Z86C06 incorporates a serial peripheral interface for communication with other microcontrollers and peripherals. **The SPI does not exist on the Z86C03.** The SPI includes features such as STOP-Mode Recovery, Master/Slave selection, and Compare mode. Table 4 contains the pin configuration for the SPI feature when it is enabled. The SPI consists of four registers: SPI Control Register (SCON), SPI Compare Register (SCOMP), SPI Receive/Buffer Register (RxBUF), and SPI Shift Register. SCON is located in bank (C) of the Expanded Register Group at address 02.

Table 4. Z86C06 SPI Pin Configuration

Name	Function	Pin Location
DI	Data-In	P20
DO	Data-Out	P27
SS	Slave Select	P35
SK	SPI Clock	P34

FUNCTIONAL DESCRIPTION (Continued)

The SPI Control Register (SCON) (Figure 18) is a read/write register that controls; Master/Slave selection, interrupts, clock source and phase selection, and error flag. Bit 0 enables/disables the SPI with the default being SPI disabled. A 1 in this location will enable the SPI, and a 0 will disable the SPI. Bits 1 and 2 of the SCON register in Master mode select the clock rate. The user may choose whether internal clock is divide-by-2, -4, -8, or -16. In slave mode, Bit 1 of this register flags the user if an overrun of the RxBUF Register has occurred. The RxCharOverrun flag is only reset by writing a 0 to this bit. In slave mode, bit 2 of the Control Register disables the data-out I/O function. If a 1 is written to this bit, the data-out pin is released to its original port configuration. If a 0 is written to this bit, the SPI shifts out one bit for each bit received. Bit 3 of the SCON Register enables the compare feature of the SPI, with the default being disabled. When the compare feature is enabled, a comparison of the value in the SCOMP Register is made with the value in the RxBUF Register. Bit 4 signals that a receive character is available in the RxBUF Register.

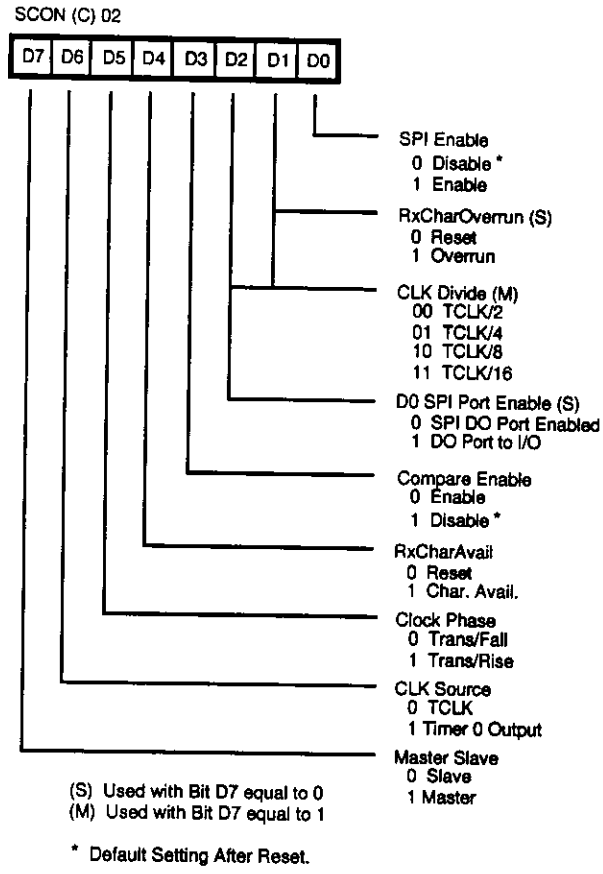


Figure 18. SPI Control Register (Z86C06 Only)

If the associated IRQ3 is enabled, an interrupt is generated. Bit 5 controls the clock phase of the SPI. A 1 in Bit 5 allows for receiving data on the clock's falling edge and transmitting data on the clock's rising edge. A 0 allows receiving data on the clock's rising edge and transmitting on the clock's falling edge. The SPI clock source is defined in bit 6. A 1 uses Timer0 output for the SPI clock, and a 0 uses TCLK for clocking the SPI. Finally, bit 7 determines whether the SPI is used as a Master or a Slave. A 1 puts the SPI into Master mode and a 0 puts the SPI into Slave mode.

SPI Operation (Z86C06 only). The SPI is used in one of two modes: either as system slave, or as system master. Several of the possible system configurations are shown in Figure 19. In the slave mode, data transfer starts when the slave select (SS) pin goes active. Data is transferred into the slave's SPI Shift Register through the DI pin, which has the same address as the RxBUF Register. After a byte of data has been received by the SPI Shift Register, a Receive Character Available (RCA/IRQ3) flag and interrupt is generated. The next byte of data will be received at this time. The RxBUF Register must be cleared, or a Receive Character Overrun (RxCharOverrun) flag will be set in the SCON Register, and the data in the RxBUF Register will be overwritten. When the communication between the master and slave is complete, the SS goes inactive.

Unless disconnected, for every bit that is transferred into the slave through the DI pin, a bit is transferred out through the DO pin on the opposite clock edge. During slave operation, the SPI clock pin (SK) is an input. In master mode, the CPU must first activate a SS through one of it's I/O ports. Next, data is transferred through the master's DO pin one bit per master clock cycle. Loading data into the shift register initiates the transfer. In master mode, the master's clock will drive the slave's clock. At the conclusion of a transfer, a Receive Character Available (RCA/IRQ3) flag and interrupt is generated. Before data is transferred via the DO pin, the SPI Enable bit in the SCON Register must be enabled.

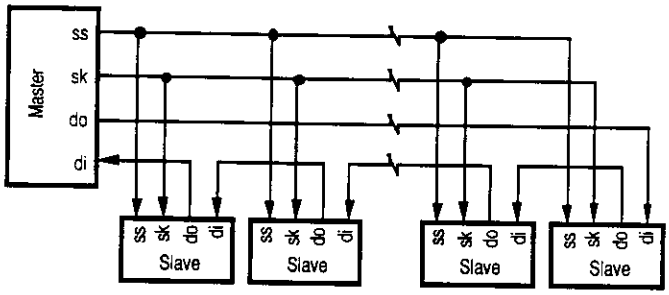
SPI Compare (Z86C06 only). When the SPI Compare Enable bit, D3 of the SCON Register is set to 1, the SPI Compare feature is enabled. The compare feature is only valid for slave mode. A compare transaction begins when the (SS) line goes active. Data is received as if it were a normal transaction, but there is no data transmitted to avoid bus contention with other slave devices. When the compare byte is received, IRQ3 is not generated. Instead, the data is compared with the contents of the SCOMP Register. If the data does not match, DO remains inactive and the slave ignores all data until the (SS) signal is reset. If the data received matches the data in the SCOMP register, then a SMR signal is generated. DO is activated if it is not tri-stated by D2 in the SCON Register, and data is received the same as any other SPI slave transaction.

When the SPI is activated as a slave, it operates in all system modes; STOP, HALT, and RUN. Slaves' not comparing remain in their current mode, whereas slaves' comparing wake from a STOP or HALT mode by means of an SMR.

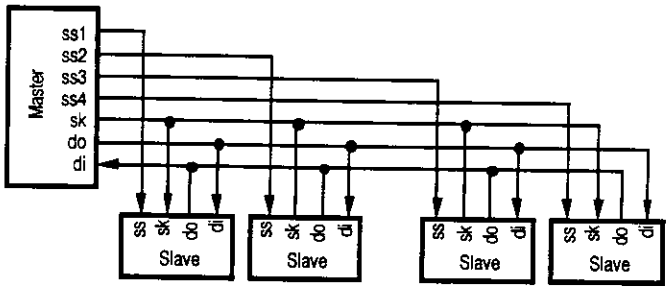
SPI Clock (Z86C06 only). The SPI clock maybe driven by three sources: Timer0, a division of the internal system clock, or the external master when in slave mode. Bit D6 of the SCON Register controls what source drives the SPI clock. A 0 in bit D6 of the SCON Register determines the division of the internal system clock if this is used as the SPI clock source. Divide by 2, 4, 8, or 16 is chosen as the scaler.

FUNCTIONAL DESCRIPTION (Continued)

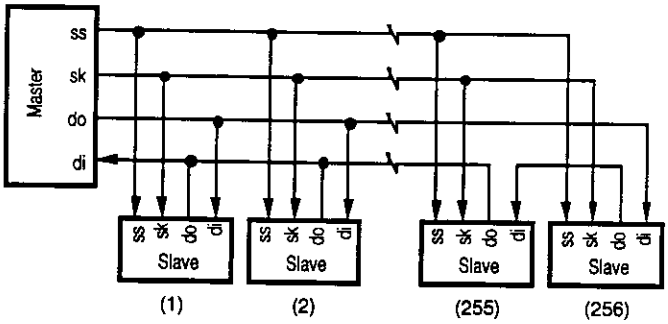
Standard Serial Setup



Standard Parallel Setup

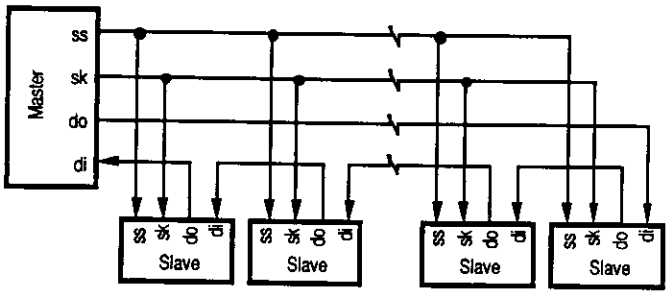


Setup For Compare



Up to 256 slaves per SS line

Three Wire Compare Setup



Multiple slaves may have the same address.

Figure 19. SPI System Configuration (Z86C06 Only)

Receive Character Available and Overrun (Z86C06 Only). When a complete data stream is received, an interrupt is generated and the RxCharAvail bit in the SCON Register is set. Bit 4 in the SCON Register is for enabling or disabling the RxCharAvail interrupt. The RxCharAvail bit is available for interrupt polling purposes and is reset when the RxBUF Register is read. RxCharAvail is generated in both master and slave modes. While in slave mode, if the RxBUF is not read before the next data stream is received and loaded into the RxBUF Register, Receive Character Overrun (RxCharOverrun) occurs. Since there is no need for clock control in slave mode, bit D1 in the SPI Control Register is used to log any RxCharOverrun (Figure 20 and Figure 21).

No	Parameter	Min	Units
1	DI to SK Setup	10	ns
2	SK to D0 Valid	15	ns
3	SS to SK Setup	.5 Tsk	ns
4	SS to D0 Valid	15	ns
5	SK to DI Hold Time	10	ns

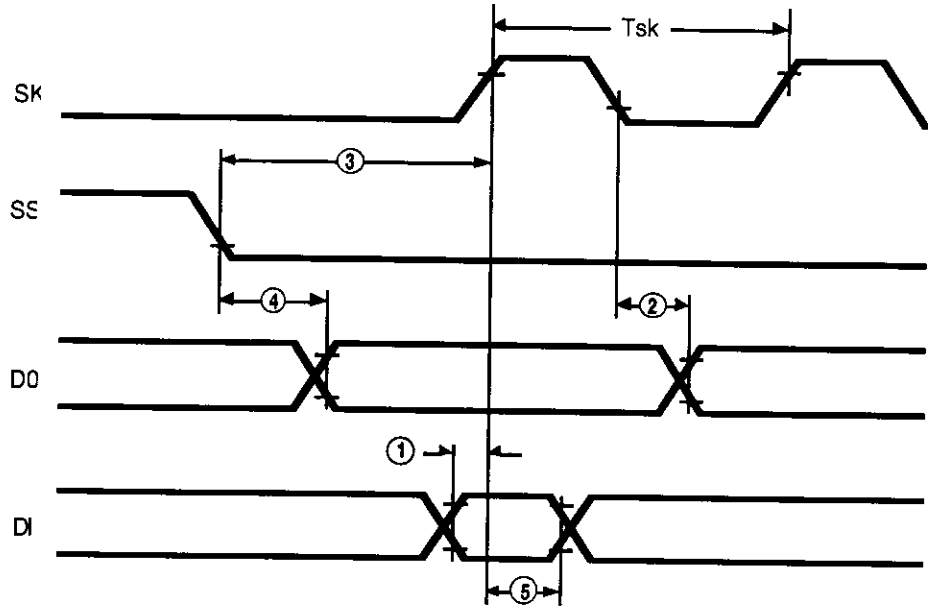


Figure 20. SPI Timing (Z86C06 Only)

FUNCTIONAL DESCRIPTION (Continued)

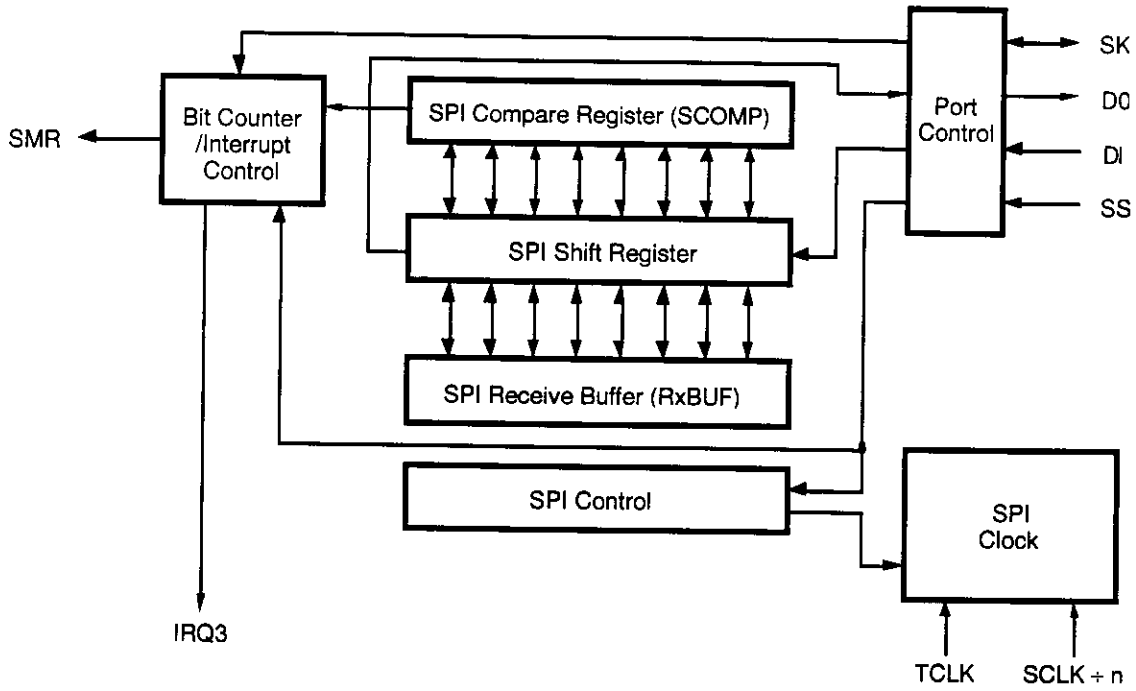


Figure 21. SPI Logic (Z86C06 Only)

PORT Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 22).

Comparator Output Port 3 (D0). Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34, and P35 and a 0 releases the Port to its standard I/O configuration.

Bits D4-D1. These bits are reserved and must be 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting D5=1. The default value is 1.

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting D6=1. The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive, it does not affect the relationship of SCLK and XTAL.

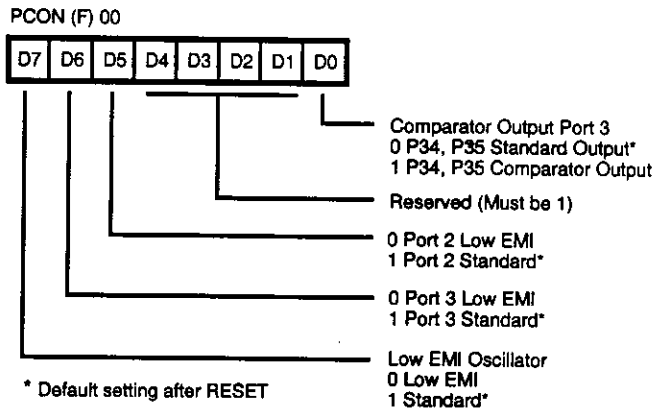


Figure 22. Port Configuration Register (PCON) (Write only)

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 23). All bits are Write Only except bit 7, which is Read Only. Bit 7 is a flag bit that is

hardware set on the condition of a STOP recovery and reset on a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. The recovery level must be active Low to work with SPI. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR specify the source of the Stop-Mode Recovery signal. Bit 1 determines whether the XTAL is divided by 1 or 2. A 0 in this location uses XTAL divide-by-two, and a 1 uses XTAL. The default for this bit is XTAL divide-by-two. Bit 0 controls the divide-by-16 prescaler of SCLK/TCLK. The SMR is located in bank F of the Expanded Register Group at address 0BH.

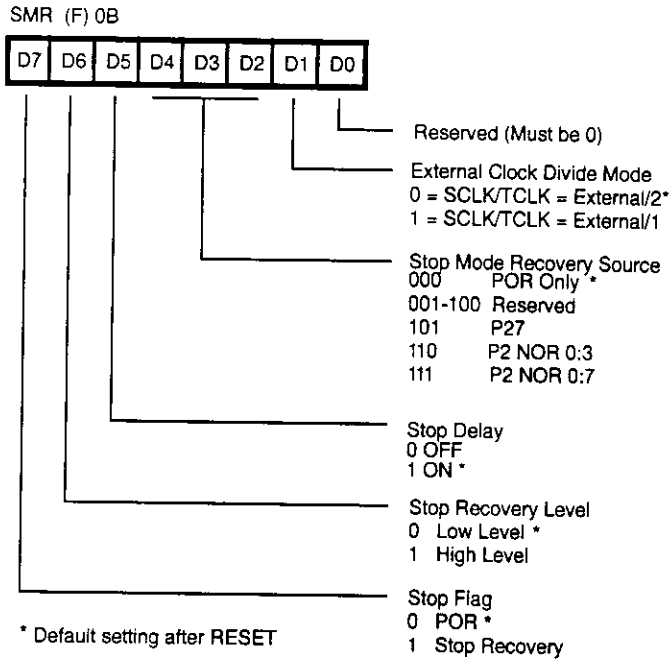


Figure 23. Stop Mode Recovery Register (Write Only except bit D7, which is Read Only.) (Z86C03)

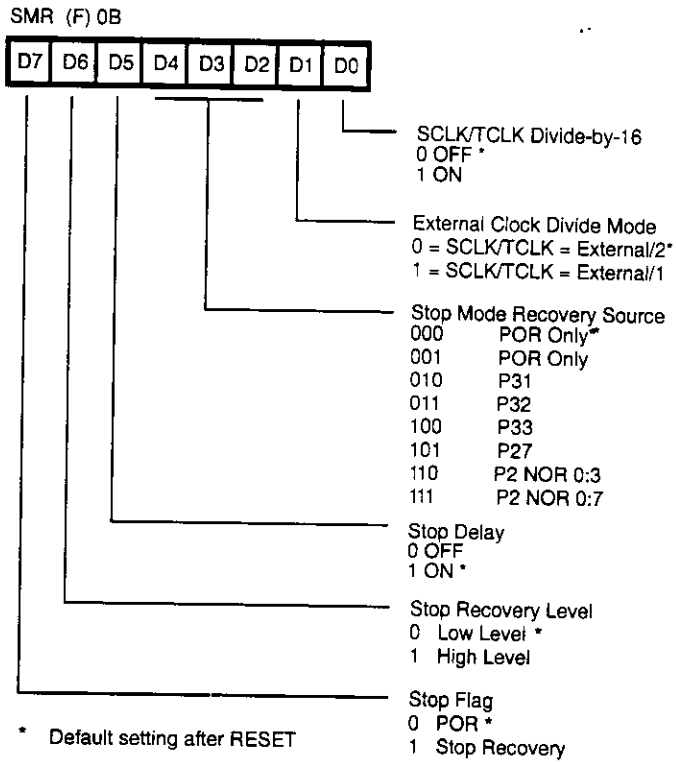


Figure 24. Stop-Mode Recovery Register (Write Only except bit D7, which is Read Only.) (Z86C06)

SCLK/TCLK Divide-by-16 Select (D0)—Z86C06 Only. D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources the counter/timers and interrupt logic).

External Clock Divide Mode (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit, together with D7 of PCON, helps further lower EMI [i.e., D7 (PCON)=0, D1 (SMR=1]. The default setting is 0.

Stop-Mode Recovery Source (D2,D3,D4). These three bits of the SMR specify the wake-up source of the Stop-Mode Recovery (Figure 25 and Table 5).

FUNCTIONAL DESCRIPTION (Continued)

Table 5. Stop-Mode Recovery Source

SMR			Operation
D4	D3	D2	Description of Action
0	0	0	POR recovery only
0	0	1	POR recovery only (C03 = Reserved)
0	1	0	P31 transition (C03 = Reserved)
0	1	1	P32 transition (C03 = Reserved)
1	0	0	P33 transition (C03 = Reserved)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0:3
1	1	1	Logical NOR of Port 2 bits 0:7

P31-P33 cannot wake up from STOP Mode if the input lines are configured as analog inputs. In the Z86C06, when the SPI is enabled and the Compare feature is active, a SMR is generated upon a comparison in the SPI Shift Register and SCOMP Register, regardless of the above SMR Register settings. If SPI Compare is used to wake up the part from STOP Mode, it is still possible to have one of the other Stop-Mode Recovery sources active. **Note:** These other Stop-Mode Recovery sources have to be active level Low (bit D6 in SMR set to 0 if P31, P32, P33, and P27 selected, or bit D6 in SMR set to 1 if logical NOR of Port 2 is selected).

Stop-Mode Recovery Delay Select (D5). This bit disables the 5 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1. If the "fast" wake up is selected, the Stop-Mode Recovery source needs to be kept active for at least 5 TpC.

Stop-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Figures 23 and 24).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. It is active High, and is 0 (cold) on POR/WDT RESET. This bit is Read Only. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

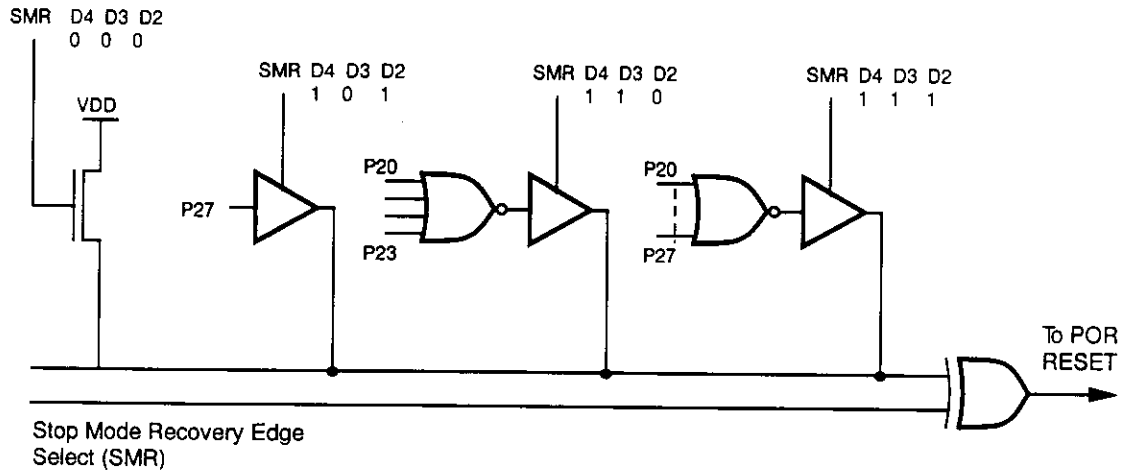
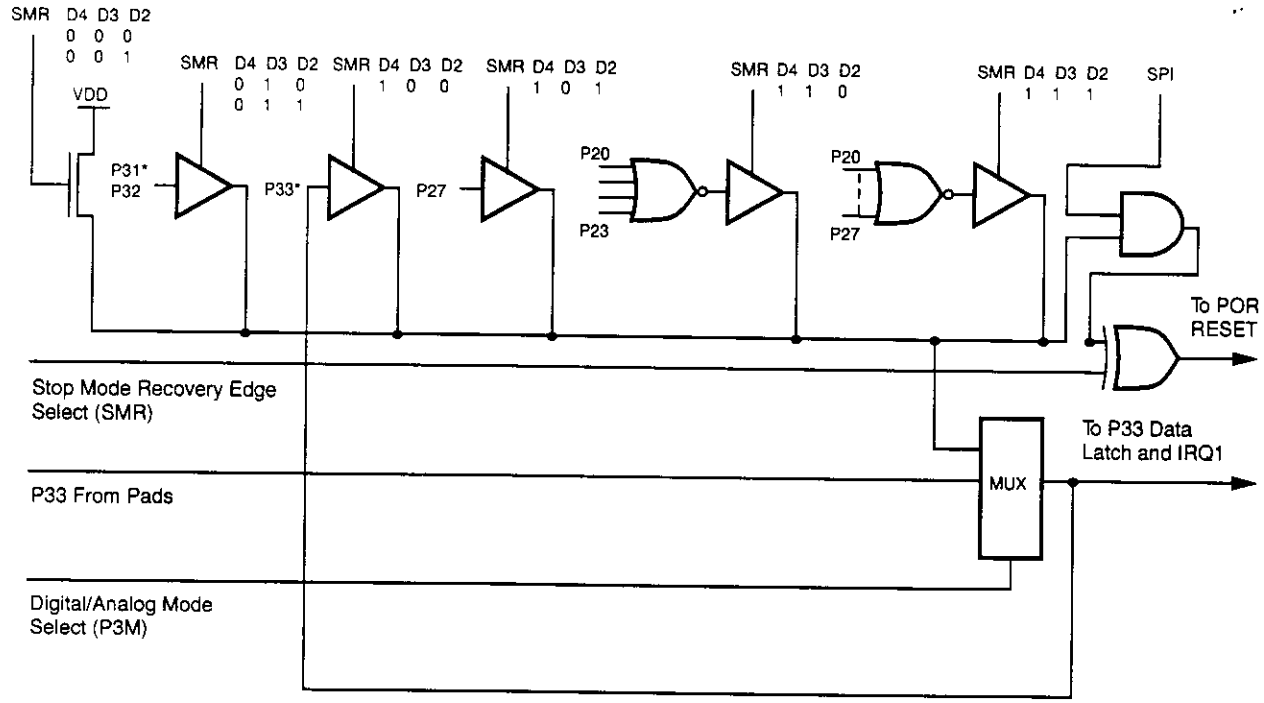


Figure 25. Stop-Mode Recovery Source (Z86C03)



***Note:** P31, P32 and P33 are not in Analog Mode.

Figure 26. Stop-Mode Recovery Source (Z86C06)

FUNCTIONAL DESCRIPTION (Continued)

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled after it has been initially enabled. The WDT circuit is driven by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDTMR register.

Note: Execution of the WDT instruction affects the Z (zero), S (sign), and V (overflow) flags.

Bits 0 and 1 control a tap circuit that determines the timeout period (on Z86C06 only). Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to 1, the WDT is only driven by the external clock during STOP Mode. This feature makes it possible to wake up from STOP Mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 27).

Note: This register is accessible only during the first 64 processor cycles (128 XTAL clocks) from the execution of the first instruction after Power-On Reset, Watch-Dog Reset or a Stop-Mode Recovery (Figure 27). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH.

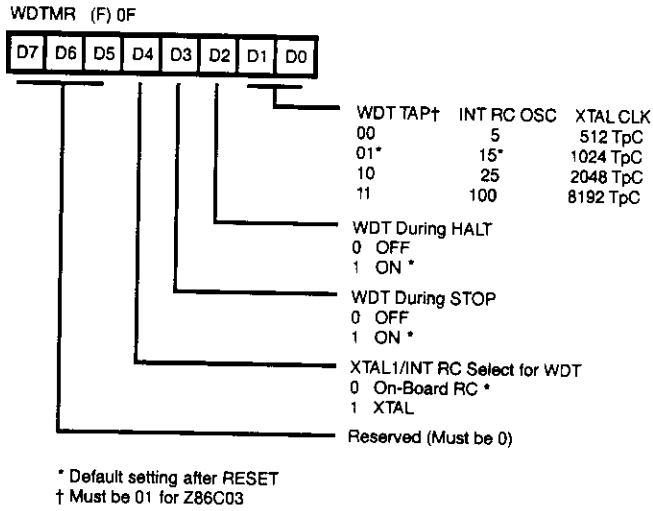
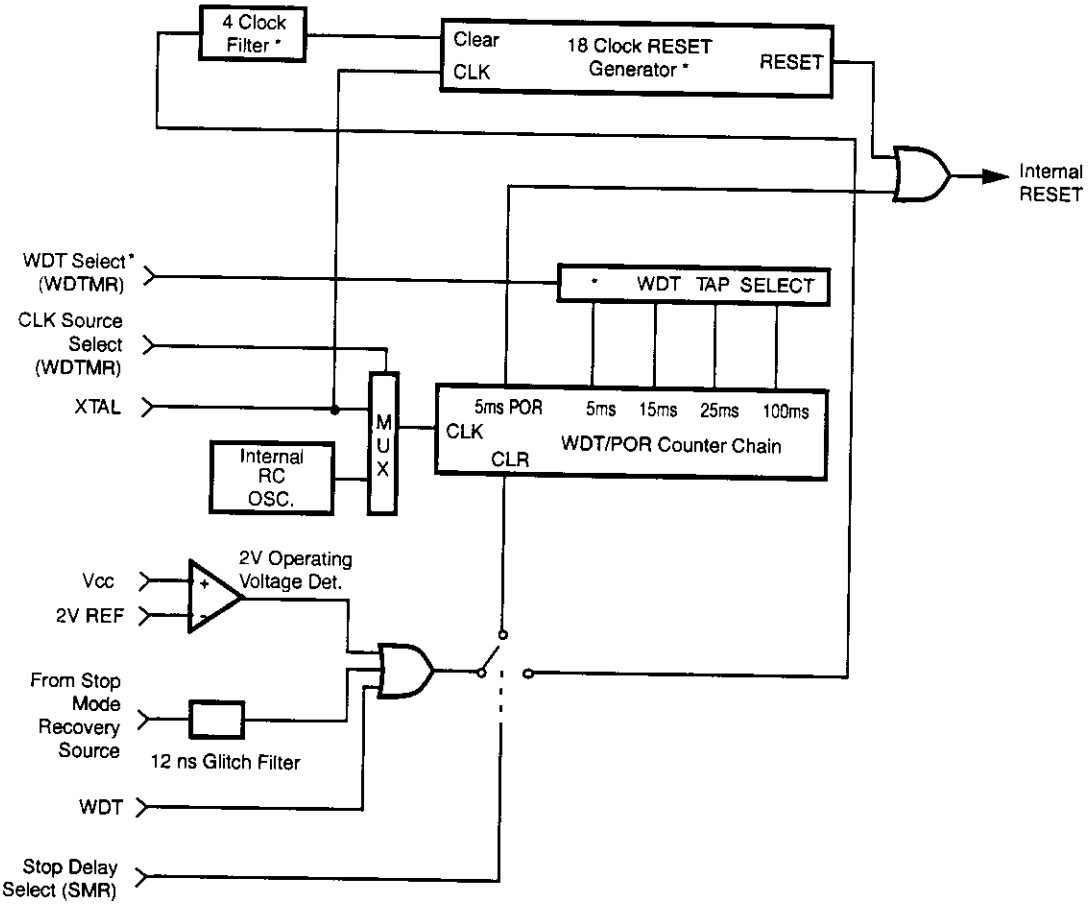


Figure 27. Watch-Dog Timer Mode Register (Write Only)



* Not available on the Z86C03, WDT fixed at 15 ms/1024TpC in the Z86C03.

Figure 28. Resets and WDT

WDT Time Select (D1, D0). Bits 0 and 1 control a tap circuit that determines the time-out period. Table 5 shows the different values that can be obtained. The default value of D0 and D1 are 1 and 0, respectively. (These select bits are present in the Z86C06 only.)

Table 6. Time-Out Period of the WDT (Z86C06 Only)

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256TpC
0	1	15 ms min	512TpC
1	0	25 ms min	1024TpC
1	1	100 ms min	4096TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 15 ms, D0 = 1 and D1 = 0.
The values given are for V_{CC} = 5.0V.
For the Z86C03, the WDT time-out value is fixed at 1024 TpC (depending on WDTMR bit D4) period. When writing to the WDTMR in the Z86C03, bit D0 must be 1 and D1 must be 0.

FUNCTIONAL DESCRIPTION (Continued)

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1. If bits D3 and D4 are both set to 1, the WDT only, is driven by the external clock during STOP mode.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the internal RC oscillator.

Bits 5, 6 and 7. These bits are reserved.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the specified voltage (typically 2.1V).

Low Voltage Protection (V_{LV}). The Low Voltage Protection trip point (V_{LV}) will be less than 3 volts and above 1.4 volts under the following conditions.

Maximum (V_{LV}) Conditions:

Case 1:	T_A = –40° to +105°C, Internal Clock (SCLK) Frequency equal or less than 1 MHz
Case 2:	T_A = –40° to +85°C, Internal Clock (SCLK) Frequency equal or less than 2 MHz

Note: The internal clock frequency (SCLK) is determined by SMR (F) 0BH bit D1.

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device is guaranteed to function normally until the Low Voltage Protection trip point (V_{LV}) is reached, for the temperatures and operating frequencies in cases 1 and 2 above. The actual low voltage trip point is a function of temperature and process parameters (Figure 29).

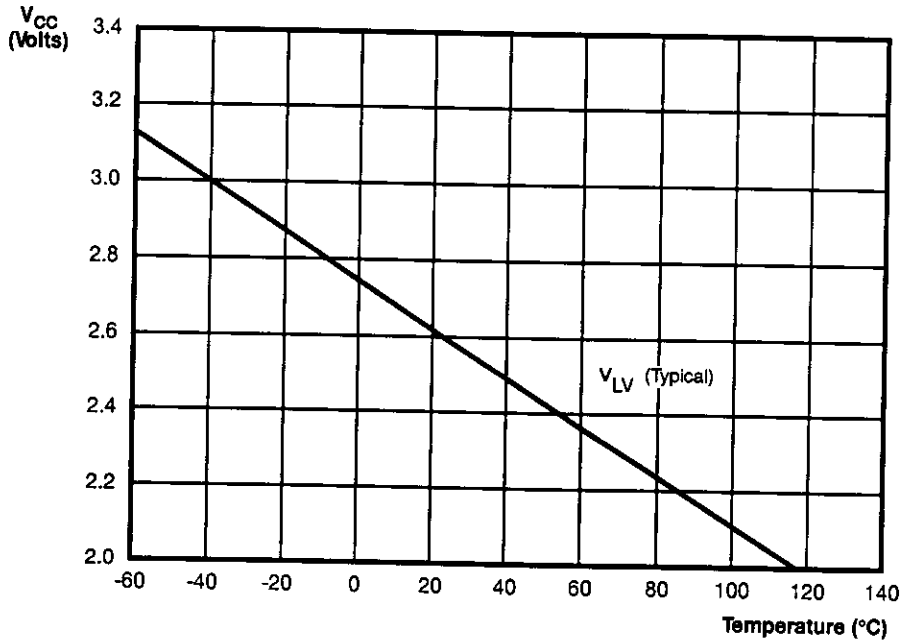
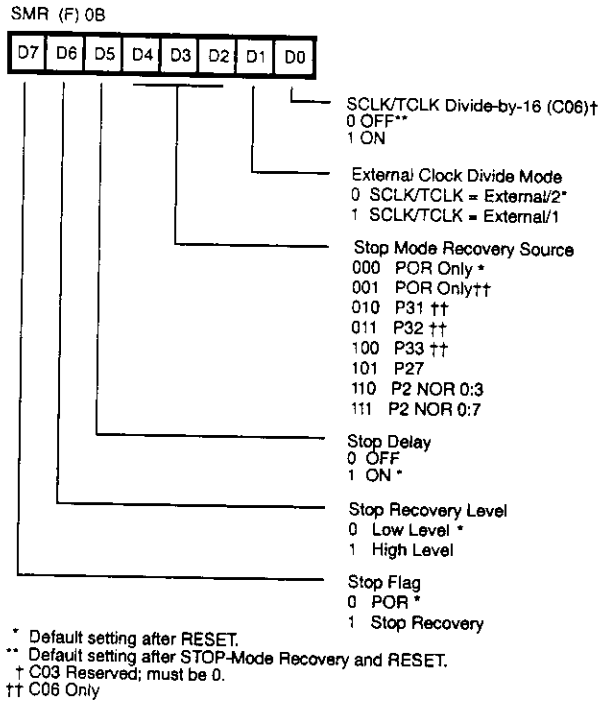


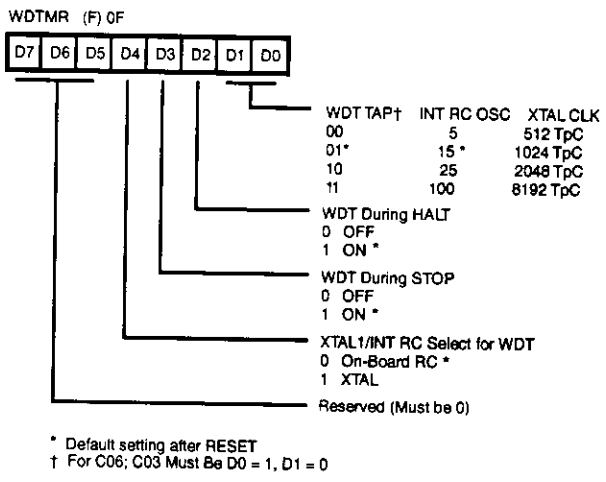
Figure 29. Typical Z86C03/C06 V_{LV} Voltage vs Temperature

EXPANDED REGISTER FILE CONTROL REGISTERS



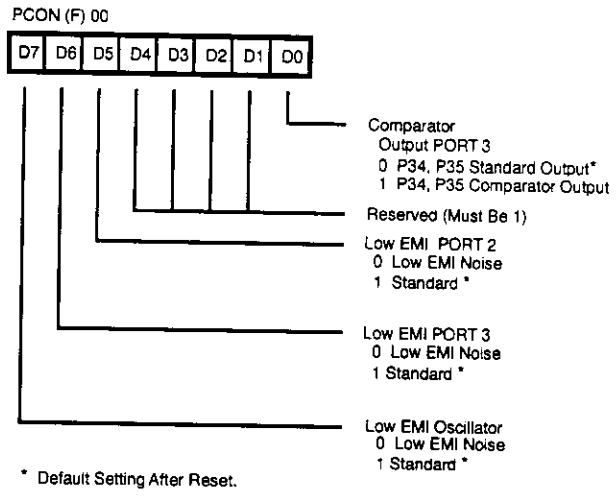
* Default setting after RESET.
** Default setting after STOP-Mode Recovery and RESET.
† C03 Reserved; must be 0.
†† C06 Only

Figure 30. Stop-Mode Recovery Register (Write Only except bit D7, which is Read Only)



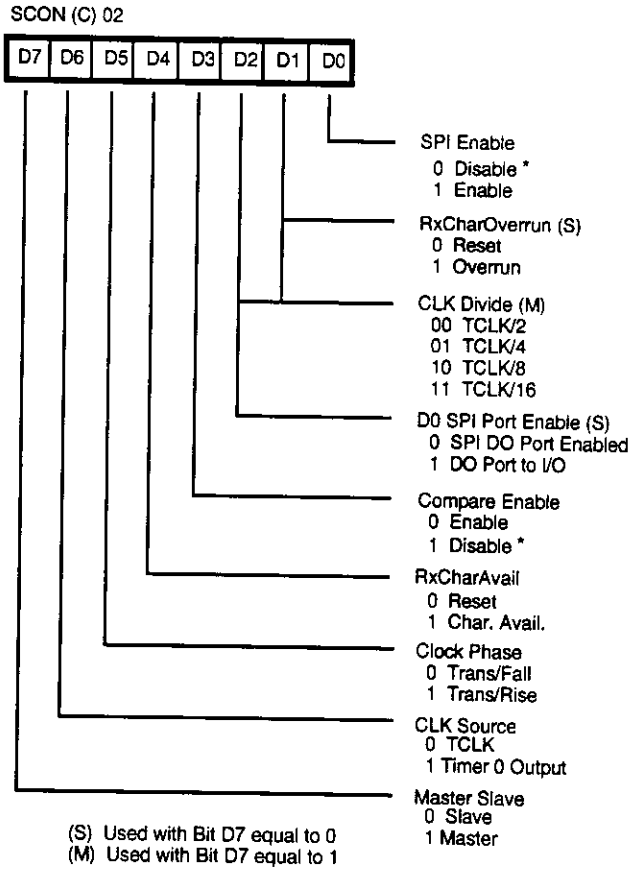
* Default setting after RESET
† For C06; C03 Must Be D0 = 1, D1 = 0

Figure 31. Watch-Dog Timer Mode Register (Write Only)



* Default Setting After Reset.

Figure 32. PORT Control Register (Write Only)



(S) Used with Bit D7 equal to 0
(M) Used with Bit D7 equal to 1

* Default Setting After Reset.

Figure 33. SPI Control Register (Z86C06 Only)

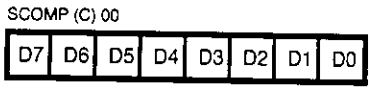


Figure 34. SPI Compare Register (Z86C06 Only)

Figure 35. SPI Receive Buffer (Z86C06 Only)

Z8 CONTROL REGISTER DIAGRAMS

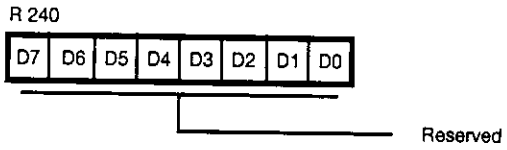


Figure 36. Reserved

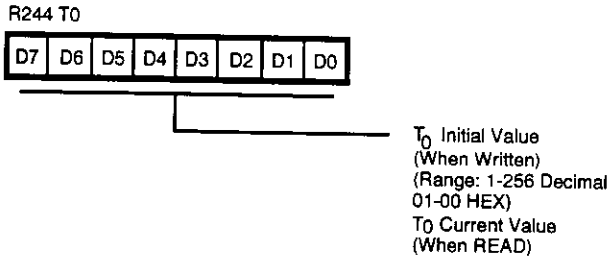


Figure 38. Counter Timer 1 Register (F2H: Read/Write)

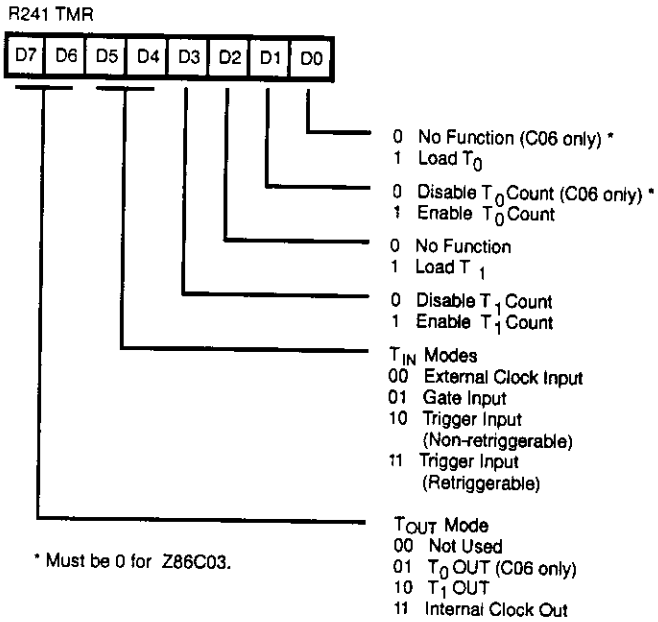


Figure 37. Timer Mode Register (F1H: Read/Write)

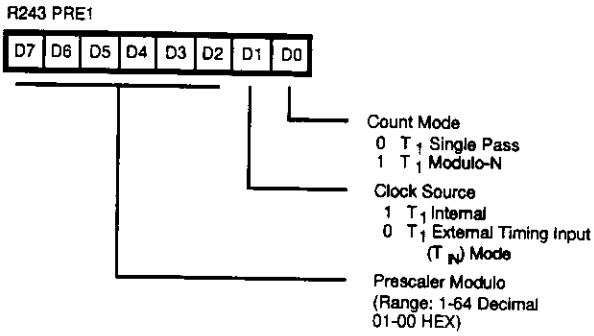


Figure 39. Prescaler 1 Register (F3H: Write Only)

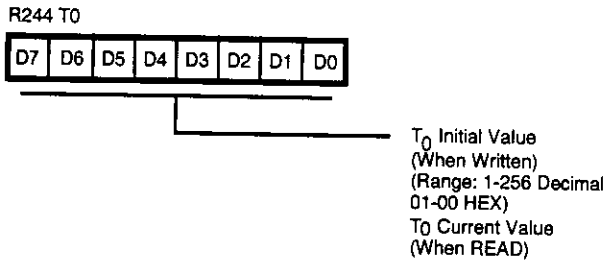


Figure 40. Counter/Timer 0 Register (F4H: Read/Write; Z86C06 Only)

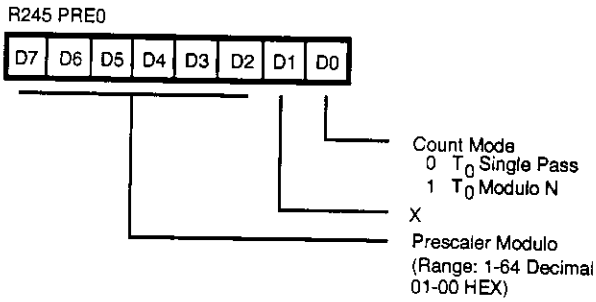


Figure 41. Prescaler 0 Register (F5H: Write Only; Z86C06 Only)

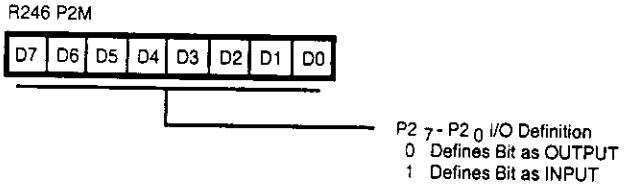


Figure 42. Port 2 Mode Register (F6H: Write Only)

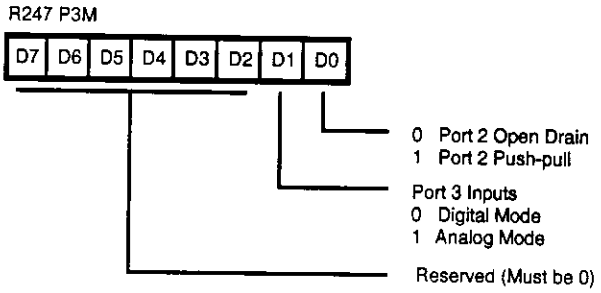


Figure 43. Port 3 Mode Register (F7H: Write Only)

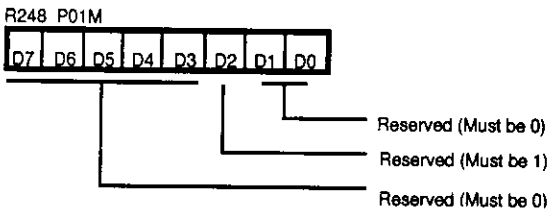


Figure 44. Port 0 and 1 Mode Register (F8H: Write Only)

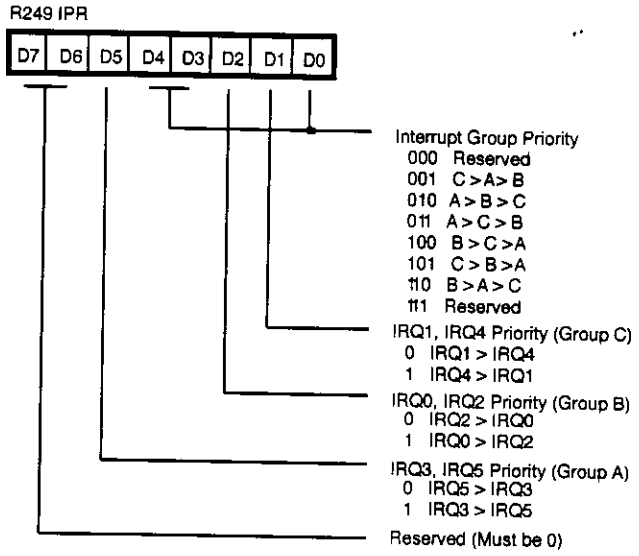


Figure 45. Interrupt Priority Register (F9H: Write Only)

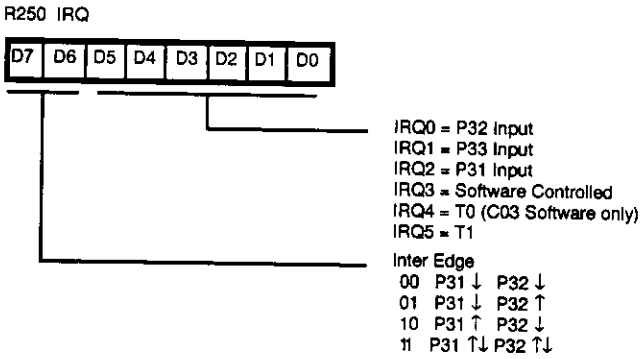


Figure 46. Interrupt Request Register (FAH: Read/Write)

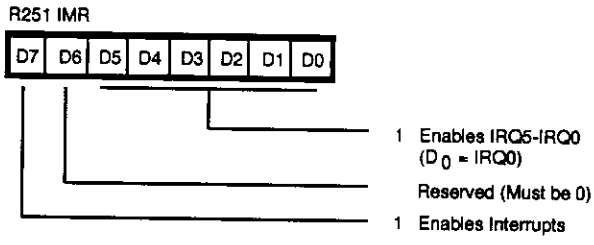


Figure 47. Interrupt Mask Register (FBH: Read/Write)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

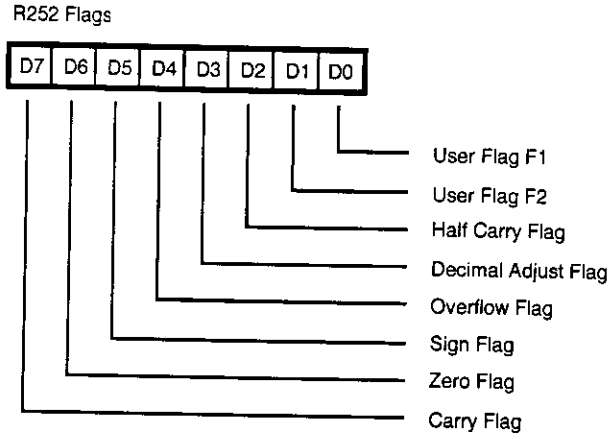


Figure 48. Flag Register (FCH: Read/Write)

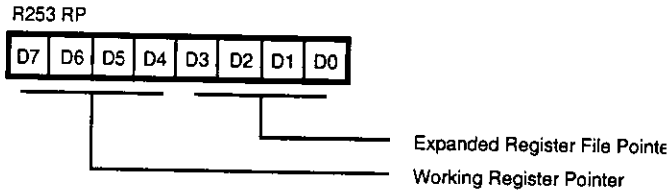


Figure 49. Register Pointer (FDH: Read/Write)

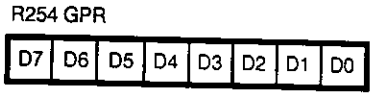


Figure 50. General Purpose Register (FEH: Read/Write)

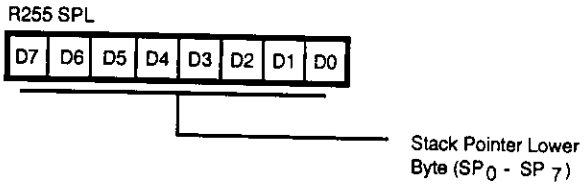


Figure 51. Stack Pointer (FFH: Read/Write)

DEVICE CHARACTERISTICS

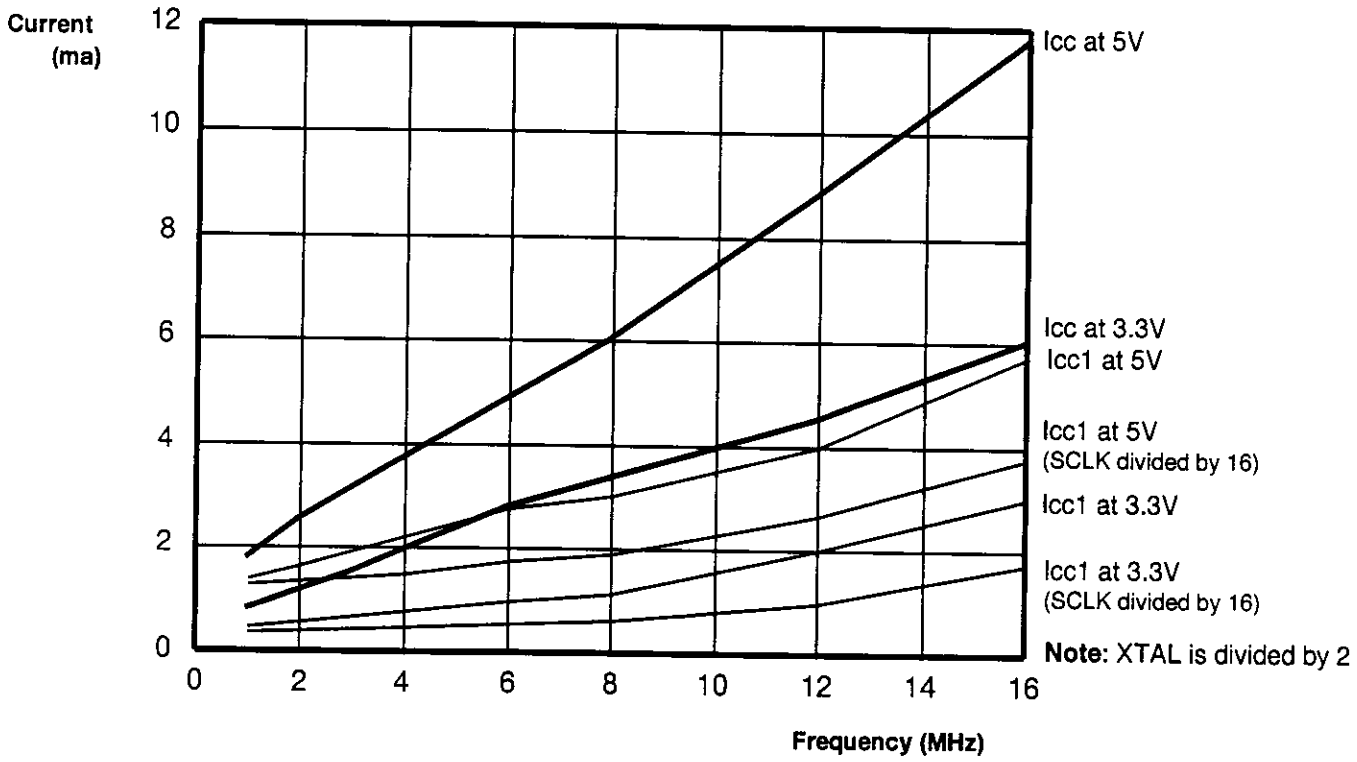
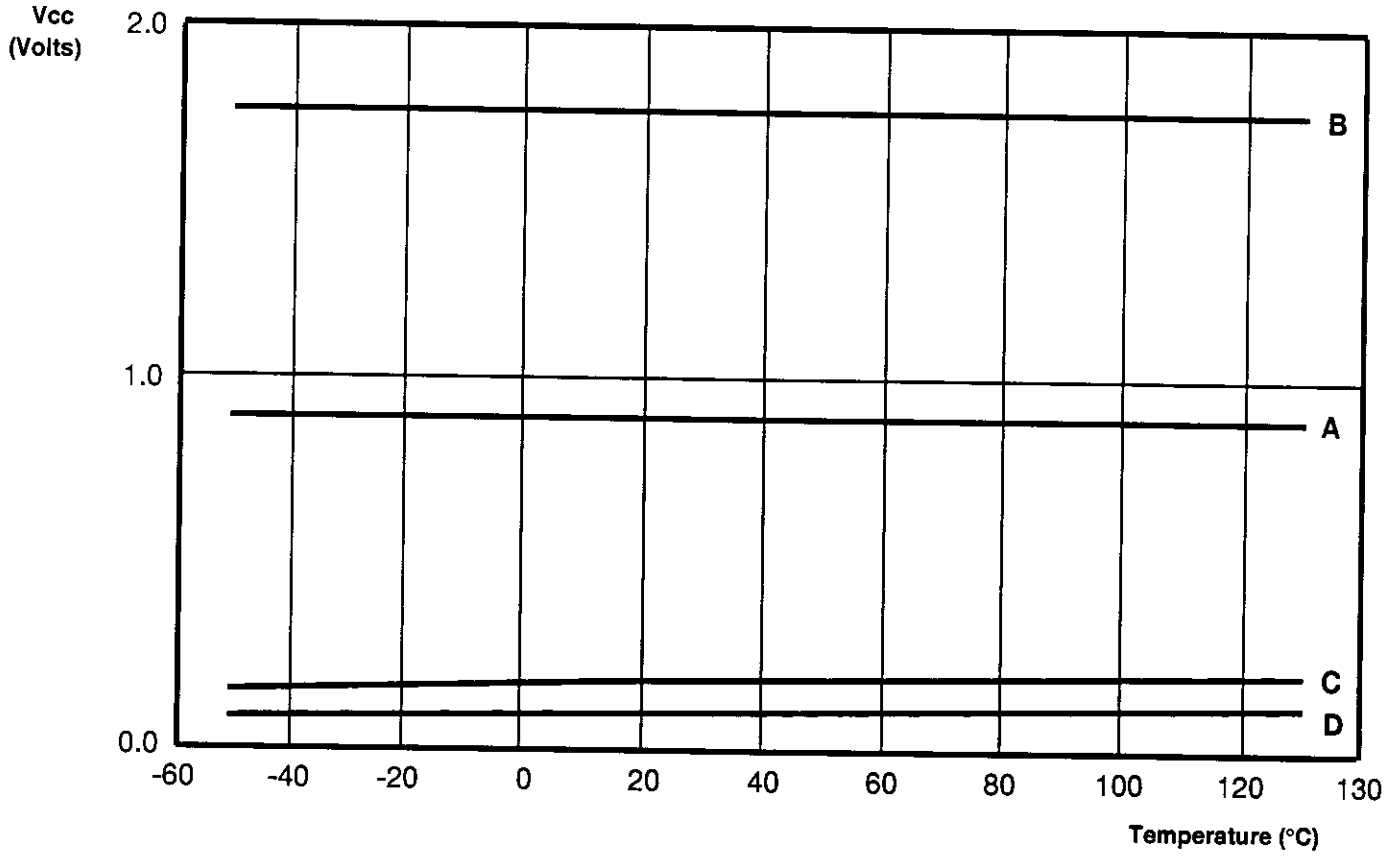


Figure 52. Typical I_{CC} vs Frequency

DEVICE CHARACTERISTICS (Continued)



Legend:
A = Vil at Vcc = 3.3V B = Vil at Vcc = 5.5V C = Vol at Vcc = 3.0V D = Vol at Vcc = 5.5V

Figure 53. Typical V_{OL}, V_{IL} vs Temperature

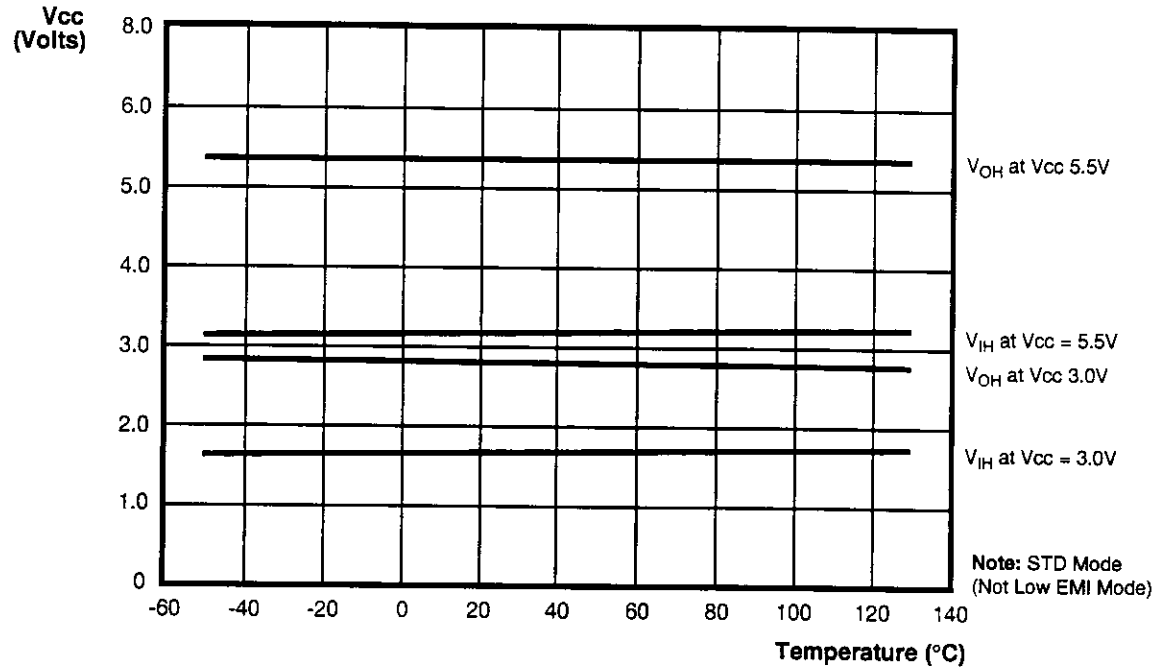


Figure 54. Typical V_{OH}, V_{IH} vs Temperature

DEVICE CHARACTERISTICS (Continued)

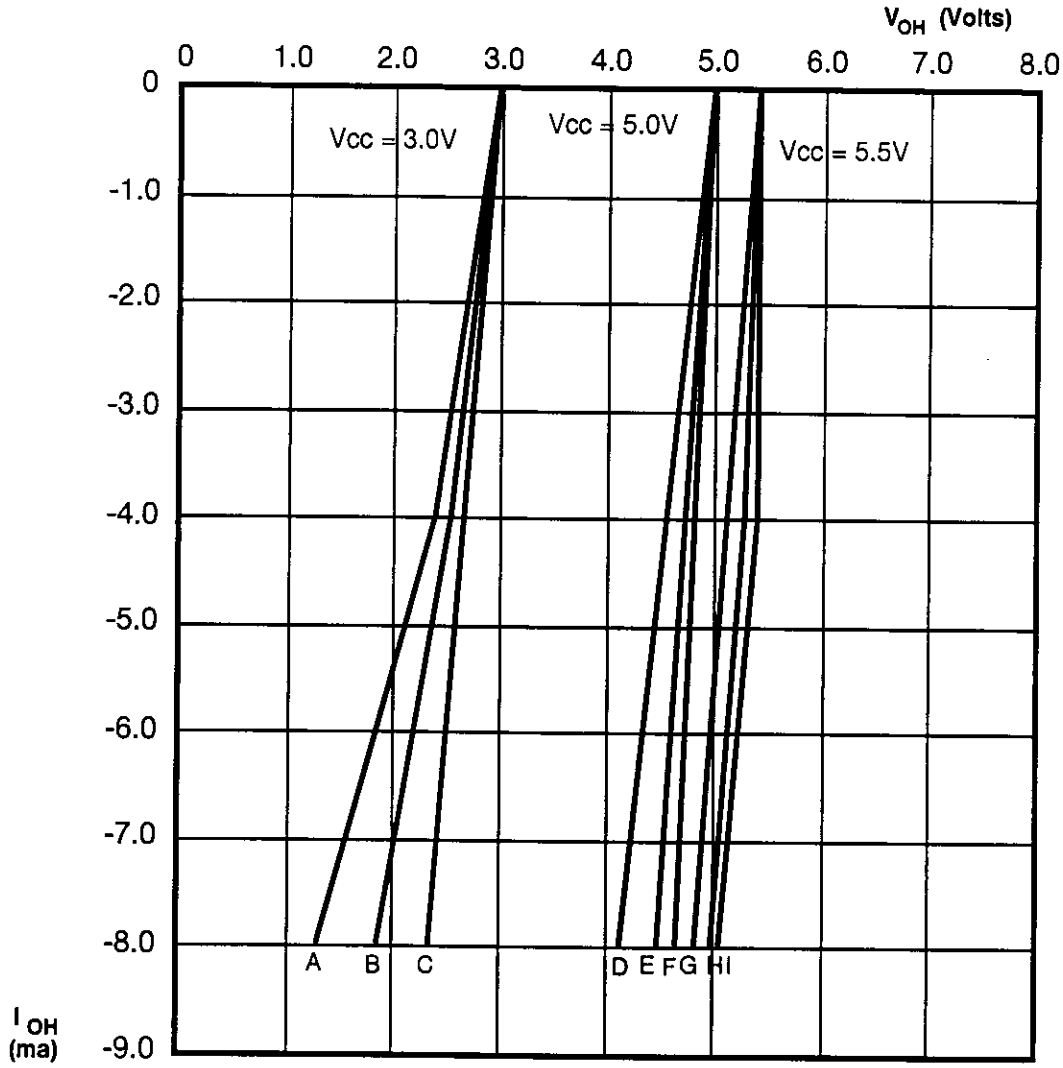


Figure 55. Typical V_{OH} vs I_{OH} Over Temperature

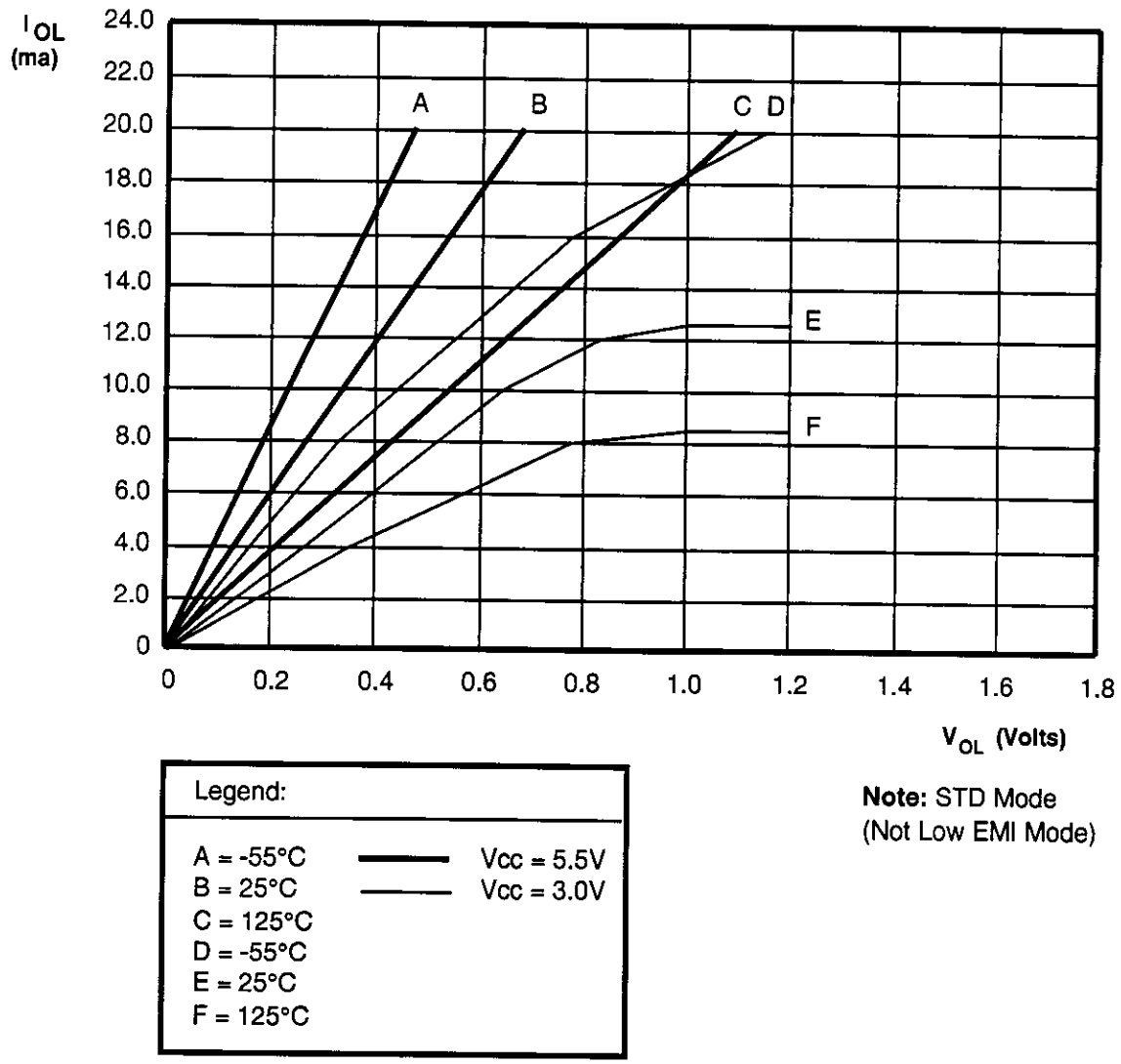


Figure 56. Typical I_{OL} vs V_{OL} Over Temperature

DEVICE CHARACTERISTICS (Continued)

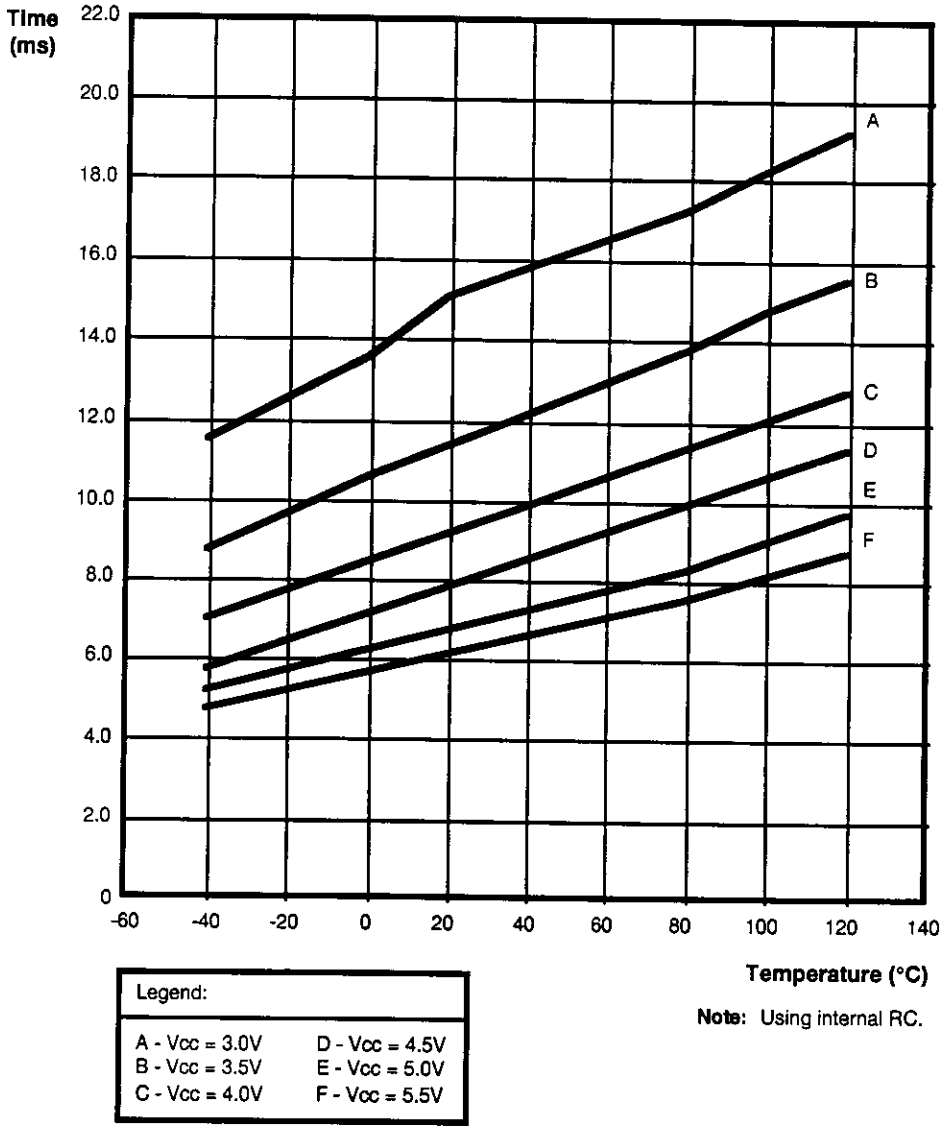
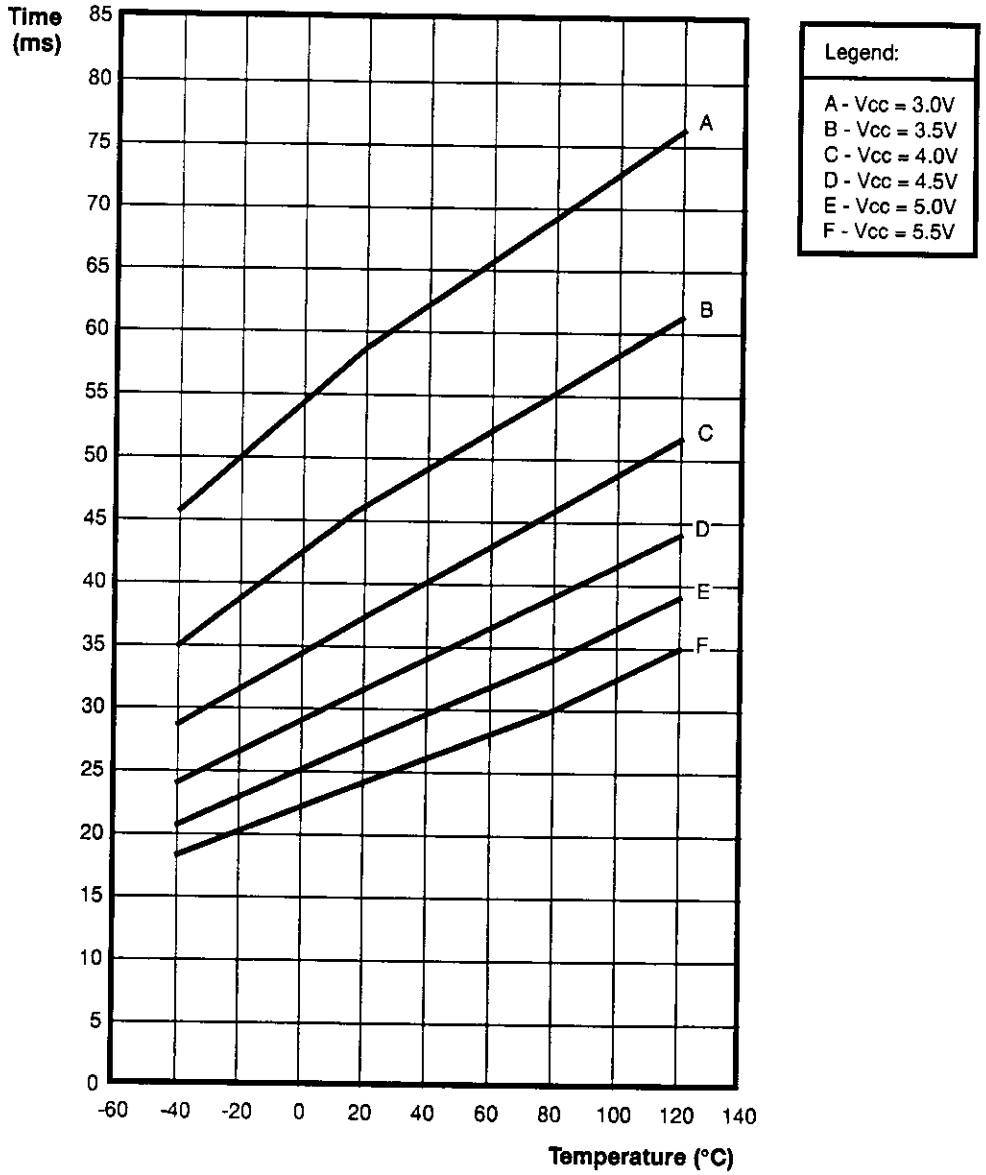


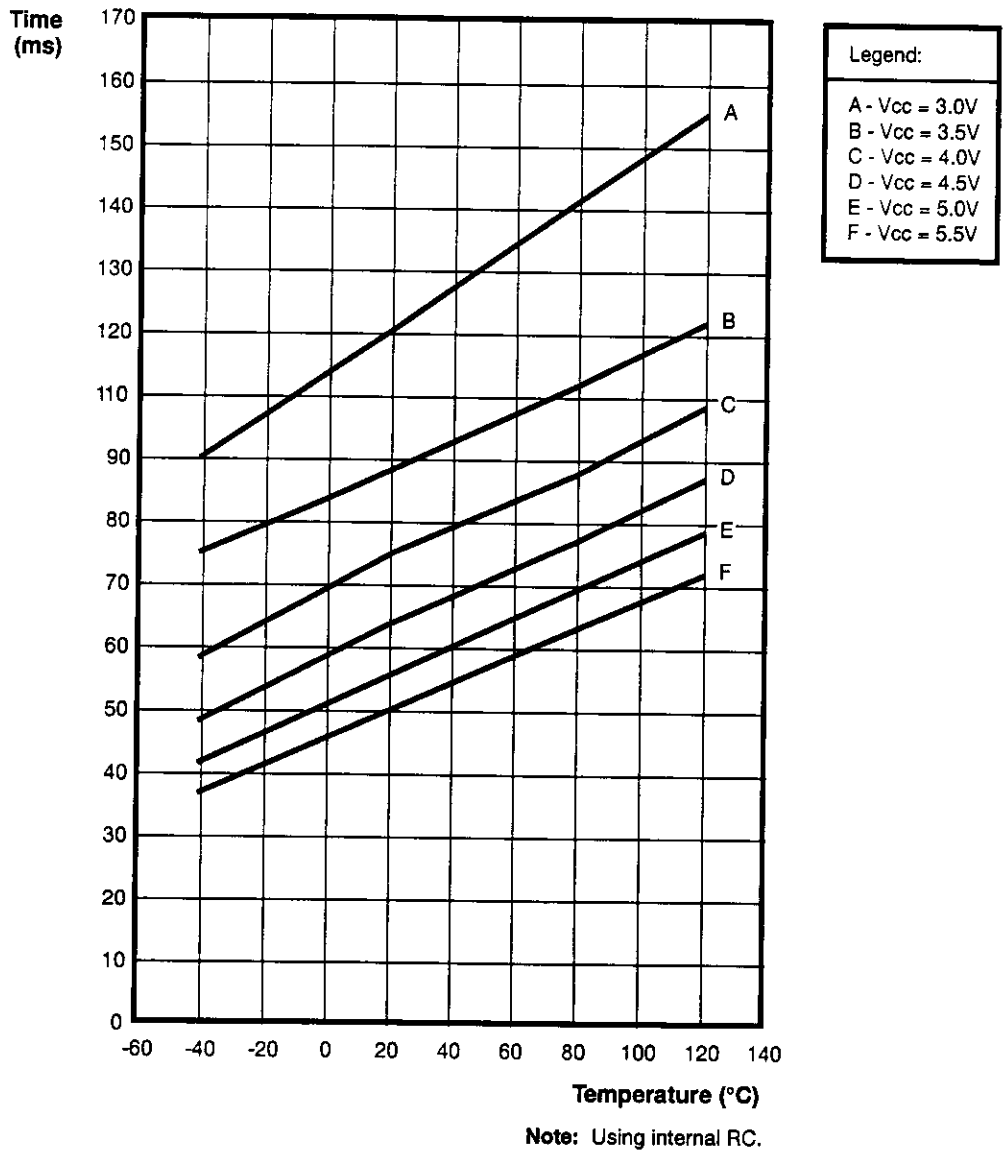
Figure 57. Typical Power-On Reset Time vs Temperature



Note: Using internal RC.

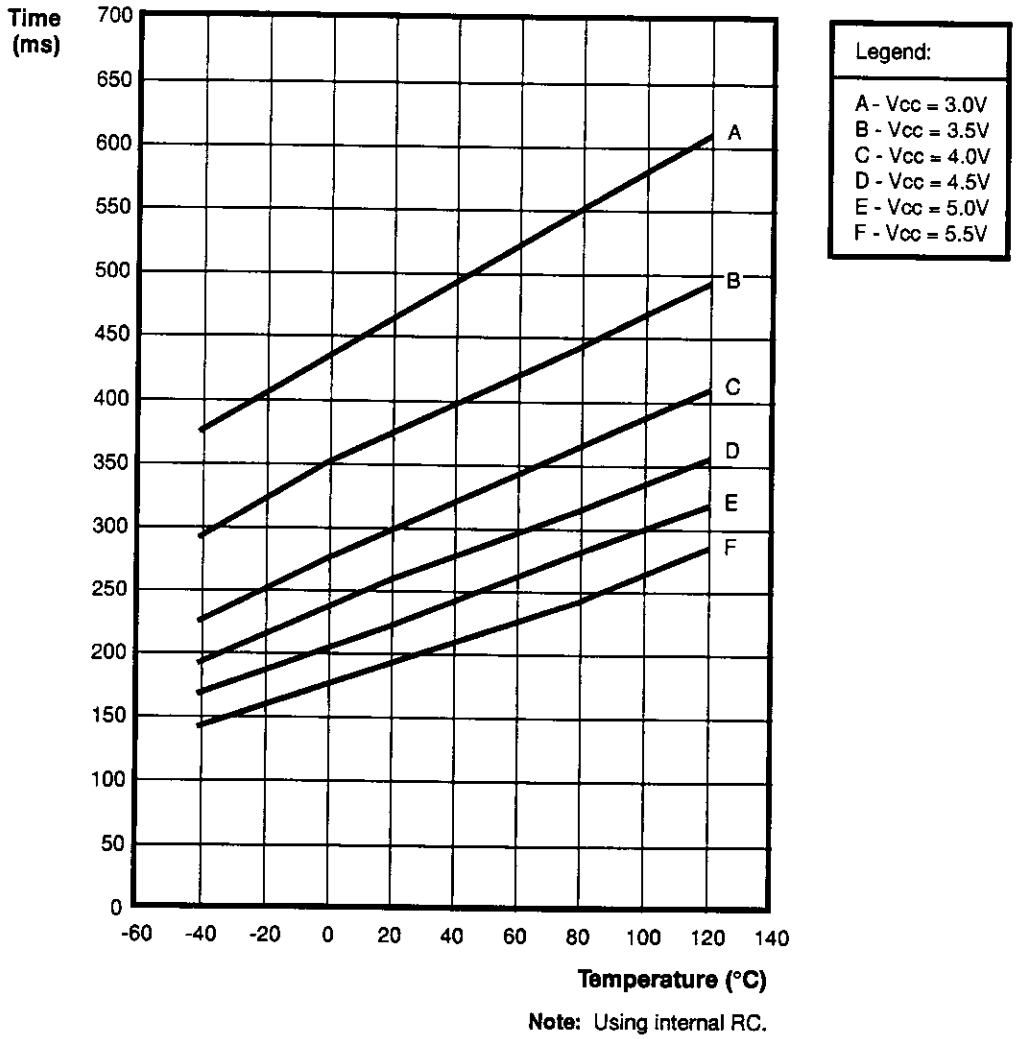
Figure 58. Typical 15 ms WDT Setting vs Temperature (Z86C06 Only)

DEVICE CHARACTERISTICS (Continued)



Note: Using internal RC.

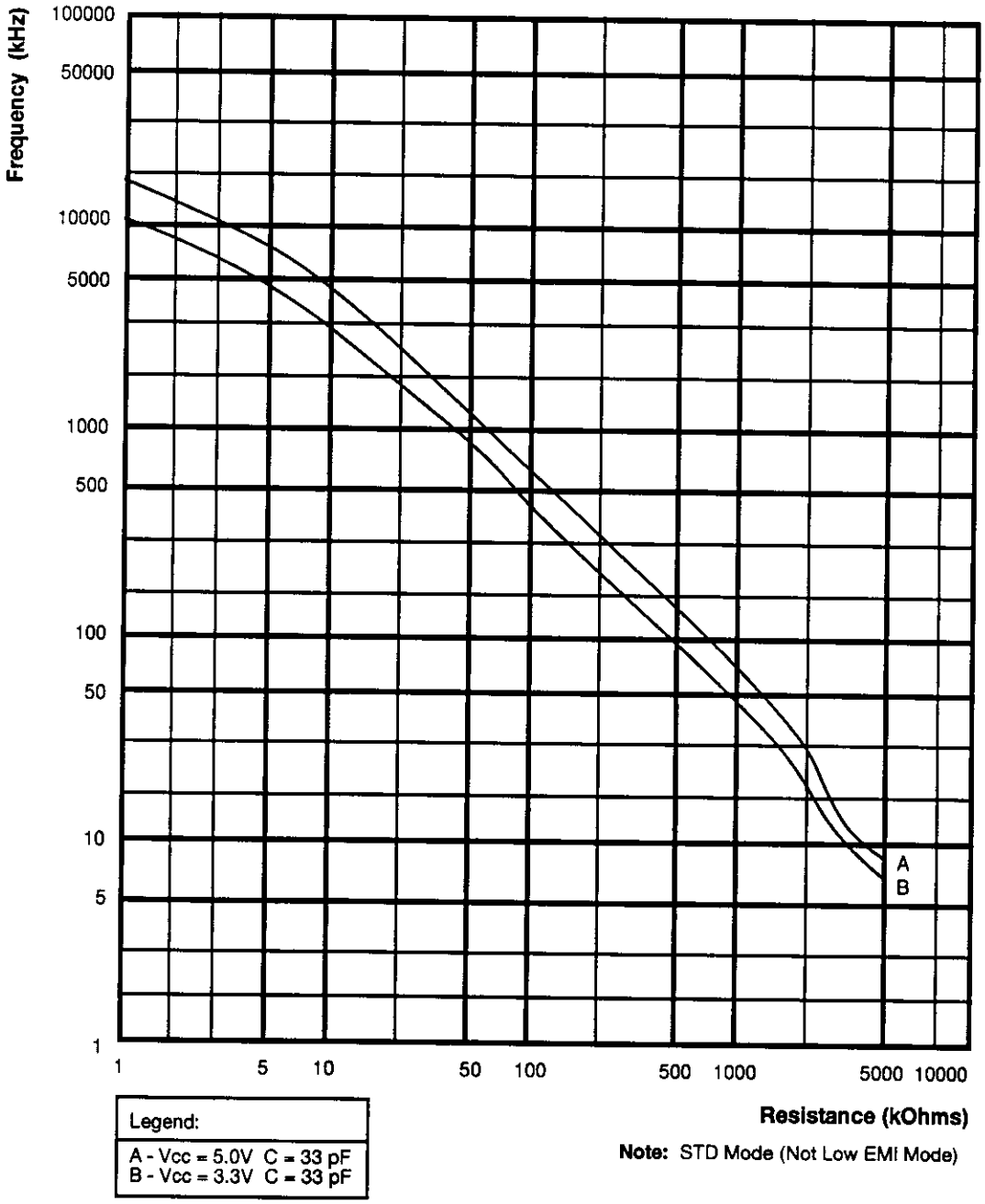
Figure 59. Typical 25 ms WDT Setting vs Temperature (Z86C06 Only)



Note: Using internal RC.

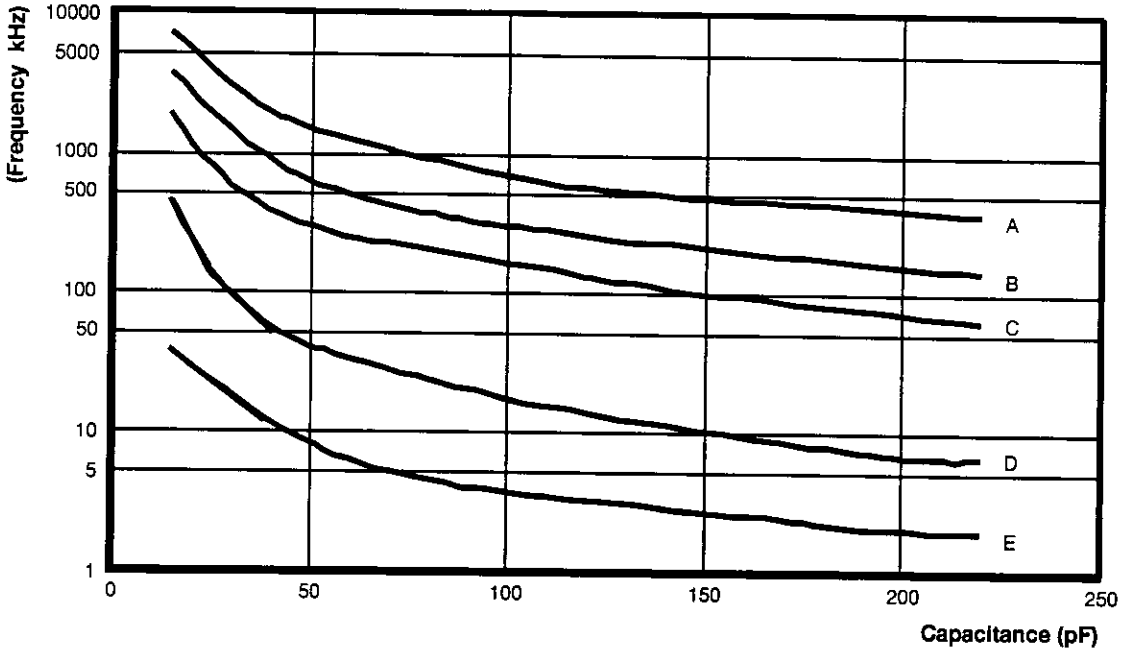
Figure 60. Typical 100 ms WDT Setting vs Temperature (Z86C06)

DEVICE CHARACTERISTICS (Continued)



Note: This chart for reference only. Each process will have a different characteristic curve.

Figure 61. Typical Frequency vs RC Resistance



Note: STD Mode (Not Low EMI Mode)

Legend:
A - Vcc = 5.0V R = 22 K Ohms B - Vcc = 5.0V R = 56 K Ohms C - Vcc = 5.0V R = 100 K Ohms D - Vcc = 5.0V R = 1 M Ohms C - Vcc = 5.0V R = 4 M Ohms

Figure 62. Typical RC Resistance/Capacitance vs Frequency

DEVICE CHARACTERISTICS (Continued)

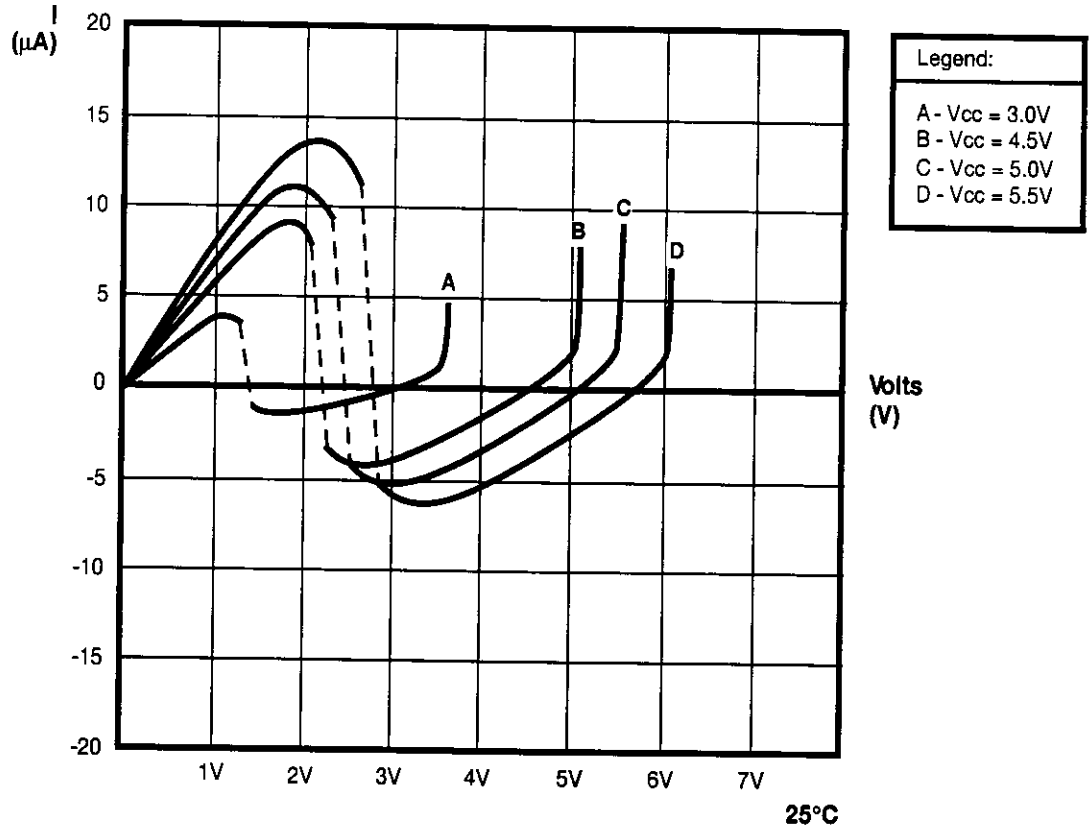
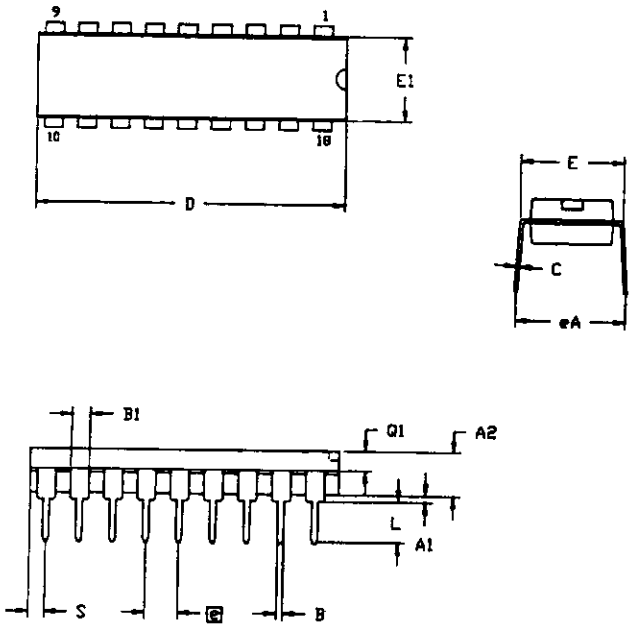


Figure 63. Auto Latch Characteristics

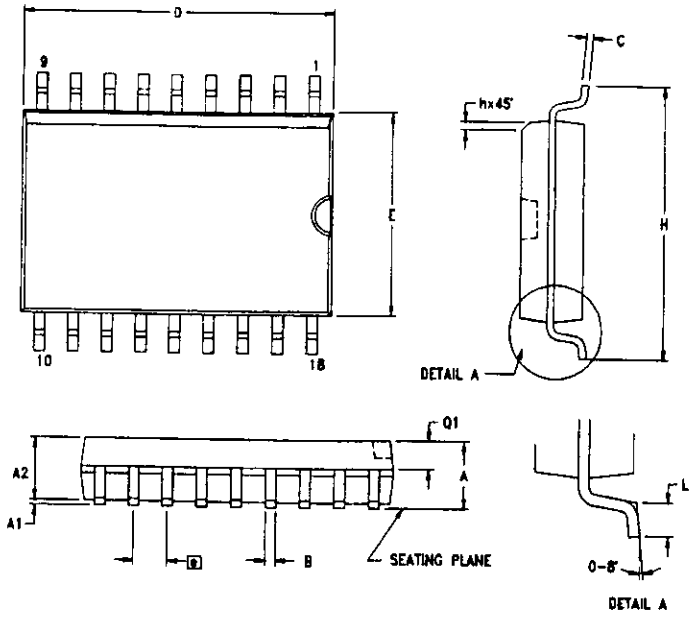
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 64. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 65. 18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C03 (8 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86C0308PSC	Z86C0308SSC	Z86C0308PEC	Z86C0308SEC

Z86C06 (12 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86C0612PSC	Z86C0612SSC	Z86C0612PEC	Z86C0612SEC

For fast results, contact your local Zilog sale offices for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
S = Plastic SOIC

Preferred Temperature
S = 0°C to +70°C

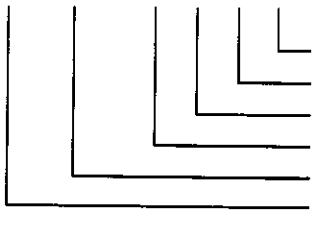
Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86C03 08 P S C is a Z86C03, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



ORDERING INFORMATION

Z86C03 (8 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86C0308PSC	Z86C0308SSC	Z86C0308PEC	Z86C0308SEC

Z86C06 (12 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86C0612PSC	Z86C0612SSC	Z86C0612PEC	Z86C0612SEC

For fast results, contact your local Zilog sale offices for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
S = Plastic SOIC

Preferred Temperature
S = 0°C to +70°C

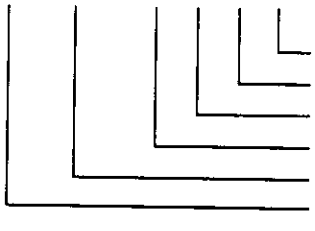
Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86C03 08 P S C is a Z86C03, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



LIMITATION

The SPI does not function on the Z86C06.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com