(MARCOM) DC2564 DOCUMENT CONTROL MASTER



PRELIMINARY PRODUCT SPECIFICATION

Z86L06 Low Voltage CMOS Z8® CCP™ Consumer Controller Processor

Z86L06

LOW VOLTAGE CMOS Z8® CCP™ CONSUMER CONTROLLER PROCESSOR

FEATURES

- 8-bit CMOS microcontroller
- 18-pin DIP package
- Low cost
- 2.0 to 3.6 volt operating range
- Two standby modes STOP and HALT
- 14 input/output lines (two with comparator inputs)
- 1 Kbyte of ROM
- 124 bytes of RAM
- Four expanded registers (file control registers)
- Two programmable 8-bit Counter/Timers
- High current output: (1)-7 ma source at 2 volts, (1)-10 ma sink at 2 volts.

- 6-bit programmable prescaler
- Six vectored, priority interrupts from five different sources
- Clock speed 8 MHz @ 2.0V
- Watch-Dog/Power-On-Reset Timer
- Two comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, RC, or external clock drive.
- Low EMI noise mode
- From 0°C to +70°C operation
- Brown-Out protection
- Auto Latches

GENERAL DESCRIPTION

The Z86L06 low voltage CCP (Consumer Controller Processor) is a member of the Z8 single-chip microcontroller family with 1 Kbyte of ROM, and 124 bytes of general-purpose RAM. The device is housed in an 18-pin DIP, and is manufactured in low voltage CMOS technology. Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. Now with the low voltage process this same processor may operate down to 2.0 volts.

The Z86L06 architecture is based on Zilog's 8-bit microcontroller core with the addition of an Expanded Register File which allows access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, and a number of ancillary features that are useful in many consumer, industrial, automotive, and advanced scientific applications.

The device applications demand powerful I/O capabilities. The CCP fulfills this with 14 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Three basic address spaces are available to support this wide range of configurations; Program Memory, Register File, and Expanded Register File. The Register File is composed of 124 bytes of general-purpose registers, two I/O port registers and fifteen control and status registers. The Expanded Register File consists of three control registers.

With powerful peripheral features such as on-board comparators, counter/timers, watch-dog timer, and serial peripheral interface, the Z86L06 meets the needs for most sophisticated controller applications (Figure 1).

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GENERAL DESCRIPTION (Continued)

Notes:

All Signals with a preceding front slash, "f", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device	
Power	V	V _{po}	
Ground	GND	V _{ss}	

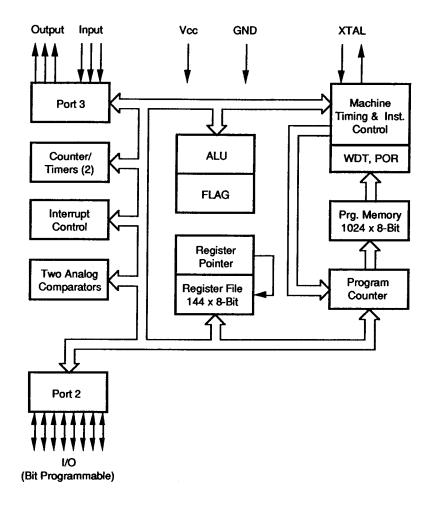


Figure 1. Functional Block Diagram

PIN DESCRIPTION

Table 1. Pin Identification

No Symbol		Function	Direction	
1-4	P24-7	Port 2 pin 4, 5, 6, 7	In/Output	
5	V_{∞}	Power Supply	·	
6	XŤĂL2	Crystal Oscillator Clock	Output	
7	XTAL1	Crystal Oscillator Clock	Input	
8-10	P31-3	Port 3 pin 1, 2, 3	Fixed Input	
11-13	P34-6	Port 3 pin 4, 5, 6	Fixed Output	
14	GND	Ground		
15-18	P20-3	Port 2 pin 0, 1, 2, 3	In/Output	

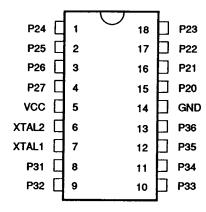


Figure 2. Pin Configuration

PIN FUNCTIONS

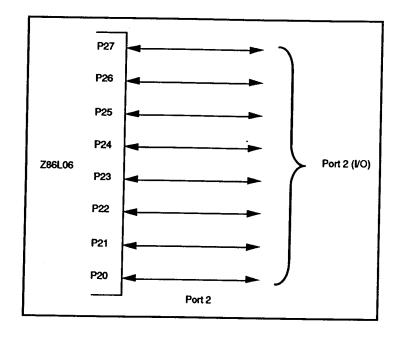
XTAL1. Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2 P20-P27. Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open drain (Figure 3).

Port 3 P31-P36. Port 3 is a 6-bit, CMOS compatible port. These six lines consist of three fixed inputs (P31-P33) and three fixed outputs (P34-P36). Pins P31, P32 and P33 are standard CMOS inputs and pins P34, P35, and P36 are push-pull outputs. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (bit 1). Pins P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input. Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). (Figures 4a and 4b).

PIN FUNCTIONS (Continued)



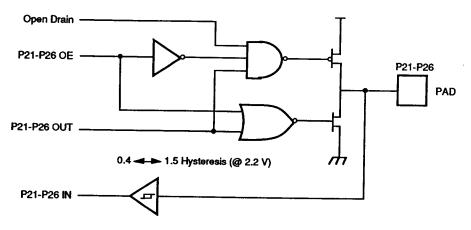
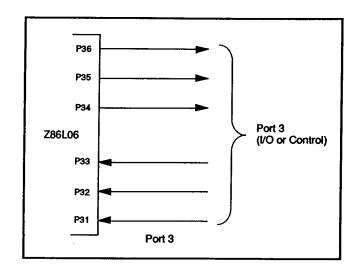


Figure 3. Port 2 Configuration



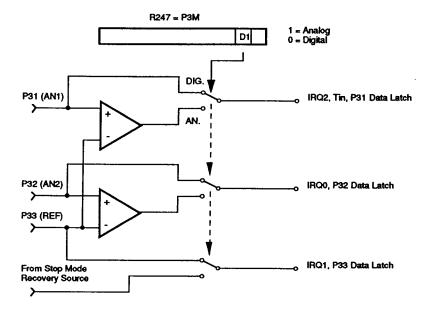


Figure 4a. Port 3 Configuration

PIN FUNCTIONS (Continued)

PORT Configuration Register (PCON). The Port Configuration Register (PCON) configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at Bank F, location 00 (Figure 5). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P35 (Figure 4b), and a 0 releases the Port to its standard I/O configuration. Bits 5 and 6 of this register

configure Ports 2 and 3, respectively, for low EMI operation. A 1 in these locations configures the port for standard operation, and a 0 configures the port for low EMI operation. Finally, bit 7 of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low noise drive. Note that the PCON Register is reset upon the occurrence of a STOP Mode Recovery, any WDT Reset, and Power-On Reset.

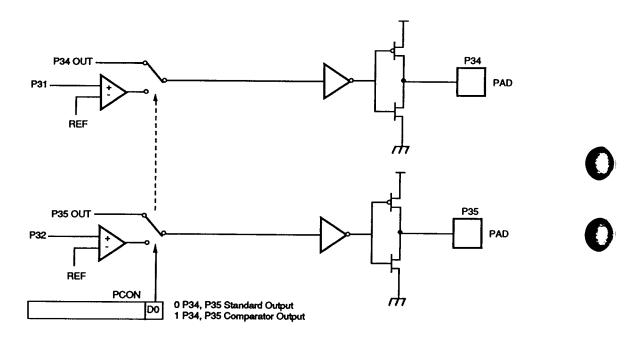
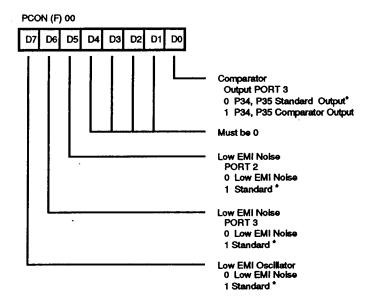


Figure 4b. Port 3 Configuration

Low EMI Option. The Z86L06 can be programmed to operate in a low EMI emission mode by the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- Low current consumption during the HALT mode.
- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 800 Ohms (typical).
- Internal SLCK/TCLK operation limited to a maximum of 4 MHz (25 ns cycle time).

Comparator Inputs. Port 3, P31 and P32, each have a comparator front end. The comparator reference voltage, P33, is common to both comparators. In analog mode, the P33 input functions as a reference voltage to the comparators. The internal P33 register and its corresponding IRQ1 is connected to the STOP Mode Recovery source selected by the SMR. In this mode, any of the STOP Mode Recovery sources are used to toggle the P33 bit or generate IRQ1. In digital mode, P33 can be used as a Port 3 register input or IRQ1 source (Figure 5).



Default setting from STOP Mode Recovery, Power-On Reset, and any WDT Reset.

Figure 5. PORT Configuration Register (PCON)

FUNCTIONAL DESCRIPTION

The Z86L06 CCP is based on Zilog's core which incorporates special functions to enhance the Z8^o MCU's application in consumer, automotive, industrial, scientific research, and advanced technologies applications.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop Mode Recovery source

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a Stop Mode Recovery operation.

Program Memory. Z86L06 can address up to 1 Kbyte of internal program memory (Figure 6). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 13 to 1023 consist of on-chip, mask-programmed ROM.

ROM Protect. The 1 Kbyte of Program Memory is mask programmable. A ROM protect feature will prevent dumping of the ROM contents by inhibiting execution of the LDC and LDCI instructions to program memory in all modes.

Expanded Register File. The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 7). These register groups are known as the ERF (Expanded Register File). Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of register RP select the working register group (Figure 8). Three system configuration registers reside in the Expanded Register File address space in Bank F. The rest of the Expanded Register addressing space is not physically implemented, and is open for future

expansion. To write to the ERF, the upper nibble of the RP must be zero. To write to the rest of the register file, the lower nibble must be zero.

Note:

When using Zlog's cross assembler version 2.1 or earlier, use the LD RP, #0X instruction rather than the SRP #0X instruction to access the ERF.

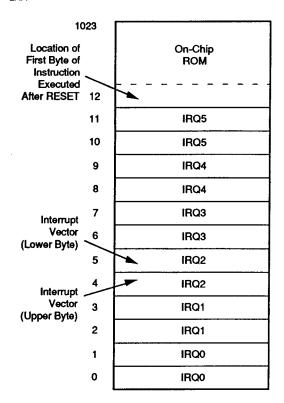


Figure 6. Program Memory Map

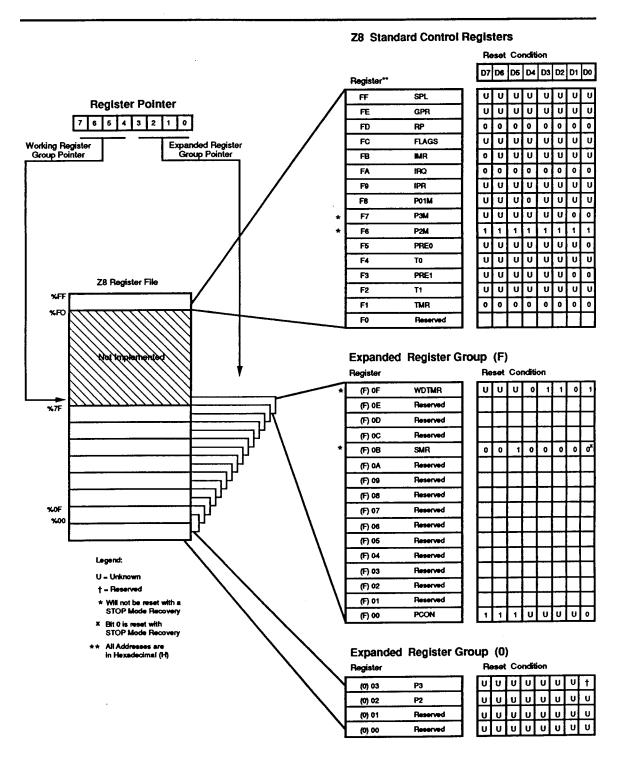


Figure 7. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

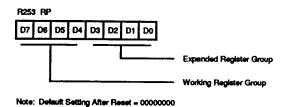


Figure 8. Register Pointer Register

Register File. The Register File consists of two I/O port registers, 124 general purpose registers, 15 control and status registers, and four system configuration registers in the Expanded Register Group (Figure 7). The instructions can access registers directly or indirectly via an 8-bit

address field. This allows a short 4-bit register address using the Register Pointer (Figure 9). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0-EF is only accessed through working registers and indirect addressing modes.

Caution: D4 of Control Register P01M (R251) must be 0. If the Z86L06 is emulated by Z86C90, D4 of P01M has to change to 0 before submission to ROM code.

GPR. The Z86L06 has one extra general purpose register located at FEH (R254).

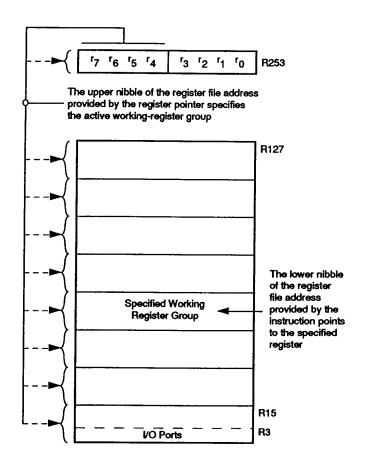


Figure 9. Register Pointer

Stack. The Z86L06 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 10).

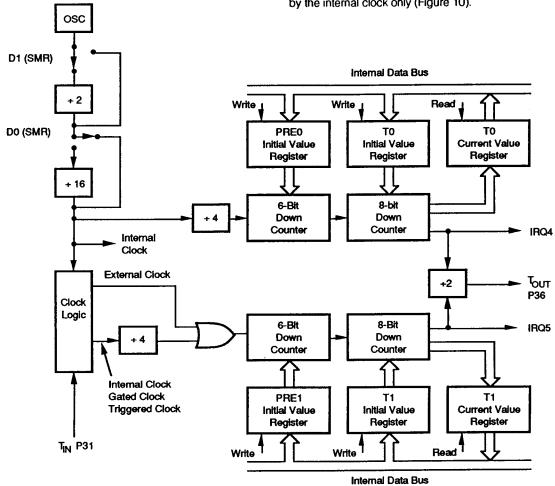


Figure 10. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the

internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 serves as a timer output (T_{Out}) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

Interrupts. The Z86L06 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 11). The six sources are divided as follows; three sources are claimed by Port 3 lines P31-P33, two sources in the counter/timers, and one source by software. The Interrupt Mask Register globally or singularly enables or disables the six interrupt requests (Table 2).

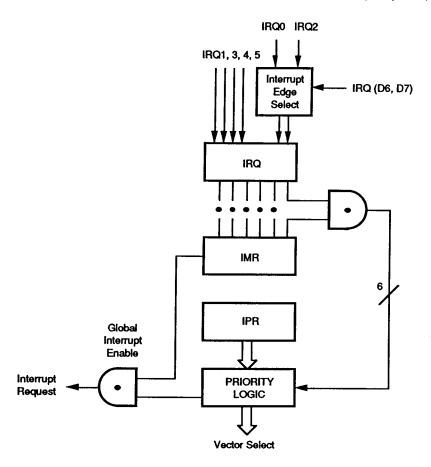


Figure 11. Interrupt Block Diagram



Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	IRQ 0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ 1	IRQ 1	2, 3	External (P33), Falling Edge Triggered
IRQ 2	IRQ 2, T _{IN}	4,5	External (P31), Rising Falling Edge Triggered
IRQ 3		6, 7	Software Generated
IRQ 4	TO	8, 9	Internal
IRQ 5	ΤI	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86L06 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs services. IRQ3 has no hardware source but can be invoked by software (write to IRQ3 Register).

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

The programming bits for the Interrupt Edge Select are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

	Table 3. IRQ Register					
11	RQ	Interrup	t Edge			
D7	D6	P31	P32			
0	0	F	F			
0	1	F	R			
1	0	R	F			
1	1	R/F	R/F			

Notes:

F = Falling Edge

R = Rising Edge

Clock. The Z86L06 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 4 MHz or 8 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal is connected across XTAL1 and XTAL2 using the recommended capacitors (C1=C2 is more than or equal to 22 pF) from each pin to ground. The RC oscillator option is mask-programmable, to be selected by the customer at the time the ROM code is submitted. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 12).



FUNCTIONAL DESCRIPTION (Continued)

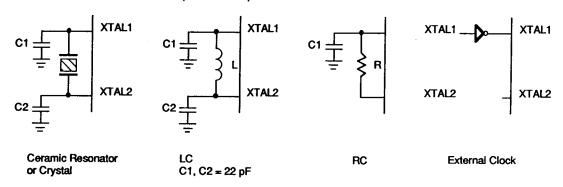


Figure 12. Oscillator Configuration

A special feature has been incorporated into the Z86L06. In low EMI noise mode (bit 7 of PCON register=0) with the RC option selected, the oscillator is targeted to consume considerably less I_{∞} current at frequencies of 10 kHz or less.

Power-On Reset. A timer circuit clocked by a dedicated on-board RC oscillator or by the XTAL oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{∞} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power fail to Power OK status
- STOP Mode Recovery (If D5 of SMR=1)
- WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after STOP Mode Recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. The STOP mode is terminated by a RESET of either WDT timeout, POR, or SMR recovery. This causes the processor to restart the application program at address 000CH.

Note, the crystal remains active in STOP mode if bits 3 and 4 of the WDTMR are enabled. In this mode, only the Watch-Dog Timer runs in STOP mode.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

FF NOP; clear the pipeline

6F STOP; enter STOP mode

Of

FF NOP; clear the pipeline

7F HALT; enter HALT mode

STOP Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP mode recovery (Figure 13). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of a STOP recovery and reset on a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR specify the source of the STOP Mode Recovery signal. Bit 1 determines whether the XTAL is divided by 1 or 2. A 0 in this location uses XTAL divide-by-two, and a 1 uses XTAL. The default for this bit is XTAL divide-by-two. Bit 0 controls the divide-by-16 prescaler of SCLK/TCLK.

SCLK/TCLK divide-by-16 select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources the counter/timers and interrupt logic). Note that Bit 0 (D0) is reset from WDT time out, POR, or SMR recovery.

XTAL Clock divide-by-2 (D1). This bit determines whether the XTAL clock is divided by two or one. When this bit is set to 1, the SCLK/TCLK is equal to the XTAL clock. This option can work together with the low EMI options in PCON register to reduce the EMI noise. Maximum frequency is 4 MHz when divide-by-1 selection is active.

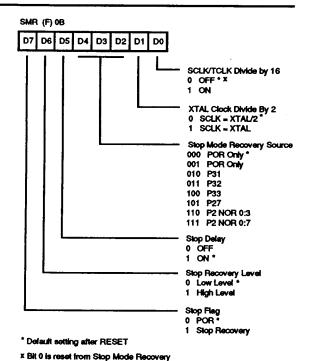


Figure 13. STOP Mode Recovery Register

FUNCTIONAL DESCRIPTION (Continued)

STOP Mode Recovery Source (D2,D3,D4). These three bits of the SMR specify the wake-up source of the STOP Mode Recovery (Figure 14 and Table 4).

Table 4. STOP Mode Recovery Source

D4	SMR D3	D2	Operation Description of Action
0	0	0	POR recovery only
0	0	1	POR recovery only
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

P31-P33 cannot wake up from STOP mode if the input lines are configured as analog inputs. Note: These other STOP Mode Recovery sources have to be active level Low (bit D6 in SMR set to 0 if P31, P32, P33, and P27 selected, or bit D6 in SMR set to 1 if logical NOR of Port 2 is selected).

STOP Mode Recovery Delay Select (D5). This bit disables the 5 ms RESET delay after STOP Mode Recovery. The default condition of this bit is 1.

STOP Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 15).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. It is active High, and is 0 (cold) on POR/WDT RESET. This bit is READ only. It is used to distinguish between cold or warm start.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and retriggered on subsequent executions of the WDT instruction. The timer circuit is driven by an on-board RC oscillator or external clock source. The POR clock source is selected with bit 4 of the WDTMR.

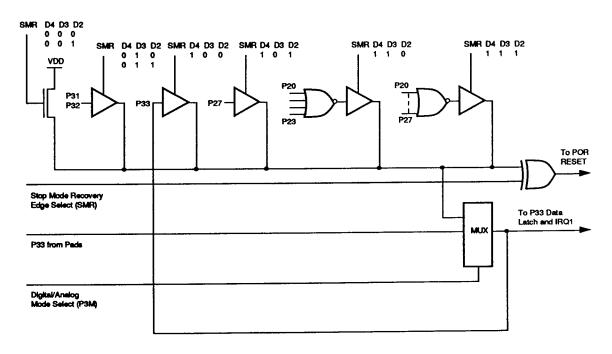
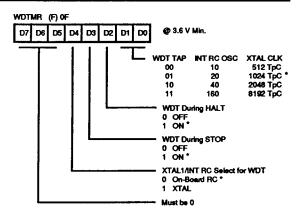


Figure 14. STOP Mode Recovery Source

Bits 0 and 1 control a tap circuit that determines the timeout period. Bit 2 determines whether the WDT is active
during HALT and bit 3 determines WDT activity during
STOP. If bits 3 and 4 of this register are both set to 1, the
WDT is only driven by the external clock during STOP
mode. This feature makes it possible to wake up from
STOP mode from an internal source. Bits 5 through 7 of the
WDTMR are reserved (Figure 15). This register is accessible
only during the first 64 processor cycles (128 XTAL clocks)
from the execution of the first instruction after Power-OnReset, Watch-Dog Reset or a STOP Mode Recovery (Figure
16). After this point, the register cannot be modified by any
means, intentional or otherwise. The WDTMR cannot be
read and is located in bank F of the Expanded Register
Group at address location OFH. It is organized as follows:



^{*} Default setting after RESET

Figure 15. Watch-Dog Timer Mode Register

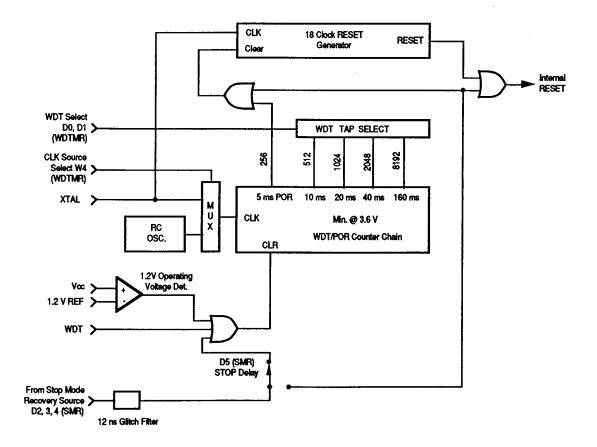


Figure 16. Resets and WDT



FUNCTIONAL DESCRIPTION (Continued)

WDT Time Select (D1,D0). Selects the WDT time-out period. It is configured as shown in Table 5 (Min. @ 3.6V).

Table 5. WDT Time Select

D1	D0	Timeout of internal RC OSC	Timeout of XTAL clock
0	0	10 ms min	512TpC
0	1	20 ms min	1024TpC
1	0	40 ms min	2048TpC
1	1	160 ms min	8192TpC

Notes:

The default on a WDT initiated RESET is 20 ms. The minumum time shown is for V_{∞} @ 3.6V.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP mode, unless as specified below, the on-board RC has to be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1. If bits D3 and D4 are both set to 1, the WDT only, is driven by the external clock during STOP mode.

On-Board, Power-On-Reset RC or External XTAL1 Oscillator Select (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

 V_{∞} Voltage Comparator. An on-board Voltage Comparator checks that V_{∞} is at the required level to ensure correct operation of the device. RESET is globally driven if V_{∞} is below the specified voltage (typically 1.2V).

Brown-Out Protection (V_{BO}). The brown-out trip voltage (V_{BO}) will be less than 2 volts and above 1.6 volts under the following condition.

Maximum (V_{no}):

T_A = 0°, +70°C, Internal Clock Frequency equal or less than 4 MHz

Note:

The internal clock frequency is one-half the external clock frequency, unless the device is in SCLK = XTAL mode with SMR (D1)=1.

The device functions normally at or above 2.0V under all conditions. For V_{cc} below 2.0V, the device will either function normally to 1.6V or the device reset will be globally activated by the Brown-Out Protection trip point (V_{BO}) is reached, for the temperature and operating frequency stated above. This will guarantee safe operation (normal operation or held in RESET between 2.0V and 1.6V V_{cc} . The actual brown-out trip point is a function of temperature and process parameters (Figure 17).

ROM Protect. ROM Protect is mask-programmable. It is selected by the customer at the time the ROM code is submitted. The selection of ROM Protect disables the LDC and LDCI instructions.

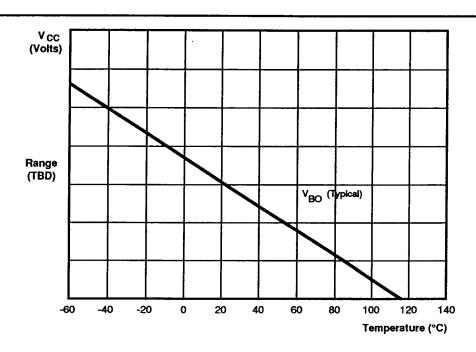


Figure 17. Typical Z86L06 $V_{\rm BO}$ Voltage vs Temperature

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units	
V _∞	Supply Voltage*	-0.3	+7.0	٧	
T _{sre}	Storage Temp	-65	+150	°C	
T _A	Oper Ambient Temp	†		°C	

Notes:

- * Voltage on all pins with respect to GND.
- † See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Figure 18).

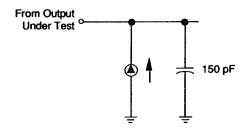


Figure 18. Test Load Configuration

DC ELECTRICAL CHARACTERISTICS (2.0V @ 8 MHz)

Sym	Parameter Note [2]	V _{cc}	T _A = 0°C Min	to +70°C Max	Typical @ +25°(Units	Conditions	Notes
	Max Input Voltage	2.0V	V _{ss} -0.3	V _{cc} +0.3	***	٧		
		3.6V	٧0.3	V _{cc} +0.3		Ÿ		
N ^{CH}	Clock Input High Voltage	2.0V	0.9°V _∞	V _∞ +0.3		v	Driven by External Clock Generator	
	_	3.6V	$0.9\mathrm{V}_{\mathrm{cc}}$	V _{cc} +0.3		V	Driven by External Clock Generator	
Va	Clock Input Low Voltage	2.0V	V _{ss} -0.3	0.1 V _{cc}		٧	Driven by External Clock Generator	
		3.6V	V _{ss} -0.3	0.1 V _{cc}		٧	Driven by External Clock Generator	
V _H	Input High Voltage	2.0V	0.9 V _{cc}	V _{cc} +0.3	1.5	V		
	Port 2	3.6V	0.9 V _{cc}	V _∞ +0.3	.~	v		
V _{ar}	Input High Voltage	2.0V	0.7 V _{cc}	V _{cc} +0.3		٧	-	
	Port 3	3.6V	0.7 V _∞	V _{cc} +0.3	1.3	V		
V _R	Input Low Voltage	2.0V	V _{ss} -0.3	0.1 V _{cc}	0.4	٧		
	Port 2	3.6V	V _{ss} -0.3	0.1 V _{cc}		V		
V _L	Input Low Voitage	2.0V	V _{ss} -0.3	0.2 V _∞		V		
	Port 3	3.6V	V _{ss} -0.3	0.2 V _{cc}	1.3	V		
V _{OH}	Output High Voltage	2.0V	V _{cc} -0.4		1.8	٧	l _{oH} = 500 μA	
		3.6V	V _{cc} -0.4		3.5	V	I _{он} = 500 µA	[6]
V _{OH}	Output High Voltage	2.0V	V _∞ -0.4		1.8	V	l _{oн} = -125 μA	
	Low EMI	3.6V	V _∞ -0.4		3.5	٧	l _{αн} = -125 μA	
V _{OH1}	Output High Voltage	2.0V	V _{cc} -0.7	V _{cc} +0.3	1.5	٧	I _{oH} = -7 mA @ 25°C	
	Port 3 (P36)	3.6V	V _∞ -0.7 V _∞ -0.7	V _∞ +0.3	2.4	٧	I _{OH} = -7 mA @ 25°C	
/a	Output Low Voltage	2.0V		0.4	0.2	٧	l _{ot} = 250 μA	
	Low EMI	3.6V		0.4	0.1	٧	$I_{oL} = 250 \mu\text{A}$	
/ _{0L1}	Output Low Voltage	2.0V		0.4	0.2	V	I _{ot} = 1.0 mA	[6]
		3.6V		0.4	0.1	V	$I_{\alpha c} = 1.0 \text{ mA}$	[6]
OL 1a	Output Low Voltage	2.0V		0.4	0.2	٧	I _a = 10 mA @ 25°C	[6]
	Port 2 (P20)	3.6V		0.4	0.1	V	I _{at} = 10 mA @ 25°C	[6]
01.2	Output Low Voltage	2.0V		0.8	0.3	٧	I _{at} = TBD,	[6]
		3.6V		1.0	0.5	٧	3 Pin Max I _{ot} = TBD,	[6] [6]
							3 Pin Max	
OFFSET	Comparator Input	2.0V		25	10	mV		
	Offset Voltage	3.6V		25	10	mV		
	Input Leakage	2.0V	-1.0	1.0		μΑ	$V_{IN} = 0V, V_{CC}$	
	(Input bias current of comparator)	3.6V	-1.0	1.0		μA	$V_{\rm IN}^{\rm m} = 0 V_{\rm cc}^{\rm m}$	

DC ELECTRICAL CHARACTERISTICS (Continued) (2.0V @ 8 MHz)

Sym	Parameter Note [2]	V _∞	T _A = 0°C Min	to +70°C Max	Typical + 25°C	Units	Conditions	Notes
	Output Leakage	2.0V	-1.0	1.0		μΑ	$V_{IN} = 0V, V_{CC}$	
.or		3.6V	-1.0	1.0		μА	$V_{IN} = 0V, V_{CC}$	
	Supply Current	2.0V		6	2.0	mA	@ 8 MHz	[3,4]
¹ cc	Coppiy Culture	3.6V		9.0	5.0	mA	@ 8 MHz	[3,4]
I _{CC1}	Standby Current	2.0V		2.0	1.0	mA	HALT Mode $V_{N} = 0V$, $V_{\infty}@8 \text{ MHz}$	[3,4]
		3.6V		4	3.0	mA	HÄLT Mode V _{IN} = 0V, V _{cc} @ 8 MHz	[3,4]
		2.0V		1.0	0.6	mA	Clock Divide by 16 @ 8 MHz	[3,4]
		3.6V		3.0	2.0	mΑ	Clock Divide by 16 @ 8 MHz	[3,4]
l _{cc2}	Standby Current	2.0V		15	1.0	μА	STOP Mode V _N = 0V, V _{cc} WDT is not Running	[5]
		3.6V		15	3.0	μА	STOP Mode $V_{\mathbb{N}} = 0V$, V_{∞} WDT is not Running	[5]
		2.0V		TBD	TBO	μА	STOP Mode $V_{N} = 0V$, V_{CC} WDT is Running	[5]
		3.6V		TBD	TBD	μА	STOP Mode V _N = 0V, V _{cc} WDT is Running	[5]
V _{ICR}	Comparator Input	nge Range		V _{cc} -1.5	i			

Notes:

Notes:
[1] V_{ss} = 0V = GND
[2] V_{cc} range 3.6V to 2.0V
[3] All outputs unloaded, I/O pins floating, inputs at rail.
[4] C_{L1} = C_{L2} = 100 pF
[5] Same as note [4] except inputs at V_{cc}
[6] STD Mode (not Low Noise)

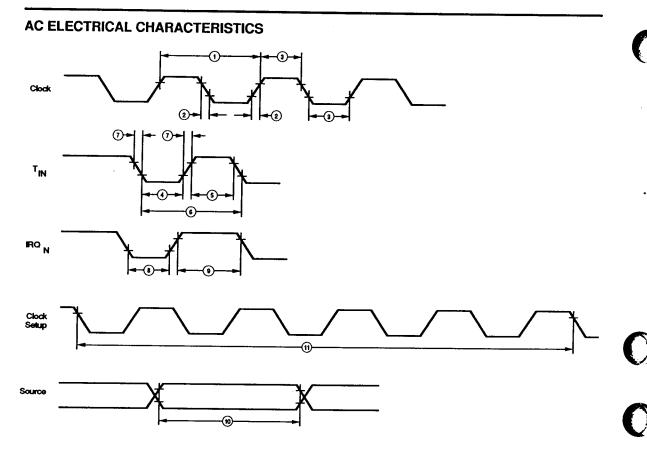


Figure 19. Additional Timing

AC ELECTRICAL CHARACTERISTICS (2.0V @ 8 MHz, Reference Additional Timing)

No	Symbol	Parameter	V_{∞} $T_{A} = 0^{\circ}\text{C to } +70^{\circ}$ Note[3] 8 MHz Min M			Hz	
1	ТрС	Input Clock Period	2.2V 3.6V	125 125	100,000	ns ns	[1] [1]
2	TrC,TfC	Clock Input Rise and Fall Times	2.2V 3.6V		25 25	ns ns	[1] [1]
3	TwC	Input Clock Width	2.2V 3.6V	37 37		ns ns	[1] [1]
4	TwTinL	Timer Input Low Width	2.2V 3.6V	250 250		ns ns	[1] [1]
5	TwTinH	Timer Input High Width	2.2V 3.6V	5TpC 5TpC			[1] [1]

AC ELECTRICAL CHARACTERISTICS (2.0V @ 8 MHz, Reference Additional Timing) (Continued)

No	Symbol	Symbol Parameter	V _{cc} Note[3]	T _A = 0°C	to +70°C IHz	Units	Notes
				Min	Max		
6	TpTin	Timer Input Period	2.2V 3.6V	8TpC 8TpC			[1] [1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	2.2V 3.6V		100 100	ns ns	[1] [1]
8a	TwlL	Int. Request Input Low Time	2.2V 3.6V	100 100		ns ns	[1,2,7] [1,2,7]
8b	····		2.2V 3.6V	5TpC 5TpC		ns ns	[1,2,8] [1,2,8]
9a	TwiH	Int. Request Input High Time	2.2V 3.6V	5TpC 5TpC			[1,2,7] [1,2,7]
9b			2.2V 3.6V	100 100		ns ns	[1,2,8] [1,2,8]
10	Twsm	STOP Mode Recovery Width Spec	2.2V 3.6V	70 70		ns ns	
11	Tost	Oscillator Start-up Time	2.2V 3.6V	TBD TBD		ns	Reg. [4]
12	Twdt	Watch-Dog Timer Refresh Time	2.2V 3.6V	25 10	110 40	ms	[5] D0 = 0 [6] D1 = 0 [6]
			2.2V 3.6V	55 20	220 80	ms ms	D0 = 1 [6] D1 = 0 [6]
			2.2V 3.6V	110 40	440 160	ms ms	D0 = 0 [6] D1 = 1 [6]
			2.2V 3.6V	440 160	1760 640	ms ms	D0 = 1 [6] D1 = 1 [6]
13	T _{POR}	Power-On Reset Time	2.2V 3.6V	12 5	55 20	ms ms	[5] D0 = 0 [6]

Notes:
[1] Timing Reference uses $0.9\,V_{\infty}$ for a logic 1 and $0.1\,V_{\infty}$ for a logic 0.
[2] Interrupt request via Port 3 (P31-P33)
[3] V_{∞} range 3.6V to 2.0V
[4] SMR-D5 = 0
[5] Reg. WDTMR
[6] Internal RC Oscillator only.
[7] Active Low interrupt

[7] Active Low interrupt
[8] Active High interrupt



EXPANDED REGISTER FILE CONTROL REGISTERS

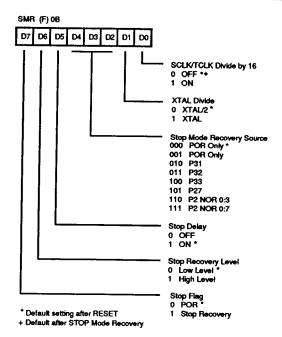


Figure 20. STOP Mode Recovery Register

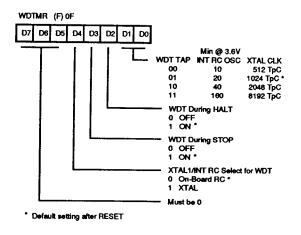


Figure 21. Watch-Dog Timer Mode Register

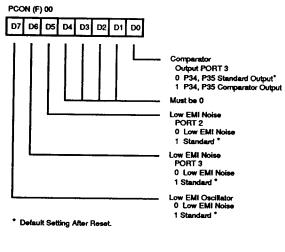


Figure 22. PORT Control Register

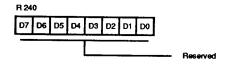


Figure 23. Reserved

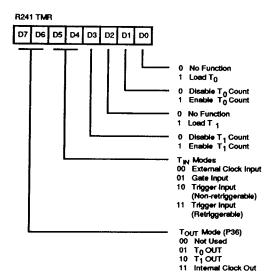


Figure 24. Timer Mode Register (F1_H: Read/Write)



Z8 CONTROL REGISTER DIAGRAMS

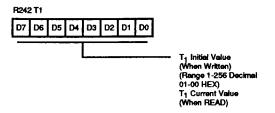


Figure 25. Counter Timer 1 Register (F2_H: Read/Write)

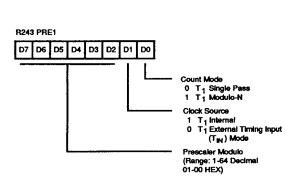


Figure 26. Prescaler 1 Register (F3_H: Write Only)

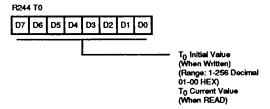


Figure 27. Counter/Timer 0 Register (F4_H: Read/Write)

and the second of the second o

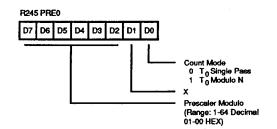


Figure 28. Prescaler 0 Register (F5_H: Write Only)

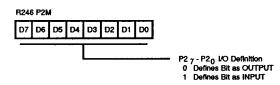


Figure 29. Port 2 Mode Register (F6_N: Write Only)

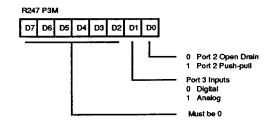


Figure 30. Port 3 Mode Register (F7_H: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

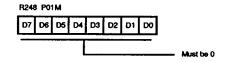


Figure 31. Port 0 and 1 Mode Register

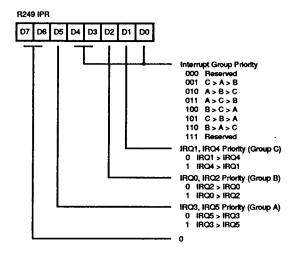


Figure 32. Interrupt Priority Register (F9_H: Write Only)

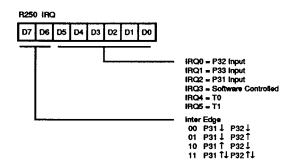


Figure 33. Interrupt Request Register (FA_H: Read/Write)

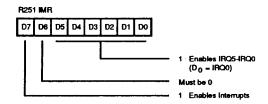


Figure 34. Interrupt Mask Register (FB_H: Read/Write)

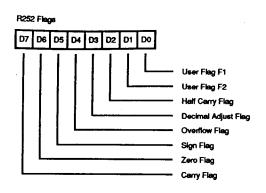


Figure 35. Flag Register (FC_H: Read/Write)

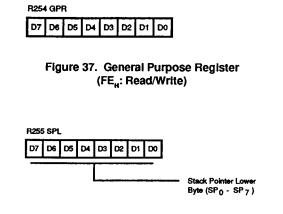


Figure 38. Stack Pointer (FF_H: Read/Write)

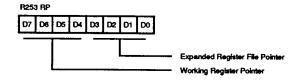


Figure 36. Register Pointer (FD_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning			
IRR	Indirect register pair or indirect working-			
	register pair address			
Irr	Indirect working-register pair only			
Χ	Indexed address			
DA	Direct address			
RA	Relative address			
IM	Immediate			
R	Register or working-register address			
r	Working-register address only			
IR .	Indirect-register or indirect			
	working-register address			
lr	Indirect working-register address only			
RR	Register pair or working register pair			
	address			

 $\mbox{\bf Symbols}.$ The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

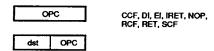
Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
Н	Half-carry flag
Affected flag	gs are indicated by:
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
×	Undefined



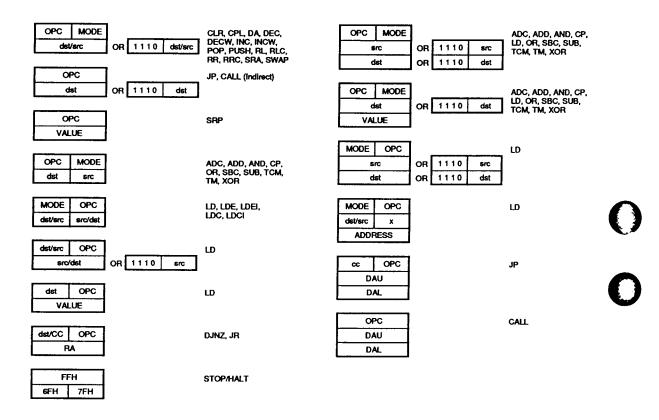
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	С	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION FORMATS



One-Byte Instructions



Two-Byte Instructions

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example:

notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst ← dst + src

dst (7)

indicates that the source data is added to the destination data and the result is stored in the destination location. The

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode	Af	igs fect		_			
	dst src		С	Z	S	٧	D	Н
ADC dst, src dst←dst + src +C	†	1[]	*	*	*	*	0	*
ADD dst, src dst←dst + src	t	0[]	*	*	*	*	0	*
AND dst, src dst←dst AND src	t	5[]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR	D6 D4	-	-	-	-	-	-
CCF C←NOT C		EF	*	-	-	-	-	-
CLR dst dst←0	R IR	B0 B1	-	-	-	-	-	_
COM dst dst←NOT dst	R IR	60 61	-	*	*	0	-	-
CP dst, src dst - src	t	A[]	*	*	*	*	-	-
DA dst dst←DA dst	R IR	40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR	00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR	80 81	-	*	*	*	-	-
DI IMR(7)←0		8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA	rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1		9F	-	-	-	-	-	-
HALT		7F		-	_	-	-	_

Instruction and Operation	Мо	dress de src	Opcode Byte (Hex)		ags fect Z	٧	D	Н	
INC dst dst←dst + 1	r R IR		rE r=0-F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c=0-F	-	-	-	•	-	-
LD dst, src dst←src	r R X Ir R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r=0-F C7 D7 E3 F3 E4 E5 E6 E7	-	-	-	-	-	-
LDC dst, src dst←src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr ←rr + 1	lr	lrr	C3	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
OR dst, src dst←dst OR src	t	4[]	- [[0
POP dst dst←@SP; SP←SP+1	R IR	50 51	
PUSH src SP←SP - 1; @SP←src	R IR	70 71	
RCF C←0		CF	0
RET PC←@SP; SP←SP + 2		AF	
RL dst	R	90	* * * *
C 7 0 4	!R	91	
RLC dst	R IR	10 11	* * * *
RR dsl	R IR	E0 E1	* * * *
RRC dst	R IR	C0 C1	* * * *
SBC dst, src dst←dst←src←C	t	3[]	* * * * 1 *
SCF C←1		DF	1
GRA dst	R IR	DO D1	* * * 0
SRP dst IP←src	lm	31	
ТОР		6F	1

Instruction and Operation	Address Mode	Opcode Byte (Hex)	Fi: Af					
	dst src		C	Z	S	٧	D	Н
SUB dst, src dst-dst-src	†	2[]	*	*	*	*	1	*
SWAP dst	R	F0	Х	*	*	Х	_	_
7 4 3 0	IR	F1						
TCM dst, src (NOT dst) AND src	†	6[]	-	*	*	0	-	-
TM dst, src dst AND src	t	7[]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†	B[]	-	*	*	0	-	-
WDT		5F	-	X	-	-	-	

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

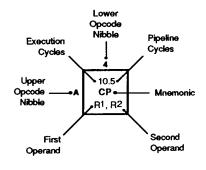
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Addres dst	ss Mode src	Lower Opcode Nibble
r	r	[2]
r	lr	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]



Lower	Nibble ((Hex)
-------	----------	-------

		0	1	2	3	4	5	6	7	8	9		A	B	С	Đ		E	F
		6.5	6.5	6.5	6.5	10.5	10.5	10.5	10.5	6.5	6.5	12/	10.5	12/10.0	6.5	12.10	0 6	.5	
	0	DEC	DEC	ADD	ADD	ADD	ADD	ADD	ADD	LD	LD		NZ	JR	LD	JP		AC.	
		R1	IR1	r1, r2	r1, lr2	R2, R1	IR2, R1	R1, IM	IR1, IM	r1, R2	r2, R1	⊢ r1,	RA	cc, RA	r1, IM	cc. D	۸ I	rj	ш
		6.5	6.5	6.5	6.5	10.5	10.5	10.5	10.5	1	1 1					11		1	
	1	RLC	RLC	ADC	ADC	ADC	ADC	ADC	ADC	1	1 1		ł	F			1		İ
		R1	IRt	r1, r2	r1, lr2	R2, R1	IR2, R1	R1, IM	IR1, IM			- 1					1	ŀ	
	_	6.5	6.5	6.5	6.5	10.5	10.5	10.5	10.5			-							
	2	INC	INC	SUB	SUB	SUB	SUB	SUB	SUB			1				1	1		
		R1	IR1	r1, r2	r1, lr2	R2, R1	IR2, R1	R1, IM	IR1, IM	11	1 1	1	•						
	3	8.0	6.1	6.5	6.5	10.5	10.5	10.5	10.5	 		1			11		1		
	3	JP	SRP	SBC	SBC	SBC	SBC	SBC	SBC	 	1 1		l						
		IRR1	IM	r1, r2	r1, lr2	R2, R1	IR2, R1	R1, IM	IR1, IM		1				łl		1		
	4	8.5 DA	8.5 DA	6.5 OR	6.5 OR	10.5 OR	10.5 OR	10.5 OR	10.5 OR		1 1				i I	1	- 1		
	•	R1	IR1	r1, r2	r1, lr2	R2, R1	IR2, R1	R1, IM	IR1, IM		1 1			[1 I			
		10.5	10.5	6.5	6.5	10.5	10.5	10.5	10.5	1 1					1	11		1	6.0
	5	POP	POP	AND	AND	AND	AND	AND	AND	11		ı] [ı		WDT
	_	R1	IR1	r1, r2	r1, lr2	R2, R1	IR2, R1	R1, IM	IR1, IM							11		ı	
		6.5	6.5	6.5	6.5	10.5	10.5	10.5	10.5	11		ı			ŀ	11			6.0
	6	COM	COM	TCM	TCM	TCM	TCM	TCM	TCM	11		1			1	11	ŀ	•	STOP
×		R1	IR1	r1, r2	r1, lr2	R2, R1	1R2, R1	R1, IM	IR1, IM		1 1	-				11	1		
Ĭ		10/12.1	12/14.1	6.5	6.5	10.5	10.5	10.5	10.5	11		1				11		1	7.0
0	7	PUSH	PUSH	TM	TM	TM	TM	TM	TM		11	1					1		HALT
2		R2	IR2	r1, r2	r1, lr2	R2, R1	IR2, R1	R1, IM	IR1, IM	l 1	1 I						1		
Upper Nibble (Hex)	_	10.5	10.5				1				1 I	1		i			1	l	6.1
<u>ē</u>	8	DECW	DECW		1	ł					11						-		DI
ᅙ		RR1	IR1		<u> </u>	<u> </u>		ļ			11				. 1		- 1		6.1
_	9	6.5 RL	6.5 RL		l			Ì			11								6.1 EI
	•	R1	IR1		l	l	ŀ				11	Į		1					
		10.5	10.5	6.5	6.5	10.5	10.5	10.5	10.5	1 1	11	İ						1	14.0
	A	INCW	INCW	CP	CP	CP	CP	CP	CP		11	İ	1						RET
		RR1	IR1	r1, r2	r1, lr2	1	IR2, R1	R1, IM	IR1, IM		11				ı		- 1	1	1
		6.5	6.5	6.5	6.5	10.5	10.5	10.5	10.5	1 1	11	ı					-	1	16.0
	В	CLR	CLR	XOR	XOR	XOR	XOR	XOR	XOR	 	11	1		1		1	-		IRET
		R1	IR1	r1, r2	r1, lr2	R2, R1	IR2, R1	R1, IM	IR1, IM	l 1	11	1					1		
		6.5	6.5	12.0	18.0			:	10.5	 	11						1		6.5
	С	RRC	RRC	LDC	rdci	1		ł	ш		11	1					1		RCF
		R1	IR1	r1, im2	Ir1, Irr2		Ļ		r1,x,R2	l 1	1 I			1			1		
	_	6.5	6.5		1	20.0		20.0	10.5		11			1		1	1		6.5 SCF
	D	SRA	SRA			CALL.		CALL	LD		11	1					-		SCF
		R1	IR1		1	IRR1	10.5	DA	r2,x,R1	11	1 I	ı					1		6.5
	E	6.5 RR	6.5 RR		6.5 LD	10.5 LD	10.5 LD	10.5 LD	10.5 LD	11	1 I	ı					1		CCF
	-	R1	IR1		r1, IR2		IR2, R1	R1, IM	IR1, IM	11	11	1		1			1		
		8.5	8.5		6.5	172, A1	10.5	11, 1141	10.1, 100	1 1	11	1							6.0
	F	SWAP	SWAP		LD	l	LD	l		ΙL	l L	Ι.	L	1	I	1	1,	L	NOP
	-	R1	IR1		lr1, r2		R2, IR1	l		V	I ▼	1	/	7	Y	LY.		٧	
						$\overline{}$							=			$\overline{\ }$	ス	=	
				2			7	3					2			3			1
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								Ву	tes per	ii iStruc	uon								



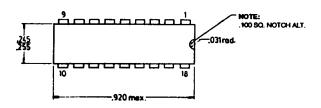
Legend: R = 8-bit address r = 4-bit address R1 or r2 = Dst address R1 or r2 = Src address

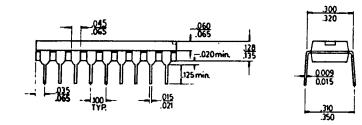
Sequence: Opcode, First Operand, Second Operand

Note: Blank areas not defined.

* 2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION





18-Pin DIP Package Diagram

ORDERING INFORMATION

Z86L06

8 MHz 18-Pin DIP Z86L0608PSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package

P = Plastic DIP

Temperature

 $S = 0^{\circ}C \text{ to } + 70^{\circ}C$

Speed

8 = 8 MHz

Environmental

C = Plastic Standard

Example:

Z 86L06 08 P S C is an 86L06, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

Environmental Flow

Temperature

Package

Speed

Product Number

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