Z8S180 SL1960

STATIC Z180™
MICROPROCESSOR

GENERAL DESCRIPTION

The Zilog Static Z180™ microprocessor Z8S180 is a software and hardware compatible member of the Z80180 family designed for fully static operations. Based on a microcoded execution unit and an advanced CMOS manufacturing technology, the Z8S180 is an 8-bit MPU which provides the benefits of reduced system costs, low power operation and Low EMI emission. The Z8S180 also offers higher performance and maintains compatibility with a large base of industry standard software written around the Zilog Z80® CPU.

Higher performance is obtained by virtue of higher operating frequencies (up to 20 MHz), reduced instruction execution times, an enhanced instruction set, and an on-chip memory management unit (MMU) with the capability of addressing up to 1 Mbyte of memory.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are several "glue" functions such as dynamic RAM refresh control, wait state generators, clock oscillator, and interrupt controller.

Because of its static design, the Z8S180 consumes a lower amount of power than the Z80180 during normal operation. It also provides two additional operating modes that drastically reduce the power consumption. First, the IDLE mode is offered in the Z8S180 by stopping the internal clocks but keeping the oscillation running. Secondly, the STANDBY mode consumes the least current (less than 10 µA) by stopping the oscillators and internal clock completely.

The Z8S180 can reduce EMI emission by offering programmable EMI options where EMI noise levels can be reduced significantly.

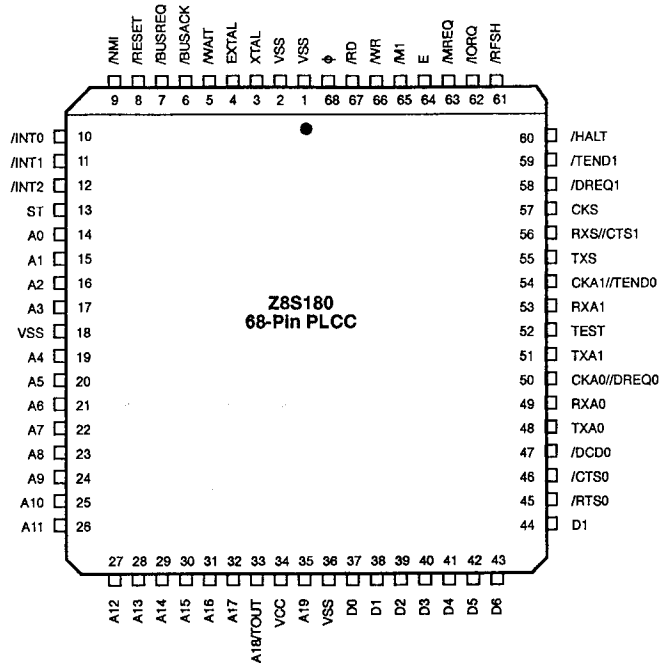
When combined with other CMOS VLSI devices and memories, the Z8S180 provides an excellent solution to system applications requiring high performance, low power operation and Low EMI emission.

Note: All Signals with an overline, "$\overline{\ }$", are active Low. For example: B/$\overline{W}$, in which WORD is active Low; or $\overline{B}$/W, in which BYTE is active Low.

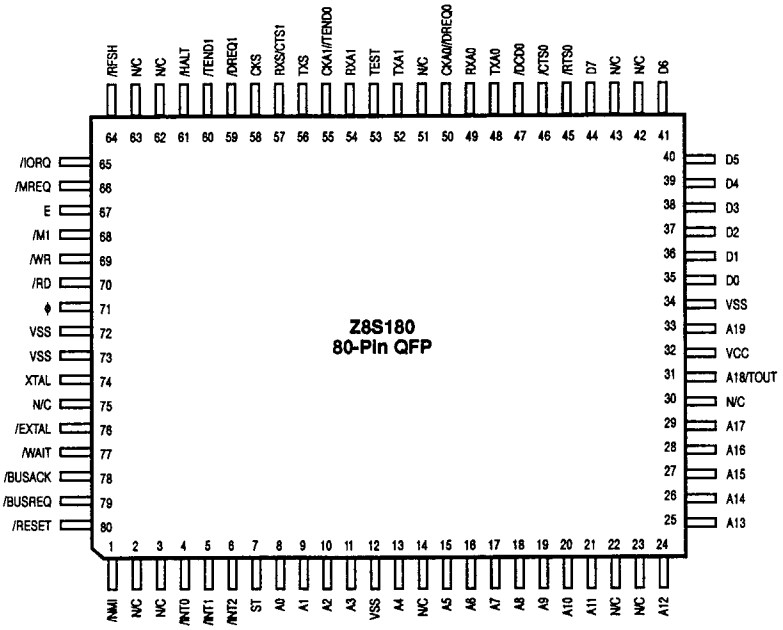
Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



68-Lead PLCC Pin Identification



80-Lead QFP Pin Identification

ABSOLUTE MAXIMUM RATINGS

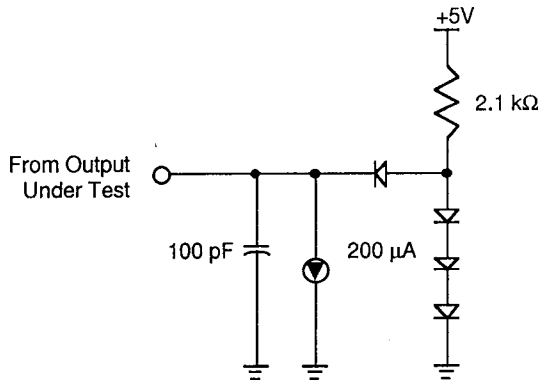
Symbol	Description	Min	Max	Unit
V_{CC}	Supply Voltage *	–0.3	+7.0	V
V_{IN}	Input Voltage	–0.3	V_{CC}+0.3	V
T_{OPR}	Operating Temp	–40	+100	C
T_{STG}	Storage Temp	–55	+150	C

Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

STANDARD TEST CONDITIONS

The DC Characteristics and Capacitance sections below apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Test Load Configuration).

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points).



Test Load Configuration

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, V_{SS}=0V, over specificied temperature range, unless otherwise noted.)

Symbol	Item	Condition	Min	Typ	Max	Unit
V_{IH1}	Input "H" Voltage Reset, EXTAL, NMI		V_{CC}–0.6		V_{CC}+0.3	V
V_{IH2}	Input "H" Voltage Except Reset, EXTAL, NMI		2.0		V_{CC}+0.3	V
V_{IL1}	Input "L" Voltage Reset, EXTAL, NMI		–0.3		0.6	V
V_{IL2}	Input "L" Voltage Except Reset, EXTAL, NMI		–0.3		0.8	V
V_{OH1}	Output "H" Voltage All Outputs	I_{OH} = –200 µA I_{OH} = –20 µA	2.4 V_{CC}–1.2			V V
V_{OH2}	Output "H" PHI	I_{OH} = –200 µA	V_{CC}–0.6			V
V_{OL1}	Output "L" Voltage All Outputs	I_{OL}= 2.2 mA			0.45	V
V_{OL2}	Output "L" PHI	I_{OL}=2.2 mA			0.45	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	V_{IN}=0.5 to V_{CC}–0.5			1.0	µA
ITL	Tri-state Leakage Current	V_{IN}=0.5 to V_{CC}–0.5			1.0	µA
I_{CC}*	Power Dissipation (Normal Operation)	f = 16 MHz f = 20 MHz		45 50	100 120	mA mA
	Power Dissipation (System STOP mode)	f = 16 MHz f = 20 MHz		10 15	30 40	mA mA
	Power Dissipation (IDLE Mode)	f = 16 MHz f = 20 MHz		TBD TBD	TBD TBD	mA mA
	Power Dissipation (STANDBY Mode)	External Oscillator, Internal Clock Stops			10	µA
Cp	Pin Capacitance	V_{IN}=0V, f = 1 MHz T_A = 25°C			12	pF

Notes:

* V_{IH}min = V_{CC}–1.0V, V_{IL}max = 0.8V (all output termianls are at no load)
V_{CC}=5.0V

Z8S180 AC CHARACTERISTICS

(V_{CC}=5V ± 10%, V_{SS}=0V, over specified temperature range, unless otherwise noted.)

No	Sym	Parameter	16 MHz Min	16 MHz Max	18.432 MHz Min	18.432 MHz Max	20 MHz Min	20 MHz Max	Unit	Note
1	tcyc	Clock Cycle time	62	DC	54	DC	50	DC	ns	[1]
2a	tCHW (Out)	Output Clock Pulse Width (high)	25	DC	22	DC	20	DC	ns	[1]
2b	tCHW (In)	Input Clock Pulse Width (high)	21	DC	17	DC	15	DC	ns	[1]
3a	tCLW (Out)	Output Clock Pulse Width (low)	25	DC	22	DC	20	DC	ns	[1]
3b	tCLW (In)	Input Clock Pulse Width (low)	21	DC	17	DC	15	DC	ns	[1]
4a	tcf (Out)	Output Clock Fall Time		6		5		5	ns	[1]
4b	tcf (In)	Input Clock Fall Time		10		10		10	ns	[1]
5a	tcr (Out)	Output Clock Rise Time		6		5		5	ns	[1]
5b	tcr (In)	Input Clock Rise Time		10		10		10	ns	[1]
6	tAD	Address vaild from Clock Rise		35		30		30	ns	
7	tAS	Address valid to /MREQ, /IORQ Fall	5		5		5		ns	
8	tMED1	Clock Fall to /MREQ Fall delay		25		25		25	ns	
9	tRDD1	Clock Fall to /RD Fall (/IOC=1)		25		25		25	ns	
		Clock Rise to /RD Fall (/IOC=0)		25		25		25	ns	
10	tM1D1	Clock Rise to /M1 Fall delay		45		35		35	ns	
11	tAH	Address Hold time (/MREQ,/IORQ,/RD,/WR)	5		5		5		ns	
12	tMED2	Clock Fall to /MREQ Rise Delay		30		25		25	ns	
13	tRDD2	Clock Fall to /RD Rise delay		30		25		25	ns	
14	tM1D2	Clock Rise to /M1 Rise delay		45		40		40	ns	
15	tDRS	Data Read Setup Time	15		10		10		ns	
16	tDRH	Data Read Hold time	0		0		0		ns	
17	tSTD1	Clock Edge to ST Fall		35		30		30	ns	
18	tSTD2	Clock Edge to ST Rise		35		30		30	ns	
19	tWS	/WAIT setup time to Clock Fall	15		15		15		ns	[2]
20	tWH	/WAIT Hold time from Clock Fall	10		10		10		ns	
21	tWDZ	Clock Rise to Data Float Delay		40		35		35	ns	
22	tWRD1	Clock Rise to /WR Fall delay		25		25		25	ns	
23	tWDD	Clock Fall to Write Data Delay		30		25		25	ns	
24	tWDS	Write Data Setup time to /WR	10		10		10		ns	
25	tWRD2	Clock Fall to /WR Rise		30		25		25	ns	
26	tWRP	/WR Pulse Width (Memory Write Cycles)	80		80		80		ns	
26a		/WR Pulse Width (I/O Write Cycles)	150		150		150		ns	
27	tWDH	Write Data Hold time from /WR Rise	10		10		10		ns	
28	tIOD1	Clock Fall to /IORQ Fall delay (/IOC=1)		30		25		25	ns	
		Clock Rise to /IORQ Fall delay (/IOC=0)		30		25		25	ns	
29	tIOD2	Clock Fall /IOQR Rise Delay		30		25		25	ns	
30	tIOD3	/M1 Fall to /IORQ Fall delay	120		100		100		ns	
31	tINTS	/INT Setup Time to Clock Fall	20		20		20		ns	
32	tINTH	/INT Hold Time from Clock Fall	10		10		10		ns	
33	tNMIW	/NMI Pulse width	40		35		35		ns	
34	tBRS	/BUSREQ Setup Time to Clock Fall	10		10		10		ns	
35	tBRH	/BUSREQ Hold Time from Clock Fall	10		10		10		ns	

Z8S180 AC CHARACTERISTICS (Continued)

(V_{CC}=5V ± 10%, V_{SS}=0V, over specified temperature range, unless otherwise noted.)

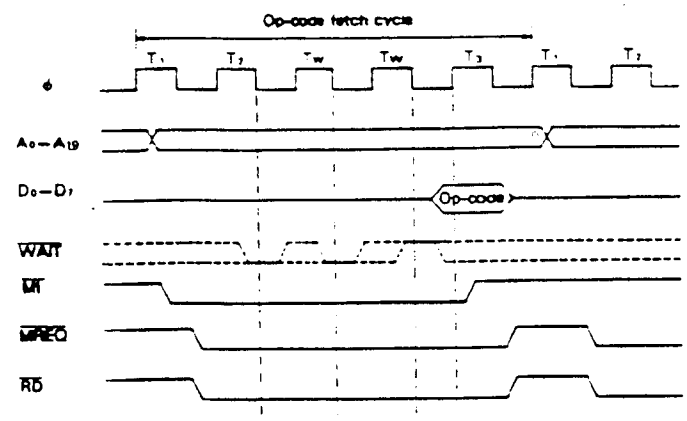
No	Sym	Parameter	16 MHz Min	16 MHz Max	18.432 MHz Min	18.432 MHz Max	20 MHz Min	20 MHz Max	Unit	Note
36	tBAD1	Clock Rise to /BUSACK Fall delay		30		25		25	ns	
37	tBAD2	Clock Fall to /BUSACK Rise delay		30		25		25	ns	
38	tBZD	Clock Rise to Bus Floating Delay Time		45		40		40	ns	
39	tMEWH	/MREQ Pulse Width (High)	45		35		35		ns	
40	tMEWL	/MREQ Pulse Width (LOW)	45		35		35		ns	
41	tRFD1	Clock Rise to /RFSH Fall Delay		25		20		20	ns	
42	tRFD2	Clock Rise to /RFSH Rise Delay		25		20		20	ns	
43	tHAD1	Clock Rise to /HALT Fall Delay		20		15		15	ns	
44	tHAD2	Clock Rise to /HALT Rise Delay		20		15		15	ns	
45	tDRQS	/DREQi Setup Time to Clock Rise	20		20		20		ns	
46	tDRQH	/DREQi Hold Time from Clock Rise	20		20		20		ns	
47	tTED1	Clock Fall to /TENDi Fall Delay		30		25		25	ns	
48	tTED2	Clock Fall to /TENDi Rise Delay		30		25		25	ns	
49	tED1	Clock Rise to E Rise Delay		35		30		30	ns	
50	tED2	Clock Edge to E Fall Delay		35		30		30	ns	
51	PWEH	E Pulse Width (High)	30		25		25		ns	
52	PWEL	E Pulse Width (Low)	60		50		50		ns	
53	tEr	Enable Rise Time		10		10		10	ns	
54	tEf	Enable Fall Time		10		10		10	ns	
55	tTOD	Clock Fall to Timer Output Delay		100		75		75	ns	
56	tSTDI	CSI/O Tx Data Delay Time (Internal Clock Operation)		100		75		75	ns	
57	tSTDE	CSI/O Tx Data Delay Time (External Clock Operation)		7.5 tcyc +100		7.5 tcyc+75		7.5 tcyc+75	ns	
58	tSRSI	CSI/O Rx Data Setup Time (Internal Clock Operation)	1		1		1		tcyc	
59	tSRHI	CSI/O Rx Data Hold Time (Internal Clock Operation)	1		1		1		Tcyc	
60	tSRSE	CSI/O Rx Data Setup Time (External Clock Operation)	1		1		1		Tcyc	
61	tSRHE	CSI/O Rx Data Hold Time (External Clock Operation)	1		1		1		Tcyc	
62	tRES	/RESET Setup time to Clock Fall	45		40		40		ns	
63	tREH	/RESET Hold time from Clock Fall	30		25		25		ns	
64	tOSC	Oscillator Stabilization Time		20		20		20	ms	
65	tEXr	External Clock Rise Time (EXTAL)		6		5		5	ns	
66	tEXf	External Clock Fall Time (EXTAL)		6		5		5	ns	
67	tRr	/RESET Rise Time		50		50		50	ms	[2]
68	tRf	/RESET Fall Time		50		50		50	ms	[2]
69	tIr	Input Rise Time (Except EXTAL, /RESET)		50		50		50	ns	[2]
70	tIf	Input Fall Time (Except EXTAL, /RESET)		50		50		50	ns	[2]

Notes:

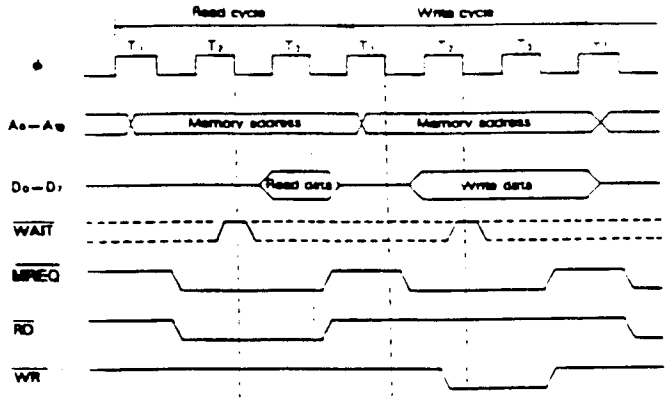
[1] tcyc=tCHW+tCLW+tcf+tcr

[2] This parameter has to be modified if other specification(s) can not be met.

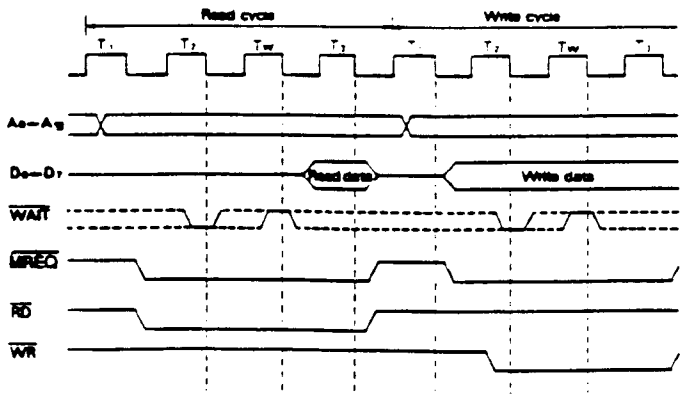
ELECTRICAL CHARACTERISTICS
Timing Diagrams



Opcode Fetch Timing (With Wait State)

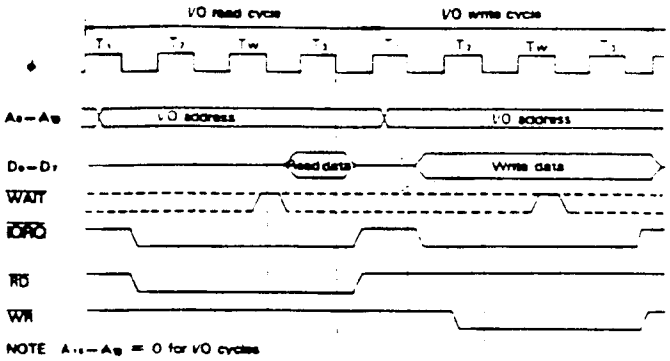


Memory Read/Write Timing (Without Wait State)

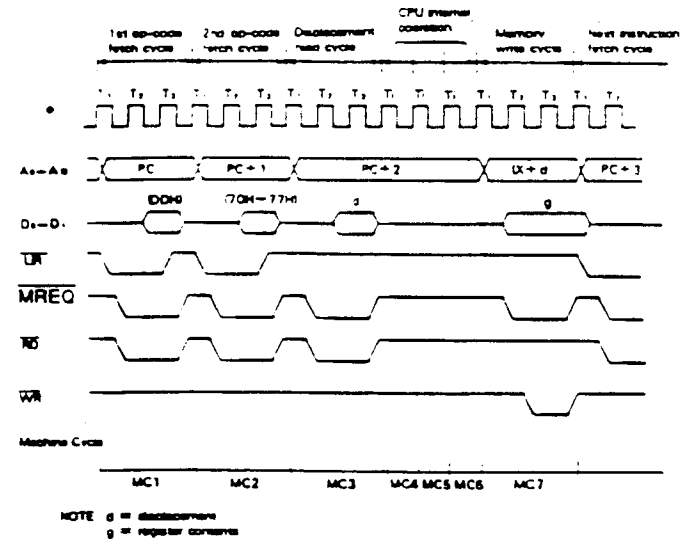


Memory Read/Write Timing (With Wait State)

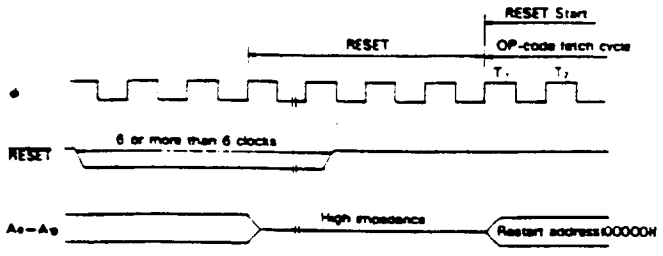
ELECTRICAL CHARACTERISTICS (Continued)
Timing Diagrams



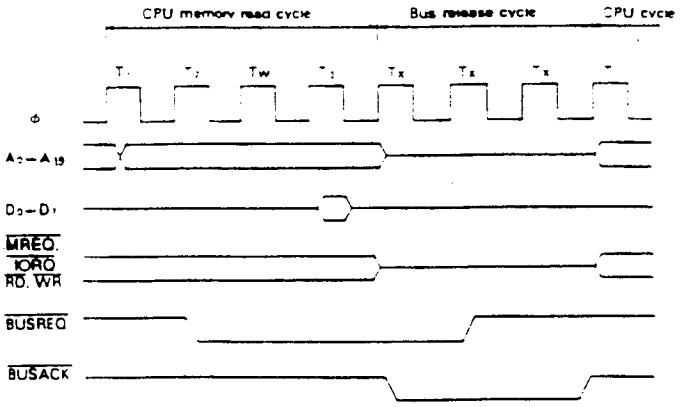
I/O Read/Write Timing



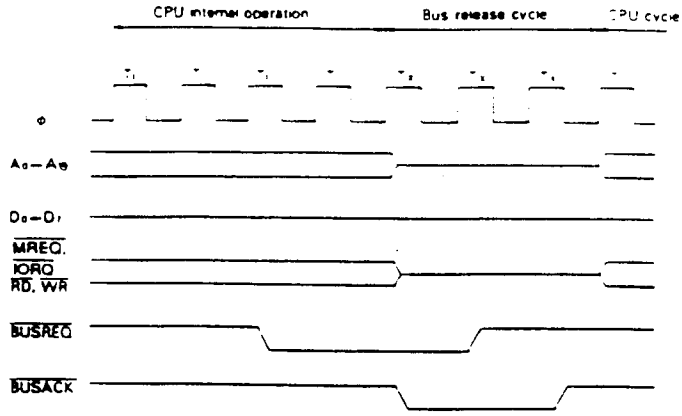
Instruction Timing



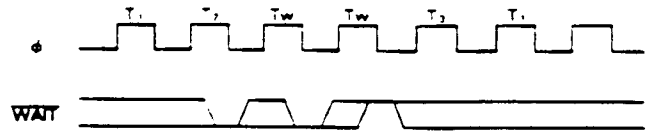
Reset Timing



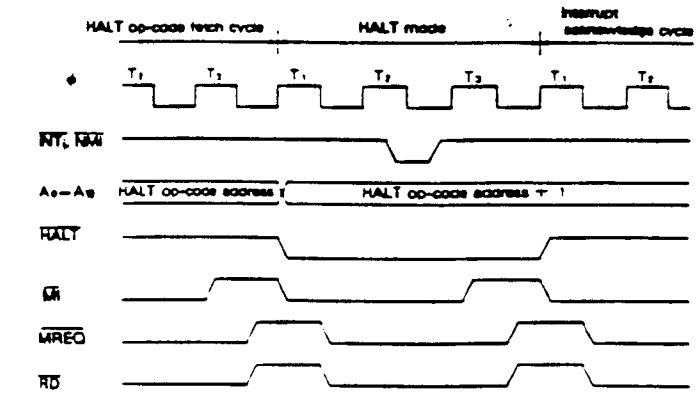
Bus Exchange Timing



Bus Exchange Timing



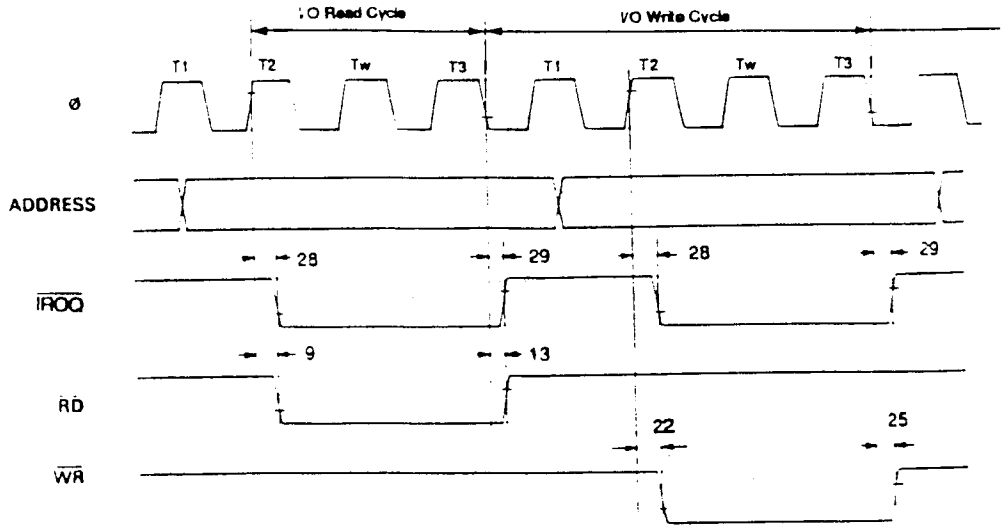
$\overline{\text{WAIT}}$ Timing



HALT Timing

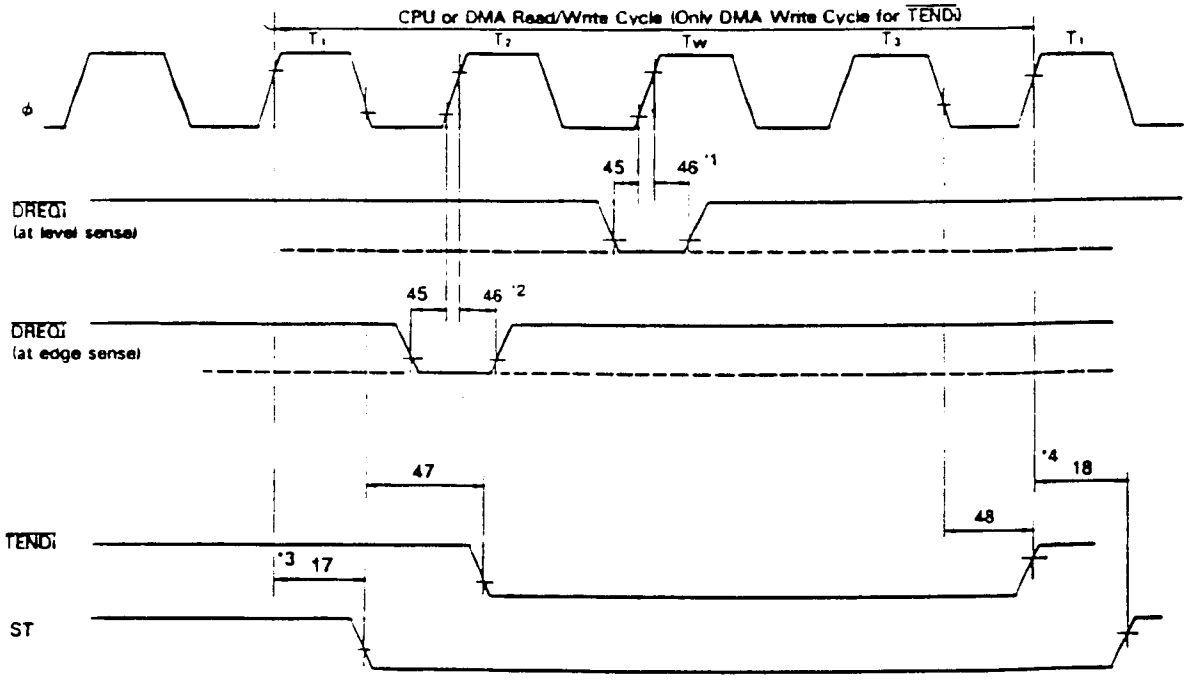
ELECTRICAL CHARACTERISTICS (Continued)

Timing Diagrams



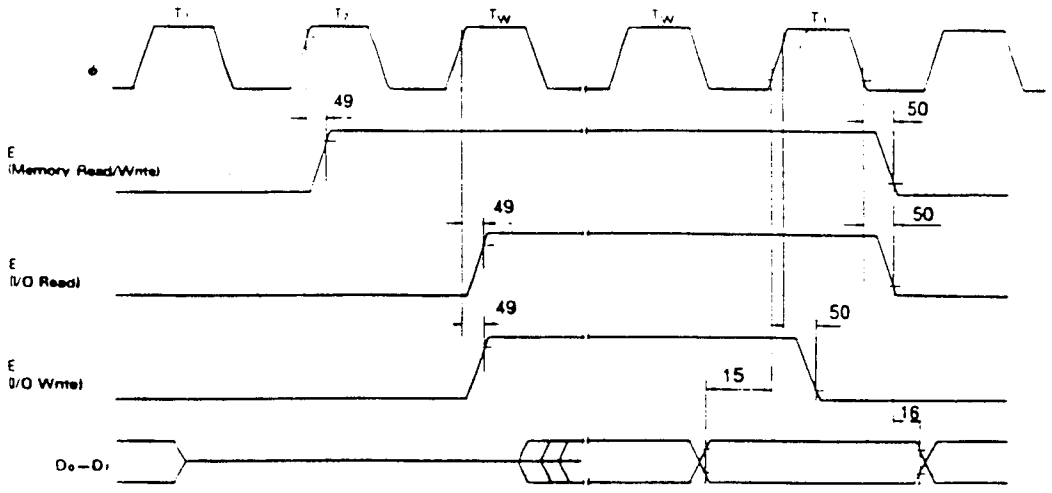
CPU Timing ($\overline{IOC}$=0)

{I/O Read Cycle / I/O Write Cycle}

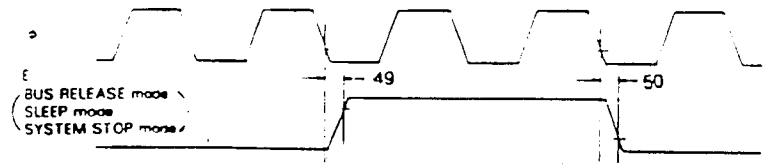


DMA Control Signals

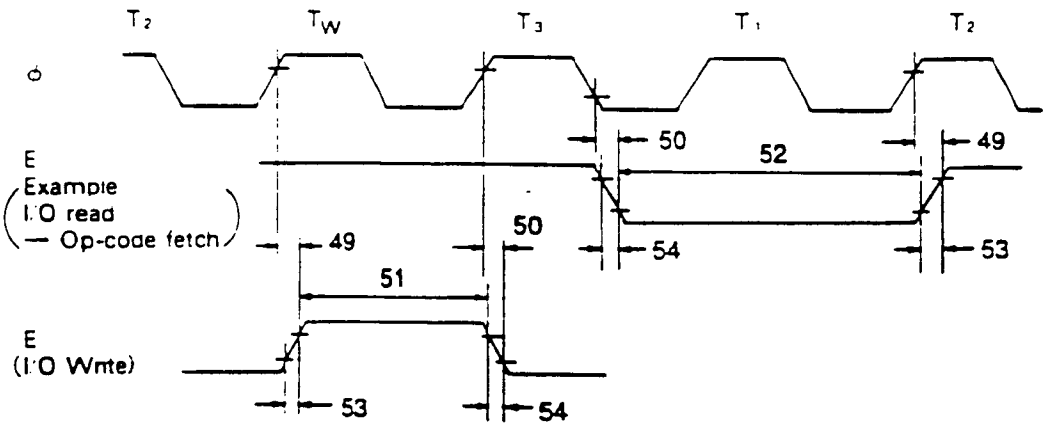
*1 t_{DRQS} and t_{DRQH} are specified for the rising edge of clock followed by T_3.
*2 t_{DRQS} and t_{DRQH} are specified for the rising edge of clock.
*3 DMA cycle starts.
*4 CPU cycle starts.



E Clock Timing (Memory Read/Write Cycle)
(I/O Read/Write Cycle)

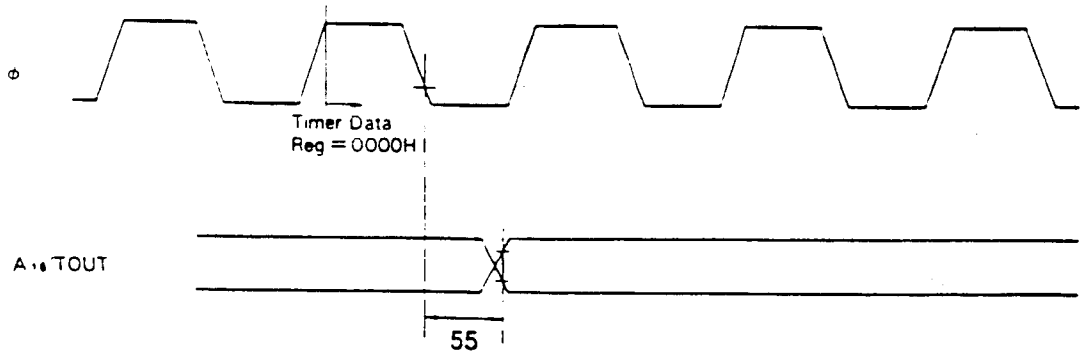


E Clock Timing (BUS RELEASE Mode
SLEEP Mode
SYSTEM STOP Mode)

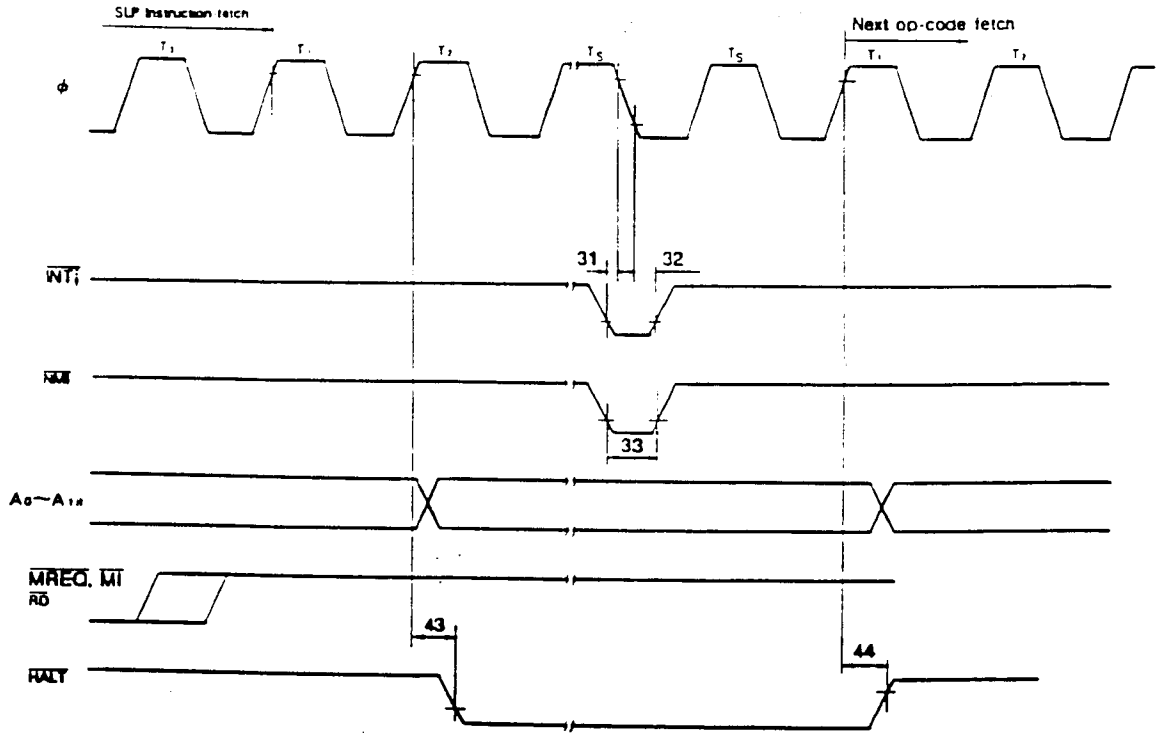


E Clock Timing (Minimum timing example of P_{WEL} and P_{WEH})

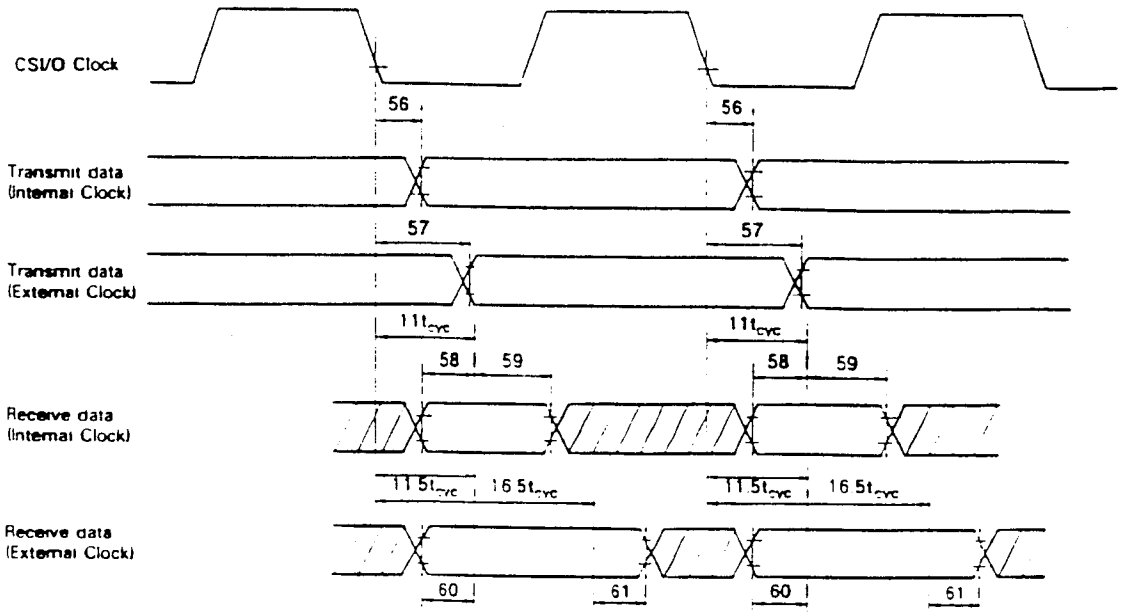
ELECTRICAL CHARACTERISTICS (Continued)
Timing Diagrams



Timer Output Timing



SLP Execution Cycle



CSI/O Receive/Transmit Timing

Z8S180 ERRATA

The following is a summary of a problem we've discovered on the current revision of the Z8S180.

The TRAP Problem

This version of the Z8S180 shows an anomaly in the operation of the TRAP bit of the INT/TRAP Control Register (ITC Register, I/O Address: 34H) when the following two conditions are gathered:

a. Extended instruction is used.

b. Operating voltage is less than 4.6 V.

Problem Description

The TRAP bit is a status bit. This bit is set by the CPU automatically to '1' when illegal opcode is fetched and is reset when the ITC is written.

In Z8S180, TRAP bit is set normally and TRAP interrupt is generated as Z80180. But the bit cannot be consistently reset by writing to the ITC register, i.e., the TRAP bit sometimes stays set and cannot be reset. Three factors determine whether the TRAP bit can be reset properly:

1. Speed
   Increasing the speed will increase the failure probability.

2. Operating Voltage
   Decreasing the operating voltage will increase the likelihood of failures.

3. Temperature
   Increasing the temperature will also increase the failure probability.

Workaround

The problem will be removed when:

a) Extended instruction is not used

or

b) Operating voltage is higher than 4.6 V

TRAP Bit Reset

The TRAP bit in the IN /TRAP Control Register (Address 34H) has to be set to 1 to reset the TRAP condition instead of writing a 0 as indicated in the databook.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com