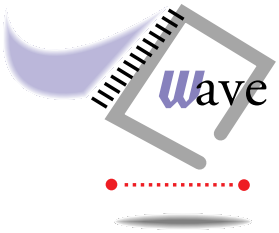

The Wave™ Chip

Z87L02/L03/L09

Flexible Frequency-Hopping Spread-Spectrum Voice/Data Cordless Controller

Product Specification

PS002100-WRL0899

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1. ARCHITECTURAL OVERVIEW

ZiLOG's Z87L02/L03/L09 is a baseband processor designed to implement Frequency-Hopping Spread-Spectrum communications in the ISM bands[1]. It is compliant with US FCC regulations. The flexibility of the Z87L0X devices allows for a variety of applications, including data or voice, point-to-point or multipoint. The 0.35 micron CMOS IC contains two DSP cores, dedicated RAM and ROM, and special-purpose circuitry to implement a spread spectrum modem. In particular, the device is capable of Time Division Duplex buffering of data or digitized voice, Frequency Shift Keying (FSK) modulation and demodulation, and frequency control of an external RF up/down converter.

The Z87L0X family is available in a variety of packages and configurations. The Z87L02 is a 100-pin VQFP or QFP device featuring internal factory-masked ROM for the DSP program code. The Z87L03 is a 144-pin VQFP version for external ROM or Flash program applications. Lastly, the Z87L09 is a 160-pin QFP in-circuit emulator version for external ROM or emulator-resident program applications.

The first application fully developed around the Z87L02/L03/L09 is a 900-MHz Spread-Spectrum Cordless Telephone. Therefore, the rest of this document is written with this application in mind. This document refers to ADPCM voice-compression software, and base station and handset modules. For data applications, the voice-compression software module is bypassed. The base station and handset correspond to master and slave (or base and terminal) functions. Additional information on data configuration is available from ZiLOG.

1.1 Z87L02 FEATURES

- Single-IC implementation of 900-MHz FHSS digital cordless telephone baseband functions
- Adaptive frequency hopping
- Transmit power control
- Error-control signalling
- Handset power management
- 32-Kbps ADPCM speech coding and decoding
- Multiple handset operation

A primary DSP (DSP1) core provides the following cordless telephone controller functions:

- ZiLOG-provided embedded software that governs transceiver operation and base-station-to-handset communications protocols

1. The Industrial, Scientific and Medical telecommunications standard refers to the operation of equipment or appliances designed to generate and use local radio-frequency energy for industrial, scientific, medical, or domestic purposes. The ISM category excludes applications in the field of telecommunications and information technology.

- OEM-modifiable software that implements user telephone features
- 32 K Words of program ROM and 512 words of data RAM, with access to an additional 1 K Word of Scratch Pad RAM configured as Program Memory
- Transceiver circuitry that provides cordless phone communications functionality
- Digital downconverter with frequency bias estimator
- FSK demodulator
- Bit synchronizer
- FSK modulator
- TDD transmit and receive buffers

A secondary DSP (DSP2) core performs the following voice processing functions:

- PCM to ADPCM transcoding
- DTMF tone generation
- Codec interface control
- 16 K Words of program ROM and 512 words of data RAM, plus an additional 1 K Word of RAM configured as Program Memory loaded by DSP1

The following additional features are provided:

- An internal low-current oscillator, driven by an external 16.384-MHz crystal that clocks the transceiver and primary DSP core to provide a low-noise reference frequency signal for an external RF synthesizer
- An internal 1-bit ADC and 4-bit DAC that supports 10.7-MHz IF signals to the external RF frequency up/downconverter
- An 8-bit ADC with multiplexed input that supports Received Signal Strength Indicator (RSSI) processing and sampling of two additional user-defined analog signals (for example, battery voltage monitoring)
- An internal I^2C interface that facilitates communication with external serial devices
- An integrated watch-dog timer to ensure robust operation
- 32 pins of programmable I/O available from DSP1, two inputs, and one output available from the secondary processor
- 8-bit data bus, plus address and control signals between primary and secondary processors, available externally for communication with other parallel devices
- Low current consumption in all cordless telephone operating modes
- 1 mA typical standby (oscillator and sleep timers on, DSP cores off)
- 20-mA typical talk (transceiver and both DSP cores on)
- Static 0.35-micron CMOS technology
- Operating frequency of 2.7 V to 3.3 V

- Operating temperature of –20°C to +70°C
- Available in a 100-pin VQFP or QFP factory-masked ROM package

1.2 Z87L03/Z87L09 FEATURES

In addition to the Z87L02 features listed above, the Z87L03/L09 includes the following:

- An external emulator interface (for DSP1 only in the Z87L09 package)
- Device configurability as:
  - Z87L02 with internal ROM
  - Z87L09 with emulation of DSP1 and DSP2 running from internal ROM
  - Z87L03/L09 with external ROM for DSP1 and internal ROM for DSP2
  - Z87L03/L09 in Z87L01 mode, with external Z87L10 (Z893X1)
- External Flash programming capability, specifically designed for up to 64 K Words of DSP1 program memory
- Available in both 144-pin VQFP (Z87L03), and 160-pin QFP (Z87L09) packages

FIGURE 1. Z87L02 FUNCTIONAL BLOCK DIAGRAM

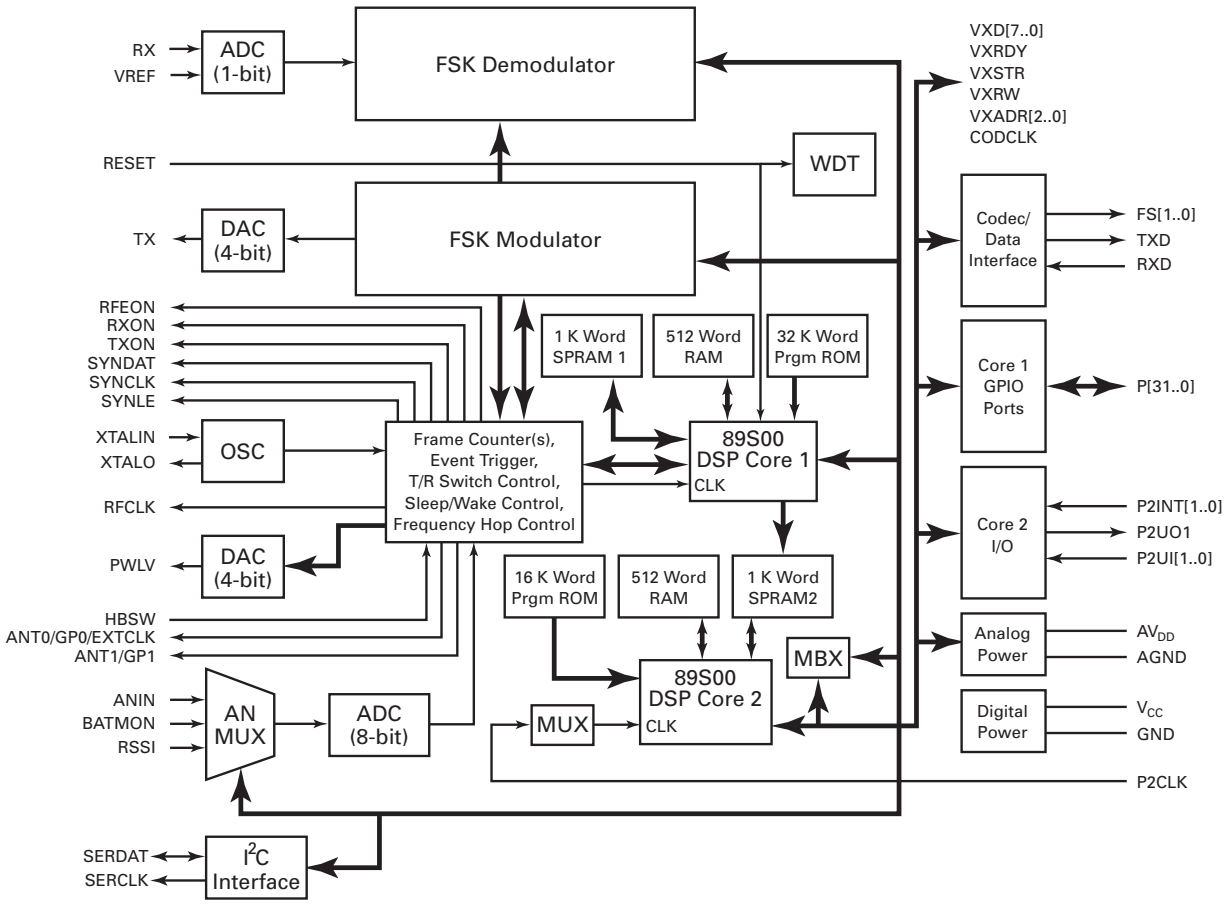
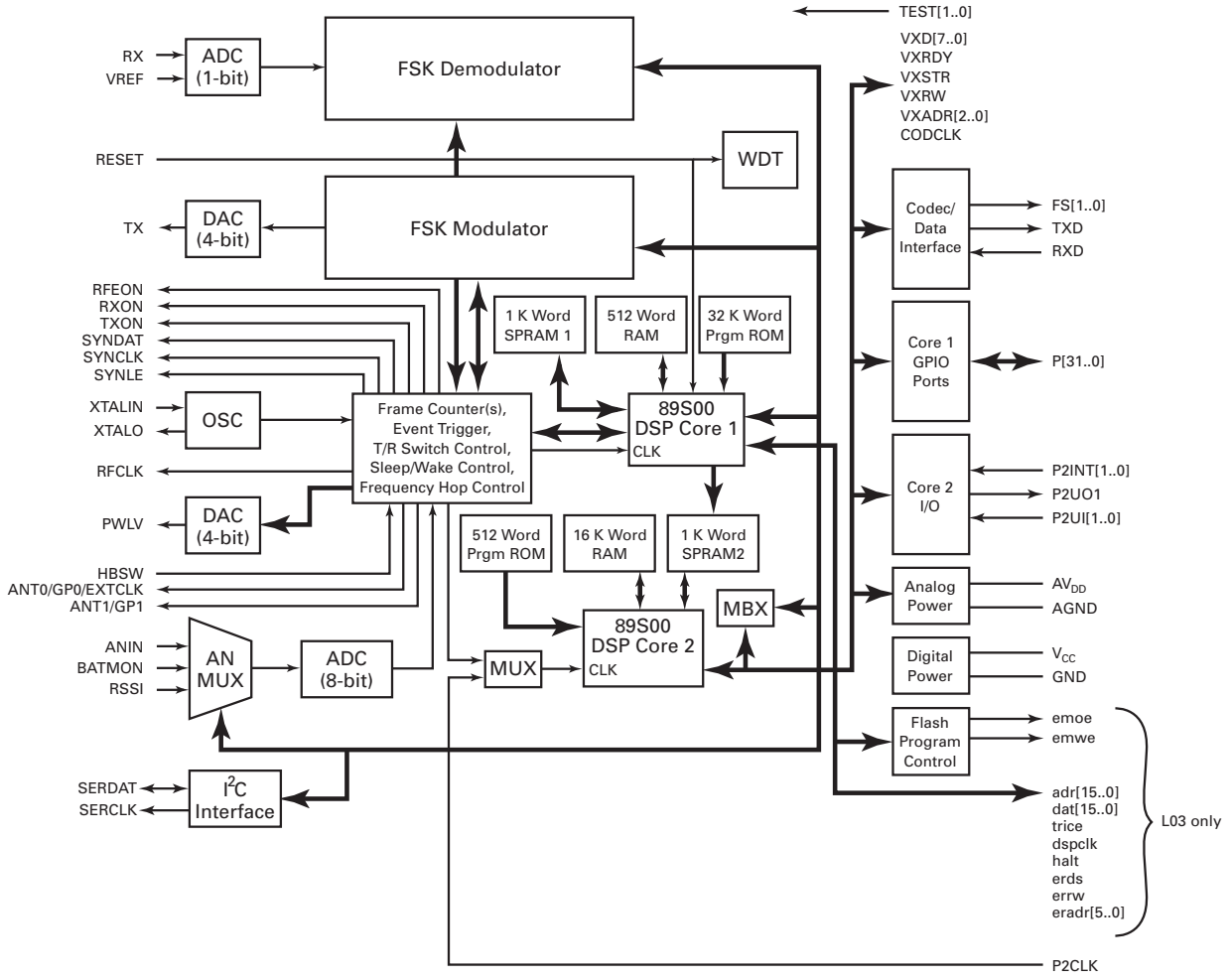


FIGURE 2. Z87L03/L09 FUNCTIONAL BLOCK DIAGRAM



2. PIN DESCRIPTION

FIGURE 3. Z87L02 100-PIN QFP

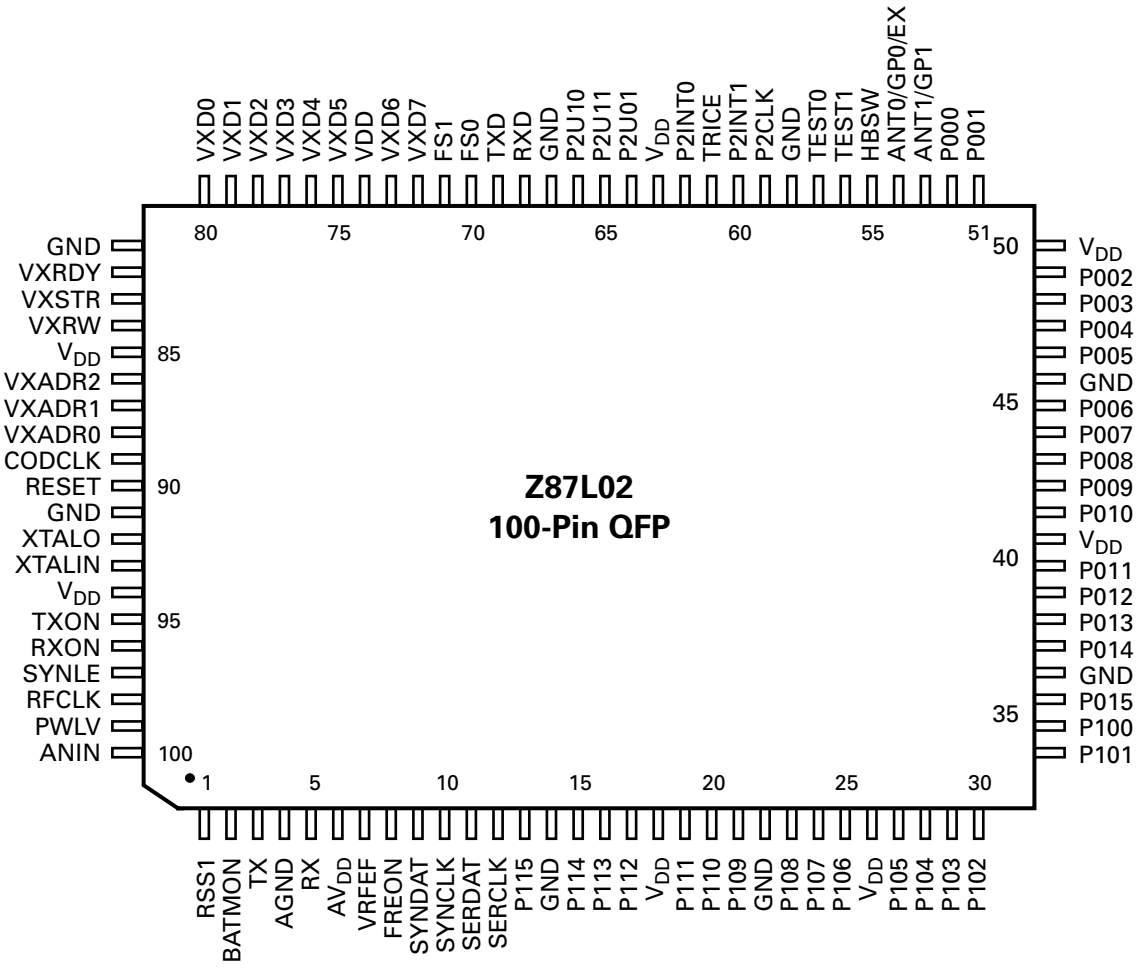


FIGURE 4. Z87L02 100-PIN VQFP

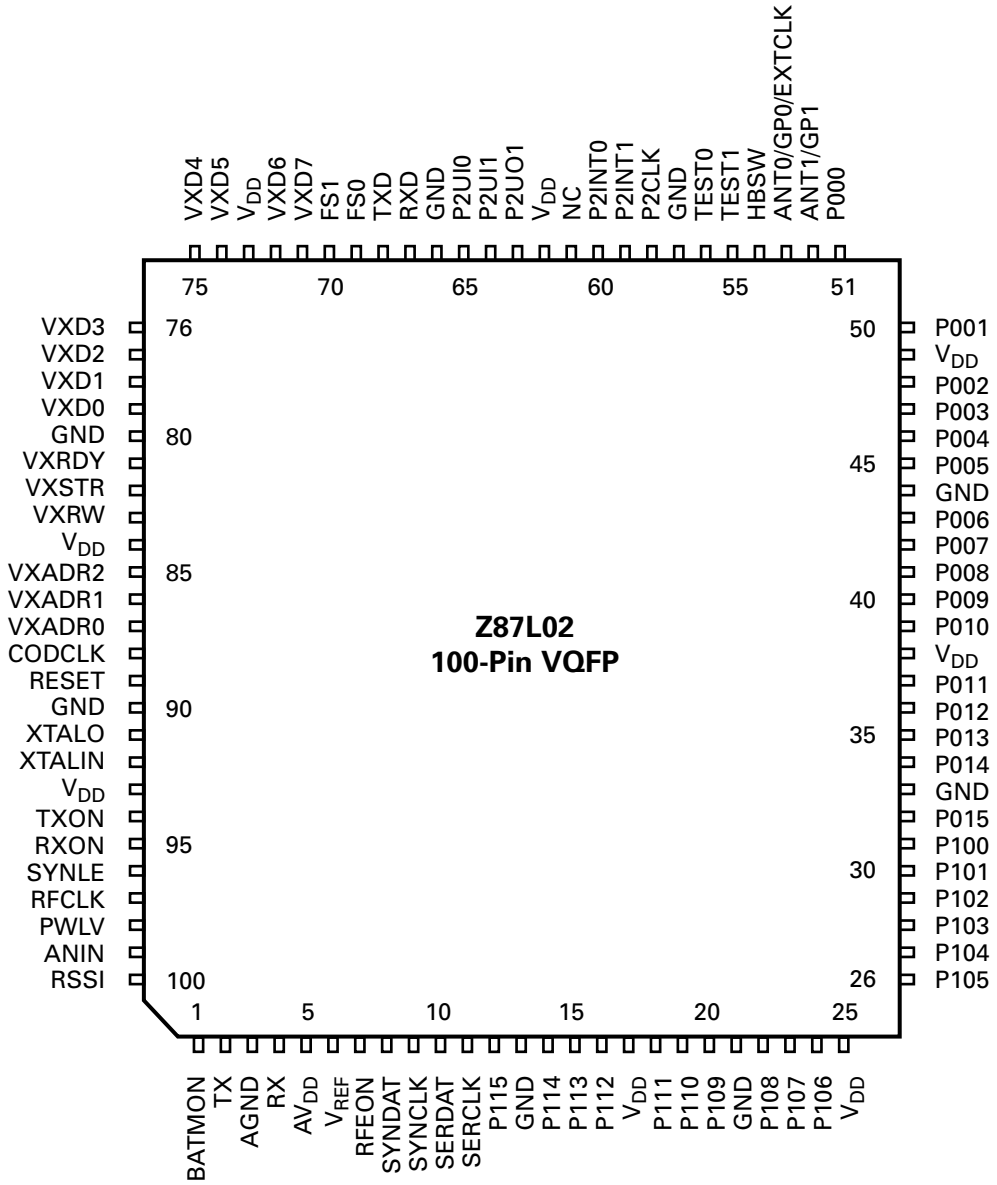


FIGURE 5. Z87L03 144-PIN VQFP

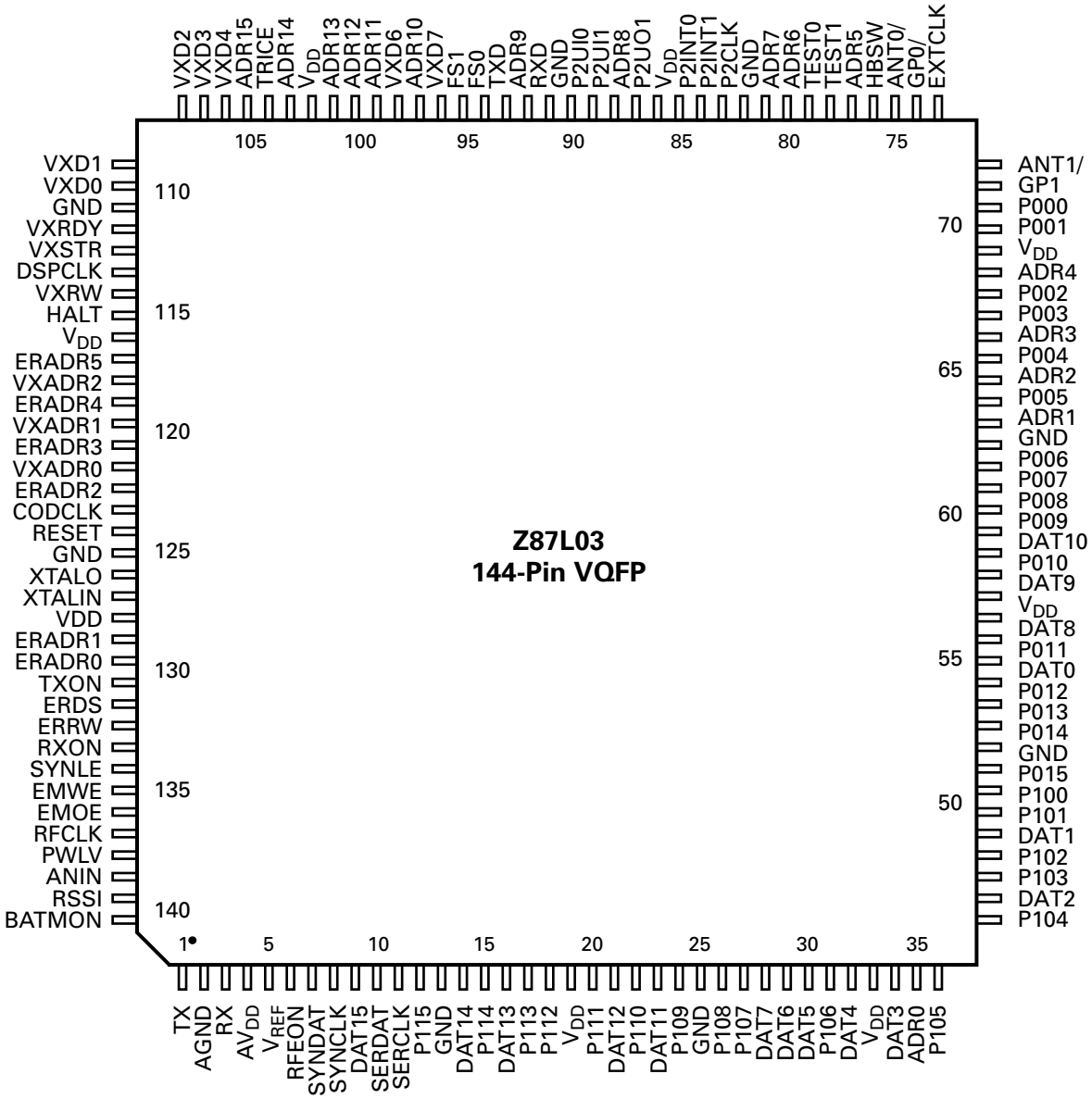


FIGURE 6. Z87L09 160-PIN QFP

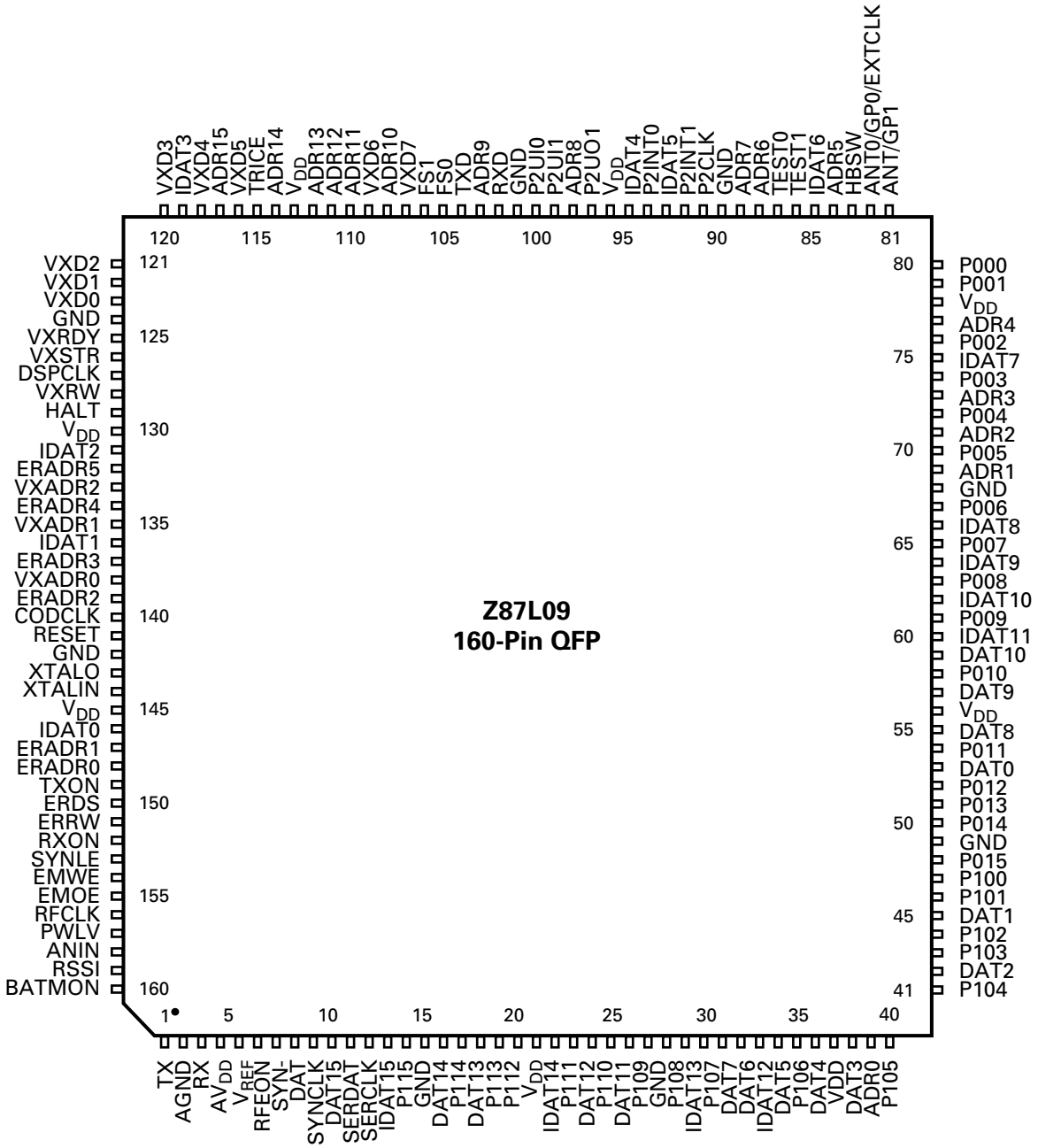


TABLE 1. PIN DESCRIPTION SUMMARY

Name	Main Function	Main Sense*	Z87L02 100-Pin VQFP Number	Z87L03 144-Pin VQFP Number	Z87L09 160-Pin QFP Number
V_{DD} (8)	Digital supply	—	17, 25, 38, 49, 62, 73, 84, 93	19, 33, 52, 69, 84, 101, 117, 130	20, 37, 56, 78, 96, 113, 130, 145
GND (8)	Digital ground	—	13, 21, 33, 44, 57, 66, 80, 90	13, 25, 45, 60, 80, 89, 111, 127	14, 27, 49, 68, 90, 101, 124, 142
AV_{DD}	Analog V_{DD}	—	5	4	4
AGND	Analog ground	—	3	2	2
BATMON	ADC analog input (Battery voltage)	AI	1	144	160
TX	Analog transmit IF signal	AO	2	1	1
RX	Analog receive IF signal	AI	4	3	3
V_{REF}	Analog reference voltage for RX signal	AO	6	5	5
RFEON	RF on/off control	O	7	6	6
SYNDAT	RF synthesizer data	O	8	7	7
SYNCLK	RF synthesizer clock	O	9	8	8
SERDAT	Data I/O, serial interface I^2C	I/O	10	10	10
SERCLK	Clock, serial interface I^2C	I/O	11	11	11
P[115..100] P[015..000]	DSP1 General-Purpose I/O	I/O/Z	12, 14, 15, 16, 18, 19, 20, 22, 23, 24, 26, 27, 28, 29, 30, 31, 32, 34, 35, 36, 37, 39, 40, 41, 42, 43, 45, 46, 47, 48, 50, 51	12, 15, 17, 18, 20, 22, 24, 26, 27, 31, 36, 37, 39, 40, 42, 43, 44, 46, 47, 48, 50, 54, 56, 57, 58, 59, 62, 64, 66, 67, 70, 71	13, 16, 18, 19, 22, 24, 26, 28, 30, 35, 40, 41, 43, 44, 46, 47, 48, 50, 51, 52, 54, 58, 61, 63, 65, 67, 70, 72, 74, 76, 79, 80
ANT0/GP0/ EXTCLK ANT1/GP1	RF diversity antenna control GPIO Outputs or External Clock output	O	53, 52	73, 72	82, 81
HBSW	Handset/Base station operation select	I	54	74	83
TEST[1..0]	Test mode select	I	55, 56	76, 77	86, 87
P2CLK	DSP2/Auxiliary voice processor clock	I/O/Z	58	81	91

NOTE: *Main Sense refers to input and output characteristics, as follows:

I = Input

O = Output

Z = 3-State

AI = Analog Input

AO = Analog Output

TABLE 1. PIN DESCRIPTION SUMMARY (CONTINUED)

Name	Main Function	Main Sense*	Z87L02 100-Pin VQFP Number	Z87L03 144-Pin VQFP Number	Z87L09 160-Pin QFP Number
P2INT[1..0]	DSP2 interrupts	I	59, 60	82, 83	92, 94
P2UO1	DSP2 user output	O	63	85	97
P2UI[1..0]	DSP2 user inputs	I	64, 65	87, 88	99, 100
RXD	Serial input from codec	I	67	90	102
TXD	Serial output to codec	O	68	92	104
FS[1..0]	Codec frame sync	I/O	69, 70	93, 94	105, 106
VXD[7..0]	DSP2 external register data bus	I/O/Z	71, 72, 74, 75, 76, 77, 78, 79	95, 97, 104, 106, 107, 108, 109, 110	107, 109, 116, 118, 120, 121, 122, 123
VXRDY	DSP2 ready	O/Z	81	112	125
VXSTR	DSP2 external register data strobe	I/O/Z	82	113	126
VXRW	DSP2 external register READ/ WRITE	I/O/Z	83	115	128
	DSP2 External Register address bus	I/O/Z	85, 86, 87	119, 121, 123	133, 135, 138
CODCLK	Codec clock	O	88	125	140
RESET	Master Reset	I	89	126	141
XTAL[1..0]	16.384-MHz crystal interface	I/O	91, 92	128, 129	143, 144
TXON	RF transmit control	O	94	133	149
RXON	RF receive control	O	95	136	152
SYNLE	RF synthesizer latch enable	O	96	137	153
RFCLK	RF synthesizer clock	O	97	140	156
PWLV	RF transmit level control	AO	98	141	157
ANIN	ADC analog input (spare)	AI	99	142	158
RSSI	ADC analog input (RSSI)	AI	100	143	159
adr[0..15]	DSP1 external Flash memory address bus	O/Z	NA	35, 61, 63, 65, 68, 75, 78, 79, 86, 91, 96, 98, 99, 100, 102, 105	39, 69, 71, 73, 77, 84, 88, 89, 98, 103, 108, 110, 111, 112, 114, 117
dat[15..0]	DSP1 external Flash memory data bus	I/O/Z	NA	9, 14, 16, 21, 23, 28, 29, 30, 32, 34, 38, 41, 49, 51, 53, 55	9, 15, 17, 23, 25, 31, 32, 34, 36, 38, 42, 45, 53, 55, 57, 59

NOTE: *Main Sense refers to input and output characteristics, as follows:

I = Input

O = Output

Z = 3-State

AI = Analog Input

AO = Analog Output

TABLE 1. PIN DESCRIPTION SUMMARY (CONTINUED)

Name	Main Function	Main Sense*	Z87L02 100-Pin VQFP Number	Z87L03 144-Pin VQFP Number	Z87L09 160-Pin QFP Number
trice	DSP1 Emulation/external Flash mode control	I	NA	103	115
dspclk	DSP1 clock	O/Z	NA	114	127
halt	DSP1 stop/single-step control	I	NA	116	129
idat[15..0]	DSP1 internal bus	O/Z	NA	NA	12, 21, 29, 33, 60, 62, 64, 66, 75, 85, 93, 95, 119, 131, 136, 146
	DSP1 External register address bus	O/Z	NA	118, 120, 122, 124, 131, 132	132, 134, 137, 139, 147, 148
erds	DSP1 External register data strobe	O/Z	NA	134	150
errw	DSP1 External register READ/ WRITE control	O/Z	NA	135	151
emwe	External Flash memory WRITE enable	O	NA	138	154
emoe	External Flash memory output enable	O	NA	139	155
NC	No internal connection	—	61	NA	NA

NOTE: *Main Sense refers to input and output characteristics, as follows:

I = Input

O = Output

Z = 3-State

AI = Analog Input

AO = Analog Output

3. PIN FUNCTIONS

V_{DD}. Digital power supply.

GND. Digital ground.

AV_{DD}. Analog power supply.

AGND. Analog ground.

TX (analog output). This pin is the IF transmit signal from the modulator and 4-bit DAC. The TX pin is a Frequency-Shift Key (FSK) modulated burst signal with the harmonic component of interest centered at 10.7 MHz. This pin is also available to the RF section for upconversion to 900 MHz.

RX (analog input). This pin is the IF receive signal from the RF downconverter to the analog comparator and FSK demodulator. The RX pin is internally biased to the V_{REF} DC voltage, requiring AC coupling to the downconverter output.

V_{REF} (analog input). This pin is the reference voltage used by the high-speed analog comparator to sample the RX input signal. The V_{REF} pin connects to AGND via a capacitor.

RFEON (output; active High). This pin controls the on/off function for the RF module. The RFEON pin is active (on) during wake periods and inactive (off) during sleep periods on the handset.

SYNDAT (output). This pin provides external RF synthesizer programming data, configurable by the user to support a variety of PLL devices. Programmable polarity is inactive (off) during sleep periods on the handset. SYNDAT is sourced from the DSP1 auxiliary GPIO port.

SYNCLK (output; active High). This pin provides an external RF synthesizer clock. Programmable polarity is inactive (off) during sleep periods on the handset. SYNCLK is sourced from the DSP1 auxiliary GPIO port.

SERDAT (input/output). This pin is an I^2C-compatible serial interface data line, to/from the hardware serial interface block.

SERCLK (input/output). This pin is an I^2C-compatible serial interface clock line, sourced from/to the serial interface block.

P[115..000] (input/output). These pins are the DSP1 general-purpose I/O ports. The direction is bit-programmable. Pins P[003..000], when configured in input mode, can also be individually programmed as DSP1 wake-up pins (wake-up active Low).

P000	WAKEUP0
P001	WAKEUP1
P002	WAKEUP2
P003	WAKEUP3

P114, when configured in input mode, can also behave as a maskable interrupt/ wake-up pin for the DSP1.

P114	INT0

ANT0/GP0/EXTCLK & ANT1/GP1 (output). These pins are the control for an optional RF antenna diversity, general-purpose outputs, or EXTCLK.

HBSW (input with internal pull-up). This pin allows handset/base configuration. The HBSW pin must either be pulled High, not connected for handset, or driven Low for base.

TEST[1..0] (input with internal pull-down, active High). These pins function as test-mode control pins. Specific test modes are explained in Table 2. TEST[1..0] is tied to GND during normal operation.

P2CLK (output/input). This pin is a DSP1 clock output to DSP2, and also routes to the external pin to support an external voice processor. Internal multiplexers can be set to disable the internal connection from the DSP1 and configure P2CLK solely as a DSP2 input for separate clock operation.

P2INT[1..0] (input; active Low). These pins facilitate DSP2 interrupt requests. Interrupts are generated on the rising edge of the input signal. Vectors for the starting addresses of interrupt service routines are stored in program memory locations 7FFFh and 7FFDh for INT0 and INT1, respectively. INT1 is the lowest priority. If the peripheral is enabled, INT1 is dedicated to the 13-bit timer.

P2UO1 (output). This pin is a DSP2 general-purpose output pin (controlled by Status Register Bit 6).

P2UI[1..0] (input). This pin is a DSP2 general-purpose input pin (controlled by Status Bits 11 and 10, respectively).

RXD (input). This pin serves as a serial input from the external codec. RXD is routed to the codec interface block, controlled by DSP2.

TXD (output). This pin serves as a serial output to the external codec. TXD is routed from the codec interface block, controlled by DSP2.

FS[1..0] (output). These pins are the individual codec frame sync pulses from the codec interface block, controlled by DSP2.

VXD[7..0] (input/output). These pins are the data bus of the DSP2 or an external voice processor. It transfers the ADPCM voice- and error-control data to and from the transceiver. Internal muxes also provide for either monitoring the DSP2 outputs or for directly driving the DSP1 inputs for test purposes.

VXRDY (input/output, active hi). This pin is the Ready control for the VXD bus. This signal is driven High (deasserted) by the DSP1 to insert wait states in the (internal or external) voice processor accesses. The internal muxes provide for

either monitoring the DSP1 output or for directly driving the DSP2 input for test purposes.

VXSTR (input/output). This pin is the data strobe signal for the VXD bus, sourced by an external voice processor or the internal DSP2. Internal muxes provide for external monitoring of the DSP2 output, or for directly driving the DSP1 input for test purposes.

VXRW (input/output). This pin is the READ/WRITE control for the VXD bus, sourced by either an external voice processor or the internal DSP2. Internal muxes provide for external monitoring of the secondary processor output, or for directly driving the DSP1 input for test purposes.

VXADR[2..0] (input/output). These pins are the address bus for the DSP2 or an external voice processor. The DSP1 acts as a peripheral of the voice processor. Internal muxes provide for external monitoring of the secondary processor outputs, or for directly driving the DSP1 inputs for test purposes.

CODCLK (output). This pin provides the clock output for the external codec; it is also provided to DSP2.

RESET (input, active Low). This pin facilitates the RESET signal to DSP1.

XTALIN, XTALO (analog input, output). These pins connect to an external 16.384-MHz crystal.

TXON (output; active High). This pin allows on/off control for the RF transmit circuitry. The TXON is active during transmit periods.

RXON (output; active High). This pin allows on/off control for the RF receive circuitry. The RXON is active during wake periods.

SYNLE (output). This pin provides an RF synthesizer Latch Enable pulse that combines with SYNDAT and SYNCLK for programming the RF PLL. This pin exhibits programmable polarity and is active during wake periods.

RFCLK (output). This pin provides the 16.384-MHz RF synthesizer reference clock. RFCLK is active during wake periods.

PWLV (analog output). This pin is the power-level control for the RF transmit circuitry and is the output from a 4-bit DAC. PWLV is active during transmit periods.

ANIN (analog input). This pin is one of three multiplexed inputs to the 8-bit ADC.

RSSI (analog input). This pin is one of three multiplexed inputs to the 8-bit ADC, and is nominally dedicated to monitoring the RF Received Signal Strength Indicator.

BATMON (analog input). This pin is one of three multiplexed inputs to the 8-bit ADC, and is nominally dedicated to monitoring the handset battery voltage.

adr[0..15] (output/high impedance). These pins are the DSP1 3-statable program memory address bus and external Flash address bus (Z87L03/L09 only).

dat[15..0] (input/output). These pins control the DSP1 program memory data bus input or the external Flash memory data bus input/output (Z87L03/L09 only).

trice (input with internal pull-up, active High). This pin is a 3-state control for the DSP1 buses adr[0..15], dat[15:0], idat[15..0], eradr[4..0], dspclk, erds and errw. This pin also engages emulation and external ROM operation when deasserted (Z87L03/L09 only).

dspclk (output/high impedance). This pin is a 3-statable DSP1 processor clock monitor (Z87L03/L09 only).

halt (input with internal pull-down, active High). This pin allows DSP1 stop/single-step control (Z87L03/L09 only). If Z87L03 is used for design, this input should be tied to GND through a 10-KΩ resistor.

idat[15..0] (output/high impedance). 3-statable DSP1 internal data bus (Z87L09 only).

eradr[5..0] (output/high impedance). 3-statable external register address bus (Z87L03/L09 only). This bus features:

- ea[2:0] external register address bus —eradr[2:0]
- Status Bits 6,5—eradr[4,3]
- High/Low Bank Select—eradr[5]. When this bit is set to 1, External register banks 4,5,6,7 are selected; otherwise External register banks 0,1,2,3 are selected. On Power-On Reset, this bit is set to 0.

erds (output/high impedance). This pin is a 3-statable external register data strobe for DSP1 (Z87L03/L09 only).

errw (output/high impedance). This pin is the 3-statable external register READ/WRITE control for DSP1 (Z87L03/L09 only).

emwe (output). This pin is the external Flash memory WRITE enable (Z87L03/L09 only). The emwe pin is set to 1 on Power-On Reset.

emoe (output). This pin allows the external Flash memory output enable (Z87L03/L09 only). The emoe pin is set to 0 on Power-On Reset.

4. OPERATIONAL DESCRIPTION

4.1 Z87L03/L09

The Z87L03/L09 can be configured to operate in three distinct modes. In addition to the nominal operation described above, the Z87L03/L09 may be configured as a stand-alone cordless telephone processor (that is, the complete Z87L03/L09 functionality, except for the voice processor and codec interface, which are disabled). This telephone processor configuration corresponds to the functionality of the ZiLOG Z87L01. The device may be further configured for internal ROM or In-Circuit Emulation/External ROM operation in both Z87L03/L09 and Z87L01 modes.

A third operating mode supports initialization of the Z87L03/L09 with external Flash configuration, specifically when the external memory is writable using on-chip Flash programming capability. In this mode, the DSP1 executes the program from the internal test ROM, downloading blocks of program data from a compatible outside source through the I^2C interface. The DSP, in turn, programs the external Flash.

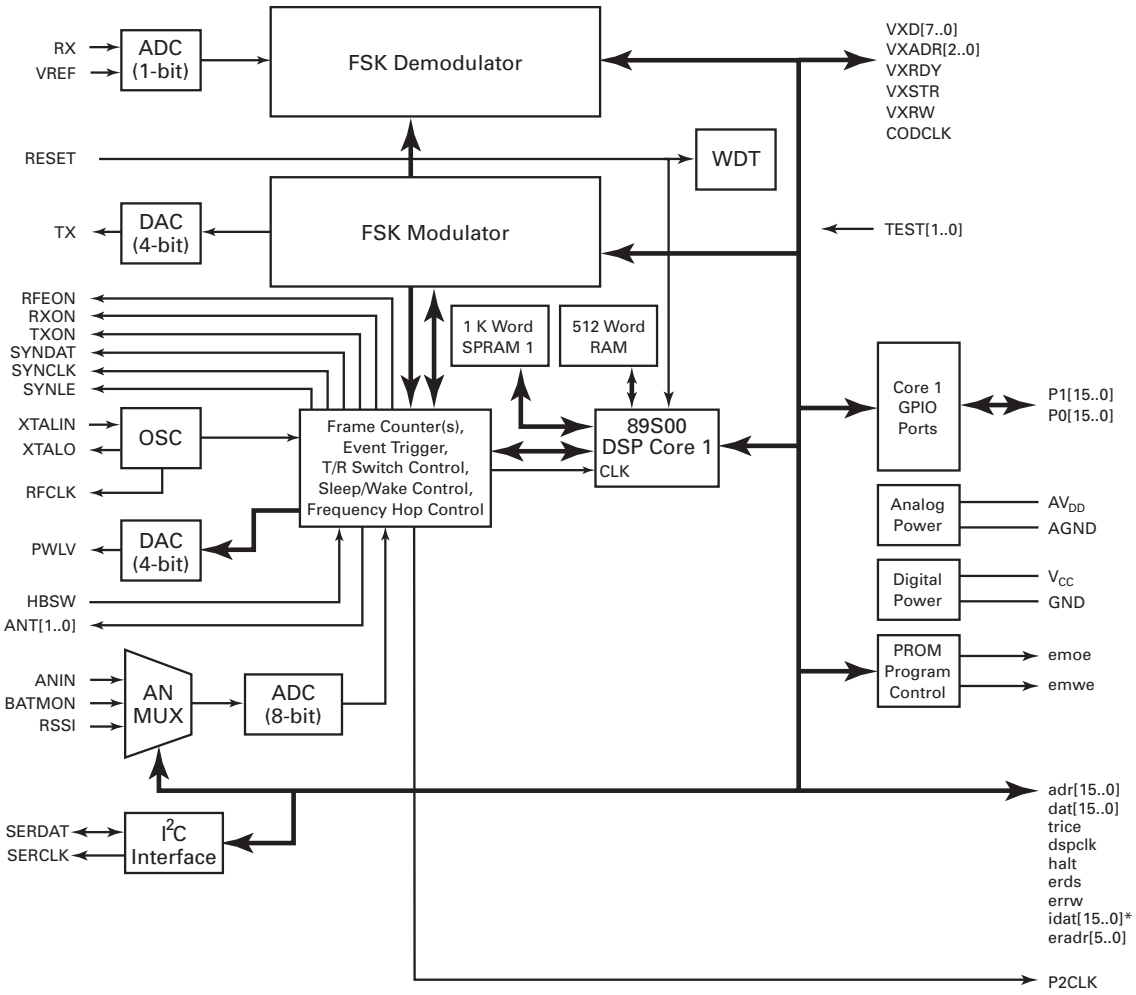
Table 2 summarizes the alternative operating modes and their corresponding enabling TEST[1..0] and trice pin assertions.

TABLE 2. Z87L03/L09 OPERATING MODE SUMMARY

	Pin Settings			DSP1 Configuration		DSP2 Configuration	
Operating Mode	**TEST1**	**TEST0**	**trice**	**Program Address**	**Program Data**	**Program Address**	**Program Data**
Z87L03/L09, internal ROM	0	0	1	To internal ROM	From internal ROM	To internal ROM	From internal ROM
Z87L09, ICE/external ROM	0	0	0	To adr[0..15] bus	From dat[15..0] bus	To internal ROM	From internal ROM
Z87L01, internal ROM	0	1	1	To internal ROM	From internal ROM	Disabled	Disabled
Z87L01, ICE/external ROM	0	1	0	To adr[0..15] bus	From dat[15..0] bus	Disabled	Disabled
Z87L01 test ROM	1	0	1	To internal ROM	Internal Data	Disabled	Disabled
Z87L03/L09, external reprogrammable memory initialization	1	1	x	See Table 4	See Table 4	Disabled	Disabled

Figure 7 illustrates the functional block diagram of the Z87L03/L09 when configured in the Z87L01 ICE/External ROM mode.

FIGURE 7. BLOCK DIAGRAM—Z87L03/L09 CONFIGURED AS Z87L01



*Note: L09 Only.

Z87L03/L09 pins are reconfigured depending on the operating mode. Table 3 lists the pin functions for both the Z87L03/L09 (including external reprogrammable memory initialization operation) and Z87L01 modes.

TABLE 3. Z87L03/L09 PINS BY MODE

Z87L03/L09 Configuration			Z87L01 Configuration		
Function	**Sense[1]**	**State on Reset[2]**	**Function**	**Sense[1]**	**State on Reset[2]**
TX	AO	O	TX	AO	O
AGND	—	—	AGND	—	—
RX	AI	I	RX	AI	I
AV_{DD}	AI	I	AV_{DD}	AI	I
V_{REF}	AI	I	V_{REF}	AI	I
RFEON	O	O	RFEON	O	O
SYNDAT	O	O	SYNDAT	O	O
SYNCLK	O	O	SYNCLK	O	O
SERDAT	I/O	I	SERDAT	I/O	I
SERCLK	O	I/O	SERCLK	O	O
P[115..100]	I/O/Z	I	P[115..100]	I/O/Z	I
GND	—	—	GND	—	—
adr[0..15]	O/Z	O/Z	adr[0..15]	O/Z	O/Z
V_{DD}	AI	I	V_{DD}	AI	I
P[015..000]	I/O/Z	I	P[015..000]	I/O/Z	I
idat[15..0]	O/Z	O/Z	idat[15..0]	O/Z	O/Z
ANT1[3]	O/Z	O**	ANT1[3]	O/Z[c]	O
ANT0[3]	O/Z	O**	ANT0[3]	O/Z[c]	O
dat12	I/O/Z	O/Z	dat12	I/O/Z	I
HBSW	I	I	HBSW	I	I
TEST1	I	I	TEST1	I	I
TEST0	I	I	TEST0	I	I
dat[15..0]	I/O/Z	I	dat[15..0]	I/O/Z	I
P2CLK	I/O/Z	O	P2CLK	O/Z	O
P2INT1	I	I	VPINT[4]	I	I
P2INT0	I	I	VPRESET[5]	O	O
P2UO1	O	O	NC	—	—
P2UI1	I	I	NC	—	—
P2UI0	I	I	NC	—	—
RXD	I	I	NC	—	—
TXD	O	O	NC	—	—

NOTES:

1. Sense abbreviations: I = Input; O = Output; Z = 3-State; AI = Analog Input; AO = Analog Output.
2. State on Reset abbreviations: I = Input; O = Output; Z = 3-State; AI = Analog Input; AO = Analog Output.
3. ANT1 and ANT0 are inputs in Test modes.
4. VPINT is connected internally to a DSP1 auxiliary port configured as an interrupt input, and to a dedicated secondary processor user output port. In the Z87L01 configuration, the pin serves as a DSP1 interrupt input from the external voice processor.
5. VPRESET is connected internally to a DSP1 auxiliary port configured as an output, and to the secondary processor's RESET input. In the Z87L01 configuration, the pin serves as the primary reset output to the external voice processor.

TABLE 3. Z87L03/L09 PINS BY MODE (CONTINUED)

Z87L03/L09 Configuration			Z87L01 Configuration		
Function	**Sense[1]**	**State on Reset[2]**	**Function**	**Sense[1]**	**State on Reset[2]**
FS1	O	O	NC	—	—
FS0	O	O	NC	—	—
VXD[7..0]	I/O/Z	I	VXD[7..0]	I/O/Z	I
VXRDY	I/O	I	VXRDY	I/O	I
trice	I	I	trice	I	I
VXSTR	O	I	VXSTR	I	I
dspclk	O	O	dspclk	O	O
VXRW	O	I	VXRW	I	I
halt	I	I	halt	I	I
eradr5	O/Z	O/Z	eradr5	O/Z	O/Z
VXADR[2..0]	O	I	VXADR[2..0]	I	I
eradr[4..0]	O/Z	O/Z	eradr[4..0]	O/Z	O/Z
CODCLK	O/Z	O	CODCLK	O/Z	O
RESET	I	I	RESET	I	I
XTALO	AO	O	XTALO	AO	O
XTALIN	AI	I	XTALIN	AI	I
erds	O/Z	O/Z	erds	O/Z	O/Z
TXON	O	O	PAON	O	O
errw	O/Z	O/Z	errw	O/Z	O/Z

NOTES:
1. Sense abbreviations: I = Input; O = Output; Z = 3-State; AI = Analog Input; AO = Analog Output.
2. State on Reset abbreviations: I = Input; O = Output; Z = 3-State; AI = Analog Input; AO = Analog Output.
3. ANT1 and ANT0 are inputs in Test modes.
4. VPINT is connected internally to a DSP1 auxiliary port configured as an interrupt input, and to a dedicated secondary processor user output port. In the Z87L01 configuration, the pin serves as a DSP1 interrupt input from the external voice processor.
5. VPRESET is connected internally to a DSP1 auxiliary port configured as an output, and to the secondary processor's RESET input. In the Z87L01 configuration, the pin serves as the primary reset output to the external voice processor.

4.2 PRODUCTION TEST MODES

A set of 2 specialized Z87L02/L03/L09 configurations, not ordinarily accessible to the user, are bundled into a fourth operating mode called the PRODUCTION TEST mode. Intended for high-speed wafer scale IC testing, this mode is accessed by setting the TEST1 and TEST0 to a logic 1, and appropriately asserting the ANT[1..0] pins, which are specially configured as inputs for this purpose. Table 4 summarizes the test configurations, corresponding program address and data sources, and Port reassignments. Following Table 4 is a full definition of the specific tests employed.

TABLE 4. Z87L02/L03/L09 PRODUCTION TESTS

Test MODE 3 TEST[1:0] = [1,1]	Test Code		Program Execution	
	ANT1	ANT0	Program Address	Program Data
DSP and ROM Tests	0	0	NA	
DSP1 Port Test[1]	0	1	NA	P[115..100]
Transceiver and Peripherals Test[2]	1	0	NA	P[115..100]

NOTES:
1. Refer to Table 5 for more specific test definitions and parameters.
2. Refer to Table 6 for more specific test definitions and parameters.

4.3 DSP AND ROM TESTS

The Z87L02/L03/L09 is configured to access the program code from an external tester. Test program code is placed on port bits P115 through P100 of the DSP1 bus. Other control signals required to perform the DSP test (DSP1 only) are accessed though ports P000 through P015, (Table 5).

TABLE 5. P BUS SIGNAL FUNCTIONS FOR DSP TEST

Name	Test Function	Direction
P[115..100]	Program Data Bus	I
P000	DSP1 status register bit 5	O
P001	DSP1 status register bit 6	O
P002	DSP1 halt signal	I
P003	DSP1 ext_wait signal	I

The DSP1 addresses its internal ROM, effectively copying the program data sequentially into ports 16 through 31 of its P bus for verification by the external tester. This operation is followed by the secondary bus, which dumps its ROM, High byte followed by Low byte, onto the VXD[7..0] pins.

4.4 DSP1 PORT TEST

Reconfiguration of the P bus for program input and output in the DSP and ROM Test does not allow testing of the normal P bus operation. The DSP1 Port Test allows the Z87L02/L03/L09 to access test program data from the internal test ROM within the DSP1 program memory to fully test the P bus.

4.5 TRANSCEIVER AND PERIPHERALS TEST

The Z87L02/L03/L09 is configured to fully test the transceiver watch-dog timer, 3 way analog mux, and the I^2C serial interface. In this mode, the external tester provides the test program through the upper 16 P bus ports. The lower 16 P bus ports are used to source or monitor test signals (Table 6).

TABLE 6. P BUS PIN DEFINITIONS FOR THE TRANSCEIVER AND PERIPHERALS TEST

	Port Configuration			
XCVR Test Mode	**Pin**	**Name**	**Direction**	**Function**
1-bit ADC Test	P001	ADCOUT	O	Internal 1-bit ADC output data, sampled on rising edges of ADCCLK.
	P002	ADCCLK	O	Sample clock output of the internal ADC (8.192 MHz).
1-bit ADC Bypass (external ADC)	P001	DEMODIN	I	Demodulator input data from the external 4, sampled by the Z87L0X on rising edges of the ADCCLK sample clock.
	P002	ADCCLK	O	Sample clock output for the external ADC (8.192 MHz).
TX 4-bit DAC Bypass (external DAC)	P[005..003]	MODOUT[3..0]	O	Modulator 3-bit output data to the external DAC, updated on rising edges of DACCLK; 4th bit should be set to 1.
	P006	MODOUTCLK	O	Sample clock of the modulator output, for reference (8.192 MHz).
TX 4-bit DAC Test	P[10..7]	DACIN[3..0]	I	4-bit input data for internal DAC
	P006	MODOUTCLK	O	Sample clock of modulator output for reference (8.192 MHz).
Modulator Test	P012	MODIN	I	Input data for the modulator, sampled on rising edges of MODCLK.
	P013	MODCLK	O	Sample clock of the internal modulator (93.091 kHz).
Modulator bypass (external modulator or baseband transfer)	P012	TXOUT	O	Baseband serial output data, updated on the rising edges of MODCLK.
	P013	MODCLK	O	Sample clock output for the external modulator (93.091 kHz).
	P011	CODCLKIN	I	Codec clock input for the handset only (2.048 MHz).
Demodulator Test	P014	DEMODOUT	O	Demodulator output data, updated on the rising edges of DEMODCLK.
	P015	DEMODCLK	O	Recovered symbol clock from the internal demodulator (93.091 kHz).
Demodulator Bypass (external demodulator or baseband transfer)	P015	RXIN	I	Baseband serial input data, sampled on the rising edges of DEMODCLK.
	P014	DEMODCLK	I	Recovered symbol clock from the external demodulator (93.091 kHz).
	P011	CODCLKIN	I	Codec clock input for the handset only (2.048 MHz).

4.6 DUAL CORE INTERFACE TEST

After individual testing of the DSP1 and DSP2 is complete, the Dual Core Interface Test is employed to exercise the interprocessor operation and communication from separate clock sources. The device is configured with both processors active. Test program data is accessed from the corresponding processor's test ROM.

5. FUNCTIONAL DESCRIPTION

5.1 PARTITIONING OF THE FUNCTIONAL BLOCKS

The Z87L02/L03/L09 is composed of 5 distinct functional blocks: transceiver, DSP1, DSP1 peripherals, secondary processor, and codec interface. These blocks are described in detail in the sections that follow.

5.2 TRANSCEIVER

The transceiver features special-purpose digital DSP and analog circuitry that implements the dedicated cordless telephone functionality. The transceiver features 3 main blocks: the receiver, transmitter and event trigger.

Contained within the receiver are the following blocks:

- A receive 1-bit ADC
- A demodulator, including:
  - IF downconverter
  - Automatic Frequency Control (AFC)
  - Limiter-discriminator
  - Matched filter
  - Bit synchronizer
  - Bit inversion
  - Frame synchronizer (Unique Word detector)
  - SNR detector
- A receive frame timing counter
- A receive buffer and voice interface

For the transmitter, the blocks include:

- A transmit buffer and voice interface
- A transmit frame timing counter (used on the base station only)
- A modulator
- A transmit 4-bit DAC

The final block of the transceiver, the event trigger, features:

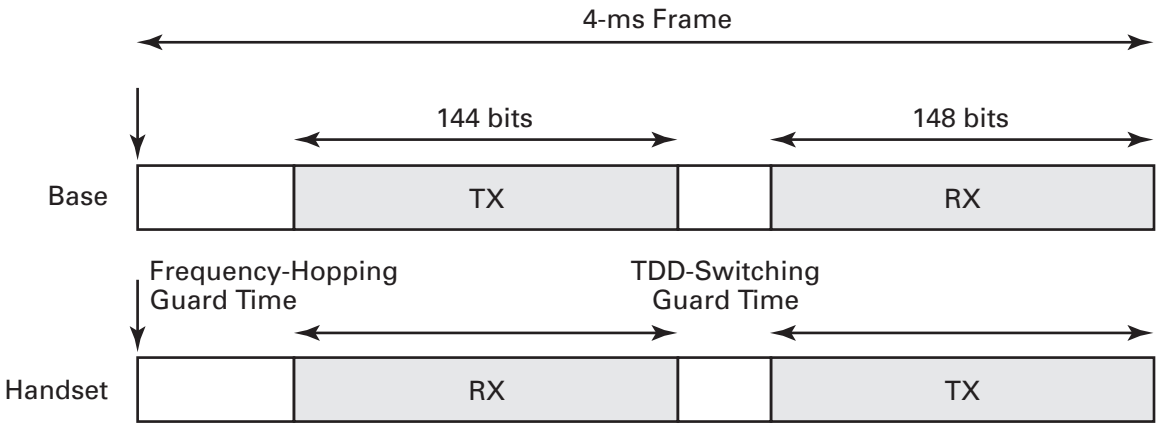
- On/off switch controls for the transmitter, receiver, and RF section
- A transmit/receive switch control
- A 4-bit DAC for setting the transmit power level
- An analog switch and 8-bit ADC for sampling the Received Signal Strength Indicator (RSSI) and handset battery voltage

5.3 BASIC TRANSCEIVER OPERATION

The transmitter and receiver operate in a time-division duplex (TDD): handset and base station transmit and receive (Figure 8).The TDD duty cycle lasts 4 ms, during which time the following events occur:

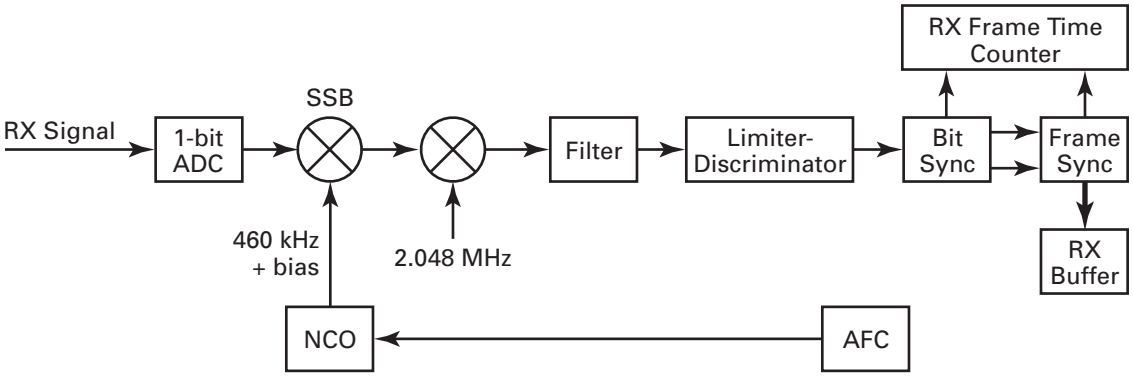
- The hopping frequency changes at the start of the cycle
- The base station transmits a frame of 144 bits while the handset receives
- The handset then transmits a frame of 148 bits while the base receives

FIGURE 8. TIMING FOR A BASIC TIME-DIVISION DUPLEX



5.4 RECEIVER BLOCK

FIGURE 9. DEMODULATOR BLOCK DIAGRAM



5.4.1 1-Bit ADC

The incoming receive signal at the RX analog input pin is sampled by a 1-bit analog-to-digital converter at 8.192 MHz.

The receive signal is modulated by Frequency Shift Keying (is the) with a carrier frequency of 10.7 MHz. The instantaneous frequency oscillates at 10.7 MHz ±32.58 kHz. The data rate is 93.09 Kbps, and the sample rate is 8.192 MHz. This rate yields 88 samples per data bit. The oversampled data is further processed by the demodulator to retrieve the baseband information.

The 1-bit converter is implemented with a fast comparator, which determines whether the RX signal is larger or smaller than a reference signal (V_{REF}). The transceiver internally generates the DC level of both the V_{REF} and RX input pins. As a result, the received signal, at 10.7 MHz, should be AC-coupled to the RX pin via a coupling capacitor. To ensure accurate operation of the converter, the user should also attach to the V_{REF} pin a network which exhibits an impedance that matches the DC impedance observed in the RX pin.

5.4.2 Demodulator

The demodulator includes a two-stage IF downconverter that brings the sampled receive signal to baseband. The narrow band 10.7-MHz receive signal, sampled at 8.192 MHz by the 1-bit ADC, provides a 2.508-MHz useful image. The first local oscillator used to downconvert this IF signal is obtained from a numerically controlled oscillator (NCO). The NCO is internal to the transceiver, and generates a nominal frequency of 460 kHz. The resulting signal is 2.048 MHz (2.508 MHz minus 460 kHz). A second downconversion by a 2.048-MHz clock, derived from the 16.384-MHz clock, brings the receive signal to baseband.

The exact frequency of the 460-kHz NCO is slightly adjusted by the Automatic Frequency Control (AFC) loop for exact downconversion of the end signal to the zero frequency. The AFC circuit detects any DC component in the output of the limiter-discriminator (Figure 10) when receiving a known sequence of data (preamble). This DC component is the *frequency bias*. The bias estimate out of the AFC can be read and subsequently filtered by the DSP processor on every frame. The processor then adds or subtract this filtered bias to/from the NCO control word to correct the NCO frequency output.

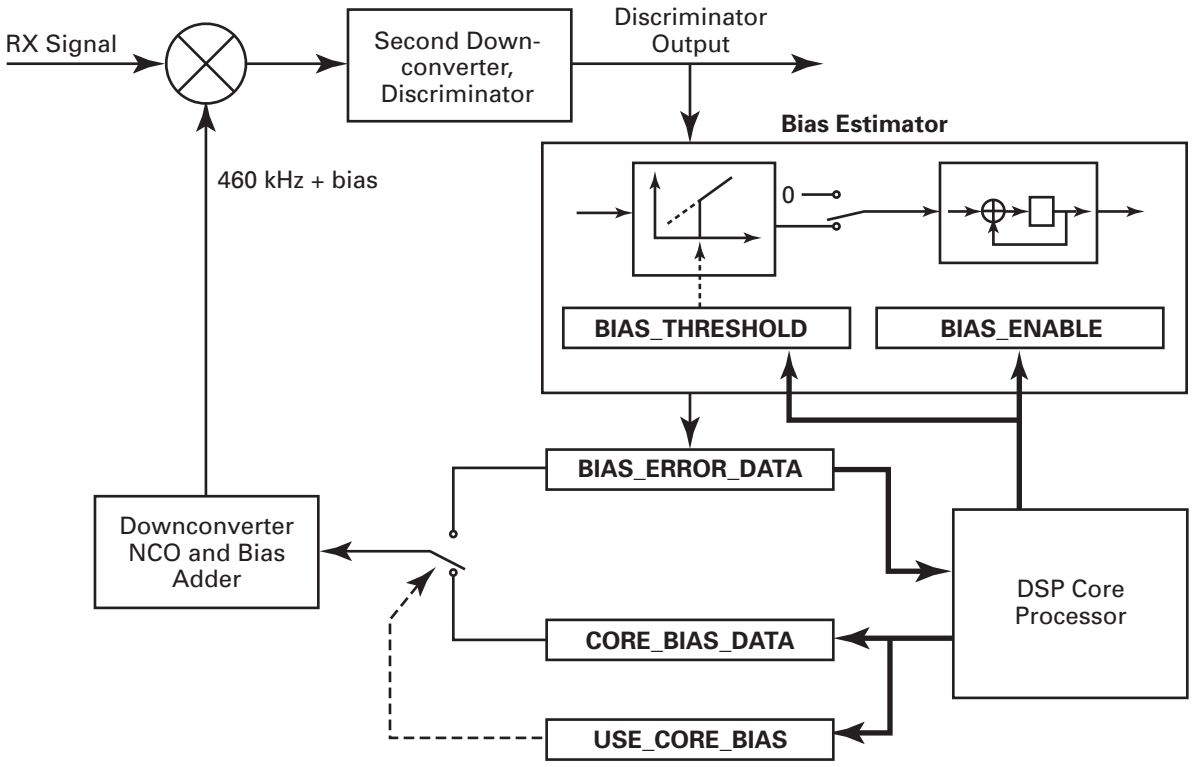
To detail further, the AFC loop features a bias estimator block, which determines the frequency offsets in the incoming add signal, which adds this bias to the 460-kHz frequency control word driving the NCO and various interface points to the DSP core processor. In particular, the DSP can read the bias estimate data and substitute its own calculated bias value to the NCO.

The bias estimator accumulates the discriminator output values (image of instantaneous frequency) that exceed a programmable threshold (BIAS_THRESHOLD). The processor can freeze the bias calculation any time by resetting the BIAS_ENABLE control bit.

The accumulated bias, available in BIAS_ERROR_DATA, can be used directly to correct the NCO frequency. Alternately, the estimated bias can be read by the DSP, further processed, and written to the CORE_BIAS_DATA field. The DSP controls which value is used by setting the USE_CORE_BIAS field. The selected value is added to the 460-kHz signal, which downconverts the receive IF signal.

In addition to correcting the difference in clock frequencies on the receiver using the AFC loop, a Z87L02-based system can also modify the frequency of the remote transmit IF signals. The software accesses this frequency via the MOD_FREQ fields.

FIGURE 10. AFC LOOP AND PROCESSOR CONTROL



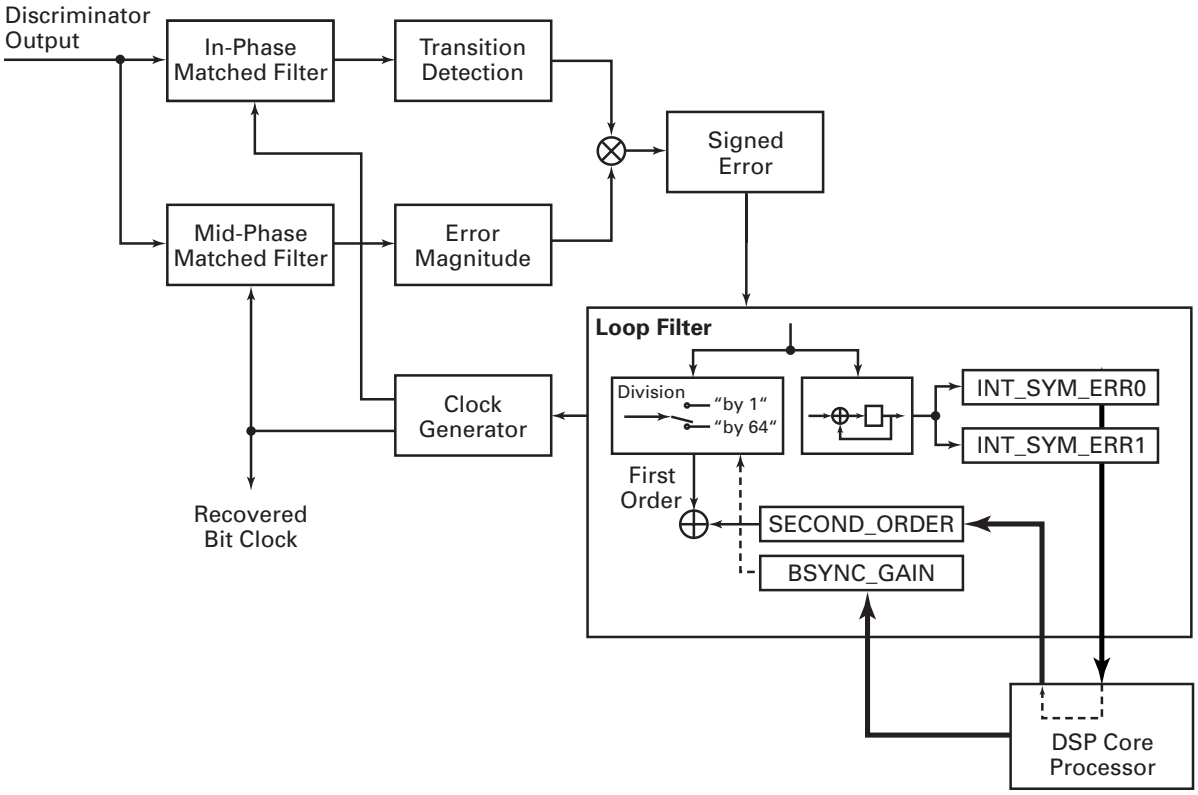
The central element of the demodulator is the limiter-discriminator. The limiter-discriminator detects the frequency variations (ideally ± 32.58 kHz) and converts them to 0 or 1 information bits. The data is first processed through low-pass filters to eliminate high-frequency spurious components introduced by the 1-bit ADC. The resulting signal is then differentiated and fed to a matched filter. In the matched filter, an integrate-and-dump operation is performed to extract the digital information from its background noise.

The symbol clock is provided by the bit synchronizer. The bit synchronizer circuit detects 0-to-1 and 1-to-0 transitions in the incoming data stream to synchronize a digital phase-lock loop (DPLL). The PLL output is a composite output of the recovered bit clock used to time the receiver on the base station, and both the receiver and transmitter on the handset.

The bit synchronizer circuit is an implementation of the Data Transition Tracking Loop (DTTL), best described in *Telecommunications Systems Engineering* by W.

Lindsey and M. Simon (Dover 1973; oh. 9, p. 442). The bit synchronizer operation is summarized in Figure 11.

FIGURE 11. BIT SYNCHRONIZER LOOP AND PROCESSOR CONTROL



The bit synchronizer loop filter is controlled by the primary DSP core processor. The DSP core can implement a first order loop by setting the SECOND_ORDER field to 0. Typically, BSYNC_GAIN is set to a *divide-by-1* operation to provide a wide closed loop bandwidth and thus a quick acquisition of the bit clock. When the bit clock is in phase with the input data, the loop bandwidth can be narrowed to maintain tracking of the receive clock with minimum impact from signal noise. To reduce the loop bandwidth, the BSYNC_GAIN can be set to a *divide-by-64*, the first order gain, while the integrated tracking error (available to the DSP in fields INT_SYM_ERR0 and INT_SYM_ERR1) can be used by the DSP software to adjust the SECOND_ORDER term.

The bit synchronizer relies on transitions in the received bit stream to operate. The bit inversion logic guarantees enough transitions for all transferred data.

At the handset, the bit synchronizer must track both the frequency and phase of the receive signal's data clock. At the base, only the phase must be tracked. The frequency is inherently correct. The base is the source of the system's data clock.

The data is packed in frames sent alternately from the base and handset every 4 ms (TDD). Therefore, additional synchronization means are necessary. This situation is realized in a frame synchronizer, based on detection of a unique word following the preamble.

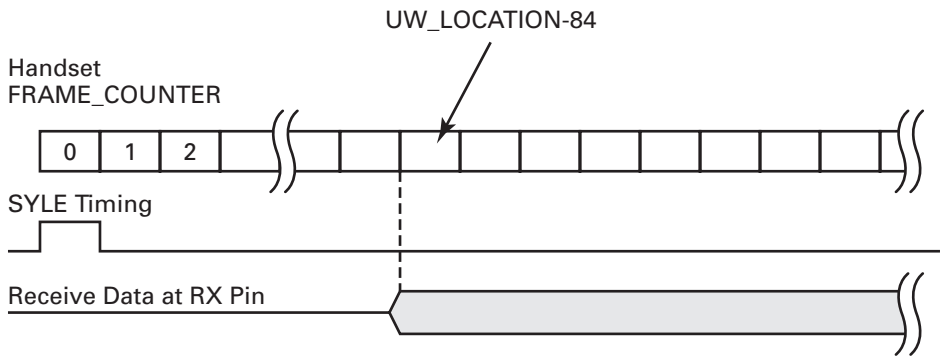
The frame synchronizer tracks the received frames and resets the receive frame counter. The synchronization is performed by recognizing certain data patterns present in the receive bit stream. A comparison is performed on-the-fly between the data pattern and the incoming bit stream. When the data match, the frame counter is reset.

Two possible 16-bit data patterns are preprogrammed in the frame synchronizer. One pattern is named Unique Word (UW), and is used in acquisition mode for first-time synchronization to an incoming signal. UW can also be used to track an acquired signal. The second pattern is named SYNC_D, and is used to track the received data frames while voice is being transferred. The transition from tracking the UW to tracking SYNC_D is controlled by the primary DSP processor through the SYNC_SEARCH_WORD field.

When the frame synchronizer matches the UW, the receive frame counter is reset to the value of UW_LOCATION. This value is programmable by the DSP1. On the handset, where the receive frame counter is used to derive all timings, UW_LOCATION actually defines the guard time between the frequency hop command and the beginning of data reception. This timing begins at FRAME_COUNTER = (UW_LOCATION–84), as illustrated in Figure 12.

On the base station, data reception starts when the receive frame counter equals UW_LOCATION–84; however, this condition has less significance. The hop pulse is synchronized with the transmit frame counter and there is no fixed relationship between transmit and receive frame counters. On the base station, the UW_LOCATION should be set to 301.

FIGURE 12. FRAME COUNTER AND UW_LOCATION ON HANDSET



Two search modes are programmable via the SYNC_SEARCH_MODE field: FULL SEARCH and WINDOW SEARCH. FULL SEARCH mode is used by the handset when first acquiring the signal from the base station. In FULL SEARCH, the hand-

set is in RECEIVE mode and continuously looks for a match with the UW. When a match is found and the time reference is established, the UW_LOCATION is set, the DSP processor on the handset detects the synchronization, switches to Time Division Duplex mode (TDD), and starts receiving and transmitting alternately. FULL SEARCH mode switches to WINDOW SEARCH mode by the DSP software.

WINDOW SEARCH mode only searches for a match in a certain time window centered around the expected match time. The window size is programmable by the DSP processor in the WINDOW_SIZE field. If the matching does not occur at the expected time, due to *bit slips*, the receive frame counter timing is adjusted.

NOTE: Although the bit synchronizer is meant to keep track of time and prevent bit slips when the phone is operating continuously in TDD mode, bit slips are still possible when the handset is in STANDBY mode, receiving only 1 time every second.

When the DSP1 switches operation to VOICE mode, the frame synchronization parameters are modified by the DSP software to WINDOW SEARCH for a SYNC_D. In this mode, the receiver searches for the SYNC_D pattern in windows of the incoming data stream. The window size is determined by the WINDOW_SIZE field.

The transition to VOICE mode proceeds in two steps through an intermediate mode. The mode is set by the DSP processor by programming the MULTIPLEX_–SWITCH field. The three modes are:

SMUX: INITIAL mode. The SMUX mode allows acquisition, AFC operation, UW synchronization, and signalling. ADPCM processor access and bit inversion are disabled.

STMUX: INTERMEDIATE mode. The STMUX mode allows SYNC_D frame synchronization and signalling. ADPCM processor access is disabled and bit inversion is enabled.

TMUX: VOICE mode. The TMUX mode allows voice transmission, SYNC_D frame synchronization and signalling. ADPCM processor access and bit inversion are enabled.

To detect synchronization, the software accesses to the SYNC_ACQ_IND status field. This field is set by the frame synchronizer hardware every time a match is detected within the allowable time window. The software must reset the IND bit by setting the SYNC_ACQ_CLEAR field.

In addition, the software can track the frame timing by reading the frame counter value, available in the FRAME_COUNTER field. On the base station, where two frame counters are in use, this field returns the value of the transmit frame counter.

Every time the frame counter wraps around to 0, a frame start indicator bit is set (FRAME_START_IND status field). The software must reset this IND bit by setting the FRAME_START_CLEAR field. If the FS_INT_ENABLE bit is set, frame starts also trigger interrupts to the DSP processor.

5.4.3 Receive Frame Counter

The receive frame counter is tasked with keeping track of time within the frame. It is initialized by the frame synchronizer logic on detection of the Unique Word. The UW is then clocked by the recovered bit clock from the bit synchronizer. On the base station, the receive frame counter is used as time base for the receiver. On the handset, it is used as time base for both the receiver and transmitter.

5.4.4 Receive Rate Buffer and Voice Interface

The voice signal is generated at the fixed rate of 32 Kbps by the secondary processor, and transmitted/received in bursts of 93.09 Kbps across the air. Data buffers in the transmitter and receiver are therefore necessary to absorb the rate differences over time. These buffers are called *rate buffers*. These buffers can store up to 144 data bits, and are organized as an array of 36 4-bit nibbles.

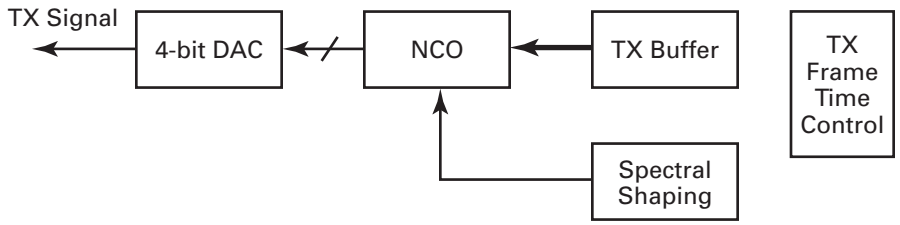
The receive rate buffer stores the received data from the demodulator. Incoming bits are arranged in 4-bit nibbles and transferred to successive locations in the rate buffer. When the end location is reached, transfers resume from the beginning (in effect, a circular buffer). The system design guarantees that no buffer overrun can occur.

The receive rate buffer can be read by both the primary and secondary DSP cores. On the DSP1, the buffer can be read as a random-access memory. The processor writes the nibble address in an address register and reads the 4-bit data from a data register. On the secondary processor side, the interface logic handles the addressing to automatically present the successive voice nibbles to the core in the order received.

5.4.5 Transmitter Block

Figure 13 presents the block diagram of the transmitter section of the Z87L02 transceiver.

FIGURE 13. TRANSMITTER BLOCK DIAGRAM



5.4.6 Transmit Rate Buffer and Voice Interface

The transmit rate buffer stores the data to be modulated. The data is sourced both from the primary (control bytes) and secondary (ADPCM voice) core processors. The secondary processor sees the transmit rate buffer as a unique pipe to write to,

while the DSP1 accesses the rate buffer as random access memory. The transmitter sees the rate buffer as a circular buffer.

5.4.7 Transmit Frame Timing Counter

On the handset, transmission does not start until the receiver has synchronized itself to the signal received from the base station. The transmission timing is based on the recovered clock. No additional counter is necessary.

On the base station, transmission timing is based on a local clock, while the receiver's timing is based on the clock recovered from the incoming signal. Two counters, respectively clocked by local and recovered clocks, are necessary to track the transmit and receive signals.

NOTE: The receive clock on the base station tracks the handset's transmit clock, which is also the handset's receive clock that tracks the transmit clock of the base station. In effect, receive and transmit clocks of the base station exhibit the exact same frequency—only their phases differ.

5.4.8 Modulator

The modulator features a numerically-controlled oscillator (NCO) which generates an FSK signal at the carrier frequency of 2.508 MHz. The carrier frequency is shifted +32.58 kHz for a `1` data bit or –32.58 kHz for a `0` data bit. To facilitate compliance with FCC regulations, the transitions from `1` to `0`, or vice-versa, are smoothed to decrease the amplitude of the side lobes of the transmit signal. In practice, the jump from one frequency to the next is performed in several smaller steps.

The carrier frequency is adjustable by the DSP core processor to provide additional frequency adjustment between base and handset. This adjustment is required in case of a frequency offset too large for sustained reliable correction by the AFC.

The modulator also includes bit inversion logic as discussed at the beginning of this Receiver Block section.

5.4.9 Transmit 4-Bit DAC

The transmit DAC clocks one new NCO value from the transceiver every (1 ÷ 8.192)-MHz period. Only the 10.7-MHz alias frequency component of the transmit signal (2.508 + 8.192-MHz image) is filtered, amplified, and upconversion to the 900-MHz ISM band by the companion RF module.

5.5 EVENT TRIGGER BLOCK

The event trigger block is responsible for scheduling the different events happening at the bit and frame levels. The event trigger block receives input from the frame counters in addition to the register interface of the primary DSP core processor.

The event trigger schedules the following transceiver and RF section events:

- Start of the 4 ms frame: a synthesizer load enable pulse is issued on the SYNLE pin
- Power-up of the modulator section and transmission of the frame on the handset and base station
- Use of the bit inversion as a function of mode
- Power-up of the demodulator section and reception of the frame on the handset and base station
- Control of RFTX and RFRX output pins, to be used as TDD control signals switching the antenna, transmitter, and receiver chains in the RF section
- Control of the RFEON pin, to be used as a general on/off switch on the RF section
- Control of the wake/sleep operation
- Control of the interface to the secondary processor and voice codec

Several control fields are available in the transceiver register set to define the timing and polarity of the receiver, transmitter, and RF section control signals.

The SYNLE signal, a *load enable* pulse that directs the external RF synthesizer to generate the next RF hop frequency, is controlled by two fields. The HOP_ENABLE field is a global enable signal for the SYNLE signals. The SYNLE_POLARITY field defines the polarity of the SYNLE pin. The leading edge of the SYNLE pulse triggers channel hopping.

In addition to the SYNLE signal, the synthesizer interface features data and clock signals for serial programming of the data values defining the RF channel. To allow interfacing of arbitrary synthesizers, two general-purpose I/O pins from the DSP1 auxiliary ports are controlled in software to realize any particular interface timing.

Another field, RFEON_POLARITY, controls the polarity of the RFEON pin. This pin is used to power the RF section on and off. The RFEON pin is asserted during wake periods, and deasserted in SLEEP mode. SLEEP mode is used by the handset to save battery life when no phone call is in process.

The transmitter control includes a global enable signal for all transmit functions called TX_ ENABLE. The transmission start is controlled by the MOD_PWR_ON field. On the base station, the value programmed in MOD_PWR_ON is referenced to the transmit frame counter.

Two additional fields, RFTX_PWR_ON and RFTX_PWR_OFF, define the duty cycle of the TXON output pin. On the base station, these fields are referenced to the transmit frame counter. The RFTX_POLARITY bit defines the polarity of the TXON pin. This pin can be used to control the transmit section and power amplifier of the external RF section.

On the receive side, two fields define the internal timing of the receiver. The start of reception is controlled by the DEMOD_PWR_ON field. Stop of reception (and receiver power down) is controlled by the DEMOD_PWR_OFF field. On the base

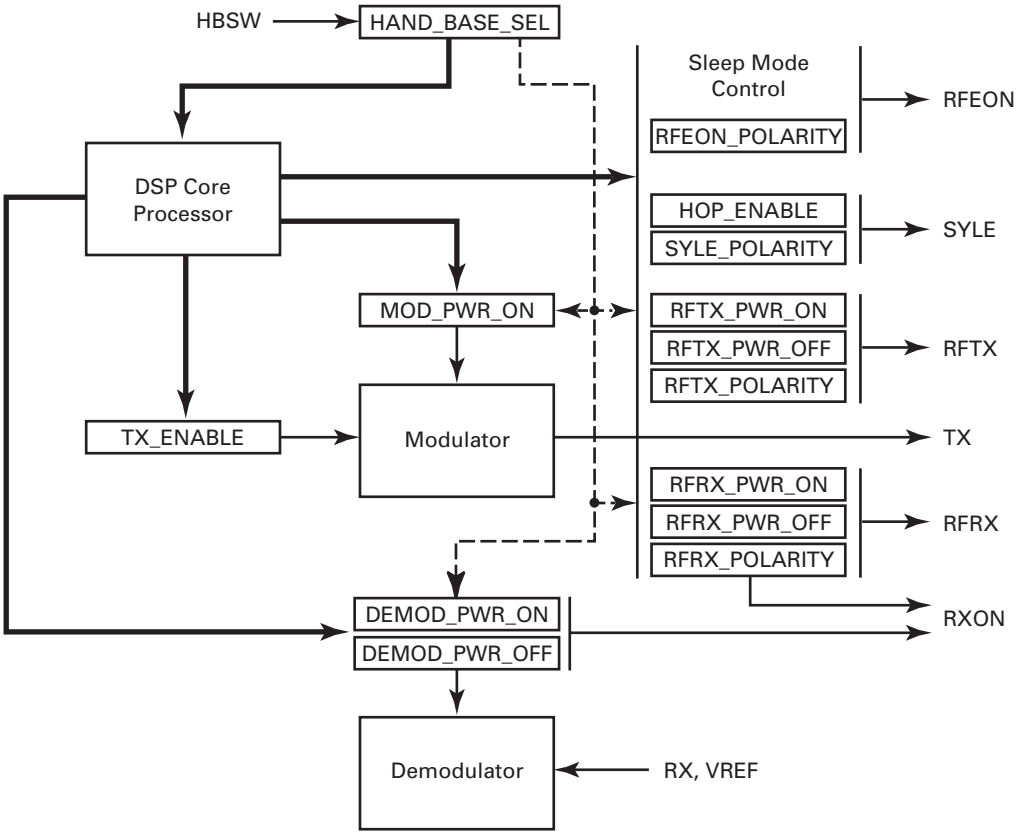
station, these fields are referenced to the receive frame counter. The RXON output pin follows the timing defined by the DEMOD_PWR_ON and DEMOD_PWR_OFF fields.

Two additional fields, RFRX_PWR_ON and RFRX_PWR_OFF, define the duty cycle of the RXON output pin. On the base station, these fields are referenced to the transmit frame counter. The RFRX_POLARITY bit defines the polarity of RXON. The RFRX pin can be used to control the receive section of the external RF module.

The various timing control registers reviewed in this paragraph should be programmed differently for the handset and base station. If the same ROM code is used on the base station and handset, the software can determine which station it runs on by reading the HAND_ BASE_SEL bit, which reflects the state of the HBSW pin.

Figure 14 summarizes the above control fields.

FIGURE 14. EVENT TRIGGER TRANSCEIVER AND RF SECTION CONTROL



To conserve the handset battery charge, the Z87L02 can be operated in a low-current-consuming SLEEP mode when the phone is not in use. In SLEEP mode, both primary and secondary processors are disabled, and only the 16.384-MHz oscillator and the sleep counters within the transceiver event trigger block are opera-

tional. SLEEP mode is entered by software command. SLEEP mode must first be enabled by setting the SLEEP_WAKE field. Then a GO_TO_SLEEP command puts the processor to sleep by temporarily stopping its clock. The sleep period can be set to last between 4 milliseconds and 1.02 seconds by programming the SLEEP_PERIOD field. In SLEEP mode, the RFEON pin is deasserted.

The processor emerges from SLEEP mode in one of two ways. Either the sleep counter counts down to 0, or one of the dedicated wake-up pins from DSP1 (port P0) is asserted prior to the normal expiration of the counter. Four port pins (P000, P001, P002 or P003) can be individually enabled to provide the wake-up function by setting the appropriate bits in P0_ WAKE_ENABLE. Typically, these port pins are connected to the telephone keypad.

When the handset's processor core wakes up, the software must establish the actual elapsed sleep time to restore synchronization with the base station's hopping sequence. For that purpose, the current value of the sleep counter is available to the processor in the SLEEP_REMAINING field, where a value of 0 indicates normal expiration of the sleep counter.

To guarantee a good operation of the wake-up pins, the wake-up signals are hardware denounced in the event trigger block. Furthermore, these signals are internally synchronized to the bit clock. As a result, the processor is assured enough time (one bit time = 10.74 µs) to read a stable value of the remaining sleep time and synchronize correctly to the base station's hopping sequence.

The interface to the secondary processor (ADPCM voice processor) features clock control, command/status interface, and a data interface. The data interface provides the ADPCM processor access to the rate buffers.

The DSP1 generates the secondary processor clock at a frequency of 16.384 MHz or 8.192 MHz, as set in VP_CLOCK. In addition, the clock can be stopped and restarted with the VP_STOP_CLOCK field to reduce power consumption.

NOTE: A software handshake between processors is necessary before stopping and after restarting the clock.

In addition to providing the voice processor main clock, the DSP1 generates a CODCLK signal which is used to synchronize data transfers between the external voice band codec and both processors.

On the base station, CODCLK is obtained by dividing the 16.384-MHz input clock. The handset CODCLK is synchronized to the base station's CODCLK signal through the receive bit sync logic. As a result, voice data sourcing and synchronizing occurs at identical rates on the handset and base, eliminating buffer overrun and underrun situations.

The DSP1 sends commands to the voice processor through the VP_COMMAND WRITE-ONLY field. This field reads the DSP2 status in the VP_STATUS READ-ONLY field. Both fields are located at the same address in the DSP1 register interface. A communication protocol must be established in software to ensure correct reception of all commands. Dedicated hardware ensures data integrity when both processors simultaneously access the same register

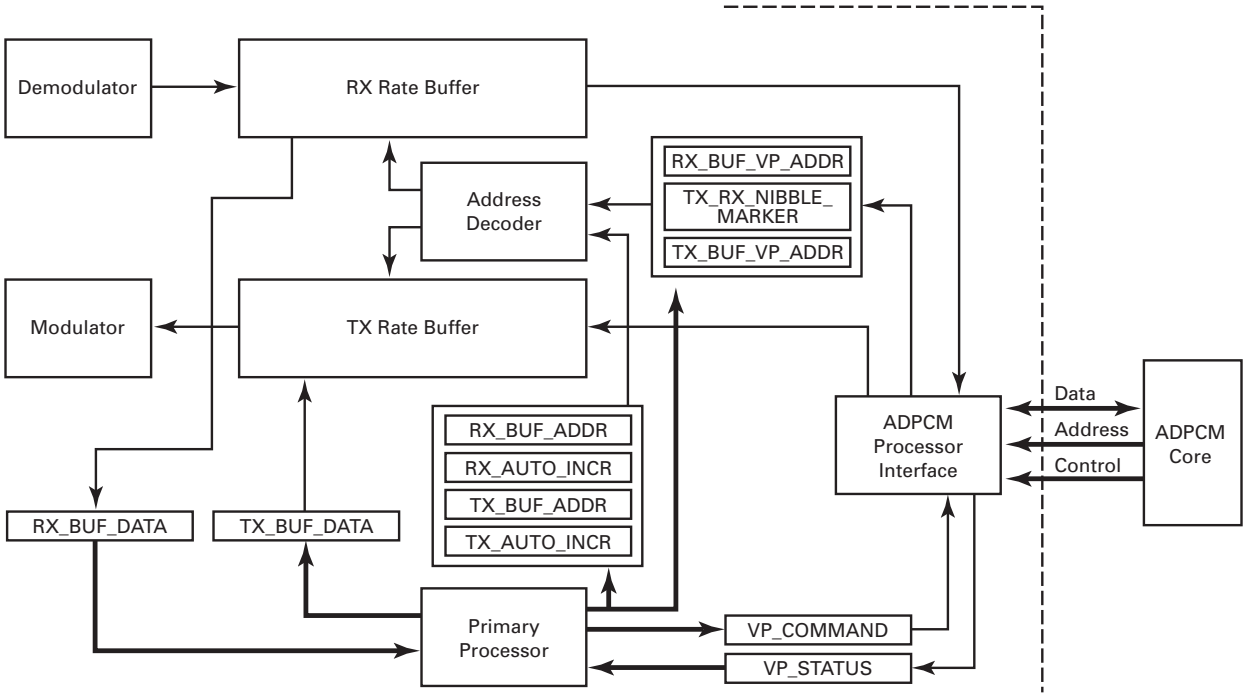
The digitized voice data is communicated between processors through the rate buffers and ADPCM processor data interface. The transmit and receive rate buffers each contain 36 4-bit nibbles (Figure 15).

To write to the transmit rate buffer, the DSP1 processor must first set the nibble address in the TX_BUF_ADDR register field, followed by a WRITE to the nibble data through TX_BUF_DATA. If the TX_AUTO_INCREMENT bit is set, the address is automatically incremented (modulo 51 = the number of nibbles in rate buffer + 15 additional data words accessible through TX_BUF_DATA) after each data WRITE. As a result, the DSP core writes successive nibbles without resetting the address each time.

The operation of the receive rate buffer is identical. The primary core processor must set the nibble address in RX_BUF_ADDR, then read the nibble from RX_BUF_DATA. If the RX_AUTO_INCREMENT bit is set, the READ address is automatically incremented (modulo 36 = number of nibbles in the rate buffer) after each data READ. As a result, the DSP core reads successive nibbles without resetting the address each time.

Through its register interface, the DSP1 also controls which rate buffer addresses the ADPCM processor can access. The nibble addresses are contained in the TX_BUF_ VP_ADDR and RX_BUF_VP_ADDR register fields. After the voice processor writes or reads a nibble to or from the transmit or receive rate buffer, the corresponding VP_ADDR is automatically incremented (modulo 36) to the next accessible address. The locations of accessible addresses are individually controlled by the secondary processor in the three TX_RX_NIBBLE_MARKER register fields. A marker bit equal to 1 enables the DSP2 to access the corresponding address; a bit equal to 0 causes the voice processor's READ or WRITE access to skip to the next nibble that returns a marker bit equal to 1.

FIGURE 15. ADPCM PROCESSOR INTERFACE AND RATE BUFFERS



5.5.1 Transmit Power Level Control 4-Bit DAC

To save battery life, the ZPhone handset transmits only the RF power required to reach the remote base station receiver with a sufficient Signal-to-Noise Ratio (SNR) margin. The on-board transmit power 4-bit DAC provides up to 16 different voltage levels to the RF section power amplifier. This DAC is directly controlled by the DSP1 software through an output register.

5.5.2 Analog Switch and 8-Bit ADC

An analog Received Signal Strength Indicator (RSSI) voltage is generated by the most recent stage of the RF downconverter. The DSP1 uses the RSSI measurements as criteria in the computation of Transmit Power Level Control voltages and adaptive frequency-hopping events. Similarly, handset battery voltage measurements are required to detect under voltage conditions and to control fast battery charging algorithms. A three-way analog multiplexer switches between 3 dedicated Z87L02 pins under DSP1 control, routing one selected signal to an 8-bit ADC for sampling 1 time every 4-ms frame.

5.6 DSP1

5.6.1 DSP Core

The DSP1 features the M89S00 static DSP core from ZiLOG's microprocessor core library. The core can be operated at full speed (16.384 MHz) or half speed

(8.192 MHz). The DSP core runs the application software which performs the following functions:

- Register initialization
- Implementation of high-level phone features and control of the phone user interface (keypad, lamps, displays, etc.)
- Control of the secondary ADPCM processor
- Control of the telephone line interface
- Ring detection by DSP processing
- Communication protocol between the handset and the base station, supporting voice and signaling channels
- Control of the RF synthesizer and adaptive frequency hopping algorithm
- Control of the RF power level adjustment algorithm
- Control of the demodulator (bit synchronizer loop filter and AFC bias estimate filtering)
- Control of the modulator (carrier frequency) and adaptive frequency alignment
- Signalling between the base and the handset, to support the above features

The DSP core is characterized by an efficient hardware architecture that allows fast arithmetic operations such as multiplication, addition, subtraction, and multiplication/accumulation of two 16-bit operands. Most instructions are executed in 1 clock cycle.

The DSP core features an internal RAM memory of 512 16-bit words, divided into two banks. Six register pointers provide circular buffering capabilities and dual-operand fetching. Three vectored interrupts are complemented by a six-level stack. In the Z87L02, one of these interrupts is allocated to the secondary ADPCM processor. A second interrupt can be triggered under software control to mark the 4-ms frame start. The third interrupt is available for user customization.

DSP1 ports feature two 16-bit general-purpose I/O ports that are directly accessible by the DSP core. These input and output pins are typically used for the implementation of the phone's user interface (keypad, LEDs, optional display, etc.), control of the base station phone line interface (on/off hook, ring detect), control of battery charging, detection of low battery conditions, and implementation of additional features for customizing the phone.

The DSP1 interfaces to the secondary processor through two different paths, a command/status interface and a data interface. The command/status interface features two dual-port registers, accessible by both the primary and DSP2 processors' register interfaces. Arbitration logic resolves access contentions.

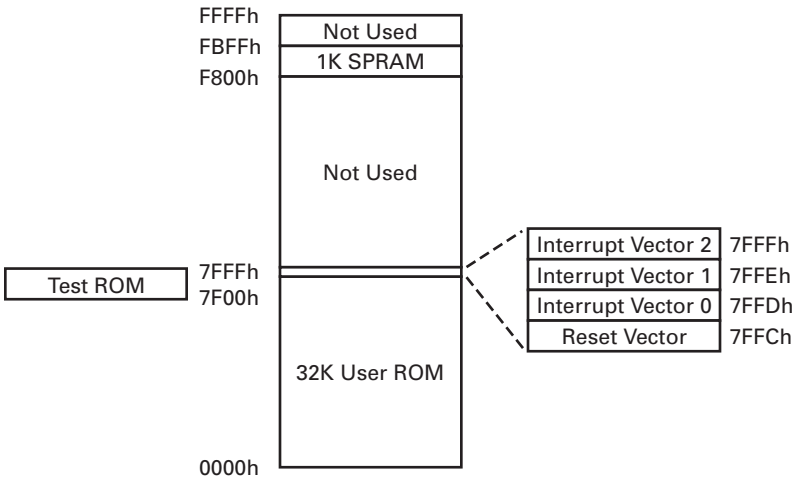
The data interface provides the secondary processor with direct access to the transceiver's receive and transmit rate buffers. Dedicated voice processor interface logic handles the addressing within the rate buffers.

The physical interface between the processors consists of an 8-bit data bus VXD[7..0], a 3-bit address VXADR[2..0] bus and the VXSTR (STROBE), VXRDY (WAIT), and VXRW (READ/WRITE) control signals. This bus is controlled by the secondary processor. In the system, the voice processor is enslaved to the DSP1. However, at the physical level, the DSP1 acts as a peripheral of the secondary processor.

5.7 DSP1 ROM AND RAM

The Z87L02 DSP1 addresses 32 K+256 words of internal factory-masked ROM. The Z87L03 DSP1 addresses either the same 32 K + 256-word block or 64 K Words of external program memory, as selected by appropriate assertion of the TEST[1..0] and trice input pins. Test ROM and Scratch Pad (SP) RAM are also addressable in either chip. A memory map for the internal ROM access is presented in Figure 16.

FIGURE 16. Z87L02/Z87L03 DSP1 INTERNAL PROGRAM MEMORY MAP



The internal ROM design consists of one block of 32 K Words of 16 bits each, dedicated to user program memory. An additional block of 256 Words is allocated to test program code. In addition, the 1 K Word of Scratch Pad RAM in the Z87L02/Z87L03 is accessible to the DSP1 through the above ROM address space.

The 32 K block of user memory is mapped into locations 0000h through 7FFFh. Four words are dedicated to the three interrupt vectors and to the starting memory location upon reset.

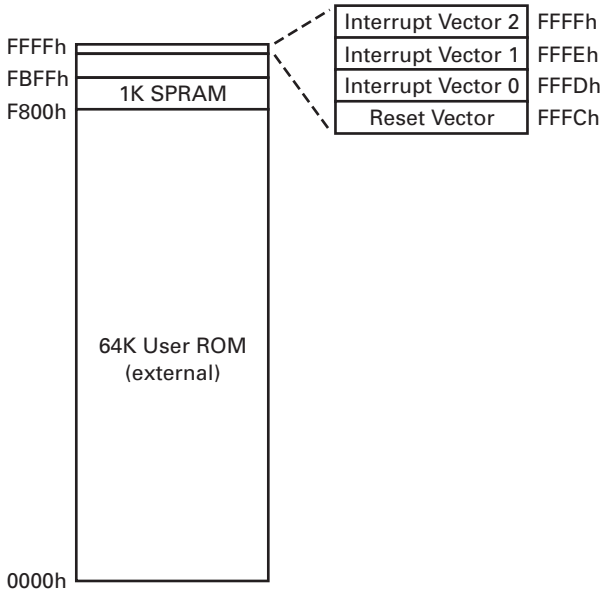
A separate test ROM is also mappable into locations 7F00h through 7FFFh. Used only during execution of wafer scale testing, this ROM is accessed by properly asserting the TEST[1..0] pins.

A block of 1 K Word of RAM is available for use as either program and/or Scratch Pad memory. This RAM is mapped into the addressable DSP1 locations

between F800h and FBFFh. It is accessed for program execution or data read through normal program memory access. The software can write into this RAM through the MEM_ADDRESS_MEM_CONTROL and MEM_DATA DSP1 registers. Upon Power-On Reset, this RAM is disabled and removed from the Program Memory Map.

In addition to the internal ROM described above, the Z87L03 may access up to 64 K words of external ROM. The memory map for the external ROM access is presented in Figure 17.

FIGURE 17. Z87L03 DSP1 EXTERNAL PROGRAM MEMORY MAP



The 64 K Words of external memory are mapped into addresses 0000h through FFFFh. The 1 K Words of Z87L03 Scratch Pad RAM are also accessible to the DSP1 through the above address space.

Four words dedicated to the three interrupt vectors and to the starting memory location upon reset are mapped into addresses FFFCh through FFFFh. The 1 K Word block of RAM is mappable into the locations between F800h and FBFFh.

The DSP1 also addresses two 256 word blocks of RAM for data memory. The RAM is mapped into a separate data address space, from addresses 0000h to 01FFh.

5.8 DSP1 PERIPHERALS

5.8.1 Oscillator

The Z87L02/Z87L03 onboard oscillator features a variable gain parallel resonant amplifier for connection either to a high-stability crystal across the XTALIN and XTALO pins, or to an external 16.384-MHz clock source driving the XTALIN pin. The resulting signal is then routed to the transceiver and DSP1 as the master system clock. In addition, the clock is also analog buffered to generate the RFCLK signal for the external RF section.

The variable gain amplifier provides for very low oscillator current consumption. High-gain/high-current amplification is required on device power up to start the oscillation, but thereafter the gain (and current) is reduced under software control to the minimum level yielding a robust clock. In addition, the analog buffer is internally biased on and off by the RFEON signal, so that RFCLK is not active during handset sleep periods. This condition helps to minimize current consumption.

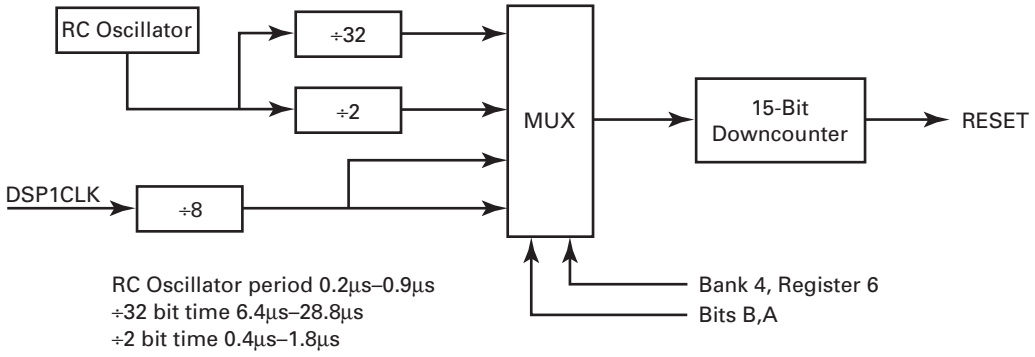
5.8.2 Serial Interface

The serial interface hardware block exhibits digital logic. This logic implements a serial communications protocol compatible with the Inter-IC (I^2C) Bus specification. The I^2C bus is a serial two-line interface consisting of a data signal (SERDAT) and a clock signal (SERCLK) that provide addressable bidirectional 8-bit oriented data transfers at up to 450 kbits/sec between compatible devices. Configured always as a master, the Z87L02/L03/L09 provides the clock and initiates transmissions to serial EEPROMs, display devices, and test equipment.

5.8.3 Watch-Dog Timer

The Watch-Dog Timer (WDT) is a digital logic block that provides a device reset command in the absence of a periodic DSP1-driven event. This timeout is used to recover from hang-ups or other malfunctions generated by environmental or user initiated events. The WDT may be disabled by software command, and the timeout period is also software programmable. The WDT is also disabled upon a system reset, and is either provided by an external source or is self-generated.

FIGURE 18. WDT BLOCK DIAGRAM



5.9 DSP2 CORE

5.9.1 DSP Processor

The DSP2 features the M89S00 static DSP core from ZiLOG's microprocessor core library. The core is operated at full speed (16.384 MHz) or half speed (8.192 MHz) under control by the DSP1 software. The DSP2 runs the application software which performs the following functions:

- ADPCM to PCM transcoding
- CRC code generation and comparison for voice frame error detection
- Voice muting upon programmable frame error patterns
- DTMF signal generation
- Volume control for voice, signaling, and DTMF tones

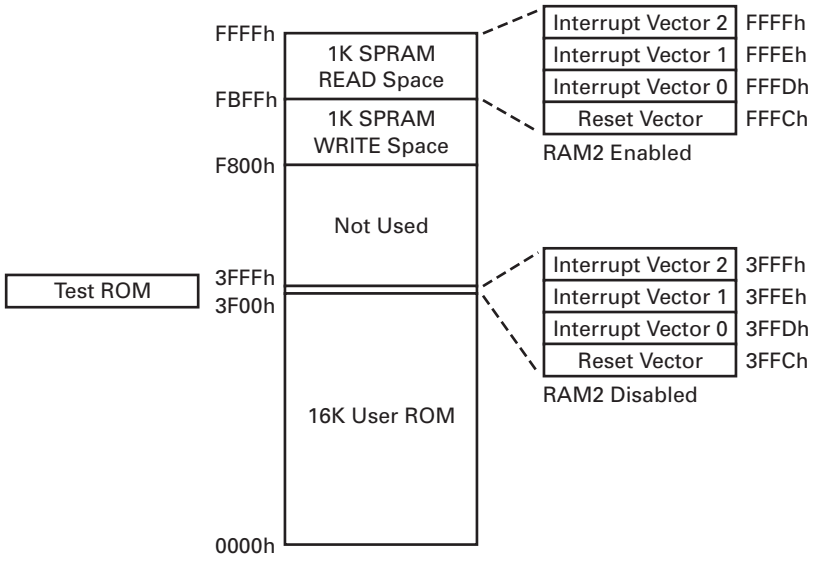
The DSP core is characterized by an efficient hardware architecture that allows fast arithmetic operations such as multiplication, addition, subtraction, and multiply-accumulate of two 16-bit operands. Most instructions are executed in one clock cycle.

The DSP core is typically operated at the internal speed of 16.384 MHz. It features an internal RAM memory of 512 16-bit words divided into two banks. Six register pointers provide circular buffering capabilities and dual operand fetching. Three vectored interrupts are complemented by a six-level stack. One interrupt is allocated to the codec interface. Another interrupt is dedicated to the internal 13-bit timer (if enabled). A third interrupt is available for user customization.

5.9.2 DSP2 ROM and RAM

The Z87L02/L03/L09 DSP2 addresses 16k+256 words of internal factory masked ROM. Test ROM and Scratch Pad RAM are also addressable as program memory. External program memory access is not available. A memory map for the internal Program Memory is presented in Figure 19.

FIGURE 19. Z87L02/L03/L09 DSP2 INTERNAL PROGRAM MEMORY MAP



The internal ROM design consists of one block of 16 K Words of 16 bits dedicated to user program memory. An additional block of 256 Words is allocated for test program code. In addition, the 1 K Word of Scratch Pad RAM in the Z87L02/ Z87L03 are accessible to the secondary processor through the above ROM address space.

The 16k of user memory is mapped into locations 0000h through 3FFFh. Four words dedicated to the three interrupt vectors and to the starting memory location upon reset are mapped into addresses 3FFCh through 3FFFh. The entire address space from 0000h through 3FFBh is available for user program code.

A separate test ROM is also mappable into locations 3EFFh through 3FFFh. Used only during execution of wafer scale testing, this ROM is accessed by properly asserting the TEST[1..0] pins.

A block of 1 K Word of RAM (RAM2) is available for use as program memory and/or Scratch Pad RAM. This RAM is mapped into the addressable DSP1 locations between FC00h and FFFFh. Upon Power-On Reset, this memory is disabled and removed from the memory maps of both DSP1 and DSP2.

RAM2 is mapped into addresses FC00h to FFFFh of the DSP2 program address space (for execution or data read). RAM2 is also mapped into addresses F800h to FBFFh for purposes of data write only. In this case, the software executes a READ operation. The data contained from one of these addresses in the SPRAM2 WRITE data register of DSP2 is written to the addressed location.

DSP2 also addresses two 256 word blocks of RAM for data memory. This RAM is mapped into a separate address space, from addresses 0000h though 01FFh.

When RAM2 is enabled, the interrupt vectors are mapped within the RAM2 space at FFFFh–FFFCh.

5.10 CODEC INTERFACE

The secondary DSP processor controls and transfers data through the codec interface, an 8- or 16-bit full-duplex serial port capable of up to 10-Mbps transmission. The codec interface provides direct-connect capabilities to an 8-bit PCM, an 8-bit PCM with hardware µ-law conversion, a 16-bit linear codec, and certain stereo audio codecs. The codec interface is implemented with a set of hardware registers and a µ-law compression logic block tied to the DSP bus. Expansion from µ law is performed in software.

The codec interface provides two independent frame synchronization signals, FS0 and FS1, allowing for two separate communications channels. CODCLK, the clock signal to drive the external codec(s), is derived from the 16.384-MHz secondary processor clock by dividing with a 4-bit prescaler. The TXD and RXD lines provide for simultaneous 8-, 16-, or 64-bit data transfers to and from the external codec. Completion of a data transfer generates an interrupt to the secondary processor.

6. DSP1 REGISTERS

Tables 7 and 8 summarize the register set associated with the DSP1 registers in Tables 10–56 and the Secondary Processor Register Summary in Table 57.

TABLE 7. DSP1 REGISTER SET, BANKS 0–3*

Bank	Address	Register	READ Description	WRITE Description	Table #
0	EXT0	MF_MUX_DATA_IN		Matched Filter input test data	10
	EXT1	MA_MUX_DATA_OUTI	Moving Average Filter output test data		11
	EXT2	MA_MUX_DATA_OUTQ	Moving Average Filter output test data		12
	EXT3	MF_MUX_DATA_OUTI	Matched Filter output test data		13
	EXT4	MF_MUX_DATA_OUTQ	Matched Filter output test data		14
	EXT5	BANK_CONTROL	High/Low Bank Select monitoring	High/Low Bank Select	15
	EXT6	INT_SYM_ERR0	Bit Sync monitoring		16
	EXT7	TX_PWR_CTRL		TXSW, RXSW pin control	17
1	EXT0	RAT_BUF_ADDR		Rate Buffer address	18
	EXT1	RAT_BUF_DATA	RX Rate Buffer data	TX Rate Buffer data, control data	19
	EXT2	BIT_SYNC	Bit Sync monitoring	Bit Sync control	20
	EXT3	RESERVED			21
	EXT4	TEST_CONFIG1	Bit Sync control/monitoring		22
	EXT5	TEST_CONFIG2		Transceiver test mode control	23
	EXT6	CONTROL	INT, WAKEUP pin control, 4-bit DAC data (PWLV)		24
	EXT7	LPF_MUX_DATA_IN		Low Pass Filter input test data	25
2	EXT0	VP_INOUT	Voice Processor Status	Voice Processor Command	26
	EXT1	RX_CONTROL	SNR estimate	UW location	27
	EXT2	BIAS_ERROR	FCW value		28
	EXT3	RSSI	8-bit ADC data (RSSI)		29
	EXT4	CORE_BIAS		Core Bias data	30
	EXT5	MOD_PWR_CTRL		MOD_PWR control	31
	EXT6	RX_PWR_CTRL		RXSW, RFEON pin control	32
	EXT7	AMP_PWR_CTRL		PAON pin control	33

NOTE: *All bits are set to 0 on Power-On Reset, unless mentioned otherwise.

TABLE 7. DSP1 REGISTER SET, BANKS 0–3* (CONTINUED)

Bank	Address	Register	READ Description	WRITE Description	Table #
3	EXT0	CONFIG1		Clock Dividers, Use Core Bias, SYNLE polarity, UW window size, Bias Threshold	34
	EXT1	CONFIG2	Remaining sleep time	ANT0/1 control, sleep period	35
	EXT2	SSPSTATE	Stop VP clock, BSync gain, Bias Enable, TX Enable, Sync Search control, Hop Enable, Frame Start control, Multiplex control, and SLEEP mode control		36
	EXT3	SSPSTATUS	Event Counter, Handset/Base, Sync Search control, and Frame Start control		37
	EXT4	GPIO0DIR	General-Purpose I/O; port 0 direction control		38
	EXT5	GPIO0DATA	General-Purpose I/O; port 0 data		39
	EXT6	GPIO1DIR	General-Purpose I/O; port 1 direction control		40
	EXT7	GPIO1DATA	General-Purpose I/O; port 1 data		41

NOTE: *All bits are set to 0 on Power-On Reset, unless mentioned otherwise.

TABLE 8. DSP1 REGISTER SET, BANKS 4–7*

Bank	Address	Register	READ Description	WRITE Description	Table #
4	EXT0	MEM_CONTROL	Flash/RAM Control monitoring	Flash/RAM control	42
	EXT1	MEM_ADDRESS	Flash/RAM address monitoring	Flash/RAM address	43
	EXT2	MEM_DATA	Flash/RAM Data	Flash/RAM data	44
	EXT3	Unassigned			NA
	EXT4	WDT_CTL_DATA	Watch-Dog Timer Value (remaining)	Watch-Dog Timer Value	46
	EXT5	BANK_CONTROL	High/Low Bank Select monitoring	High/Low Bank Select	47
	EXT6	OSC/TEST_CONTROL	Osc gain/Test mode monitoring	Osc gain/TEST mode control	48
	EXT7	RF/ADC/GP_CONTROL	RF Interface/ADC_SEL/ ANT/GP	RF Interface/ ADC_SEL/ANT/GP	49
5	EXT0	I^2C_CONTROL	I^2C control monitoring	I^2C Control	50
	EXT1	I^2C_CMD	I^2C command monitoring	I^2C Command	51
	EXT2	I^2C_DATA	I^2C READ Data	I^2C WRITE Data	52
	EXT3	RESERVED			NA
	EXT4	RESERVED			NA
	EXT5	BANK_CONTROL	High/Low Bank Select monitoring	High/Low Bank Select	55
	EXT6	RESERVED			NA
	EXT7	RESERVED			NA
6	EXT0	Unassigned			NA
	EXT1	Unassigned			NA
	EXT2	Unassigned			NA
	EXT3	Unassigned			NA
	EXT4	Unassigned			NA
	EXT5	BANK_CONTROL	High/Low Bank Select monitoring	High/Low Bank Select monitoring	63
	EXT6	Unassigned			NA
	EXT7	Unassigned			NA

NOTE: *All bits are set to 0 on Power-On Reset, unless mentioned otherwise.

TABLE 8. DSP1 REGISTER SET, BANKS 4–7* (CONTINUED)

Bank	Address	Register	READ Description	WRITE Description	Table #
7	EXT0	CONFIG1		Clock Dividers, Use Core Bias, SYNLE polarity, UW window size, Bias Threshold	34
	EXT1	CONFIG2	Remaining Sleep time	ANT0/1 control, sleep period	35
	EXT2	SSPSTATE	Stop VP clock, BSync gain, Bias Enable, TX Enable, Sync Search control, Hop Enable, Frame Start control, Multiplex control, and SLEEP mode control		36
	EXT3	SSPSTATUS	Event Counter, Handset/Base, Sync Search control, and Frame Start control		37
	EXT4	GPIO0DIR	General-Purpose I/O port 0 direction control		38
	EXT5	GPIO0DATA	General-Purpose I/O port 0 data		39
	EXT6	GPIO1DIR	General-Purpose I/O port 1 direction control		40
	EXT7	GPIO1DATA	General-Purpose I/O port 1 data		41

NOTE: *All bits are set to 0 on Power-On Reset, unless mentioned otherwise.

Table 9 presents specific functions for each register bank selection.

TABLE 9. BANK SWITCHING

Bank	Hi/Low Bank	Status Register	Bank Function
0	0	xxxx xxxx x00x xxxx b	Test point access, TDD Switching control
1	0	xxxx xxxx x01x xxxx b	Rate Buffer access, Test configuration, miscellaneous
2	0	xxxx xxxx x10x xxxx b	Voice processor interface, RF interface, etc.
3	0	xxxx xxxx x11x xxxx b	Configuration, Status, General-Purpose Port data and direction
4	1	xxxx xxxx x00x xxxx b	Flash/WDT Control
5	1	xxxx xxxx x01x xxxx b	I^2C
6	1	xxxx xxxx x10x xxxx b	Unassigned
7	1	xxxx xxxx x11x xxxx b	Unassigned

6.1 BANK 0 REGISTERS

TABLE 10. BANK 0, REGISTER 0

MF_MUX_DATA_IN		EXT0		
Field	**Bank 0 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fed----------	R W		Returns 0 No effect
MF_MUX_DATA_IN	---cba9876543210			Access to test data for the Matched Filters
		R W	XXXXh	Returns 0 Writes test data

TABLE 11. BANK 0, REGISTER 1

MA_MUX_DATA_OUTI		EXT1		
Field	**Bank 0 Bit Position**	**R/W**	**Data**	**Description**
MA_MUX_DATA_OUTI	fedcba9876543210			Access to test data output from the Moving Average filters, channel I
		R W	XXXXh	Reads test data No effect

TABLE 12. BANK 0, REGISTER 2

MA_MUX_DATA_OUTQ		EXT2		
Field	**Bank 0 Bit Position**	**R/W**	**Data**	**Description**
MA_MUX_DATA_OUTQ	fedcba9876543210			Access to test data output from the Moving Average filters, channel Q
		R W	XXXXh	Reads test data No effect

TABLE 13. BANK 0, REGISTER 3

MF_MUX_DATA_OUTI		EXT3		
Field	**Bank 0 Bit Position**	**R/W**	**Data**	**Description**
MF_MUX_DATA_OUTI	fedcba9876543210			Access to test data output from the In-Phase Matched Filter
		R W	XXXXh	Reads test data (bits [17..2]) No effect

TABLE 14. BANK 0, REGISTER 4

MF_MUX_DATA_OUTQ			EXT4	
Field	**Bank 0 Bit Position**	**R/W**	**Data**	**Description**
MF_MUX_DATA_OUTQ	fedcba9876543210			Access to test data output from the Mid-Phase Matched Filter
		R	XXXXh	Reads test data (bits [17..2])
		W		No effect

TABLE 15. BANK 0, REGISTER 5

BANK_CONTROL			EXT5	
Field	**Bank 0 Bit Position**	**R/W**	**Data**	**Description**
BANK_CONTROL	---------------0			Bits 15–1 return 0
		R/W		Changes Bank accessible by DSP1 If set to 0, only Registers in Bank[3:0] are accessible If set to 1, only Registers in Bank[7:4] are accessible Set to 0 on Power-On Reset

TABLE 16. BANK 0, REGISTER 6

INT_SYM_ERR0			EXT6	
Field	**Bank 0 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fedcba98--------	R		Returns 0
		W		No effect
INT_SYM_ERR0	--------76543210			READ access to the bit synchronizer's second order loop integrated symbol error
		R	XXh	Reads error data bits [7..0] (bits [23..8] are in Bank 1, ext 2)
		W		No effect

TABLE 17. BANK 0, REGISTER 7

TX_PWR_CTRL		EXT7		
Field	**Bank 0 Bit Position**	**R/W**	**Data**	**Description**
TXRX_PWR_POLARITY	f---------------			Controls the polarity of the TXSW and RXSW output pins Returns 0
		R	0	TXSW and RXSW active High
		W	1	TXSW and RXSW active Low
TX_PWR_ON	-edcba98--------			Determines TXSW output pin turn-on time referenced to the active frame counter
		R		Returns 0
		W	XXh	Bits 6–0 of turn-on time (=(x modulo 128) –1)
RESERVED	--------7-------	R		Returns 0
		W		No effect
TX_PWR_OFF	---------6543210			Determine TXSW output pin turn-off time referenced to the active frame counter
		R		Returns 0
		W	XXh	Bits 6–0 of turn-off time (=(x modulo 128) –1)

6.1.1 TX_PWR_ON, TX_PWR_OFF

These fields control the TXSW output pin, which is meant to control the RF module's transmit antenna switch. These fields can also be used to control the RF module's transmitter power supply. The turn-on and off times are provided in a number of transmitted bit periods, and are referenced to the active frame counter. Although only 7 bits are programmable, a total of 9 bits is necessary to define any particular instant of the frame. The additional two bits return fixed values, which depend on whether the base or the handset is selected.

Changes to these values take effect immediately.

NOTE: To disable transmit power continuously, clear TX_ENABLE.

6.2 BANK 1 REGISTERS

TABLE 18. BANK 1, REGISTER 0

RAT_BUF_ADDR		EXT0		
Field	**Bank 0 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	f---------------	R		Returns 0
		W		No effect
RX_AUTO_INCREMENT	-e--------------			Controls the auto-increment feature of the RX rate buffer
		R		Returns 0
		W	0	Disables auto-increment
			1	Enables auto-increment
RX_BUF_ADDR	--dcba98--------			Access to RX rate buffer address
		R	00h	Returns 0
		W	...	Address 0
			23h	...
			...	Address 23h = 35
				Illegal
RESERVED	--------7-------	R		Returns 0
		W		No effect
TX_AUTO_INCREMENT	---------6------			Controls the auto-increment feature of the TX rate buffer
		R		Returns 0
		W	0	Disables auto-increment
			1	Enables auto-increment
TX_BUF_ADDR	----------543210			Access to TX rate buffer address
		R		Returns 0
		W	00h	Address 0
			...	...
			23h	Address 23h = 35
			24h	TX/RX Ring Counter
			25h	TX Nibble Marker bits [15..0]
			26h	TX Nibble Marker bits [31..16]
			27h	TX Nibble Marker bits [35..32]
			28h	MOD_FREQ_DEV 0
			29h	MOD_FREQ_DEV 1
			2Ah	MOD_FREQ_DEV 2
			2Bh	MOD_FREQ_DEV 3
			2Ch	MOD_FREQ_DEV 4
			2Dh	MOD_FREQ_DEV 5
			2Eh	MOD_FREQ_DEV 6
			2Fh	MOD_FREQ_DEV 7
			30h	MOD_FREQ_DEV 8
			31h	MOD_FREQ_DEV 9
			32h	MOD_CENTER_FREQ
			...	Illegal

TABLE 19. BANK 1, REGISTER 1

RAT_BUF_DATA		EXT1		
Field	**Bank 1 Bit Position**	**R/W**	**Data**	**Description**
RX_BUF_DATA	----------3210			Access to the RX rate buffer data
		R	Xh	Reads value at current address
TX_BUF_DATA	----------3210			Access to the TX rate buffer data
		W	Xh	Writes value at current address
CTRL_DATA	fedcba9876543210			Access to rate buffer control or modulator settings
		W	XXXXh	Writes value at current address

TABLE 20. BANK 1, REGISTER 2

BIT_SYNC		EXT2		
Field	**Bank 1 Bit Position**	**R/W**	**Data**	**Description**
INT_SYM_ERR1	fedcba9876543210			READ access to the bit synchronizer's second order loop integrated symbol error
		R	XXXXh	Reads error data bits [23..8] (bits [7..0] are in bank 0, ext6)
SECOND_ORDER_ARM	fedcba9876543210			WRITE access to the bit synchronizer's second-order arm
		W	XXXXh	Writes 16-bit value

TABLE 21. BANK 1, REGISTER 3

RESERVED		EXT3		
Field	**Bank 1 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fedcba9876543210	R		Returns 0
		W		No effect

TABLE 22. BANK 1, REGISTER 4

TEST_CONFIG1			EXT4	
Field	**Bank 1 Bit Position**	**R/W**	**Data**	**Description**
ET_TEST_MODE	fed----------	R/W		Controls event trigger test modes
			XXX	Test mode
FC_TEST_MODE	---cb----------	R/W		Controls transmit and receive frame counter test modes
			XX	Test mode
TX_IF_DAC_CODING	-----a----------	R/W		Controls coding of TX IF 4-bit DAC
			0	Unsigned Binary
			1	2's Complement
RX_IF_ADC_MODE	-------87-------	R/W		Controls test mode of RX IF 1-bit ADC
			00*	Nominal operation
			01	1-bit ADC Test mode (writes digital output to P0)
			10	1-bit ADC Bypass (reads digital input from P0)
			11	Illegal
TX_IF_DAC_MODE	------9---5-----	R/W		Controls test mode of TX IF 4-bit DAC
			00*	Nominal operation
			01	4-bit DAC Bypass mode (writes digital output to P0)
			10	4-bit DAC Test mode (reads digital input from P0)
			11	Illegal
RESERVED	---------6-4----	R/W		Returns 0 No effect
DEMOD_MODE	------------32--	R/W		Controls test mode of Demodulator
			00*	Nominal operation
			01	Demodulator Test mode (writes demodulator data on P0)
			10	Demodulator Bypass (reads baseband data from P0)
			11	Illegal
MOD_MODE	--------------10	R/W		Controls test mode of Modulator
			00*	Nominal operation
			01	Modulator Test mode (reads data to modulate from P0)
			10	Modulator Bypass mode (writes baseband data to P0)
			11	Illegal

NOTE: *Indicates the reset value.

ALL MODES. The Z87L02/L03/L09 can support several test or bypass modes at the same time. For the Port P0 pin allocation, see Table 6.

RX_IF_ADC_MODE. In ADC TEST mode, TX_ENABLE and FULL SEARCH should be set to FALSE to force continuous reception and operation of the ADC. Check that the ADCCLK output is continuously toggling at 8.192 MHz.

TX_IF_DAC_MODE. In DAC Test mode, the PAON pin must be on continuously for power to be applied to the DAC. To verify that the PAON pin is on, place the chip in MOD_MODE = 01 (TEST mode), and check that the PAON pin stays at 1. Also set TX_ENABLE.

TABLE 23. BANK 1, REGISTER 5

TEST_CONFIG2		EXT5		
Field	**Bank 1 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fedcba987-------	R		Returns 0
		W		No effect
MF_MODE	---------65-----			Controls the test mode of Matched Filters
		R		Returns 0
		W	00*	Nominal operation MF Test mode
			01	(route MF_MUX_DATA_IN to MFs)
			10	MF Bypass mode
			11	Illegal
MA_I1_MODE	----------4----			Controls the test mode of Moving Average Filter 1, channel I
		R		Returns 0
		W	0*	Nominal operation
			1	MAI 1 Bypass mode
MA_I2_MODE	----------3---			Controls the test mode of Moving Average Filter 2, channel I
		R		Returns 0
		W	0*	Nominal operation
			1	MAI 2 Bypass mode
MA_Q1_MODE	----------2--			Controls the test mode of Moving Average Filter 1, channel Q
		R		Returns 0
		W	0*	Nominal operation
			1	MAQ 1 Bypass mode

NOTE: *Indicates the reset value.

TABLE 23. BANK 1, REGISTER 5 (CONTINUED)

TEST_CONFIG2		EXT5		
Field	**Bank 1 Bit Position**	**R/W**	**Data**	**Description**
MA_Q2_MODE	---------- 1-			Controls the test mode of Moving Average Filter 2, channel Q
		R		Returns 0
		W	0*	Nominal operation
			1	MAQ 2 Bypass mode
LPF_MUX_IN	--------------0			Controls the test mode of Low Pass Filters
		R		Returns 0
		W	0*	Nominal operation
			1	LPF Test mode (routes LPF_MUX_DATA_INI, Q to LPFs)

NOTE: *Indicates the reset value.

TABLE 24. BANK 1, REGISTER 6

CONTROL		EXT6		
Field	**Bank 1 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fedcb----------	R		Returns 0
		W		No effect
FS_INT_ENABLE	-----a----------	R/W		Controls frame start interrupt (INT1)
			0*	Disables frame start interrupt
			1	Enables frame start interrupt
INTERRUPT_0_ENABLE	------9---------	R/W		Controls interrupt 0 (INT0 on P0114)
			0*	Disables interrupt 0
			1	Enables interrupt 0
INTERRUPT_2_ENABLE	-------8--------	R/W		Controls interrupt 2 (INT2 used by DSP2 UO0)
			0*	Disables interrupt 2
			1	Enables interrupt 2

NOTE: *Indicates the reset value.

TABLE 24. BANK 1, REGISTER 6 (CONTINUED)

CONTROL		EXT6		
Field	**Bank 1 Bit Position**	**R/W**	**Data**	**Description**
P0_WAKEUP_ENABLE	--------7654----	R/W		Controls wake-up pins (P0[3..0])
			0000*	Disables all wake-up pins
			1xxx	Enables P03 as wake-up pin (if in input mode)
			x1xx	Enables P02 as wake-up pin (if in input mode)
			xx1x	Enables P01 as wake-up pin (if in input mode)
			xxx1	Enables P00 as wake-up pin (if in input mode)
TX_PWR_DAC_DATA	------------3210	R/W		Access to TX power 4-bit DAC output data
			Xh	Sets output value

NOTE: *Indicates the reset value.

TABLE 25. BANK 1, REGISTER 7

LPF_MUX_DATA_IN		EXT7		
Field	**Bank 1 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fed------------	R		Returns 0
		W		No effect
LPF_MUX_DATA_INI	---cba98--------			Access to test data for Low-Pass Filter, channel I
		R		Returns 0
		W	XXh	Writes test data
RESERVED	--------765-----	R		Returns 0
		W		No effect
LPF_MUX_DATA_INQ	----------43210			Access to test data for Low-Pass Filter, channel Q
		R		Returns 0
		W	XXh	Writes test data

6.3 BANK 2 REGISTERS

TABLE 26. BANK 2, REGISTER 0

VP_INOUT		EXT0		
Field	**Bank 2 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fedcba98--------	R W		Returns 0 No effect
STATUS	--------76543210			Access to the voice processor's Command/Status mailbox
		R	XXh	Reads a Status byte from the voice processor
COMMAND	--------76543210			Access to the voice processor's Command/Status mailbox
		W	XXh	Writes a Command byte to the voice processor

TABLE 27. BANK 2, REGISTER 1

RX_CONTROL		EXT1		
Field	**Bank 2 Bit Position**	**R/W**	**Data**	**Description**
SNR_ESTIMATE	fedcba9876543210			Access to a channel measurement (SNR) estimate
		R	XXXXh	SNR value from previous frame
UW_LOCATION	-------876543210			Location of the Unique Word
		W	XXXXh	Initializes the value that the receive frame counter is set to on detection of the Unique Word

TABLE 28. BANK 2, REGISTER 2

BIAS_ERROR		EXT2		
Field	**Bank 2 Bit Position**	**R/W**	**Data**	**Description**
BIAS_ERROR_DATA	fedcba9876543210			Access to the bias estimate of the AFC loop
		R	XXXXh	Current bias estimate value
		W		No effect

BIAS_ERROR_DATA. This value is used to bias the downconverter's NCO if the USE_CORE_BIAS register field is reset.

TABLE 29. BANK 2, REGISTER 3

RSSI		EXT3		
Field	**Bank 2 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fedcba98--------	R		Returns 0
		W		No effect
RSSI_DATA	--------76543210			Access to the 8-bit ADC (can be used for RSSI data)
		R		Returns latest value on 8-bit DAC
		W	XXh	No effect

RSSI_DATA. This value is sampled 1 time per frame (4ms), at bit 72 (the approximate middle) of the received data.

TABLE 30. BANK 2, REGISTER 4

CORE_BIAS		EXT4		
Field	**Bank 2 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fed----------	R		Returns 0
		W		No effect
CORE_BIAS_DATA	---cba9876543210			Stores value for the bias data of the downconverter's NCO
		R	XXXXh	Returns 0
		W		Updates bias value (2's complement number)

CORE_BIAS_DATA. This value is used if the USE_CORE_BIAS register field is set.

TABLE 31. BANK 2, REGISTER 5

MOD_PWR_CTRL		EXT5		
Field	**Bank 2 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	f---------------	R		Returns 0
		W		No effect
MOD_PWR_ON	-edcba98--------			Determines modulator turn-on time referenced to the active frame counter
		R		Returns 0
		W	XXh	Bits 6–0 of turn-on time (= (Time modulo 128) – 1)
RESERVED	--------76543210	R		Returns 0
		W		No effect

MOD_PWR_ON. This field controls the turn-on time for the internal modulator and NCO. Although only 7 bits are programmable, a total of 9 bits is necessary to

define any particular instant of the frame. The additional two bits exhibit fixed values, which depend on whether the base or the handset is selected. The modulator's turn-off time occurs a fixed count (number of bits) after the turn-on time: 144 bits on the base, 148 bits on the handset. Changes to this value take effect immediately.

NOTE: To disable the modulator, clear TX_ENABLE.

TABLE 32. BANK 2, REGISTER 6

RX_PWR_CTRL		EXT6		
Field	**Bank 2 Bit Position**	**R/W**	**Data**	**Description**
RFEON_POLARITY	f---------------			Controls the polarity of the RFEON output pin
		R		Returns 0
		W	0	Active High
			1	Active Low
RX_PWR_ON	-edcba98--------			Determines the RXSW output pin turn-on time and internal power up of the receiver, referenced to the receive frame counter
		R	XXh	Returns 0
		W		Bits 6–0 of turn-on time (=(x modulo 128) –1)
RESERVED	--------7-------	R		Returns 0
		W		No effect
RX_PWR_OFF	---------6543210			Determine RXSW output pin turn-off time and internal power down of receiver, referenced to the receive frame counter
		R	XXh	Returns 0
		W		Bits 6–0 of turn-off time (=(Time modulo 128) –1)

RX_PWR_ON, RX_PWR_OFF. This field controls the RXSW output pin as well as internal receive hardware. The RXSW pin is meant to control the RF module's receive antenna switch, and can also be used to control the RF module's receiver power supply. The turn-on and off times are provided in number of received bit periods, and are referenced to the Receive Frame Counter. Although only 7 bits are programmable, a total of 9 bits is necessary to define any particular instant of the frame. The additional two bits return fixed values, which depend on whether the base or the handset is selected. Changes to these values take effect immediately.

NOTES: To enable receive power continuously, clear TX_ENABLE and set SYNC_SEARCH_MODE to FULL_SEARCH (as is true in acquisition mode).

The polarity of the RXSW output pin is controlled by the TXRX_PWR_POLARITY bit in the TX_PWR_CTRL register.

TABLE 33. BANK 2, REGISTER 7

AMP_PWR_CTRL		EXT7		
Field	**Bank 2 Bit Position**	**R/W**	**Data**	**Description**
AMP_PWR_POLARITY	f---------------			Controls the polarity of the PAON output pin
		R		Returns 0
		W	0	Active High
			1	Active Low
AMP_PWR_ON	-edcba98--------			Determines the PAON output pin turn-on time referenced to the active frame counter
		R		Returns 0
		W	XXh	Bits 6–0 of turn-on time (=(x modulo 128) –1)
RESERVED	--------7-------	R		Returns 0
		W		No effect
AMP_PWR_OFF	---------6543210			Determine the PAON output pin turn-off time referenced to the active frame counter
		R		Returns 0
		W	XXh	Bits 6–0 of turn-off time (=(x modulo 128) –1)

AMP_PWR_ON, AMP_PWR_OFF. This field controls the PAON output pin, meant to control an RF module's power amplifier. The turn-on and turn-off times are provided in number of transmitted bit periods and are referenced to the active frame counter. Although only 7 bits are programmable, a total of 9 bits is necessary to define any particular instant of the frame. The additional two bits exhibit fixed values, which depend on whether the base or the handset is selected. Changes to these values take effect immediately.

NOTE: To disable the power amplifier, clear TX_ENABLE in SSP_STATE. To enable the power amplifier, set MOD_MODE = 01 (Test mode) in TEST_CONFIG1.

6.4 BANK 3 REGISTERS

TABLE 34. BANK 3, REGISTER 0

CONFIG1		EXT0		
Field	**Bank 3 Bit Position**	**R/W**	**Data**	**Description**
CORE_CLOCK	f---------------			Controls the clock to the Z87L0X DSP core
		R		Returns 0
		W	0	Clock = 16.384 MHz
			1[1]	Clock = 8.192 MHz
DBP_CLOCK	-e--------------			Controls the CLKOUT(DSP2) output pin (clock for the voice processor)
		R		Returns 0
		W	0	CLOCKOUT = 16.384 MHz
			1[2]	CLOCKOUT = 8.192 MHz
USE_CORE_BIAS	--d------------			Controls which bias value is used by the downconverter NCO
				Returns 0
		R	0[1]	Use internally calculated bias
		W	1	Use CORE_BIAS register value from DSP core
SYNLE_POLARITY	---c-----------			Controls the polarity of the hop pulse (SYNLE pin)
		R		Returns 0
		W	0	SYNLE is a positive pulse
			1	SYNLE is a negative pulse
UW_WINDOW_SIZE	----ba98--------			Defines the search window size (in bits) for the windowed search mode (for Unique Word or SYNC_D words)
		R		Returns 0
		W	0000	Window size =1
			0001	Window size = 3 (1 ±1)
			1111	Window size = 31 (1 ±15)
BIAS_THRESHOLD	--------76543210			Bias estimator threshold value
		R		Returns 0
		W	XXh	Sets the bias value

NOTES:
1. The Core Clock is at 16.384 MHz during the reset pulse; then it initializes to 8.192 MHz.
2. The CLKOUT pin is at 16.384 MHz during the reset pulse; then it initializes to 8.192 MHz.

CORE_CLOCK. This field is internally synchronized to avoid glitches. Changes to this bit occur immediately.

DBP_CLOCK. This field is internally synchronized to avoid glitches. Changes to this bit occur immediately.

SYNLE_POLARITY. Changes to this bit occur immediately.

BIAS_THRESHOLD. The bias threshold must be coded as a negative value (opposite of the threshold value) coded in the 2's complement. The nominal value for the threshold is –45 (= D3h). Internally, this value is sign-extended to 13 bits.

This value is set as a programmable option, in case the discriminator output levels do not match simulation results.

TABLE 35. BANK 3, REGISTER 1

CONFIG2		EXT1		
Field	**Bank 3 Bit Position**	**R/W**	**Data**	**Description**
ANTENNA_SW_DEFEAT	f---------------			Controls antenna switching (ANT0 and ANT1 pins) on the base (on the handset, the antenna switching is disabled)
		R		Returns 0
		W	0	Enable antenna switching
			1	Disable antenna switching
ANTENNA_SW_OFFSET	-edcba98-------			Controls antenna switching time
		R		Returns 0
		W	XXh	Offset in number of 2.048MHz clock cycles
SLEEP_PERIOD	--------76543210	W		Programs a sleep duration in
			00h	SLEEP mode
			01h	Illegal
			...	Sleep period = 1 frame (4ms)
			FFh	Sleep period = 255 frames (1.020s)
SLEEP_REMAINING	-------76543210	R		Returns value of sleep counter when SLEEP mode is interrupted by a WAKE signal
			00h	Normal expiration of sleep counter
			01h	One frame left before normal
			...	expiration
			FFh	255 frames left before normal expiration

SLEEP_PERIOD. Changes to this bit take effect immediately.

TABLE 36. BANK 3, REGISTER 2

SSPSTATE		EXT2		
Field	**Bank 3 Bit Position**	**R/W**	**Data**	**Description**
SW_SYNLE	f---------------			Controls accelerated synthesizer programming during sleep
		R/W	0*	Not active
			1	Active
STOP_CODCLK	-e--------------			Inhibits toggling of codec clock output during sleep
		R/W	0*	CODCLK is free running
			1	CODCLK remains high
DBP_STOP_CLOCK	--d------------			Controls toggling of the CLKOUT output pin (the clock for the voice processor)
		R/W	0*	CLKOUT is free running
			1	CLKOUT remains high
BSYNC_GAIN	---c-----------			Selects gain for bit sync first order loop
		R/W	0*	Nominal gain
			1	Gain divided by 64
BIAS_ENABLE	----b----------			Controls the closed-loop AFC circuit
		R/W	0*	No new bias estimation is performed (latest estimate used)
			1	Enables updates to BIAS_ERROR_DATA (bias estimate)
TX_ENABLE	-----a---------			Global enable for all transmit functions
		R/W	0*	Transmitter disabled
			1	Transmitter enabled
SYNC_SEARCH_WORD	------9--------			Controls the word searched for in search mode
		R/W	0*	Search for UW pattern (Unique Word)
			1	Search for SYNC_D pattern
SYNC_SEARCH_MODE	-------87-------			Controls the search mode (and frame synchronization)
		R/W	00*	No search
			01	WINDOW SEARCH (<= UW_LOCATION & WINDOW_SIZE)
			10	FULL SEARCH (during whole frame)
			11	Not used
HOP_ENABLE	---------6------			Enables transmission of the hop pulse
		R/W	0	Hop pulse disabled
			1	Hop pulse enabled

NOTE: *Indicates the reset value.

TABLE 36. BANK 3, REGISTER 2 (CONTINUED)

SSPSTATE		EXT2		
Field	**Bank 3 Bit Position**	**R/W**	**Data**	**Description**
SYNC_ACQ_CLEAR	----------5-----			Clears the SYNC_ACQ_IND flag
		R		Returns the most recent value written
		W	1→0	Clears the flag
FRAME_START_CLR	----------4----			Clears the FRAME_START_IND flag
		R		Returns the most recent value written
		W	0→1	Clears the flag
SLEEP_WAKE	----------3---	R/W		Enable bit for entering SLEEP mode
			0	Wake mode only
			1	SLEEP mode can be activated by GO_TO_SLEEP command
MULTIPLEX_SWITCH	----------21-	R/W		Controls the operation of the transceiver
			00*	SMUX (bit inversion and voice processor access disabled)
			01	Bit inversion is enabled; voice processor access is disabled
			10	Reserved
			11	TMUX (bit inversion and voice processor access enabled)
GO_TO_SLEEP	---------------0			Command bit to place the DSP core in SLEEP mode
		R		Returns the most recent value written
		W	0→1	DSP core enters SLEEP mode

NOTE: *Indicates the reset value.

DBP_STOP_CLOCK. When this bit is set to 1, the DBP clock is stopped within two clock periods. When this bit is set to 0, the DBP clock restarts within two clock periods. In every case, the DBP clock minimum specifications for High time and Low time are respected.

BSYNC_GAIN. Changes to this bit take effect immediately.

BIAS_ENABLE. This bit is a global enable for the Automatic Frequency Control. When the bit is set, the AFC hardware updates the current BIAS_ERROR_DATA during specific time windows. This operation is controlled by the event trigger hardware, making it a suitable operation for the AFC. When the bit is reset, the AFC operation is suspended. However, the current BIAS_ERROR_DATA, resulting from previous bias estimations, can still be used to bias the downconverter NCO.

TX_ENABLE. Global control for all system transmit functions, including PAON pin control (through AMP_PWR_ON/OFF register fields), TXSW pin control (through TX_PWR_ON/OFF register fields), power to the modulator, and NCO

(through MOD_PWR_ON and WAKE/SLEEP modes) is managed by TX_ENABLE. Changes to this bit take effect immediately.

HOP_ENABLE. Changes to this bit take effect immediately.

SLEEP_WAKE. This bit must be set to 1 to enable the core to put itself to sleep via the GO_TO_SLEEP command. To prevent the core from entering SLEEP mode, the SLEEP_WAKE bit must be reset to 0. The core may be awakened by a Port 0 wake-up pin when the sleep period has not expired. If the bit is not reset to 0, the core reenters SLEEP mode when the wake-up input is deasserted.

NOTE: By design, a wake-up input exhibits a minimum duration of 10 µs, to allow the software to safely reset the SLEEP_WAKE bit.

TABLE 37. BANK 3, REGISTER 3

SSPSTATUS		EXT3		
Field	**Bank 3 Bit Position**	**R/W**	**Data**	**Description**
EVENT_COUNTER	fedcba987-------			Current active frame counter value
		R	00h	First value at beginning of frame (0)
			...	
			173h	Most recent value at end of frame (371)
			...	Illegal values
		W		No effect
RESERVED	---------65-----	R		Returns 0
		W		No effect
HAND_BASE_SEL	----------4----			Reflects status of Handset/Base select pin (HBSW)
		R	0	Base (HBSW = 0)
			1	Handset (HBSW = 1)
		W		No effect
SYNC_ACQ_IND	----------3---			Indicates detection of a Sync word (UW or SYNC_D depending on SYNC_SEARCH_WORD search mode)
		R	0	No sync word detected
			1	Sync word detected
		W		No effect
FRAME_START_IND	----------2--			Indicates start of a new frame
		R	0	No start of new frame (1 written to FRAME_START_CLR)
			1	New frame started
		W		No effect
RESERVED	----------10	R		Returns 0
		W		No effect

EVENT_COUNTER. This field reads the double-buffered current value of the active frame counter. In ICE mode, this value is frozen while the HALT pin is asserted.

TABLE 38. BANK 3, REGISTER 4

GPIO0DIR		EXT4		
Field	**Bank 3 Bit Position**	**R/W**	**Data**	**Description**
DIRECTION0	fedcba9876543210			Independent control of the Port 0 pin direction
		R/W	..0.	Sets the pin in input mode
			..1.	Sets the pin in output mode

TABLE 39. BANK 3, REGISTER 5

GPIO0DIR		EXT5		
Field	**Bank 3 Bit Position**	**R/W**	**Data**	**Description**
DATA0	fedcba9876543210			Access to Port 0 data
		R	XXXXh	Reads pin values
		W	XXXXh	Writes output pin values

TABLE 40. BANK 3, REGISTER 6

GPIO0DIR		EXT6		
Field	**Bank 3 Bit Position**	**R/W**	**Data**	**Description**
DIRECTION1	fedcba9876543210			Independent control of Port 1 pin direction
		R/W	..0.	Pin in input mode
			..1.	Pin in output mode

TABLE 41. BANK 3, REGISTER 7

GPIO0DIR		EXT7		
Field	**Bank 3 Bit Position**	**R/W**	**Data**	**Description**
DATA1	fedcba9876543210			Access to Port 1 data
		R	XXXXh	Reads pin values
		W	XXXXh	Writes output pin values

6.5 BANK 4 REGISTERS

TABLE 42. BANK 4, REGISTER 0

MEM_CONTROL		EXT0		
Field	**Bank 4 Bit Position**	**R/W**	**Data**	**Description**
DSP1_SPRAM1_WR	---------------0	R/W		Writing a 1 to this bit writes to DSP1's SPRAM1 using the address in Bank 4 Register 1 and Data in Bank 4 Register 2.
			0*	No effect.
			1	Strobes SPRAM1
DSP2_SPRAM2_WR	--------------1-	R/W		Writing a 1 to this bit writes to DSP2's SPRAM2 using the address in Bank 4 Register 1 and Data in Bank 4 Register 2.
			0*	No effect.
			1	Strobes SPRAM2
SPRAM1_DSP1_EN	-------------2--	R/W		When a 1 is written to this bit, it enables mapping of SPRAM1 into the DSP1's Program Data address space at the addresses F800h–FBFFh.
			0*	SPRAM1 Disabled.
			1	SPRAM1 Enabled.
SPRAM2_DSP2_EN	------------3---	R/W		When a 1 is written to this bit, it enables mapping of SPRAM2 into the DSP2's Program Data address space at the addresses FC00h–FFFFh.
			0*	SPRAM2 Disabled.
			1	SPRAM2 Enabled.
SPRAM1_ADDR_SRC	-----------4----	R/W		When a 1 is written to this bit, the source of the address for SPRAM1 is Bank 4 Register 1; if there is a 0, the source is DSP1's Program Counter (PC).
			0*	Source DSP1 PC.
			1	Source Bank 4 Register 1.
SPRAM2_ADDR_SRC	----------5-----	R/W		When a 1 is written to this bit, the source of the address for SPRAM2 is Bank 4 Register 1. When a 0 is written to this bit, the source is DSP2's Program Counter (PC).
			0*	Source DSP2 PC.
			1	Source Bank 4 Register 1.

NOTE: *Indicates reset value.

TABLE 42. BANK 4, REGISTER 0 (CONTINUED)

MEM_CONTROL		EXT0		
Field	**Bank 4 Bit Position**	**R/W**	**Data**	**Description**
EMOE	---------6------	R/W		This bit controls the emoe pin. Resets to 0.
			0*	Set emoe pin to 0.
			1	Set emoe pin to 1.
EMWE	--------7-------	R/W		Data in this bit is being reflected on pin emwe.
			0*	Set emwe pin to 0.
			1	Set emwe pin to 1.
FLASH_ADR_SRC	-------8--------	R/W		This bit defines the source of the Address for the external Flash:
			0	Source DSP1 PC.
			1	Source Bank 4 Register 1.
FLASH_DATA_DIR	------9---------	R/W		This bit defines the direction of the dat[15:0] pins. Set to 0 on POR; valid only if there is a 1 in Bank 4, Register 0, Bit 8.
			0	dat[15..0] input mode.
			1	dat[15..0] output mode.
RESERVED	fedcba----------	R		Returns 0.
		W		No effect.

NOTE: *Indicates reset value.

TABLE 43. BANK 4, REGISTER 1

MEM_ADDRESS		EXT0		
Field	**Bank 4 Bit Position**	**R/W**	**Data**	**Description**
MEM_ADDR[15:0]	fedcba9876543210	R/W		This register contains the address that goes to the SPRAM1 and SPRAM2, when either is being accessed for writing, and Flash Memory when Flash is being accessed for both WRITE and READ.

TABLE 44. BANK 4, REGISTER 2

MEM_DATA		EXT2		
Field	**Bank 4 Bit Position**	**R/W**	**Data**	**Description**
MEM_DATA[15:0]	fedcba9876543210	R/W		This register contains data written to SPRAM1, SPRAM2, or Flash. Reading this register is valid only when there is a 1 in Bank 4, Register 1, Bit 8 (FLASH PROGRAMMING mode).

TABLE 45. BANK 4, REGISTER 4

WDT_CTL_DATA		EXT4		
Field	**Bank 4 Bit Position**	**R/W**	**Data**	**Description**
WDT_VAL	-edcba9876543210	R/W		WDT count down counter
WDT_ENABLE	f--------------	R/W	1 0	Enables WDT. Disable, reset to 0.

TABLE 46. BANK 4, REGISTER 5

BANK_CONTROL		EXT5		
Field	**Bank 4 Bit Position**	**R/W**	**Data**	**Description**
BANK_SELECT	---------------0	R/W	1 0	Bank[7:4] is accessible. Bank[3:0] is accessible.

TABLE 47. BANK 4, REGISTER 6

OSC/TEST_CONTROL		EXT6		
Field	**Bank 4 Bit Position**	**R/W**	**Data**	**Description**
DSP2_TST_ROM_EN	---------------0	R/W	1 0	Enables DSP2 test ROM. Disables DSP2 test ROM.
DSP2_RST	--------------1-	R/W	1 0	Clears a reset of DSP2. Causes a reset of DSP2.
DSP2_CLK_SRC	-------------2--	R/W	1 0	Switches source of the clock for DSP2 to P2CLK pin. Transceiver of DSP1.
P2CLK_EN	------------3---	R/W	1 0	Enables P2CLK. This bit must be set only after bit 2 of the sam register is set to 1. Starts/Stops clock on its own rising edge.

NOTE: *Indicates reset value.

TABLE 47. BANK 4, REGISTER 6 (CONTINUED)

OSC/TEST_CONTROL		EXT6		
Field	**Bank 4 Bit Position**	**R/W**	**Data**	**Description**
DSP1_WAIT_CTRL	----------4----	R/W		Wait State Enable for DSP1.
			1	All accesses to External registers exhibit one Wait State.
			0	There is no wait state if the bit is 0.
STOP_DSP2_CLK	----------5-----	R/W		This bit stops the DSP2 clock High.
			1	Stop
			0	Run; reset to 0.
DSP1_TEST_ROM	---------6------	R/W		Disables DSP1 test ROM mode.
			1	Disable
			0	Enable
RESERVED	--------7-------	N/A		
OSC_GAIN_CTL	------98--------	R/W		Control gain of the oscillator's amplifier after power-on.
			00*	Maximum gain
			01	Gain 1
			10	Gain 2
			11	Minimum gain
WDT_CLK_SEL	----ba----------	R/W		WDT Clock select control
			00	Internal osc/32 6.4µs—28.8µs
			01	DSPCLK/8
			10	Internal osc/2.4µs—1.8µs
			11	DSPCLK/8
RESERVED	fedc------------	N/A		

NOTE: *Indicates reset value.

TABLE 48. BANK 4, REGISTER 7

RF/ADC/GP_CONTROL		EXT7		
Field	**Bank 4 Bit Position**	**R/W**	**Data**	**Description**
SYNCLK	---------------0	R/W		This bit is reflected on pin SYNCLK
SYNDAT	--------------1-	R/W		This bit is reflected on pin SYNDAT
ADC_DECODE	------------32--	R/W		Decode ADC channels:
			00	RSSI
			01	BATMON
			10	ANIN
			11	Not used
ENABLE_GPIO	----------4----	R/W	0	Enables ANT0,ANT1 to be used as GPO outputs
			1	Enables GP
ANT0/GPIO0	----------5-----	R/W		GP0 control
			1	Sets GP0
			0	Clears GP0

TABLE 48. BANK 4, REGISTER 7 (CONTINUED)

RF/ADC/GP_CONTROL			EXT7	
Field	**Bank 4 Bit Position**	**R/W**	**Data**	**Description**
ANT1/GP1	---------6------	R/W		GP1 control
			1	Sets GP1
			0	Clears GP1
GP0/EXTCLK_SELECT	--------7-------	R/W		If ENABLE_GPIO = 1 and this bit = 1 then ANT0/GP0/EXTCLK Becomes EXTCLK Output
STOP_EXTCLK	-------8--------	R/W		This bit controls the EXTCLK output.
			1	Stops the clock High
			0	Clock running
WDT_OUTPUT_SELECT	------9---------	R/W		Mux WDT prescaler output to ANT1.
EXTCLK CLOCK SELECT	---cba----------	R/W	000	XTAL/2
			001	P2CLK
			010	P2CLK/2
			011	P2CLK/4
			100	XTAL/4
			101	XTAL/8
			110	DSP2CLK
ENABLE P114 WAKEUP FUNCTION	--d----------	R/W	0	Enables wake-up function on P114
			1	Disables wake-up function on P114 Wake-up function when enabled is active Low
RESERVED	fe----------	N/A		

6.6 BANK 5 REGISTERS

TABLE 49. BANK 5, REGISTER 0

I^2C_CONTROL			EXT0	
Field	**Bank 5 Bit Position**	**R/W**	**Data**	**Description**
I^2C_CLK_SELECT	----------10	R/W		I^2C Clock Select (Master Clock DSP1 16.38 or 8.192Mhz)
			00	614 clks/bit (13.2kHz @ 8.192Mhz)
			01	124 clks/bit (65.5kHz @ 8.192Mhz)
			10	31 clks/bit (262kHz @ 8.912Mhz)
			11	18 clks/bit (451kHz @ 8.192Mhz)
I^2C_ENABLE	----------4-2--	R/W		Enables I^2C interface
			0-0	Disables
			1-1	Both bits must be 1 to enable the I^2C port.

TABLE 50. BANK 5, REGISTER 1

I^2C_CMD		EXT1		
Field	**Bank 5 Bit Position**	**R/W**	**Data**	**Description**
I^2C_BUSY	---------------0	R/W		READ
			0	Idle
			1	Busy; WRITE = No Effect
I^2C_RESET	--------------1-	R/W		Returns 1
			0	No Effect
			1	Reset I^2C interface
I^2C_COMMAND	---------654----	R/W	000	Send Start bit, address the byte specified by the data register, then the fetch acknowledgment bit in data(0)
			001	Send the byte of data specified in the data register, then fetch acknowledgment bit stored in bit 0
			010	Send bit 7 of data register as an acknowledgment bit, then receive a data byte
			011	Send bit 7 of the data register as an acknowledgment bit
			10X	10X—Null operation; must be used with a reset bit
			110	110—Received one data byte.
			111	111—Send Stop bit; one cycle is generated.

TABLE 51. BANK 5, REGISTER 2

I^2C_DATA		EXT2		
Field	**Bank 5 Bit Position**	**R/W**	**Data**	**Description**
I^2C_DATA	--------76543210	R/W		When written, this bit sends data out of SERDAT; when read, this bit is the received data on SERDAT.

TABLE 52. BANK 5, REGISTER 3

RESERVED		EXT3		
Field	**Bank 5 Bit Position**	**R/W**	**Data**	**Description**
Reserved	fedcba9876543210	N/A		

TABLE 53. BANK 5, REGISTER 4

RESERVED		EXT4		
Field	**Bank 5 Bit Position**	**R/W**	**Data**	**Description**
Reserved	fedcba9876543210	N/A		

TABLE 54. BANK 5, REGISTER 5

BANK_CONTROL		EXT5		
Field	**Bank 5 Bit Position**	**R/W**	**Data**	**Description**
BANK_CONTROL	---------------0	R/W	1	Bank[7:4] is accessible
			0	Bank[3:0] is accessible

TABLE 55. BANK 5, REGISTER 6

RESERVED		EXT6		
Field	**Bank 5 Bit Position**	**R/W**	**Data**	**Description**
Reserved	fedcba9876543210	N/A		

TABLE 56. BANK 5, REGISTER 7

RESERVED		EXT7		
Field	**Bank 5 Bit Position**	**R/W**	**Data**	**Description**
Reserved	fedcba9876543210	N/A		

7. DSP2 PROCESSORS

TABLE 57. SECONDARY PROCESSOR REGISTER SUMMARY

Address	Register	READ Description	WRITE Description	Table #
EXT0	P1_COMMAND/P2_STATUS	P1 Command	P2 Status	58
EXT1	VOICE_DATA	Receive Voice	Transmit Voice	59
EXT2	RESERVED			60
EXT3	SP RAM2 WRITE Data register	Read back register Data	Write Data	61
EXT4	TIMER_CONFIGURATION		Timer Control	62
EXT5	CODEC_INTF_CH0_DATA	Channel 0 TXD	Channel 0 RXD	63
EXT6	CODEC_INTF_CH1_DATA	Channel 1 TXD	Channel 1 RXD	64
EXT7	CODEC_INTF_CONFIGURATION		Codec Interface Configuration 0, Codec Interface Configuration 1	65, 66

Tables 58 through 64 present the secondary processor registers in detail.

TABLE 58. REGISTER 0

P1_COMMAND/P2_ STATUS				
Field	**EXT0 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fedcba98--------	R/W		Returns 0 No effect
COMMAND	--------76543210			Access to DSP1's Command/Status mailbox
		R	XXh	Reads Command byte from DSP1
STATUS	--------76543210			Access to the voice processor's Command/Status mailbox
		W	XXh	Writes a Status byte to DSP1

TABLE 59. REGISTER 1

VOICE_DATA				
Field	**EXT1 Bit Position**	**R/W**	**Data**	**Description**
RESERVED	fedcba98--------	R/W		Returns 0 No effect
RX_VOICE	--------76543210	R	XXh	Reads a received ADPCM voice; reads a CRC from the transceiver
TX_VOICE	--------76543210			Access to the voice processor's Command/Status mailbox
		W	XXh	Writes a transmit ADPCM voice; writes a CRC to the transceiver

TABLE 60. REGISTER 2

RESERVED				
Field	**EXT2 Bit Position**	**R/W**	**Data**	**Description**
Reserved	fedcba9876543210	R/W		

TABLE 61. REGISTER 3

RESERVED				
Field	**EXT3 Bit Position**	**R/W**	**Data**	**Description**
SP RAM2 WRITE Data register	fedcba9876543210	R/W		This data is written to SP RAM2 when DSP2 reads address space F800–FBFF

TABLE 62. REGISTER 4

TIMER_CONFIGURATION				
Field	**EXT4 Bit Position**	**R/W**	**Data**	**Description**
COUNTER_ENABLE	f---------------	R/W		Returns 0
			0	Disable
			1	Enable (Default)
COUNT_ENABLE	-e-------------	R/W		Returns 0
			0	Disable (Default)
			1	Enable
CLOCK_SOURCE	--d------------	R/W		Returns 0
			0	Use P2CLK/2 as source
			1	Use FSYNC (8 kHz) as source
COUNT_VALUE	---cba9876543210	R/W		Returns 0
			XXXXh	Set 13-bit timer down count value

TABLE 63. REGISTER 5

CODEC_INTF_CH0_DATA				
Field	**EXT5 Bit Position**	**R/W**	**Data**	**Description**
CH0_TXD	fedcba9876543210	R	XXXXh	Reads Transmit PCM data from the codec, channel 0
CH0_RXD	fedcba987654320	W	XXXXh	Writes Receive PCM data to the codec, channel 0

TABLE 64. REGISTER 6

CODEC_INTF_CH1_DATA	EXT6			
Field	**Bit Position**	**R/W**	**Data**	**Description**
CH1_TXD	fedcba9876543210	R	XXXXh	Reads Transmit PCM data from the codec, channel 1
CH1_RXD	fedcba987654320	W	XXXXh	Writes Receive PCM data to the codec, channel 1

Register 7, Table 65, is double-buffered. Successive WRITE operations allow sharing the register between two distinct command sets, as a WRITE operation loads the input buffer while shifting its contents to the output buffer. The CODEC_INTF_CONFIGURATION_0 register is loaded with the first WRITE operation, and the CODEC_INTF_CONFIGURATION_1 register is loaded with the second WRITE operation.

TABLE 65. REGISTER 7 OUTPUT BUFFER—1ST WRITE OPERATION

CODEC_INTF_ CONFIGURATION _0				
Field	**EXT7 Bit Position**	**R/W**	**Data**	**Description**
CODEC_0_ENABLE	f---------------	R/W		Returns 0
			0	Disable (Default)
			1	Enable
FSYNC_SOURCE	-e--------------	R/W		Returns 0
			0	External Source (Default)
			1	Internal Source
CODEC_MODE	--dc------------	R/W		Returns 0
			00	8-bit, with hardware µ-law companding
			01	8-bit, no hardware µ-law companding
			10	Reserved
			11	Reserved
FSYNC_COUNTER	----ba987654----	R/W		Returns 0
			XXh	CODCLK/FSYNC ratio prescaler (up counter)
CODCLK_COUNTER	------------3210	R/W		Returns 0
			Xh	P2CLK/CODCLK ratio prescaler (up counter)

TABLE 66. REGISTER 7 OUTPUT BUFFER—2ND WRITE OPERATION

CODEC_INTF_ CONFIGURATION _1				
Field	**EXT7 Bit Position**	**R/W**	**Data**	**Description**
CODEC_1_ENABLE	f---------------	R/W		Returns 0
			0	Disable (Default)
			1	Enable
CODCLK_SOURCE	-e---------------	R/W		Returns 0
			0	External Source (Default)
			1	Internal Source
WAIT _STATE_EXT6	--dc------------	R/W		Returns 0
			00	no wait states (nws)
			01	nws READ; wait states (ws) WRITE
			10	ws READ; nws WRITE
			11	ws READ; ws WRITE
WAIT _STATE_EXT5	----ba----------	R/W		Returns 0
			00	no wait states (nws)
			01	nws READ; wait states (ws) WRITE
			10	ws READ; nws WRITE
			11	ws READ; ws WRITE
WAIT _STATE_EXT4	------98--------	R/W		Returns 0
			00	no wait states (nws)
			01	nws READ; wait states (ws) WRITE
			10	ws READ; nws WRITE
			11	ws READ; ws WRITE
WAIT _STATE_EXT3	--------76------	R/W		Returns 0
			00	no wait states (nws)
			01	nws READ; wait states (ws) WRITE
			10	ws READ; nws WRITE
			11	ws READ; ws WRITE
WAIT _STATE_EXT2	----------54----	R/W		Returns 0
			00	no wait states (nws)
			01	nws READ; wait states (ws) WRITE
			10	ws READ; nws WRITE
			11	ws READ; ws WRITE
WAIT_STATE_EXT1	------------32--	R/W		Returns 0
			00	no wait states (nws)
			01	nws READ; wait states (ws) WRITE
			10	ws READ; nws WRITE
			11	ws READ; ws WRITE

TABLE 66. REGISTER 7 OUTPUT BUFFER—2ND WRITE OPERATION (CONTINUED)

CODEC_INTF_ CONFIGURATION _1				
Field	**EXT7 Bit Position**	**R/W**	**Data**	**Description**
WAIT_STATE_EXT0	----------10	R/W		Returns 0
			00	no wait states (nws)
			01	nws READ; wait states (ws) WRITE
			10	ws READ; nws WRITE
			11	ws READ; ws WRITE

8. INSTRUCTION SET DESCRIPTION

Refer to ZiLOG's *Z89C00 Instruction Set* for a complete description of primary and DSP2 processors.

8.1 INSTRUCTION SET SUMMARY

TABLE 67. INSTRUCTION SET SUMMARY

Instruction	Description	Op Code	Synopsis	Operands	# Words	# Cycles	Example
ABS	Absolute	1001000	ABS[<cc>,]<src>	<cc>,A	1	1	ABS NC,A
	Value	1001000		A	1	1	ABS A
ADD	Addition	1001001	ADD<dest>,<src>	A,<pregs>	1	1	ADD A,P0:0
		1000001		A,<dregs>	1	1	ADD A,D0:0
		1000100		A,<limm>	2	2	ADD A,#%1234
		1000101		A,<memind>	1	3	ADD A,@@P0:0
		1000011		A,<direct>	1	1	ADD A,%F2
		1000001		A,<regind>	1	1	ADD A, @P1:1
		1000000		A,<hwregs>	1	1	ADD A,X
AND	Bitwise AND	1011001	AND<dest>,<src>	A,<pregs>	1	1	AND A,P2:0
		1010001		A,<dregs>	1	1	AND A,D0:1
		1010100		A,<limm>	2	2	AND A,#%1234
		1010101		A,<memind>	1	3	AND A,@@P1:0
		1010001		A,<direct>	1	1	AND A, %2C
		1010001		A,<regind>	1	1	AND
		1010000		A,<hwregs>	1	1	A,@P1:2+LOOP
							AND A, EXT3
CALL	Subroutine	0010100	CALL	<cc>,<direct>	2	2	CALL sub1
	call	0010100	[<cc>,]<address>	<direct>	2	2	CALL Z,sub2
CCF	Clear carry flag	1001010	CCF	None	1	1	CCF
CIEF	Clear Carry flag	1001010	CIEF	None	1	1	CIEF
COPF	Clear OP flag	1001010	COPF	None	1	1	COPF
CP	Comparison	0111001	CP<src1>,<src2>	A,<pregs>	1	1	CP A,P0:0
		0110001		A,<dregs>	1	1	CP A,D3:1
		0110101		A,<memind>	1	3	CP A,@@P0:0
		0110011		A,<direct>	1	1	CP A,%FF
		0110001		A,<regind>	1	1	CP A,@P2:1+
		0110000		A,<hwregs>	1	1	CP A,STACK
		0110100		A,<limm>	2	2	CP A,#%FFCF
DEC	Decrement	1001000	DEC [<cc>,]<dest>	<cc>A,	1	1	DEC NZ,A
		1001000		A	1	1	DEC A
INC	Increment	1001000	INC [<cc>,] <dest>	<cc>,A	1	1	INC PL,A
		1001000		A	1	1	INC A
JP	Jump	0100110	JP	<cc>,<direct>	2	2	JP NIE,Label
		0100110	[<cc>,]<address>	<direct>	2	2	JP Label

TABLE 67. INSTRUCTION SET SUMMARY (CONTINUED)

Instruction	Description	Op Code	Synopsis	Operands	# Words	# Cycles	Example

LD	Load destination with source	0000000
		0000001
		0001001
		0000001
		0000101
		0000011
		0000111
		0000100
		0001100
		0001010
		0000110
		0000010
		0001001
		0000001
		0000100
		0100101
		0000101
		0000001
		0000000
			LD<dest>,<src>	A,<hwregs>
				A,<dregs>
				A,<pregs>
				A,<regind>
				A,<memind>
				A,<direct>
				<direct>,A
				<dregs>,<hwregs>
				<pregs>,<simm>
				<pregs>,<hwregs>
				<regind>,<limm>
				<regind>,<hwregs>
				<hwregs>,<pregs>
				<hwregs>,<dregs>
				<hwregs>,<limm>
				<hwregs>,<accind>
				<hwregs>,<memind>
				<hwregs>,<regind>
				<hwregs>,<hwregs>
					1
					1
					1
					1
					1
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						1
						1
						3
						1
						1
						1
						1
						1
						1
						1
						1
						1
						2
						3
						3
						1
						1
							LD A,X
							LD A,D0:0
							LD A,P0:1
							LD A,@P1:1
							LD A,@D0:0
							LD A, 124
							LD 124, A
							LD DO:0, EXT7
							LD P1:1,#%FA
							LD P1:1,EXT1
							LD
							@P1:1,#%1234
							LD @P1:1+,X
							LD Y,P0:0
							LD SR,D0:0
							LD PC,#%1234
							LD X,@A
							LD Y,@D0:0
							LD A,@P0:0-
							LOOP
							LD X, EXT6

MLD	Multiply	1010010 1010010 1011011 1011011	MLD<srcl>,<srcl> [,<bank switch>]	<hwregs>,<regind> <hwregs>,<regind>,< bank switch> <regind>,<regind> <regind>,<regind>,< bank switch>	1 1 1 1	1 1 1 1	MLD A,@P0:0+LOOP MLD A,@P1:0,OFF MLD @P1:1,@P2:0 MLD @P0:1,@P1:0,ON
MPYA	Multiply and add	1010010 1010010 1011011 1011011	MPYA <srcl>,<src2> [,<bank switch>]	<hwregs>,<regind> <hwregs>,<regind>, <bank switch> <regind>,<regind> <regind>,<regind>, <bank switch>	1 1 1 1	1 1 1 1	MPYA A@P0:0 MPYA A,@P1:0,OFF MPYA @P1:1,@P2:0 MPYA@P0:1,@P 1:0,ON
MPYS	Multiply and subtract	0010010 0010010 0011011 0011011	MPYS<src1>,<src 2> [,<bank switch>]	<hwregs>,<regind> <hwregs>,<regind>, <bank switch> <regind>,<regind> <regind>,<regind>, <bank switch>	1 1 1 1	1 1 1 1	MPYS A,@P0:0 MPYS A,@P1:0,OFF MPYS @P1:1,@P2:0 MPYS @P0:1,@P1:0,ON
NEG	Negate	1001000 1001000	NEG <cc>,A	<cc>, A A	1 1	1 1	NEG NZ,A NEG A
NOP	No operation	0000000	NOP	None	1	1	NOP

TABLE 67. INSTRUCTION SET SUMMARY (CONTINUED)

Instruction	Description	Op Code	Synopsis	Operands	# Words	# Cycles	Example
OR	Bitwise OR	1101001	OR <dest>,<src>	A, <pregs>	1	1	OR A, P0:1
		1100001		A, <dregs>	1	1	OR A, D0:1
		1100100		A, <limm>	2	2	OR A,#%202
		1100101		A, <memind>	1	3	OR A,@@P2:1+
		1100011		A, <direct>	1	1	OR A, %2C
		1100001		A, <regind>	1	1	OR A, @P1:0-
		1100000		A, <hwregs>	1	1	LOOP
							OR A, EXT6
POP	Pop value from stack	0001010	POP <dest>	<pregs>	1	1	POP P0:0
		0000100		<regs>	1	1	POP D0:1
		0000010		<regind>	1	1	POP @P0:0
		0000000		<hwregs>	1	1	POP A
PUSH	Push value onto stack	0001001	PUSH <src>	<pregs>	1	1	PUSH P0:0
		0000001		<dregs>	1	1	PUSH D0:1
		0000001		<regind>	1	1	PUSH @P0:0
		0000000		<hwregs>	1	1	PUSH BU5
		0000100		<limm>	2	2	PUSH #12345
		0100101		<accind>	1	3	PUSH @A
		0000101		<memind>	1	3	PUSH @@P0:0
RET	Return from subroutine	0000000	RET	None	1	2	RET
RL	Rotate Left	1001000	RL <cc>,A	<cc>,A	1	1	RL NZ,A
		1001000		A	1	1	RL A
RR	Rotate Right	1001000	RR <cc>,A	<cc>,A	1	1	RR C,A
		1001000		A	1	1	RR A
SCF	Set C flag	1001010	SCF	None	1	1	SCF
SIEF	Set IE flag	1001010	SIEF	None	1	1	SIEF
SLL	Shift left logical	1001000	SLL	[<cc>,]A	1	1	SLL NZ,A
		1001000		A	1	1	SLL A
SOPF	Set OP flag	1001010	SOPF	None	1	1	SOPF
SRA	Shift right arithmetic	1001000	SRA<cc>,A	<cc>,A	1	1	SRA NZ,A
		1001000		A	1	1	SRA A
SUB	Subtract	0011001	SUB<dest>,<src>		1	1	SUB A,P1:1
		0010011		A,<pregs>	1	1	SUB A,D0:1
		0010100		A,<dregs>	2	2	SUB A,#%2C2C
		0010101		A,<limm>	1	3	SUB A,@D0:1
		0010011		A, <memind>	1	1	SUB A,%15
		0010001		A, <direct>	1	1	SUB A, @P2:0-
		0010000		A, <regind>	1	1	LOOP
				A, <hwregs>			SUB A, STACK
XOR	Bitwise exclusive OR	1111001	XOR <dest>,<src>	A, <pregs>	1	1	XOR A, P2:0
		1110001		A, <dregs>	1	1	XOR A,D0:1
		1110100		A, <limm>	2	2	XOR A,#13933
		1110001		A, <memind>	1	3	XOR A,@P2:1+
		1110011		A, <direct>	1	1	XOR A, %2F
		1110001		A, <regind>	1	1	XOR A, @P2:0
		1110000		A, <hwregs>	1	1	XOR A, BUS

9. ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS

NOTE: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 68. ABSOLUTE MAXIMUM RATINGS*

Symbol*	Parameter	Min	Max	Units
V_{DD}, AV_{DD}	DC Supply Voltage	–0.5	5.0	V
V_{IN}	Input Voltage	–0.5	V_{DD}+0.5	V
V_{OUT}	Output Voltage	–0.5	V_{DD}+0.5	V
T_{STG}	Storage Temperature	–65	+150	°C

NOTE: *These voltage ratings are referenced to GND and all inputs and outputs are referenced to V_{DD}.

9.2 STANDARD TEST CONDITIONS

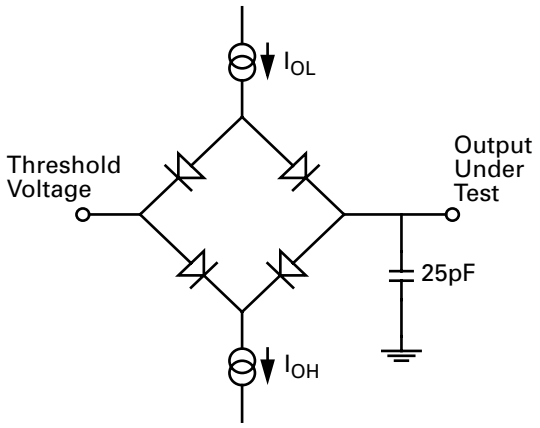
The electrical characteristics listed below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pins (Figure 20). Standard test conditions are as follows:

$2.7V \leq V_{DD} \leq 3.3V$

GND = 0V

T_A = –20°C to +70°C

FIGURE 20. STANDARD TEST LOAD DIAGRAM



9.3 OPERATING CONDITIONS AND DC ELECTRICAL CHARACTERISTICS

TABLE 69. OPERATING CONDITIONS AND DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Conditions
V_{DD}, AV_{DD}	Supply Voltage	2.7	3.3	V	
V_{IH}	Input High Voltage	0.7 x V_{DD}	V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	GND–0.3	V_{DD} x 0.3	V	
V_{OH}	Output High Voltage	V_{DD} – 0.4		V	I_{OH} = –2 mA
V_{OL}	Ouput Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OL2}	Ouput Low Voltage[1]		1.2	V	I_{OL} = 6 mA
I_L	Input Leakage	–2	+2	µA	V_{DD} 2.7V–3.3V
I_{CC}	Supply Current		25	mA	V_{DD} 2.7V–3.3V
I_{CC2}	Standby Mode Current		2	mA	V_{DD} 2.7V–3.3V
T_A	Operating Temperature[2]	–20	+70	°C	

NOTES:
1. Maximum 3 pins total from P0[15..0], P1(15:0).
2. 1 mA typical at 25°C and 3.0V.

TABLE 70. 8-BIT ADC—TEMPERATURE: –20°C TO +70°C

Parameter	Minimum	Typical	Maximum	Units
Resolution	—	8	—	bit
Integral nonlinearity	—	0.5	1	LSB
Differential nonlinearity	—	—	—	LSB
Sample window	5	—	120	ns
Input voltage range	—	—	AV_{DD}	V
Input resistance	—	25	—	KΩ
Input capacitance	—	20	—	pF

NOTE: *8-bit ADC only tested for 6-bit resolution.

TABLE 71. 4-BIT DAC—TEMPERATURE: –20°C TO +70°C

Parameter	Minimum	Typical	Maximum	Units
Resolution	—	4	—	bit
Integral non-linearity	—	0.25	0.5	LSB
Differential non-linearity	—	0.25	1	LSB
Settling time (1/2 LSB)	—	—	25	ns
Output voltage range	—	0.2 AV_{DD} to 0.6 AV_{DD}	—	V
Resistive output load	—	330	—	Ohm
Capacitive output load	—	25	—	pF

9.4 INPUT/OUTPUT PIN CHARACTERISTICS

All digital pins (except V_{DD}, AV_{DD}, GND, AGND, V_{REF}, RX, TX and PWLV) exhibit an internal capacitance of 7 pF. The RX analog input pin exhibits an input capacitance of 1.5 pF. The RSSI analog input pin exhibits an input capacitance of 7 pF.

TABLE 72. 1-BIT ADC—TEMPERATURE = –20°C TO +70°C

Parameter	Min	Typical	Maximum	Units
Input Voltage Range	250	350	AV_{DD}	mV
Input Resistance	10	18	25	kOhm
Input Capacitance	—	10	—	pF

10. TIMING DESCRIPTION

TABLE 73. CLOCKS, RESET, AND RF INTERFACE—PER STANDARD TEST CONDITIONS UNLESS OTHERWISE SPECIFIED

No.	Symbol	Parameter	Min	Max	Units
1	TpC	MCLK input clock period[1]	61	61	ns
2	TwC	MCLK input clock pulse width	26	35	ns
3	TrC, TfC	MCLK input clock rise/fall time		15	ns
4	TrRFC, TfRFC TrCC, TfCC, TrCO, TfCO	RFCLK, P2CLK, CODCLK output rise/fall times	2	15	ns
5	TwR	RESET input Low width	18		TpC
6	TrRF, TfRF	RF output controls rise/fall time[2]	2	15	ns
7	Trd	External ROM READ cycle time[3]	122	122	ns
8	Tacc	External ROM address to data access time[3]		90	ns
9	FSCL	Clock frequency, SERCLK[4]	0	100	kHz
10	TSCLl	SERCLK pulse width, low[4]	4.7		µs
11	TSCLh	SERCLK pulse width, high[4]	4.0		µs
12	TSDAOv	SERCLK Low to SERDAT out valid[4]	0.1	3.5	µs
13	TBUF	Intertransmission time[4]	4.7		µs
13	TSTAho	START hold time[4]	4.0		µs
15	TSTAsu	START setup time[4]	4.7		µs
16	TSDAIho	SERDAT in hold time[4]	0.0		µs
17	TSDAIsu	SERDAT in setup time[4]	50		ns
18	TSDAOho	SERDAT out hold time[4]	100		ns
19	TSDAIr	SERDAT in rise time[4]		1	µs
20	TSDAIf	SERDAT in fall time[4]		300	ns
21	TSCLr,TSCLf, TSDAOr, TSDAOf	Output signal rise/fall time[4]	2	6	ns
22	TSTOPsu	STOP setup time[4]	4.7		µs

NOTES:
1. MCLK is an external digital clock applied to the XTALIN pin in lieu of a crystal, frequency 16.384MHz ±25ppm.
2. RF Controls are RFEON, TXON, RXON, SYNDAT, SYNCLK and SYNLE.
3. The DSP is in Divide-by-2 mode @ 8.192 MHz.
4. Values shown are for reference only. The clock selection in Register 0, Bank 5 determines the final value.

10.1 VOICE PROCESSOR INTERFACE TIMING

The DSP1 is a peripheral device for the secondary processor or separate external voice processor. The interface, from the DSP1 perspective, is composed of an

input address bus, a bidirectional data bus, strobe and READ/WRITE input control signals, and a ready/wait output control signal.

READ cycles refer to data transfers from the primary to the secondary or external processor. WRITE cycles refer to data transfers from the secondary or external processor to the DSP1.

TABLE 74. VOICE PROCESSOR INTERFACE

Signal Name	Function	Direction
VXADR[2..0]	Address Bus	Voice Proc. to Primary Proc.
VXDAT[7..0]	Data Bus	Bidirectional
VXSTR	Strobe Control Signal	Voice Proc. to Primary Proc.
VXRW	READ/WRITE Control Signal	Voice Proc. to Primary Proc.
VXRDY	Ready Control Signal	Primary Proc. to Voice Proc.

TABLE 75. VOICE PROCESSOR INTERFACE TIMING—PER STANDARD TEST CONDITIONS UNLESS OTHERWISE SPECIFIED

No.	Symbol	Parameter	Min	Max	Units
28	TsAS	Address, READ/WRITE setup time before strobe falls	10		ns
29	ThSA	Address, READ/WRITE hold time after strobe rises	3		ns
30	TaDrS	Data READ access time after strobe falls		30	ns
31	ThDrS	Data READ hold time after strobe rises	8.5		ns
32	TwS	Strobe pulse width with WAIT state*	80		ns
33	TsDwS	Data WRITE setup time before strobe rises	10		ns
34	ThDwS	Data WRITE hold time after strobe rises	3		ns
35	TaDrRY	Data READ valid before Ready falls	22		ns
36	TdSRY	Strobe High after Ready falls	0		ns

NOTE: *Requires wait state on voice processor READ cycles.

10.2 CODEC INTERFACE TIMING

FIGURE 21. CODEC PROCESSOR INTERFACE TIMING—PER STANDARD TEST CONDITIONS UNLESS OTHERWISE SPECIFIED

No.	Symbol	Parameter	Min	Max	Units
37	CCLKsu	CODCLK setup time from P2CLK rise		18	ns
38	FSsu	FS0/FS1 setup time from CODCLK rise		7	ns
39	TXDsu	TXD setup time from CODCLK rise		9	ns
40	RXDsu	RXD setup time to CODCLK fall	9		ns
41	RXDho	RXD hold time from CODCLK fall	0		ns

FIGURE 22. CLOCKS, RESET, RF INTERFACE AND EXTERNAL ROM TIMING

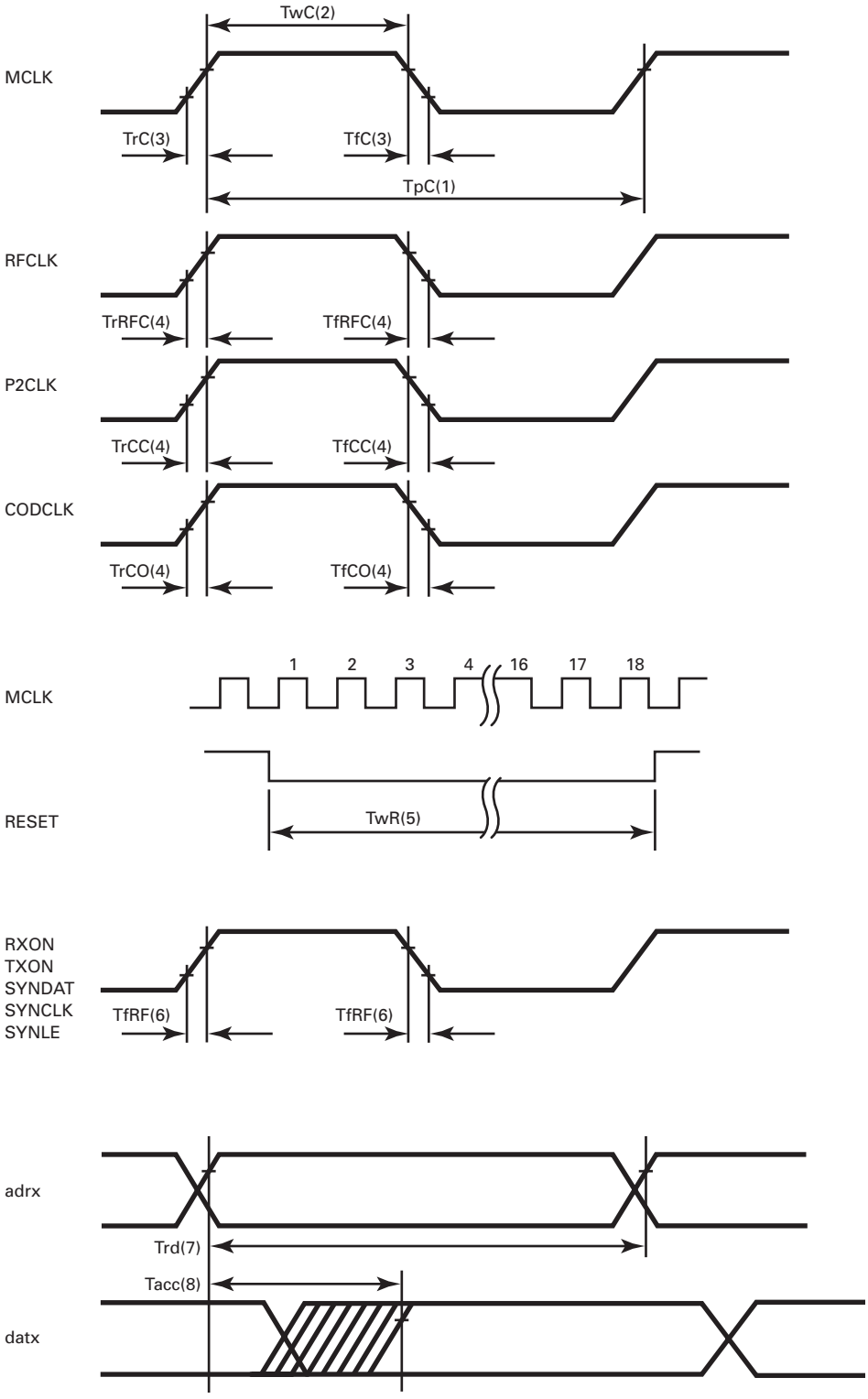


FIGURE 23. SERIAL INTERFACE AND FLASH PROGRAMMER TIMING DIAGRAMS

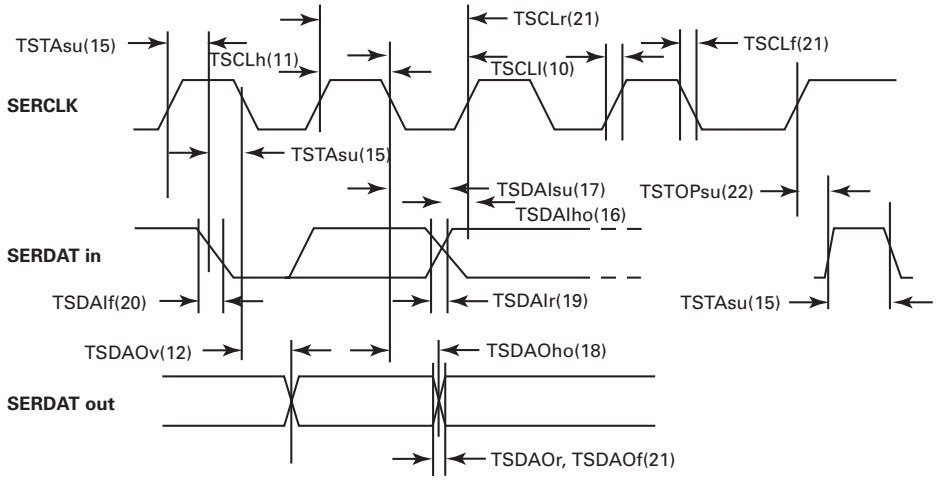


FIGURE 24. VOICE PROCESSOR INTERFACE BUS TIMING DIAGRAMS

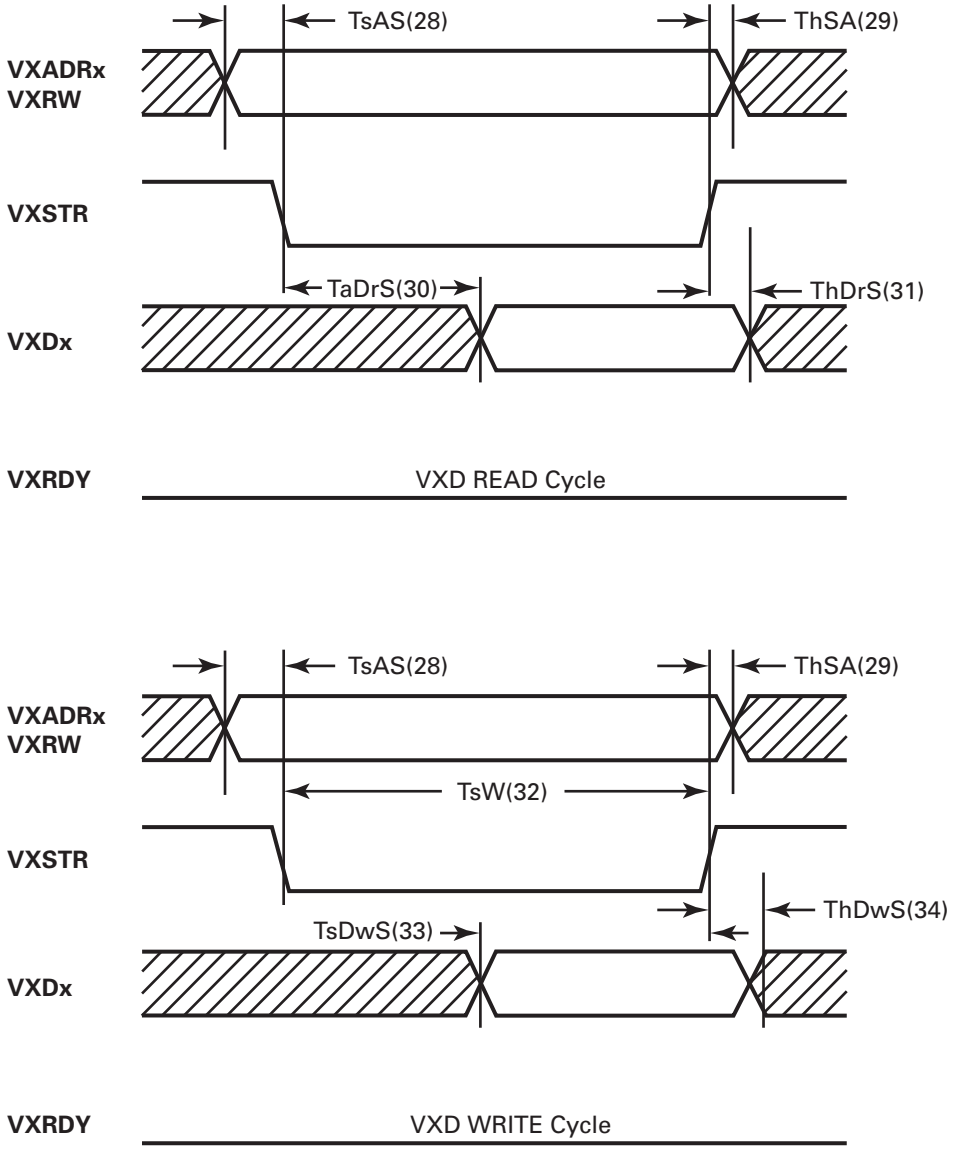


FIGURE 25. VOICE PROCESSOR INTERFACE BUS TIMING DIAGRAMS

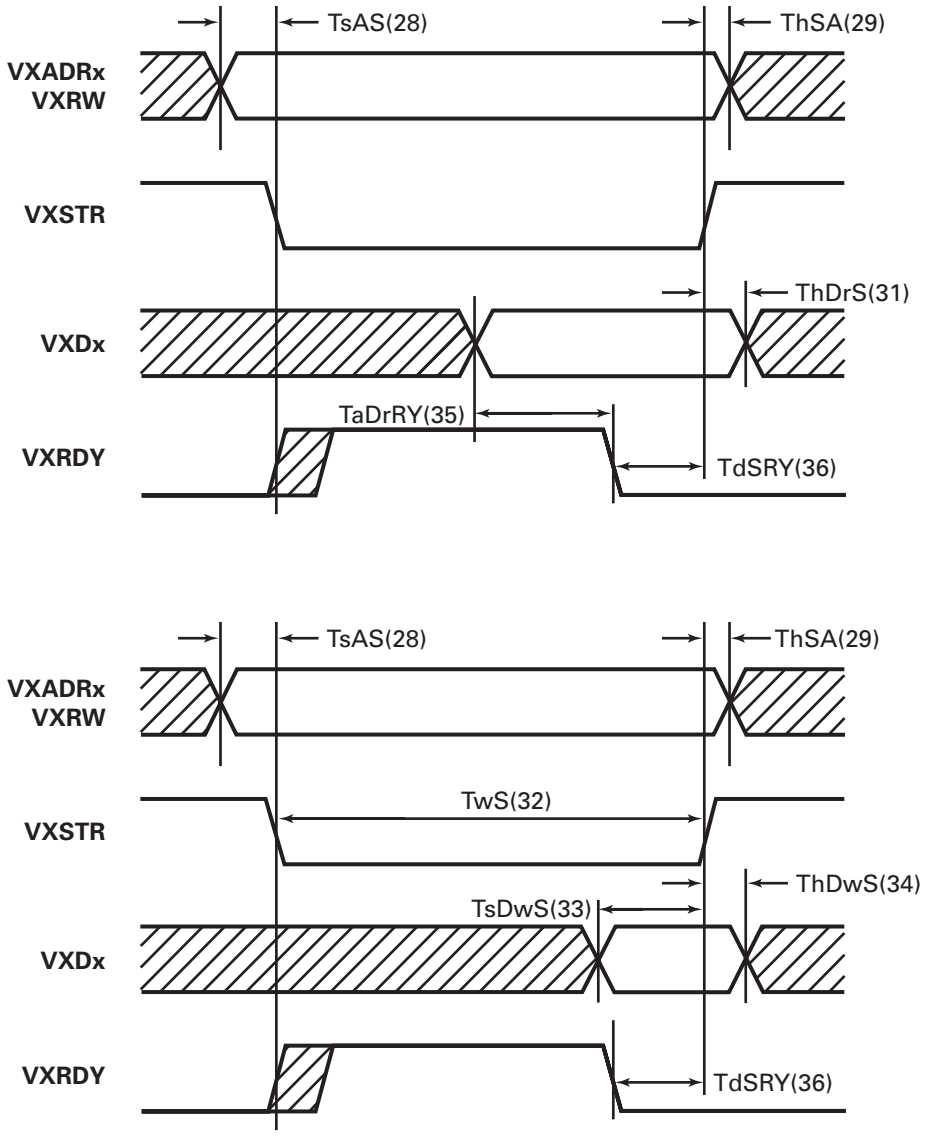
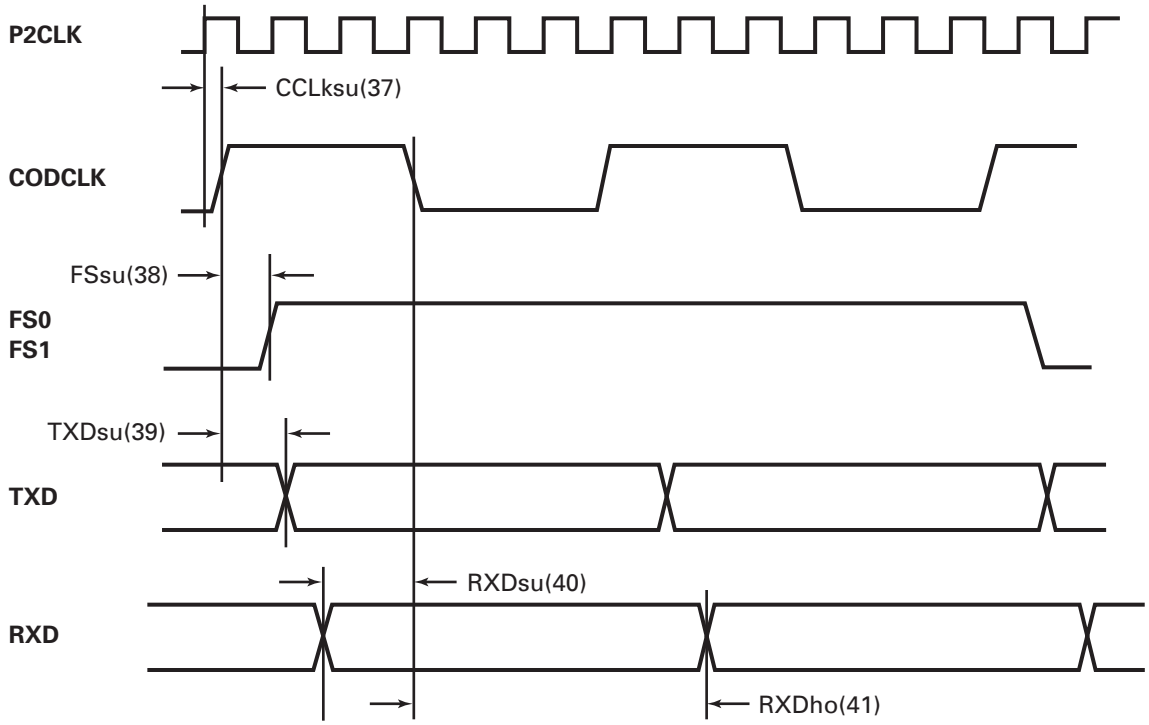


FIGURE 26. CODEC INTERFACE TIMING

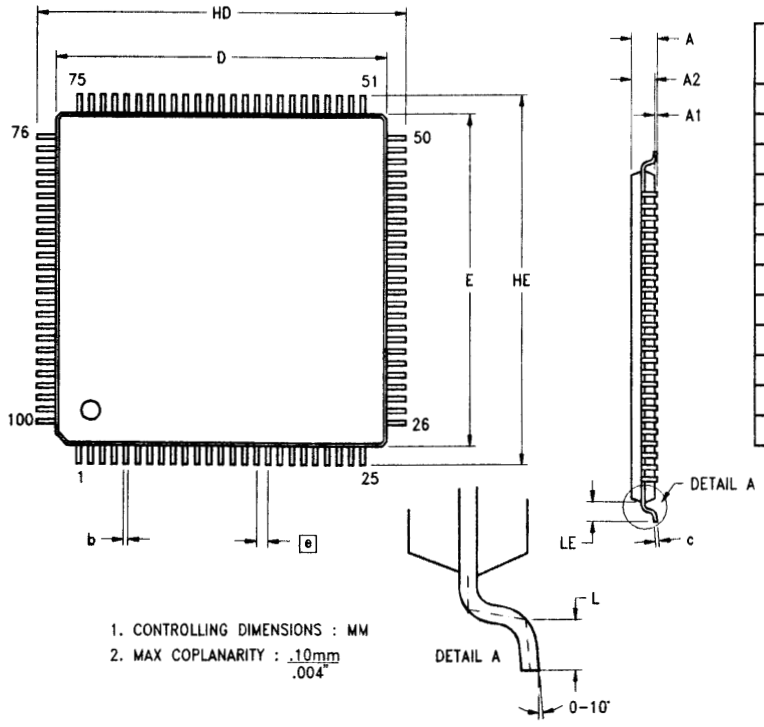


11. PACKAGING INFORMATION

TABLE 76. PACKAGING SPECIFICATIONS

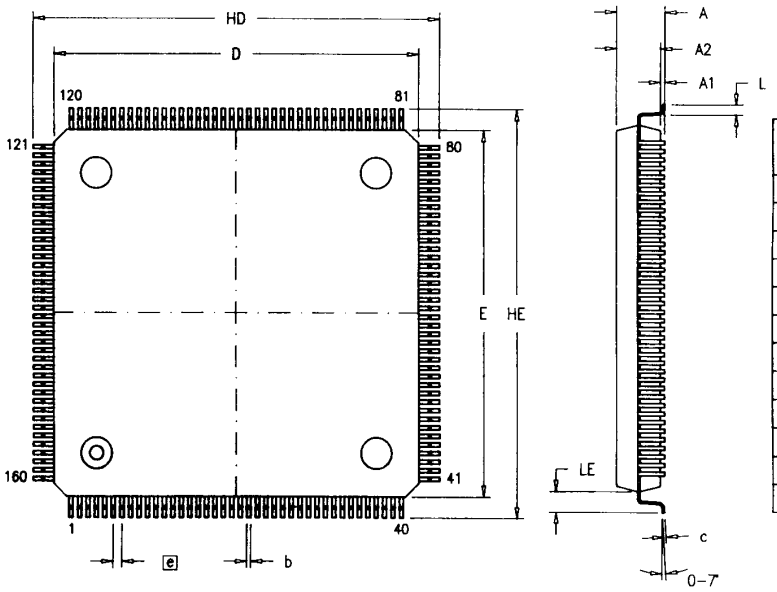
Part Number	Frequency	Temperature Range	Package Type	Pin Count	Voltage Range
Z87L0216ASC	16.384 MHz	–20°C to +70°C	VQFP	100	2.7V–3.3V
Z87L0916FSC	16.384 MHz	–20°C to +70°C	QFP	160	2.7V–3.3V
Z87L0316ASC	16.384 Mhz	–20°C to +70°C	VQFP	144	2.7V–3.3V
Z87L0216FSC	16.384 MHz	–20°C to +70°C	QFP	100	2.7V–3.3V

FIGURE 27. 100-PIN VQFP PACKAGE DIAGRAM



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.006	.010
c	0.10	0.20	.004	.008
HD	15.85	16.15	.624	.636
D	13.90	14.10	.547	.555
HE	15.85	16.15	.624	.636
E	13.90	14.10	.547	.555
e	0.50 TYP		.0197 TYP	
L	0.35	0.65	.014	.026
LE	0.90	1.10	.035	.043

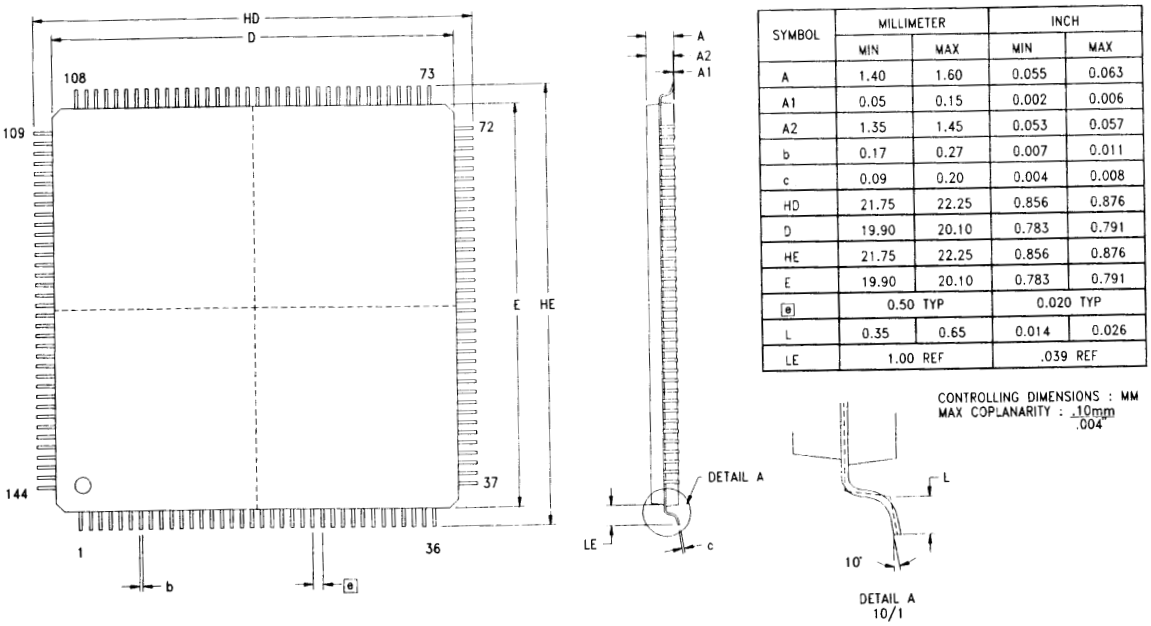
FIGURE 28. 160-PIN QFP PACKAGE DIAGRAM



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	–	4.07	–	0.160
A1	0.25	–	0.010	–
A2	3.17	3.67	0.125	0.144
b	0.23	0.38	0.009	0.015
c	0.13	0.23	.005	.009
HD	30.95	31.45	1.219	1.238
D	27.90	28.10	1.098	1.106
HE	30.95	31.45	1.219	1.238
E	27.90	28.10	1.098	1.106
e	0.65 TYP		.0256 TYP	
L	0.65	0.95	0.026	0.037
LE	1.60 REF		0.063	

1. CONTROLLING DIMENSIONS : mm
2. MAX. COPLANARITY : 10mm / 0.004"

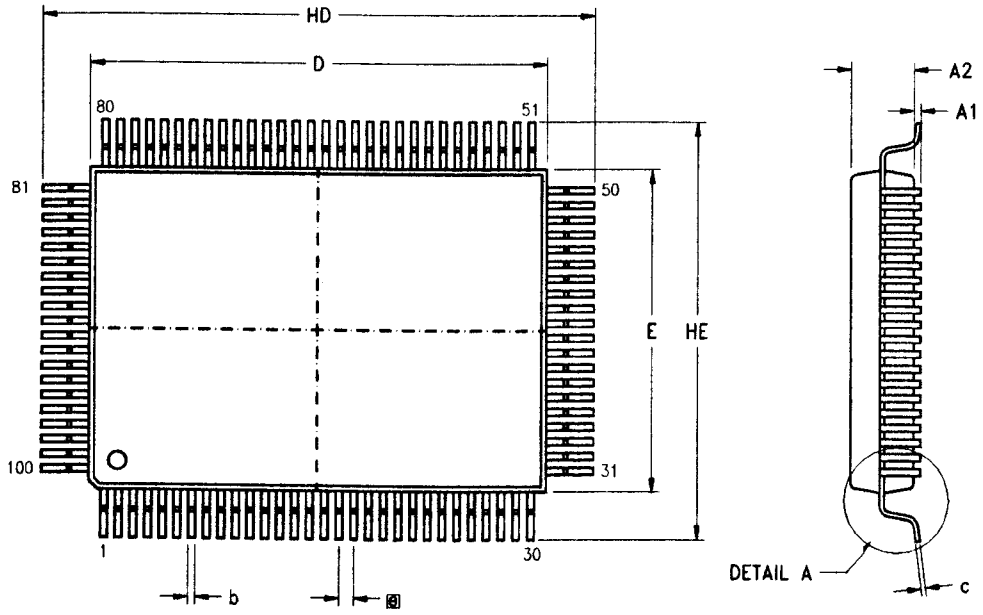
FIGURE 29. 144-PIN VQFP PACKAGE DIAGRAM



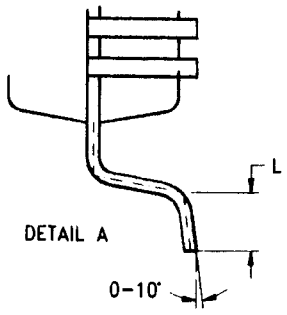
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
HD	21.75	22.25	0.856	0.876
D	19.90	20.10	0.783	0.791
HE	21.75	22.25	0.856	0.876
E	19.90	20.10	0.783	0.791
e	0.50 TYP		0.020 TYP	
L	0.35	0.65	0.014	0.026
LE	1.00 REF		.039 REF	

CONTROLLING DIMENSIONS : MM
MAX COPLANARITY : .10mm / .004"

FIGURE 30. 100-PIN QFP PACKAGE DIAGRAM



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.25	0.40	.010	.016
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.65 TYP		.0256 TYP	
L	0.70	1.10	.028	.043



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. MAX COPLANARITY : .10 / .004

12. ORDERING INFORMATION

Standard Temperature	
100-Pin QFP	Z87L0216FSC
100-Pin VQFP	Z87L0216ASC
144-Pin VQFP	Z87L0316ASC
160-Pin QFP	Z87L0916FSC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes	
Preferred Package	F = Quad Flat Pack
Longer Lead Time	A = Very Thin Quad Flat Pack
Speed	16 = 16 MHz
Standard Temperature	S = 0°C to +70°C
Environmental Flow	C = Plastic Standard

12.1 PART NUMBER DESCRIPTION

The ZiLOG part numbers consist of a number of components.

EXAMPLE: The Z87L0316ASC is a 16-MHz VQFP, 0ºC to 70ºC, with Plastic Standard Flow.

Z	ZiLOG Prefix
87	Wireless Product
L03	Product Number
16	Speed, in MHz
A	Very Thin Quad Flat Pack
SC	Temperature and Environmental Flow

13. PRECHARACTERIZATION PRODUCT

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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CUSTOMER FEEDBACK FORM

Z87L02/L03/L09 PRODUCT SPECIFICATION

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see Return Information, below). We also welcome your suggestions!

CUSTOMER INFORMATION

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

PRODUCT INFORMATION

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

RETURN INFORMATION

ZiLOG
System Test/Customer Support
910 E. Hamilton Avenue, Suite 110, MS 4–3
Campbell, CA 95008
Fax: (408) 558-8536
Email: tools@zilog.com

PROBLEM DESCRIPTION OR SUGGESTION

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

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