ZSBI050

OTP 555 TIMER

PRELIMINARY PRODUCT SPECIFICATION

PS002000-SEC1099

ZiLOG WORLDWIDE HEADQUARTERS • 910 E. HAMILTON AVENUE • CAMPBELL, CA 95008
TELEPHONE: 408.558.8500 • FAX: 408.558.8300 • INTERNET: HTTP://WWW.ZILOG.COM

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1. ARCHITECTURAL OVERVIEW

The ZSBI050 OTP Timer is a monolithic 8-pin CMOS mixed-signal integrated circuit. It is designed for applications which could utilize the industry-standard 555 timer. However, the in-circuit programming capabilities of the ZSBI050 offers the customer a clear advantage over traditional 555 timers. The ZSBI050 OTP Timer consists of 4 major blocks:

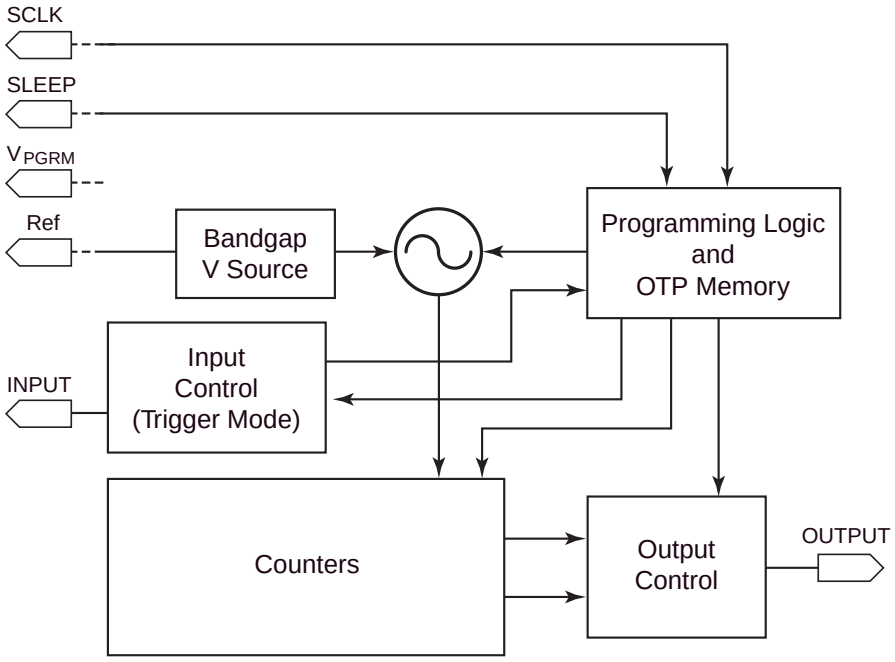
- Precision Oscillator
- Mode Control Logic
- Counter Timer
- One-Time Programmable Memory

1.1 ZSBI050 FEATURES

- Delay Times from Milliseconds to Days
- Only 1 External Resistor
- 3 Triggering Modes
- No External Potentiometer Required for Calibration
- In-Circuit Programming
- Variable Duty Cycle
- Small 8-pin SOIC or DIP Package

1.2 FUNCTIONAL BLOCK DIAGRAM

FIGURE 1. ZSBI050 BLOCK DIAGRAM



2. PIN DESCRIPTIONS

FIGURE 2. ZSBI050 8-PIN DIP AND SOIC DEVICES

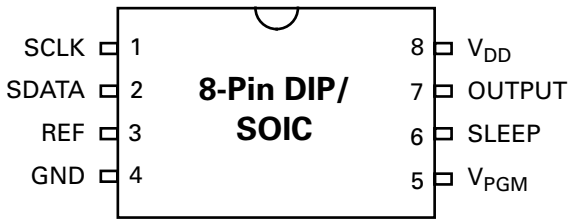


TABLE 1. PIN DESCRIPTION SUMMARY

Pin #	Pin Name	Pin Function	Direction	Minimum	Maximum
1	SCLK	Serial Clock	Input	–0.5 Volts	+5.5 Volts
2	SDATA	Serial Data I/O Monostable Trigger In	Input/Output	–0.5 Volts	+5.5 Volts
3	REF	External Resistor	Input	–0.5 Volts	+5.5 Volts
4	GND	Ground	Output	–0.5 Volts	+5.5 Volts
5	V_{PRGM}	OTP Program Voltage	Input	–0.5 Volts	+7.5 Volts
6	SLEEP	SLEEP Mode Input	Output	–0.5 Volts	+5.5 Volts
7	OUTPUT	Output	Input	–0.5 Volts	+5.5 Volts
8	V_{DD}	Voltage Supply	Input	–0.5 Volts	+5.5 Volts

3. OPERATIONAL DESCRIPTION

The ZSBI050 features an internal free-running oscillator, followed by several user-programmable divide-by-N counters. The output of these counters is gated by the various functions supported by the ZSBI050. The user may select either monostable or astable modes of operation. This device is programmed by shifting a 35-bit control word into the internal holding register of the ZSBI050 and enabling the write control to permanently characterize the device. Prior to writing the control word, the ZSBI050 operates from the data stored in the holding register.

3.1 INTERNAL RC OSCILLATOR

The internal RC oscillator operates in a frequency range of 9 kHz to over 4 MHz, depending on the value of the external resistor (see Table 2). An on-chip bandgap is driven into the external resistor, creating a constant current source for the RC oscillator.

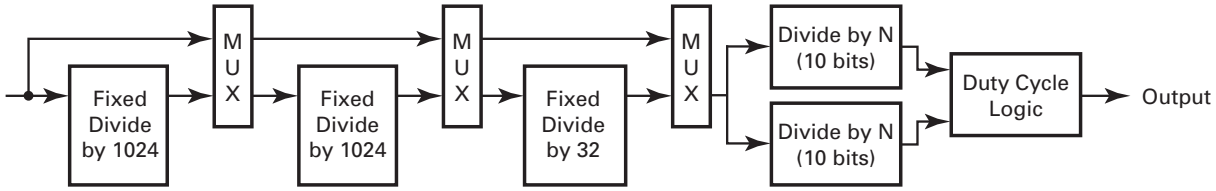
TABLE 2. EXTERNAL RESISTOR VALUE TO OPERATING FREQUENCY

R_{EXT} (kΩ)	Internal Oscillator Frequency (kHz)
0.993	4111.7
2.212	3671.2
3.35	3015.5
5.06	2320.1
7.43	1764.3
9.92	1413.9
12.88	1146.5
15.97	960.0
21.57	741.6
23.78	681.9
32.8	511.9
35.8	472.8
42.6	404.0
67.4	264.8
74.4	241.8
103.0	178.3
128.2	129.1
157.7	112.7
277.6	69.6
509	37.7
997	20.2
2200	9.09

3.2 COUNTER TIMER

The counter timer block divides the clock source from the precision oscillator into the required output frequency or delay. The counter timer block consists of 5 dividers. Two of the blocks are 10-bit programmable divide-by-N counters that run in parallel. These blocks set the primary divider and duty cycle. The remaining 3 blocks are fixed divisors of 1024, 1024, and 32. Each of the fixed divisions can be bypassed.

FIGURE 3. COUNTER TIMER BLOCK DIAGRAM



3.3 MODE CONTROL LOGIC

The mode control logic features the following miscellaneous control and timing logic:

- Serial input shift registers
- Programming logic
- Mode control logic
- Power-on reset

3.3.1 Serial Input Registers

Prior to programming bit `0` (the PROGRAM DISABLE bit), the ZSBI050 operates from the data contained in the input registers. When bit `0` is programmed, the device operates from the values programmed into OTP memory. Data is shifted into the serial input register via the SDATA pin.

3.4 OTP MEMORY

When the required operation for the ZSBI050 is selected, the device can be permanently programmed. This programming is achieved by physically burning the fuse contained in the memory block. This block contains the 35 fuses that set the mode, timing and divider chain in `N` values. When a fuse is programmed, the programming cannot be changed or erased.

3.5 OPERATING CHARACTERISTICS

Configuring the ZSBI050 requires 2 values: the necessary output mode and the required delay or frequency. After determining these values, the device is ready to program. A series of fixed and variable dividers determines the delay, which is approximated by the following equation:

$$t_d = 3\mu s(N_{prim})(2^{10})^{b_{21}}(2^{10})^{b_{22}}(2^5)^{b_{23}}$$

where N_{PRIM} is the primary delay value and K is the enable bit (1 or 0) for the fixed dividers. These enable bits are stored in bit locations 21–23 of the configuration word. The basic delay (t_d) described above is the foundation for each of the ZSBI050's 4 operating modes.

An example design, calling for a 25–ohm external resistor to bias the onboard oscillator, results in a base frequency of 600 kHz, which allows for a minimum output timing of 7 µs (no dividers enabled) and a maximum timing of 66 hours (all dividers enabled). If smaller or larger counting times are required, the user can modify the external resistor to change the oscillator frequency, which modifies the allowable timing.

The ZSBI050 goes into SLEEP mode when the SLEEP pin is driven to logical 1. Under SLEEP mode conditions, the internal oscillator and all digital circuitry are powered down, resulting in lower current draw.

3.6 OPERATING MODES

The ZSBI050 supports either monostable or astable modes of operating. Table 3 indicates a list of all supported modes.

TABLE 3. SUPPORTED OPERATING MODES

Monostable Oscillator		Astable Oscillator	
Retriggerable	Nonretriggerable	50/50 duty cycle	Variable duty cycle
Rising-edge trigger	Rising-edge trigger	Free running	Free running
Falling-edge trigger	Falling-edge trigger	Gated input	Gated input
Trigger on both edges	Trigger on both edges		

3.6.1 Mode Selection

Mode selection is performed by programming bits 24, 25, 28 and 29. Table 4 indicates the modes that can be selected with these bits.

TABLE 4. MODE SELECTION

Bit 24	Bit 25	Bit 28	Bit 29	Value	Description
X	X	0	0	Astable	50/50 duty cycle oscillator
X	X	1	0	Astable	Variable duty cycle oscillator
0	0	0	1	Retriggerable Monostable	Rising edge
1	0	0	1	Retriggerable Monostable	Falling edge
X	1	0	1	Retriggerable Monostable	Both edges
0	0	1	1	Nonretriggerable Monostable	Rising edge

NOTE: X = "Don't care".

TABLE 4. MODE SELECTION (CONTINUED)

Bit 24	Bit 25	Bit 28	Bit 29	Value	Description
1	0	1	1	Nonretriggerable Monostable	Falling edge
X	1	1	1	Nonretriggerable Monostable	Both edges

NOTE: X = "Don't care".

3.6.2 Astable Multivibrator

Programmable Fixed Frequency Oscillator. The normal oscillator mode produces a square wave with a period equal to the programmed delay and a 50% duty cycle. There is also an output gating function, in which the SDATA pin can be used to force the output to 0. After returning SDATA to 1, the timer resets and outputs a full period, not a randomly-truncated period. The output frequency for this mode is calculated as follows:

$$F_{OUT} = \frac{F_{OSC}}{(2N_{PRIM} + 4) \times K}$$

where K is the product of all fixed dividers.

Variable Duty Cycle Oscillator. The duty cycle of the VARIABLE DUTY CYCLE oscillator mode is equal to the ratio of the secondary divider to the primary divider. This method allows the timer to set the duty cycle with a precision of up to 0.1%. Unlike the normal oscillator mode, however, the period of the variable-duty cycle output is half that of the delay resulting from the above equation. Output gating is possible as described in the Serial Input Registers section. The output frequency for this mode can be calculated as follows:

$$F_{OUT} = \frac{F_{OSC}}{(2N_{PRIM} + 4) \times K}$$

$$\text{Duty Cycle} = \frac{N_{PRIM} - N_{DUTY}}{N_{PRIM} = 2}$$

where K is the product of all fixed dividers.

3.6.3 Monostable Multivibrator

The monostable mode sets the timer to function as either a retriggerable or a nonretriggerable monostable multivibrator. The pulse width of the monostable output is equal to half of the delay, as shown in the equation that follows. The trigger input is the SDATA pin, and triggering occurs on a rising edge, a falling edge or both edges as dictated by the configuration word. Because SDATA is used as the triggering input, no output gating is possible in monostable mode. The output period can be calculated as follows:

$$T_{OUT} = T_{OSC}(N_{PRIM} + 4) \times K$$

where K is the product of all fixed dividers.

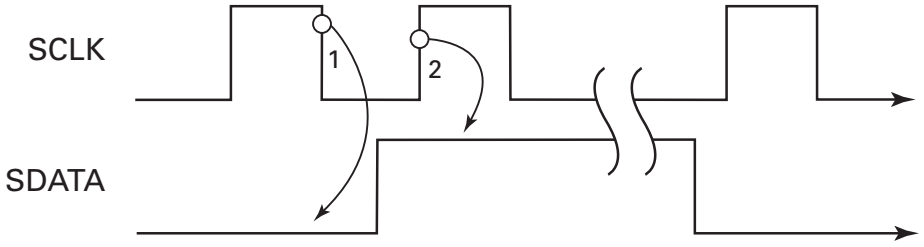
3.6.4 Communication Modes

The SCLK and SDATA lines are used to clock data into and out of the ZSBI050. Both the phase and the level of the SCLK line control the function of the SDATA line as follows:

1. To load the input registers:

   The rising edge of SCLK shifts the value of SDATA into the holding registers. The SDATA line must not change while the clock is High (Figure 4).

FIGURE 4. SERIAL DATA INPUT



NOTES:

1. SCLK must be Low when SDATA changes.
2. SDATA must be stable when SCLK changes.

2. To enable PROGRAMMING mode:

   While the SCLK line is High, raise the SDATA line. As a result, the ZSBI050 enters PROGRAMMING mode.

3. To read fuse data:

   Prior to burning bit `0` (the PROGRAM DISABLE bit) fuse, read the data by writing a single logical `1` into bit location `35`, and follow by writing 34 logical `0`s. When this action is performed, the SDATA line becomes an output, and the value of the fuses can be read. 1 bit is presented at the SDATA line for each rising edge of SCLK.

3.7 NORMAL OPERATING CONDITIONS

Unless otherwise specified, the device shall operate nominally under any combination of the conditions indicated in Table 5.

TABLE 5. OPERATING CONDITIONS

Operational Voltage	4.5–5.5 V_{DD}
V_{PRGM}	OTP Program Voltage: –0.5 Volts to +7.5 Volts
Temperature	Operating and storage: –40 to +85 °C

3.8 NON-OPERATING CONDITIONS

Under conditions outside those described in this section, the unit is not expected to operate and may become damaged.

4. CONTROL REGISTERS

TABLE 6. CONTROL REGISTERS

Control Word Bits	Program Value	Usage
0	Memory Protect Flag	This bit is set to 1 when all other bits are programmed. After this bit is programmed, no further programming of the ASIC memory is allowed.
10:1	Duty Cycle	The 10-bit value that sets the duty cycle of the oscillator (enabled only in VARIABLE DUTY CYCLE mode)
20:11	Primary Divider Value	The 10-bit value sets the interval between output pulses in conjunction with fixed dividers.
22:21	Fixed Divider Enable	Each bit enables a fixed divider of 2^{10}.
23	Fixed Divider Enable	The bit enables a fixed divider of 2^{5}.
24:25	Trigger Select	2-bit value sets TRIGGER mode: 00: Rising Edge 01: Falling Edge 1x: Both Edges
26	Binary 0	Reserved; must be 0.
27	Binary 1	Reserved; must be 0.
29:28	Mode Select	This 2-bit value sets the mode of operation: 00: Normal Oscillator 01: Variable Duty Cycle Oscillator 10: Retriggerable Monostable 11: Nonretriggerable Monostable
34:30	Binary 00011	Reserved; must be 0.

5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

TABLE 7. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+85	°C	
Storage Temperature	–40	+85	°C	
Voltage on V_{DD} pin with respect to GND	–0.5	+5.5	V	
Total Power Dissipation		175	mW	
Maximum Current into V_{DD}		32	mA	
Input Voltage	V_{SS}–0.5V	V_{DD}+0.5V	V	
Maximum Current into an Input Pin	–10	+10	µA	
Output Short Circuit Duration		3	sec	
Supply Voltage		5.5		
Supply Current		32	mA	
ESD Protection		2	kV	1

NOTE:
1. Mil. Std. 883C, Method 3015.7.

5.2 DC CHARACTERISTICS

TABLE 8. DC CHARACTERISTICS—TEMPERATURE RANGE (T_A) = 0°C TO +70°C

Symbol	Parameter	V_{DD}	Min	Typical @ 25°C	Max	Units	Conditions
C_{REF}	Reference Capacitor	5.0V	50.0		1000	pF	
R_{REF}	Reference Resistor	5.0V	1.0		2200	kΩ	
F_{OSC}	RC Oscillator Frequency Range	5.0V	20		4000	kHz	Set by the resistor on the OSC pin.
I_{CC}	Supply Current	5.0V			32	mA	
I_{IN}	Input Current	5.0V			400	pA	
I_O Source	Output Current	5.0V	27			mA	
I_O Sink	Output Current	5.0V	37				
V_{PROG}	V_{PROG} voltage while burning fuse	6.0V	6.5		7.5	mA	
I_{PROG}	Current Draw into V_{PROG} while burning fuse	5.0V	10		30	mA	
T_{PROG}	Time required to burn fuse	5.0V			10	msec	

Notes:
1. The normal operating voltage (V_{DD}) range is: 4.5V–5.5V.
2. GND = 0V.

TABLE 8. DC CHARACTERISTICS—TEMPERATURE RANGE (T_A) = 0°C TO +70°C (CONTINUED)

Symbol	Parameter	V_{DD}	Min	Typical @ 25°C	Max	Units	Conditions
t_d	Temperature Drift	5.0V	–1		+1	%	
TK_{OSC}	K_{OSC} Absolute Accuracy	5.0V	–20		+20	%	
T_{PON}	Delay from power-up until ASIC is guaranteed to operate	5.0V			50	msec	
T_{HALT}	HALT mode recovery time	5.0V			50	msec	

Notes:
1. The normal operating voltage (V_{DD}) range is: 4.5V–5.5V.
2. GND = 0V.

6. PROGRAMMING OVERVIEW

The ZSBI050 is controlled by 35 bits of nonvolatile memory. These bits are shifted into an internal holding register, which functions like nonvolatile memory during calibration and testing. When the program characteristics are determined, the data is burned into internal memory. An optional PROGRAM DISABLE bit is provided to lock the device from being further modified.

The unprogrammed state of the internal memory is a logical `0`. Therefore, only logical `1`s require programming into the ZSBI050's memory. Due to power limitations, only 1 bit can be programmed at a time. Therefore, the programming cycle must be repeated for each logical `1` programmed.

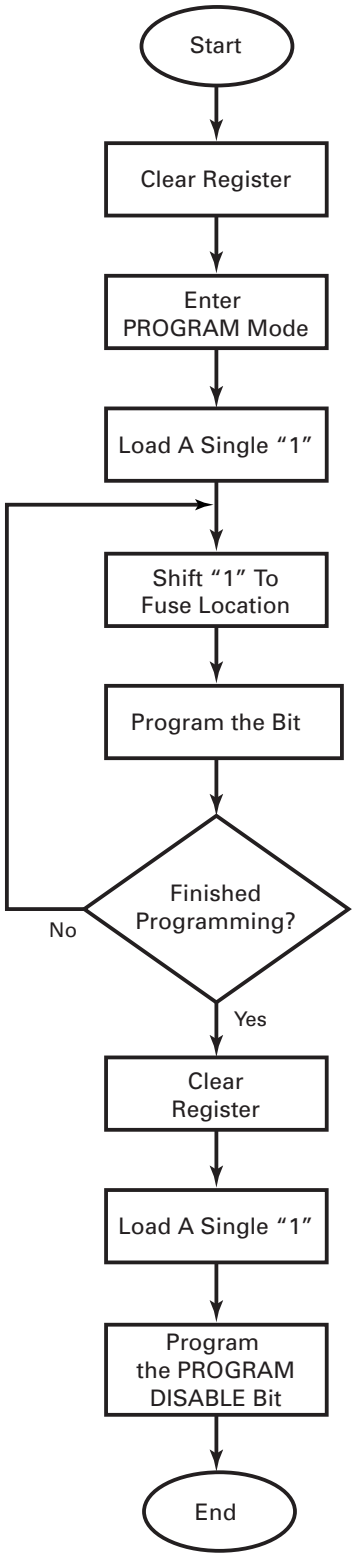
As stated above, the ZSBI050 operates from the temporary holding register until programmed, allowing the user the ability to *calibrate* the device as necessary until the required frequency is obtained.

The ZSBI050 supports one-time in-circuit programming of the internal memory. The Programming section that follows is a summary of the programming steps.

6.1 PROGRAMMING

To prevent damaging the ZSBI050, only 1 fuse can be programmed at a time. To perform this programming, clear the holding register and load a single logical `1` into the bit location to be programmed. Figure 5 illustrates a step-by-step description of the process.

FIGURE 5. PROGRAMMING FLOW DIAGRAM



To setup programming, perform steps 1–3:

1. Apply power to the chip
2. Bring SCLK and SDATA to a logical 0 and V_{PRGM} to Ground.
3. Clear the internal holding register:
   a. Shift 35 logical 0s into the ZSBI050.
   b. Always force SCLK Low before changing the state of SDATA.

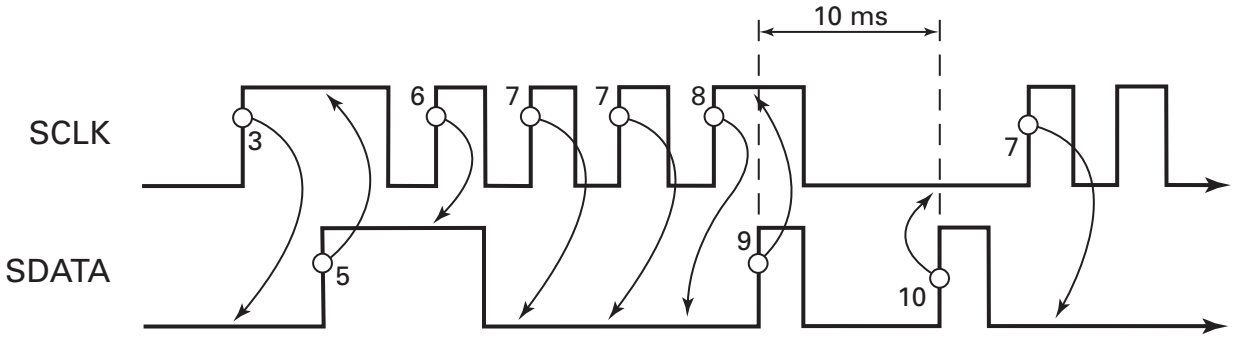
NOTE: All transitions are edge-triggered. A minimum of 10 µs of setup and hold time must be maintained.

To perform the Program Sequence, follow steps 4–13:

4. Apply 7.0 V_{DC} to the V_{PRGM} pin. The current on this pin should be limited to 50 mA. *Only 1 fuse can be programmed at a time.*
5. While the SCLK line is High, raise the SDATA line. The 0 to 1 transition of the SDATA line, while the clock is a logical 1, starts the programming cycle.
6. Write a single logical 1 into the ZSBI050.
7. Shift the logical 1 into the correct bit location by loading a series of logical 0s until the logical 1 is shifted into the bit position to be programmed.

   NOTE: Bit 0 is the PROGRAM DISABLE bit and must be programmed last. No further programming is possible after bit 0 is programmed.

FIGURE 6. SERIAL TIMING PROGRAMMING SEQUENCE



8. Shift the last logical 0 and hold SCLK High.
9. With SCLK High, raise SDATA to start bit programming.
10. After 10 ms, the second rising edge of SDATA ends bit programming.
11. Repeat steps 7 through 13 until all bits are programmed.

Program the PROGRAM DISABLE bit by performing steps 12–13:

12. Repeat the cycle starting from Step 3 above (the CLEAR REGISTER bit). In step 7, program only bit 1 (the PROGRAM DISABLE bit) location.
13. Remove V_{PRGM} and V_{CC}. This action completes the programming cycle.

7. APPLICATION INFORMATION

Figures 7 and 8 illustrate an application for a design requiring a 1-minute time-out. The input is provided by an external switch, which may remain closed longer than 1-minute. However, the load (LED) must terminate after the time-out period.

The ZSBI050 OTP Timer's output remains High until the input is returned to a logical Low and the time-out period expires. However, the input must be capacitively-coupled. The ZSBI050 is programmed in a nonretriggerable mode with its input set to the negative edge. No external components are required for triggering.

For timing accuracy, the ZSBI050 OTP Timer must be calibrated with the 5 MΩ potentiometer. This test requires about 1 minute for each timer for which the potentiometer is adjusted. Several attempts must be made before the ZSBI050 OTP Timer is set for 1 minute. With the ZSBI050, the system can be calibrated, whereby a single output pulse with no delay is programmed into the divider by automated test equipment in less than 1 second. The correct `N` value can be calculated and programmed into the ZSBI050.

FIGURE 7. A SAMPLE NONRETRIGGERABLE APPLICATION

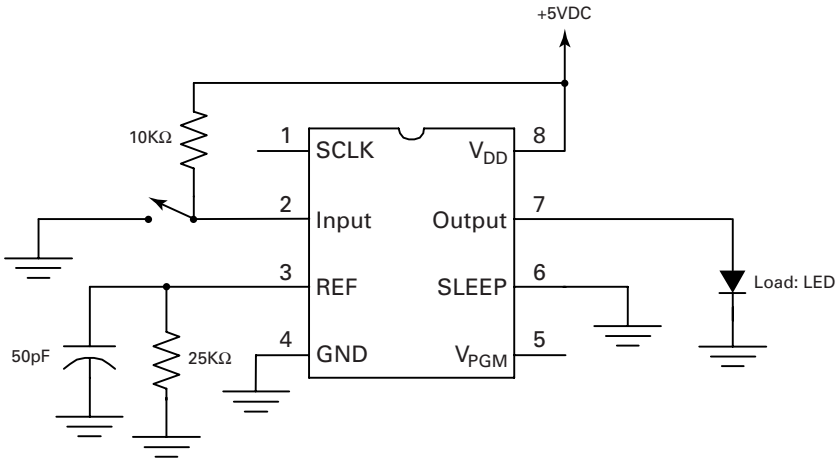
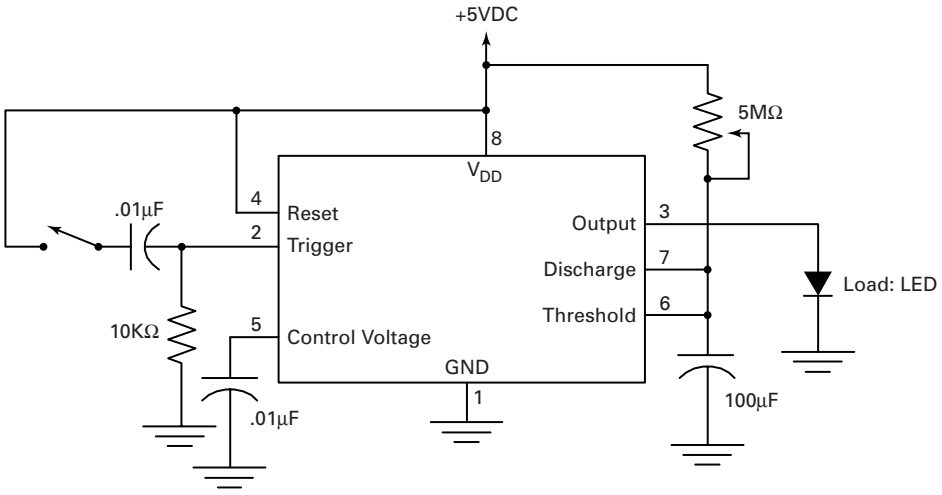


FIGURE 8. AN INDUSTRY-STANDARD 555 NONRETRIGGERABLE APPLICATION

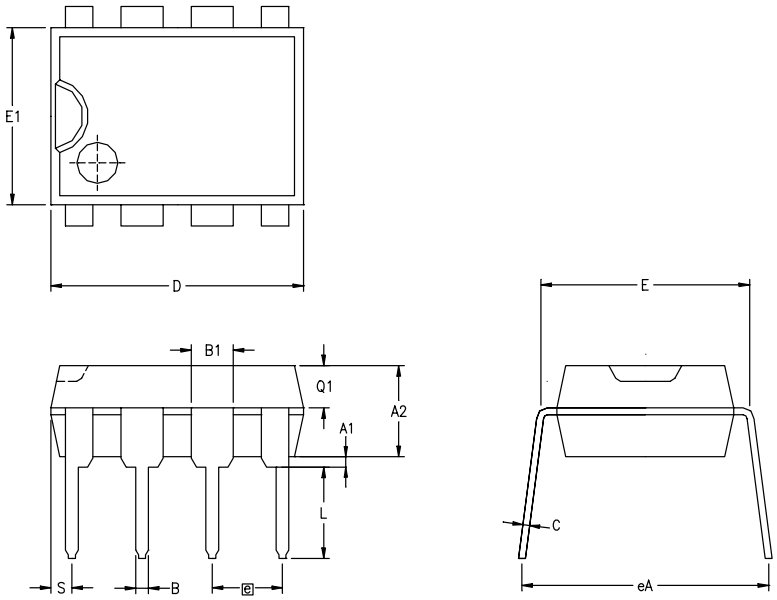


8. PRECHARACTERIZATION PRODUCT

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

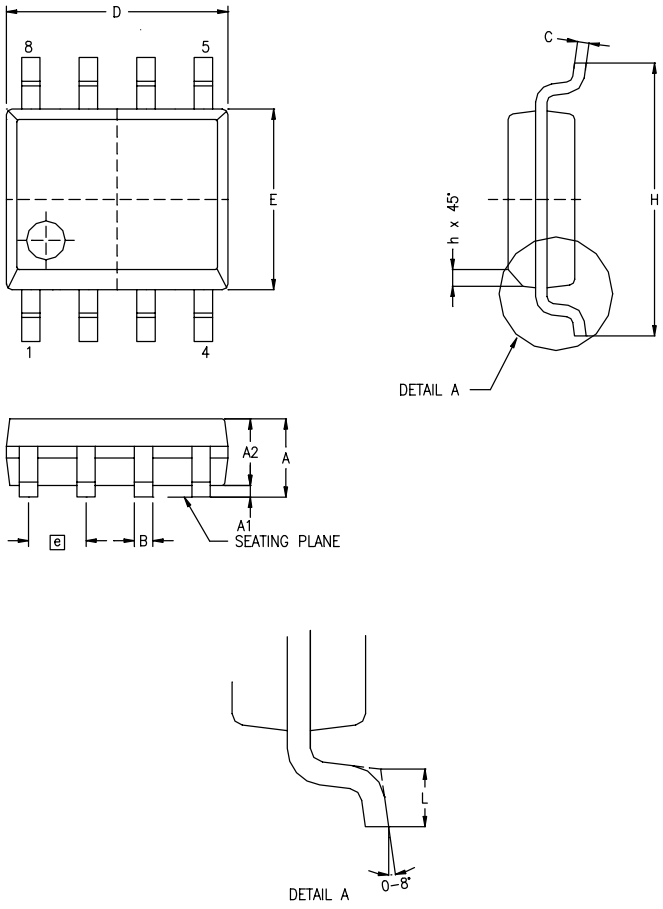
9. PACKAGING

FIGURE 9. 8-PIN PDIP PACKAGE



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	0.015	0.032
A2	3.25	3.43	0.128	0.135
B	0.38	0.53	0.015	0.021
B1	1.40	1.65	0.055	0.065
C	0.20	0.30	0.008	0.012
D	9.02	9.27	0.355	0.365
E	7.62	8.26	0.300	0.325
E1	6.20	6.58	0.244	0.259
e	2.54 BSC		0.100 BSC	
eA	7.87	9.14	0.310	0.360
L	3.18	3.43	0.125	0.135
Q1	1.40	1.65	0.055	0.065
S	0.64	0.89	0.025	0.035

FIGURE 10. 8-PIN SOIC PACKAGE



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.55	1.73	0.061	0.068
A1	0.10	0.25	0.004	0.010
A2	1.40	1.55	0.055	0.061
B	0.36	0.48	0.014	0.019
C	0.18	0.25	0.007	0.010
D	4.80	4.98	0.189	0.196
E	3.81	3.99	0.150	0.157
e	1.27 BSC		.050 BSC	
H	5.84	6.15	0.230	0.242
h	0.25	0.40	0.010	0.016
L	0.46	0.81	0.018	0.032

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

9.1 PHYSICAL DESIGN REQUIREMENTS

TABLE 9. PHYSICAL DESIGN REQUIREMENTS

Packaging Description	JEDEC Drawing MS-012—Plastic 8-lead gull-wing SOIC Body Width: 150 mils Lead Pitch: 50 mils
Package Construction	Solid package construction capable of allowing machine application of the ASIC with no degradation of performance. Lead integrity testing passes JEDEC Standard No. 22-B105-A. JEDEC default conditions are acceptable as minimum.
Solderability	ASIC passes JEDEC Standard No. 22-B102-A for Solderability. JEDEC default conditions are acceptable as minimum.
Solder Heat	ASIC provides resistance to solder heat consistent with current industry standards. No special preparation of specimen required.

9.2 TOP MARK

The Top Mark contains 3 lines, as follows:

Line 1	pZiLOG
Line 2	ZSBI050
Line 3	YYXXBB

Part number ZSBI050SZ000SC denotes a small-outline integrated circuit (SOIC), and ZSBI050PZ000SC denotes a plastic dual-inline package (PDIP).

Date code: Year (YY), week (XX), and lot coding (BB): YYXXBB

10. ORDERING INFORMATION

ZSBI050 Available Packages	
Standard Temperature	
8-Pin DIP	ZSBI050PZ000SC
8-Pin SOIC	ZSBI050SZ000SC

For faster results, contact your local ZiLOG sales offices for assistance in ordering the part(s) required.

Code Example	
Preferred Package	P = Plastic Dual In-Line Package
Longer Lead Time	S = Small Outline Integrated Circuit
Speed	Not Applicable
Standard Temperature	S = 0°C to +70°C
Environmental Flow	C = Plastic Standard

10.1 PART NUMBER DESCRIPTION

ZiLOG part numbers consist of a number of components. For example, part number ZSBI050PZ000SC is a ZSBI050 DIP that operates in the 0ºC to +70ºC temperature range, with Plastic Standard Flow. The ZSBI050PZ000SC part number corresponds to the code segments indicated in the following table.

Z	ZiLOG Prefix
SB	Security/Building Control
I	Interface
050	Product Number
PZ	Package
000	Analog Device
S	Temperature
C	Environmental Flow

11. DISCLAIMER

ZiLOG, Inc.
910 East Hamilton Avenue, Suite 110
Campbell, CA 95008
Telephone (408) 558-8500
FAX 408 558-8300
Internet: HTTP://WWW.ZILOG.COM

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