

ZFx86-TV™


Multimedia x86 PC Microcontroller



**ZF's PC-on-a-chip with on-chip
2D Graphics, and PAL/NTSC/RGB
Video Output**

Aimed specifically at Graphics/TV oriented applications, the ZFx86-TV™ microcontroller takes core x86 CPU functionality and combines it with a powerful multi-standard/multi-format 2D graphics engine and flexible output options. And as part of the ZFx86 Family of PC-compatible microcontrollers, you're assured of consistent tools, support and a future-safe product evolution.

Features

- Subset of traditional PC H/W features
- 2D Graphics Controller backwards compatible to SVGA
- PAL/NTSC, Y/C CVSB, and RGB, interlaced or non-interlaced
- Low power—four modes let you design power versus performance
- Low BOM cost—system level architecture minimizes integration complexity
- Long product life—process and packaging technology and roadmap ensure longterm availability† 
- Bundled S/W & firmware:
License for ZFx86-TV port of Phoenix Rev 4.0 Standard PC BIOS included with ZFx86-TV. Phoenix BIOS executable image, various RTOS evaluation packages†, Linux OS, and Windows CE evaluation package† are included in the ZF Micro Devices TV Integrated Development System.
- Patented ZF FailSafe H/W and S/W features unique to embedded market
- Proven industry standard architecture, both ISA and PCI fully implemented with minimal multiplexing

Low on Noise, Heat and Power

Drawing only 1.4W maximum and less than 500mW with APM, the ZFx86-TV is well suited to applications such as Internet Enabled Set-Top Boxes and Digital TVs where airflow for heat dissipation is restricted and heatsinks and fans are unacceptable.

ZFx86-Family Has The Lowest BOM Cost

Of prime importance in the design of any OEM product is the overall system cost in production. The ZFx86-TV architecture was created specifically to be cost-effective, allowing PC functionality and compatibility to be incorporated in high volume multimedia OEM products. The ZFx86-TV integrates a standard 5th generation x86 core, Synchronous DRAM controller, graphics subsystem, video pipeline, and support logic including PCI, ISA, and IDE controllers to provide a consumer orientated PC compatible subsystem on a single device. The device is based on a tightly coupled Unified Memory Architecture (UMA), sharing memory between the CPU, graphics and the video. The ZFx86-TV provides a subset of the traditional PC motherboard hardware functionality found in other members of the ZFx86 family, for a lower bill of materials cost than other solutions. ZFx86-family are the only devices that include a BIOS license (ZFx86 port of Phoenix Rev 4.0 Standard PC BIOS)†.

*Perfect For Set Top Boxes and
Graphic-rich Appliances*

Unique FailSafe™ System Features

PRELIMINARY

Long Product Life

ZF Micro Devices' goal is to serve our customers by providing stable, reliable products uniquely suited to the needs of the embedded and information appliance markets. We understand that many companies using embedded processors want to provide their products to their customers over an extended lifetime.[‡]

System Level Architecture

Designing a product with an embedded PC is not a trivial matter. The product architecture must be conceived of from the beginning as a system or delays in both software and hardware development are inevitable.

PC compatibility issues (both hardware and software) must be carefully considered because the consequences of any incompatibility can manifest themselves as field failures.

The ZF_{x86}-family of PC-compatible microcontrollers—including the ZF_{x86}-TV—incorporate the core features of a PC motherboard with all the most common peripherals and a number of enhancements developed by ZF exclusively for the embedded market. Ease of integration, reliability and failsafe operation in harsh environments were the guiding factors in the design process.

Bundled S/W & Firmware Completes PC "System"

Included with every ZF Micro Devices Integrated Development System are a Phoenix BIOS executable image, Windows CE Platform Builder evaluation[†] and disk image, various RTOS evaluation packages[†], and a full Linux OS (not a demo). A license for the ZF_{x86}-TV port of Phoenix Rev 4.0 Standard PC BIOS[†] is included with each device.

There are no licensing hassles, no porting, and no searching for drivers to support peripherals. Time-to-market is shortened and system reliability is increased.

Patented Embedded Features

FailSafe

Under certain conditions, power irregularities or other operating anomalies can corrupt an embedded design's flash memory and halt operation. The ZF FailSafe circuitry combined with an external ZF boot ROM allows system recovery if such a corruption takes place. This can even be achieved remotely when no operator is in attendance.

ZF-Logic

As increasing numbers of everyday devices incorporate computer intelligence, the microprocessor architecture knowledge required by system designers becomes more demanding. ZF-Logic allows access to X86 system architecture with a minimal amount of high-level microprocessor experience. ZF-Logic gives you simple and reliable control of chip selects and GPIO. Lower system integration costs are achieved because devices can be added to the ISA bus without external logic. The result is shorter time-to-market cycles and more reliable products.

Industry Standard Architecture Completely Implemented

The PC is the architecture of choice for embedded applications because of ease of software development, low manufacturing system cost and fast time-to-market. If the embedded processor selected is not fully PC compatible all these key measures of success can be lost. ZF_{x86}-TV provides a versatile combination of a high integration multimedia-ready device at the lowest BOM cost in the industry without sacrificing full PC compatibility. There are minimal multiplexed signals, no missing interrupts, and a limited complement of standard peripherals. It is the fastest, most cost-effective means of integrating PC motherboard functionality in an OEM product.

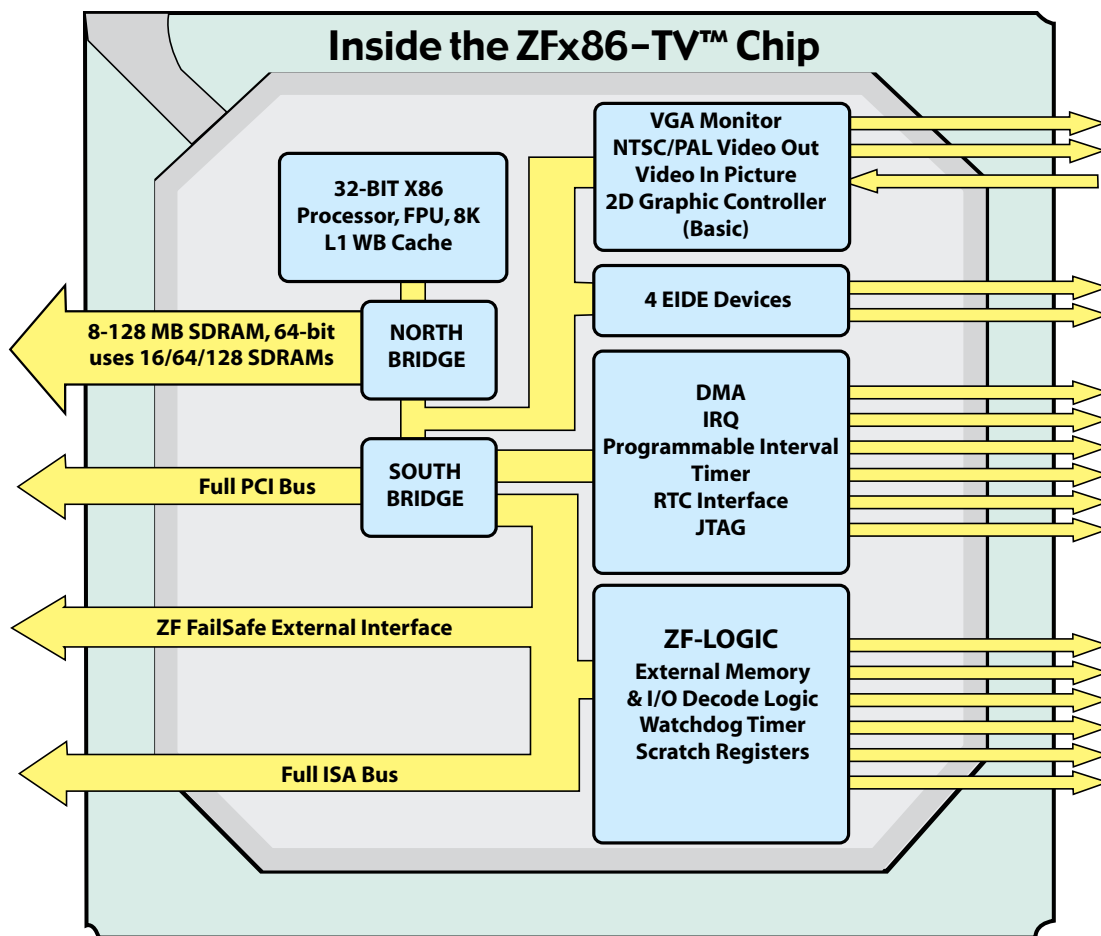
A high speed 5th generation x86 32 bit processor is married to a synchronous DRAM controller. A graphics engine and video processing block provide full 2-D multimedia support. The TV uses the Unified Memory Architecture (UMA), sharing memory between the CPU, graphics engine and video for good performance. An ISA bus brings with it all the well-understood ISA devices to help solve many of the potential challenges unique to embedded applications. Enhanced with such ZF proprietary embedded features as ZF-logic, 16 GPIO, ZTAG interface, and integrated ISA bus decoding, ZF_{x86}-TV allows for seamless and glueless system integration.

By combining the hardware and software needed to implement full PC compatibility in a single device, it lowers the exposure to development risks and significantly reduces time-to-market.

This unique ZF_{x86}-TV integrated design is ideal for applications that require multimedia support, computing intensive processes, low power consumption, high reliability and a small overall product size.

Accelerate Your Time-to-Market

PRELIMINARY— Contents Subject To Change



A True PC "System-on-a-Chip"

No processor— regardless of the level of integration, is a system until it boots. If it doesn't come with a fully implemented PC BIOS, and an operating system, it won't run. ZFx86-TV is a very complete System-on-a-Chip that includes the BIOS (externally) combined with FailSafe circuitry (in external ROM) that ensures your system will always be accessible.

Compatibility

The ZFx86-TV is fully compatible with all standard PC software. It will run any standard operating system capable of running on a fully compatible PC with FPU such as Linux, DOS, many RTOS, Windows CE, Windows 9x, and Windows NT.

Specifications *(continued next page)*

Processor Core

- ◆ Fully static 32-bit 5-stage pipeline, fully PC compatible.
- ◆ Floating point unit (FPU).
- ◆ 8KByte unified instruction and data cache with write back and write through capability.
- ◆ Parallel processing integral floating point unit, with automatic power down.
- ◆ Core clock speeds up to 100 MHz in x1 clock mode and 150 MHz in x2 mode.

2D Graphics Controller

- ◆ 64-bit windows accelerator.
- ◆ Backward compatibility to SVGA standards.
- ◆ Hardware acceleration for text, bitblts, transparent blts and fills.
- ◆ Up to 64 x 64 bit graphics hardware cursor.
- ◆ Up to 4MB long linear frame buffer.
- ◆ 8-, 16-, 24- and 32-bit pixels.
- ◆ Drivers available for various OSes.

CRT Controller

- ◆ Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz display.
- ◆ Requires external frequency synthesizer and reference sources.
- ◆ 8-, 16-, 24-bit pixels.
- ◆ Interlaced or non-interlaced output.

Video Input port

- ◆ Accepts video inputs in CCIR 601 mode.
- ◆ Optional 2:1 decimator
- ◆ Stores captured video in off setting area of the onboard frame buffer.
- ◆ Video pass through to the TV output for full screen video images.
- ◆ HSYNC and B/T generation or lock onto external video timing source.

Video Pipeline

- ◆ Two-tap interpolative horizontal filter.
- ◆ Two-tap interpolative vertical filter.
- ◆ Color space conversion (RGB to YUV and YUV to RGB).
- ◆ Programmable window size.
- ◆ Chroma and color keying for integrated video overlay.

Video Output

- ◆ NTSC-M; PAL-B, D, G, H, I, M, N encoding.
- ◆ 4 analog outputs in two configurations:
 - R,G,B + CVBS
 - C,Y5,CVBS1 + CVBS2
- ◆ Flicker-free interlaced output.
- ◆ Programmable two tap filter with gamma correction or three tap flicker filter.
- ◆ Interlaced or non-interlaced operation mode.
- ◆ Progressive to interlaced scan converter.
- ◆ Cross color reduction by specific trap filtering on luma within CVBS flow.
- ◆ Power down mode available on each DAC.

ZFx86-TV runs at a cool half Watt (average)—not a typical 8 to 10 Watts

COOL



PRELIMINARY— Contents Subject To Change

Specifications (continued)

SDRAM Controller

- ◆ 64-bit SDRAM (Synchronous DRAM) support—up to 100MHz.
- ◆ Integrated system memory, graphic frame memory and video frame memory
- ◆ 2MB up to 128 MB system memory, using 16-, 64- and 128-Mbit SDRAMs.
- ◆ Supports buffered, non buffered, registered DIMMs, in sizes of 8, 16, 32, 64, and 128 MB
- ◆ Supports up to 4 memory banks.
- ◆ 4-line write buffers for CPU to SDRAM and PCI to SDRAM cycles.
- ◆ 4-line read prefetch buffers for PCI masters.
- ◆ Programmable latency and programmable timing for SDRAM parameters.
- ◆ Supports -8, -10, -12, -13, -15 memory parts
- ◆ Supports memory hole between 1MB and 8MB for PCI/ISA busses.

PCI Controller

- ◆ Compliant with PCI 2.1 specification.
- ◆ Integrated PCI arbitration interface. Up to 3 masters can connect directly. External logic allows for greater than 3 masters.
- ◆ Translation of PCI cycles to ISA bus and ISA master initiated cycle to PCI.
- ◆ Support for burst read/write from PCI master.
- ◆ 0.25X, 0.33X and 0.5X Host clock PCI clock.

Full ISA Master/Slave

- ◆ Generates the ISA clock from either 14.318 MHz oscillator clock or PCI clock
- ◆ Supports programmable extra wait state for ISA cycles
- ◆ Supports I/O recovery time for back to back I/O cycles.
- ◆ Fast Gate A20 and Fast reset.
- ◆ Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- ◆ Supports flash ROM.
- ◆ Supports ISA hidden refresh.
- ◆ Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus.

EIDE Controller

- ◆ Compatible with EIDE (ATA-2).
- ◆ Backward compatibility with IDE (ATA-1).
- ◆ Supports up to 4 IDE devices
- ◆ Supports PIO and Bus Master IDE
- ◆ Supports up to Mode 5 timings
- ◆ Concurrent channel (PIO & DMA modes), 4 x 32-Bit Buffer FIFO/channel
- ◆ Support for 11.1/16.6 MB/s, I/O Channel Ready PIO data transfers.
- ◆ Support for 13.3/16.6 MB/s DMA data transfers.
- ◆ Bus Master with scatter/gather capability.
- ◆ Multi-word DMA support for fast IDE drives.
- ◆ Individual drive timing for all four IDE devices.
- ◆ Supports both legacy & native IDE modes.
- ◆ Supports hard drives larger than 528MB, CD-ROM, and tape peripherals.

Integrated Peripheral Controller

- ◆ 2X8237/AT compatible 7-channel DMA controller.
- ◆ 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- ◆ Three 8254 compatible Timer/Counters.
- ◆ Coprocessor error support logic.

Power Management

- ◆ Four power saving modes: On, Doze, Standby, Suspend.
- ◆ Programmable system activity detector
- ◆ Supports Intel & Cyrix SMM and APM.
- ◆ Supports STOPCLK.
- ◆ Supports 10 trap and restart.
- ◆ Independent peripheral time-out timer to monitor hard disk, serial and parallel ports.
- ◆ 128K SM_RAM address space from 0XA0000 to 0xB0000.

GPIO—16 General Purpose I/O

JTAG—Available at outside pins

Programmable GP-Clock—Programmable up to 135 MHz.

Electrical Characteristics—Dual voltage device — 5V tolerant, 3.0V to 3.6V I/O, and 2.25V to 2.75V core voltage

Mechanical / Environmental

- ◆ Standard Part—Up to 133Mhz (0 to +70°C) Ambient Temperature
- ◆ Package: 388-pin Plastic Ball Grid Array, 35mm x 35mm

FailSafe Boot ROM

- ◆ Can use off-chip code and static RAM to update software under adverse conditions
- ◆ Allows execution of multiple instruction sets: DRAM clear, Flash erase, executable load and run, etc.

ZF-Logic

- ◆ Programmable clock—Free running up to 135 MHz.
- ◆ External memory decode logic
 - Two memory mapped chip selects
 - Base address and size registers
- ◆ General Purpose Chip Select mapper
 - Four I/O mapped chip selects
 - Base address and size registers
- ◆ Boot strap register (can be set by external DIP switches)
 - Allows customized booting conditions
- ◆ Programmable interval timer

Z-Tag Interface

- ◆ High speed interface to download S/W
- ◆ Uses GPIO lines
- ◆ Communication protocol compatible with serial EEPROMs

Software Included with ZFx86-TV Integrated Development System

- ◆ Executable image of ZFx86-TV port of Phoenix Rev 4.0 PC BIOS
- ◆ Linux OS
- ◆ Microsoft Windows CE, and various RTOS Evaluation packages[†]

Software Compatibility

- ◆ Linux and DOS, Windows CE™, Windows™ 9x/ NT™
- ◆ Most PC-compatible RTOS

Ordering Information

- ◆ ZFx86BGA388 -TV— ZFx86-TV PC-on-a-Chip (Phoenix BIOS run-time license included).
- ◆ ZFx86TVIDS-K-01 — Integrated Development System for US. Includes board, case with power supply, hard disk, floppy and CD-ROM, cables, S/W, manuals, reference design and CAD files.
- ◆ ZFx86TVIDS-KE-01 — Integrated Development System for export outside the US (same contents).

[†] Customers of ZF Micro Devices products are responsible for obtaining any development tools and/or additional licenses required to support their specific applications

[‡] Full ZF Micro Devices Long Term Availability statement is available upon request

PRELIMINARY— Contents Subject To Change



Corporate Headquarters
1052 Elwell Court
Palo Alto, CA 94303
Toll Free: 1.800.683.5943
Tel: 1.650.965.3800
Fax: 1.650.965.4050
Email: info@zfmicro.com
For Sales Offices:
www.zfmicro.com

South American Office
Freire 2077 8° piso, "D"
Buenos Aires, Argentina
(1428)
Tel/Fax: +54.11.4543.0049