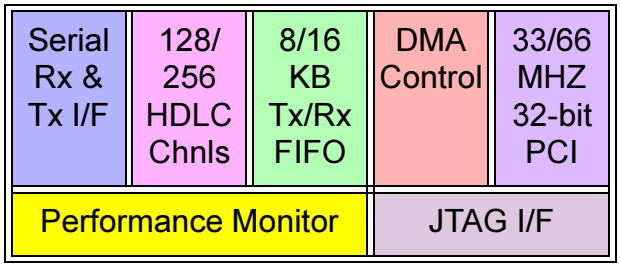
ZCC STEALTH

Communications Controller

PB005505-0801 **Preliminary Product Brief**

Product Block Diagram



Overview

The ZiLOG Communications Controller ZCC STEALTH is a standalone multi-channel HDLC communication controller that implements the logic required to interface with eight bidirectional communication links. It is used to process data in HDLC format, accommodate up to 256 different HDLC channels with a temporary storage buffer and to transfer bi-directional data to the PCI system memory. Essentially, the ZCC STEALTH is a single-chip PCI bus multi-channel HDLC controller.

You can select the operation mode that fits your particular application requirements. The modes are as follows:

- Base Mode—In this mode, the ZCC STEALTH is a multi-channel HDLC controller that supports 128 bidirectional channels in E1 and T1 data formats. To operate in Base mode, the EMODE signal must be low.
- Enhanced Mode—In this mode, the ZCC STEALTH is a multi-channel HDLC controller that supports 256 bidirectional channels in E1, 2E1, 4E1, T1, 2T1, 4T1 and H-MVIP (2 or 8 Mbps) data formats. To operate in Enhanced mode, the EMODE signal must be high and the ZMS bit must be set.

In Base and Enhanced modes, the ZCC STEALTH supports unchannelized HDLC data in transmit and receive directions. In addition, the ZCC STEALTH supports transparent (non-HDLC) data for channelized and unchannelized operation.

Features

The following list contains the main features of the ZCC STEALTH in Base Mode:

- 33MHz full-duplex operation
- Low-power CMOS technology
- 256-pin plastic ball-grid array (PBGA) package
- Serial Interface
  - Eight receive and eight transmit links
  - Links can be channelized (T1/E1) or unchannelized
  - Channelized links can have a maximum of 128 user (HDLC or Transparent) channels mapped in each direction
  - A maximum of 32 time-slots can be concatenated to form super-channels
  - Maximum throughput of 104Mbps over eight links during unchannelized operation when ZCLK is at 33MHz
  - Supports a maximum of 52MHz clock rate on links 0-2 and a maximum of 10MHz clock rate on links 3-7 during unchannelized operation
- HDLC
  - Supports all HDLC Layer 2 functions such as zero bit stuffing/destuffing, flag generation/detection, frame check sequence generation/detection, abort generation/detection, error detection (abort, long frame, CRC error, short frames, non-octet frame), etc.

  - Supports Transparent operation (HDLC controller bypassed)
  - Supports 64Kbps or 56Kbps channel format
  - Supports 2-level priority for packet transmission
- FIFO
  - 8KB transmit and receive FIFO
  - FIFO organized into 16-byte blocks, minimum of 3 blocks per channel
  - FIFO blocks can be chained, a maximum of 512 blocks per chain
- DMA
  - Efficient scatter-gather DMA
  - On-chip DMA descriptor reference table cache to minimize PCI bus accesses
  - Supports DMA descriptor bursting to conserve PCI bus bandwidth
  - Supports programmable transfer sizes for DMA receive and transmit
- PCI
  - PCI interface compliant with PCI Standard 2.2
  - Supports 2.5V and 3.3V PCI signaling environment
  - Supports a maximum of 128-byte PCI burst size for packet data transfers
- Programmable Performance Monitor logic with counter to monitor accumulate system events
- IEEE 1149.1 compliant JTAG interface

The ZCC STEALTH, in Enhanced Mode, contains the following additional features:

- 66MHz full-duplex operation
- Supports 2T1/E1, 4T1/E1 and H-MVIP links
- Supports a maximum of 32T1/E1 connections over eight links
- Frame synchronization can be achieved using external synchronization pulses or gapped clocks
- Programmable frame synchronization delay
- A maximum of 128 time-slots can be concatenated to form super-channels
- A maximum of 256 bi-directional HDLC channels are available for channelized operation
- 16KB transmit and receive FIFO

Architecture

The framework of the ZCC STEALTH is illustrated in Figure 1 and the main blocks are summarized below.

Serial Interface

The serial interface block can accept channelized or unchannelized data. When carrying channelized data, the time between two syncs is divided into a number of time-slots that are associated with a channel number. Data in the disabled channels is ignored. You can configure a maximum of 128 channels in Base Mode and 256 channels in Enhanced Mode. When carrying unchannelized data, all of the data on the link is assigned to one channel.

HDLC

The HDLC block performs HDLC protocol operations (layer 2 of OSI layers) on incoming and outgoing data. HDLC operations are the same for channelized or unchannelized data. This block performs general HDLC operations, such as the detection/insertion of Flag, FCS, Abort, and bit stuffing/destuffing. When carrying transparent data, no HDLC operations are performed and the data is passed directly to the FIFO.

FIFO

The FIFO block is a temporary storage buffer for channel data. The PCI Host determines the size of the buffer allotted to each channel, depending on the data rate of each channel. For maximum efficiency, the FIFO is divided into 16-byte blocks that are linked to form a larger buffer. In Base Mode, the maximum buffer size is 8K on transmit and receive and in Enhanced Mode it is 16K.

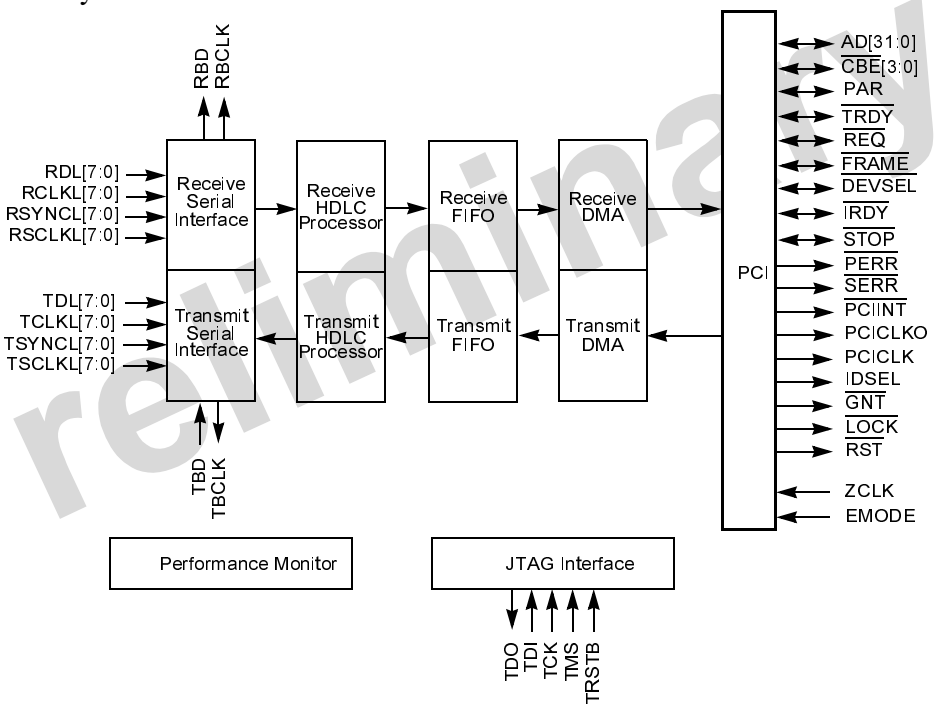


Figure 1. ZCC STEALTH Block Diagram

DMA

The DMA block consists of receive and transmit DMA engines. During packet transmission, if data in the transmit FIFO falls below the low-water mark, the transmit DMA requests a burst transfer of data to the FIFO through the PCI bus. Similarly, when a new packet is to be transmitted, it requests a burst transfer to fill the FIFO with the initial bytes of the new packet to be transmitted.

During packet reception, if data in the receive FIFO reaches the high-water mark, the receive DMA requests a burst transfer of data from the FIFO through the PCI bus. Similarly, when an end-of-packet is reached, it requests a burst transfer of the remaining bytes of data.

Performance Monitor

The performance of the ZCC STEALTH is monitored by this block. The performance monitor continuously checks various events and holds their status. The PCI Host retrieves the status information when needed.

PCI

The PCI acts as a master when servicing a DMA request. It arbitrates the requests between the receive and transmit DMA engines and provides sufficient buffering to support 128-byte bursts. The PCI acts as a slave (target) when the PCI Host is reading and writing the registers.

Applications and Support Tools

- ZCC Evaluation Board
- ZCC Configuration tool set for Window NT
- ZCC Configuration tool set for VxWorks

Related Products

Z85C30–Industry Standard Dual Channel Multiprotocol Serial Communications Controller

Z85230–Enhanced Serial Communications Controller

Z16C30–Dual Channel High Speed Serial Communications Controller

Ordering Information

The ZCC STEALTH can be ordered from ZiLOG referencing part number ZCC0256NP066SC, 66 MHz PCI, 256 PBGA. For more information regarding ordering, please consult your local ZiLOG sales office. The ZiLOG website at www.zilog.com lists all regional offices, as well as additional ZCC STEALTH product information.

Part Number	Description
ZCC0256NP066SC	66 MHz PCI, 256 PBGA ZCC with 256 HDLC channels and eight physical ports