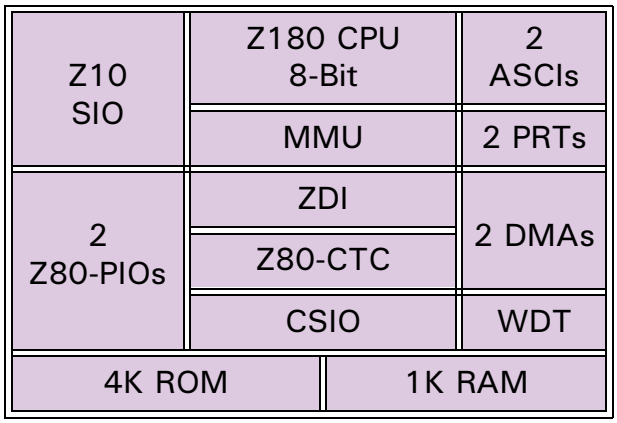
Z80S188
ENHANCED INTELLIGENT PERIPHERAL CONTROLLER

Product Block Diagram



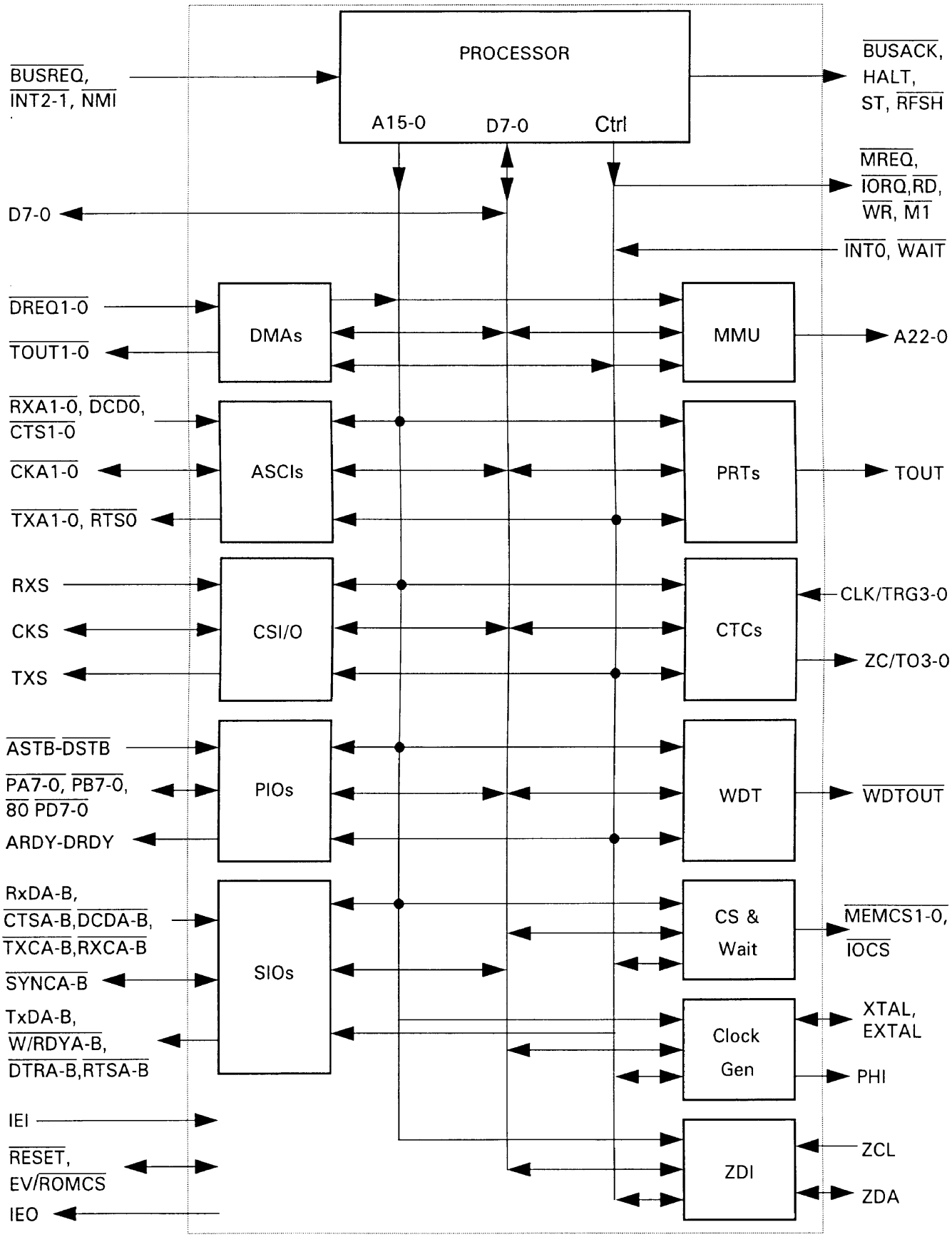
Features

- Code-compatible with Z80 and Z8x180
- Two multiprotocol serial I/O channels (Z80SIO)
- Four 8-bit parallel ports with handshake logic (2 Z80-PIOs)
- Four Counter/Timer channels (Z80-CTC)
- Two 16-Bit Programmable Reload Timers (PRTs)
- 4K ROM with security protection
- 1K RAM with security protection
- Enhanced Memory Management Unit (MMU) addresses up to 8 MB
- Two Direct Memory Access channels (DMAs)
- Two Enhanced UART channels (ASCIs)
- Clocked Serial I/O interface (CSI/O)
- Watch-Dog Timer (WDT)
- Chip Select and Wait-State generators
- Three Interrupt Request inputs
- 32-Bit CRC on SIO channels
- ZiLOG Debug Interface (ZDI)
- DC to 33-MHz operating frequency @ 5.0V
- DC to 20-MHz operating frequency @ 3.3V
- Clock divide-by-2, -1X, or -2X
- Fully-static CMOS design with low-power standby modes
- 160-Pin QFP package

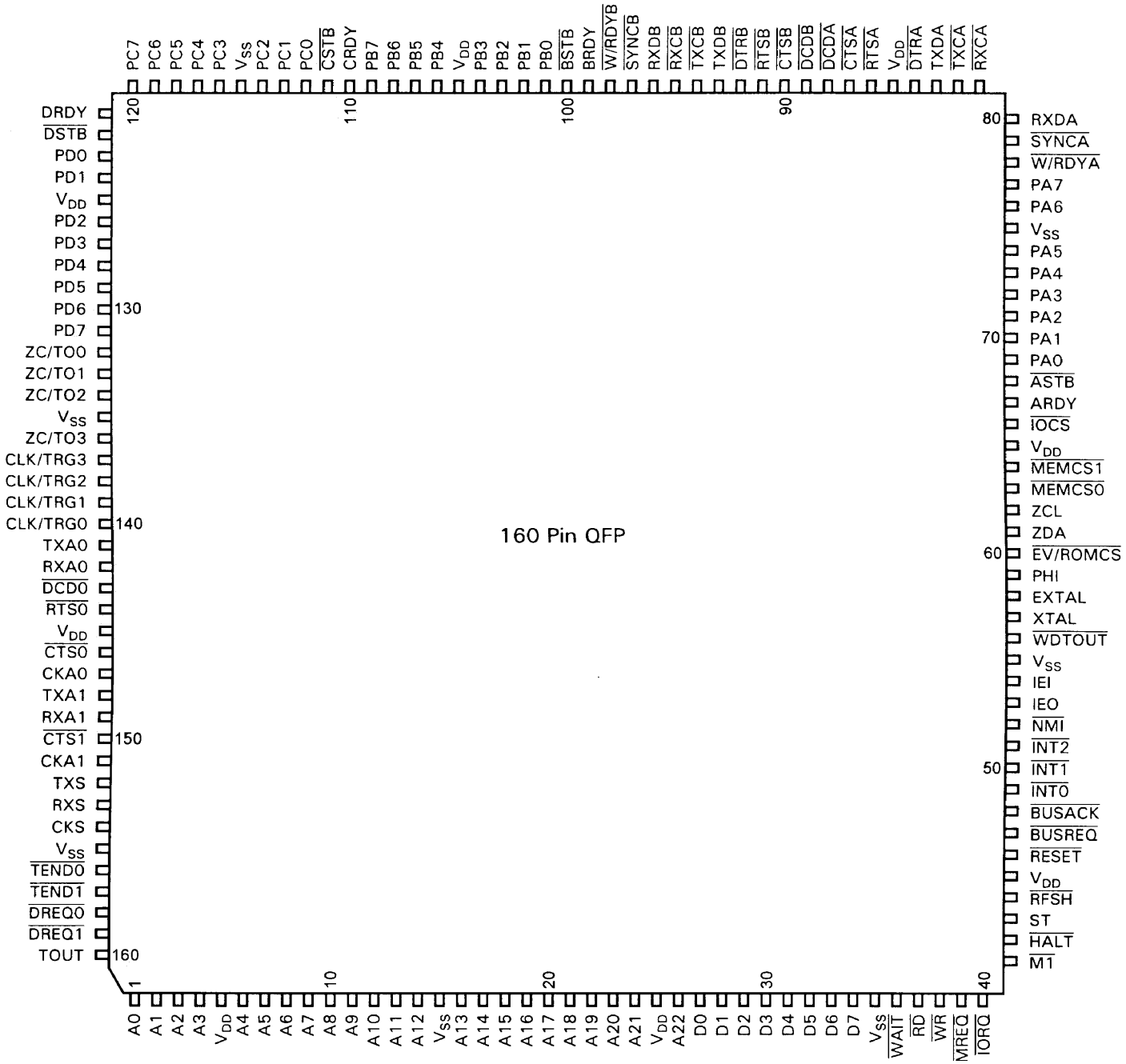
General Description

The Z80S188 ZiLOG Enhanced Intelligent Peripheral Controller is a highly integrated 8-bit CMOS microprocessor that includes SIO, CTC, CGC, WDT, and PIO functions, plus 4 KB of ROM with ROM protect, and 1 KB of RAM with RAM protect in a single 160-pin QFP package. Security options can protect sensitive code and data in internal RAM and ROM. This intelligent peripheral controller is well-suited for a broad range of applications ranging from error-correcting modems to enhancement/cost reductions of existing hardware using Z80-based discrete peripherals.

BLOCK DIAGRAMS



PIN-OUTS AND PIN DIRECTION



Functional Description

Functionally, the on-chip SIO, PIO, CTC and the Z80 CPU are compatible with discrete Z80 devices and the Z84C15.

The following subsections describe each individual functional unit of the EIPC.

Z8S180 CPU . The CPU provides all of the capabilities and pins of the ZiLOG Z80180 CPU. This feature allows 100% software compatibility with existing Z80 software, while offering increased performance. The Z8S180 block includes two 16-bit Counter/ Timers, two DMAs, two UARTs, a CSIO, and an 8MB MMU.

Memory Management Unit (MMU). The MMU allows the user to map the memory used by the CPU (logically only 64 KB) into the 8 MB addressing range supported by the Z80SI88. The organization of the MMU maintains object code compatibility with the Z80 CPU, while offering access to an extended memory space. This feature is accomplished by using an effective common area/banked area scheme. The MMU is backward-compatible with current 8S180-based products.

Central Processing Unit. The CPU is microcoded to provide a core that is object-code compatible with the Z80 CPU. This CPU also provides a superset of the Z80 instruction set, including 8-bit multiply.

DMA Controller. The DMA controller provides high-speed transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory-to/from-I/O, and I/O-to-I/O. Transfer modes supported are Request, Burst, and Cycle Steal. DMA transfers can access the full 8-MB address range with a block length up to 64 KB and can cross over 64 K boundaries.

Asynchronous Serial Communication Interface (ASCI). The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable Baud Rate Generator (BRG) and modem-control signals. The ASCI channels can also support a multiprocessor communication format as well as break detection and generation.

Programmable Reload Timers (PRT). Two separate channels, each containing a 16-bit counter/timer and count reload register. An enhanced prescaler selects one of sixteen clock rates, ranging from the system clock to the system clock divided by 16384. PRT channel 1 provides waveform generation output.

Parallel Input/Output Ports. These ports provide interfaces to external devices via four 8-bit parallel ports. The parallel ports (designated Port A through Port D) are byte-wide and completely compatible with the PIO. These two ports have several modes of operation, input, output, bidirectional, or bit control mode. Each port features two handshake signals, Ready (RDY) and Strobe ($\overline{\text{STB}}$) which are used to control data transfers. The RDY signal indicates that the port is ready for data transfer while ($\overline{\text{STB}}$) is an input to the port that indicates when data transfer has occurred. Each of the ports can be programmed to issue an interrupt at the occurrence of specified status conditions and generate unique interrupt vectors when the CPU responds.

Counter/Timers. Four individual 8-bit counter/timer channels are compatible with the CTC. The counter/timers can be programmed for a broad range of counting and timing applications. Typical applications include event counting, interrupt and interval counting, and serial baud rate clock generation.

Each of the Counter/Timer channels, designated Channels 0-3, feature an 8-bit prescaler (when used in timer mode) and its own 8-bit counter to provide a wide range of count resolution. Each of the channels contain its own Clock/Trigger input to quantify the counting process and an output to indicate zero crossing/timeout conditions. Each channel can generate a unique interrupt vector in response to the Interrupt Acknowledge cycle.

Serial I/O. Two separate multiprotocol serial I/O channels are completely compatible with the SIO. These channels basic function as serial-to-parallel and parallel-to-serial converters can be programmed by a CPU for a broad range of serial communications applications. Each channel, designated Channel A and Channel B, is capable of supporting all common asynchronous and synchronous protocols, such as:

- Monosync
- Bisync, or
- SDLC/HDLC

The Z80S188 SIOs can handle a 32-bit CRC and include Schmitt-trigger inputs on the $\overline{\text{TXC}}$ and $\overline{\text{RXC}}$ pins of both channels.

Watch-Dog Timer (WDT). This logic unit detects program runaway, and returns the device to normal operation. At Power-on Reset (POR), this unit is enabled. During the power-down mode of operation (either IDLE 1/2 or STOP), the Watch-Dog Timer is halted.

32-Bit CRC Generation/Checking. SIO channels can use the 32-bit CRC generator/checker instead of the original 16-bit CRC generator/checker in synchronous communication modes. The polynomial to be used in this mode is the same as for the protocols such as V.42, and is:

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X32 + X26 + X23 + X22 + X1 6 + X1 2 + X1
1 + X1 0 + X8 + X7 + X5 + X4 + X2 + X + 1
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APPLICATIONS AND SUPPORT TOOLS

The following development tools are available for the programming and debug of this device:

- Softool C-compiler (supports 8 MB addressing)
- Z80S18800ZCO Evaluation Board

Related Products

Other Z80 products of interest are:

Z84C15	Enhanced Intelligent Peripheral
Z80180/S180	Enhanced Z80 Megacell
Z80181	Smart Access Controller
Z80182	ZiLOG Intelligent Peripheral
Z80S183	Enhanced Controller
Z80185/195	Smart Peripheral Controller
Z80189	Z8S180 and Parallel I/O

Electrical Features Summary

- 50 µA maximum Supply Current
- 4.75V to 5.25V Operating Range

Ordering Information

Part	PSI	Description
Z80S188	Z80S18833PSC xxxx	160 Quad Flat Pack (QFP); 33MHz; Standard Temperature

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