PRODUCT BRIEF

TWO-CHANNEL DOLBY AC-3/MPEG-1 AUDIO DECODER

FEATURES

- Multi-Function Two-Channel Output Decoder
  - Six-channel Dolby AC-3 to two-channel Surround Sound Compatible
  - Six-channel AC-3 to two-channel output
  - Two-channel MPEG-1 audio layers 1 and 2
  - One- or two-channel PCM to two channel mono or stereo
- Low-Cost Self -Contained Solution
  - Glue-less connection to most input and output streams
  - Simple bit-serial SPI compatible interface to host
  - Internal oscillator with x2 PLL for use with 33 MHz crystal
  - Programmable internal I/O clock generators
  - 52-pin Plastic Leaded Chip Carrier (PLCC) packaging
- Flexible System Component
  - Internal ROM contains all decoder algorithms
  - Control by simple commands from host microprocessor
  - Industry standard decoder functions

- Flexible Audio Input/Output
  - Works with virtually all serial audio D/A converters
  - Master or slave I/O with programmable internal clocks
  - 16-, 18- or 20-bit word sizes
  - Formats: I^2S, EIAJ right-justified, single-bit delayed or non-delayed data, frame sync or frameless
  - Protocols: AC-3/IEC 958 (S/PDIF) or unformatted
  - Sample rates: 48 kHz, 44.1 kHz or 32 kHz
  - Input data rates up to 384 kbits per second
- Full implementation of standards with choices of:
  - Speaker configuration
  - Mixing, dynamic range compression and dialog normalization
  - Complete system status information from bit-stream

APPLICATIONS

- The complete solution for two-channel decoding for:
  - CD and Digital Audio Tape consumer electronics
  - Television set-top boxes

  - Multimedia computing
  - Virtual Reality
  - Professional digital audio
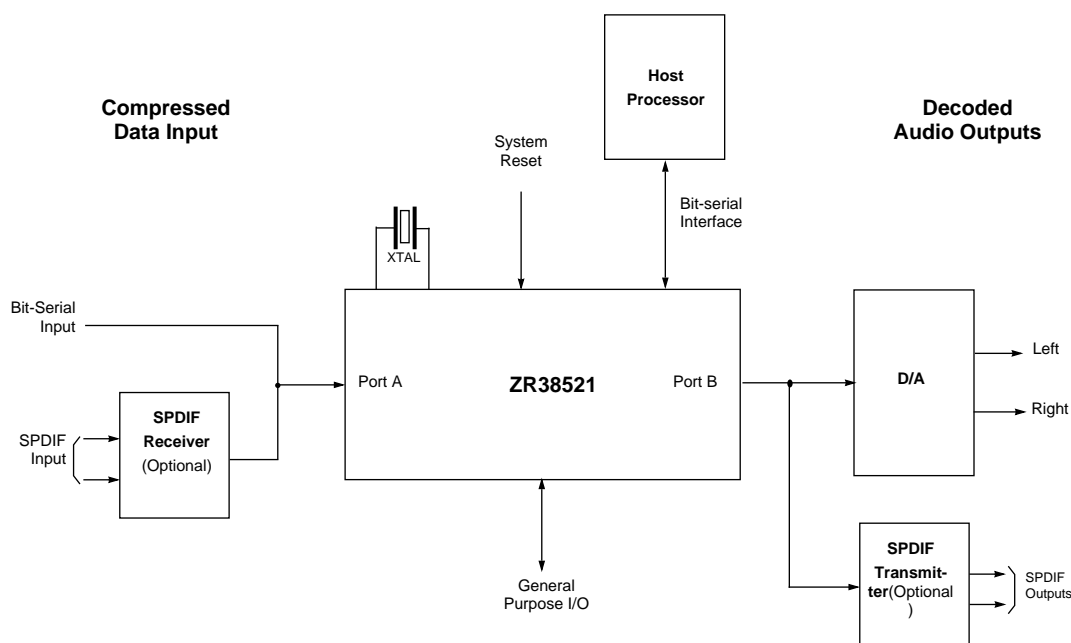
Figure 1. ZR38521 Configuration Diagram

GENERAL DESCRIPTION

The Zoran ZR38001 is the first programmable digital signal processor capable of real-time single-chip decoding of the Dolby Laboratories AC-3 six-channel digital surround sound algorithm. The ZR38521 is a derivative design with AC-3 and MPEG-1 two-channel algorithms pre-programmed in internal ROM. Useful in a number of different configurations, it provides even lower cost system solutions than a ZR38001.

From a single compressed digital data stream (with a choice of formats), the ZR38521 generates all of the signals for virtually all serial audio D/A converters to produce the decoded two channel analog outputs. The available decoding functions, illustrated in Figure 2, are:

■ Compressed six-channel Dolby AC-3 to two decoded Left Total and Right Total channels that are Dolby Surround compatible. Dynamic range is selectable

■ Compressed six-channel AC-3 to two decoded sound channels. Stereo or mono loudspeaker configuration and dynamic range are selectable

■ Two-channel MPEG-1 to two decoded channels of sound with stereo or mono loudspeaker configurations selectable

■ One- or two-channel PCM with stereo or mono loudspeaker configurations selectable.

The ZR38521 is as flexible in its hardware configuration as in its functional operation. Figure 1 shows the possibilities. The base configuration is a ZR38521 with its clock crystal, a controlling host microprocessor, the desired input interface and the appropriate output D/A converter or digital interface.

A connection is made with the host through an inexpensive bit-serial peripheral interface (SPI compatible). A simple command structure with the ZR38521 permits selecting the decoder functions and their parameters along with sending operating commands like Play and Stop. Status information is returned from the decoder to the host through the same command structure. Additional control and interaction with the system can take place through the four user-defined single-bit general-purpose I/O ports built into the ZR38521.

The ZR38521 is useful in many different digital audio applications partly because of the flexibility of its input/output ports. Three sample rates of 48, 44.1 and 32 kHz are supported with the processor being selectable as either slave or master for input and outputs separately. Word size can be 16, 18 or 20 bits with word select of either polarity or frame synchronization. Formats can be I^2S with delayed data, EIAJ with LSB justification, ones with non-delayed data or frameless ones with no synchronization signal. Special protocols supported are AC-3/IEC 958 (S/PDIF) and the continuous frameless format.

Individual port programmable dividers are used when the ZR38521 is a master with I/O clocking derived from its crystal clock. The master-rate clock is output as well as the bit-rate clocks. Or the output port's internal divider can be used with an external master clock.
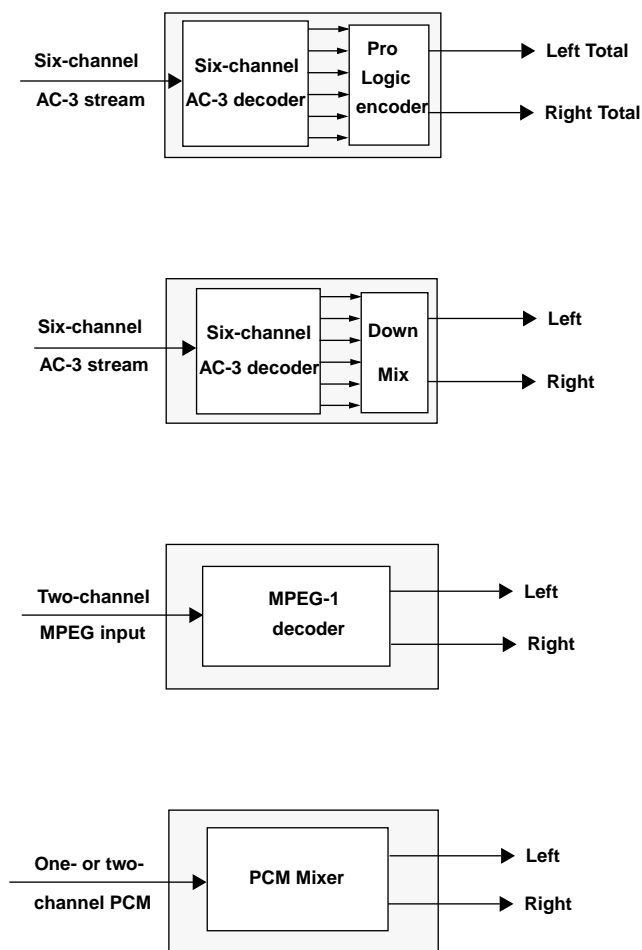

Figure 2. ZR38521 Decoding Functions