



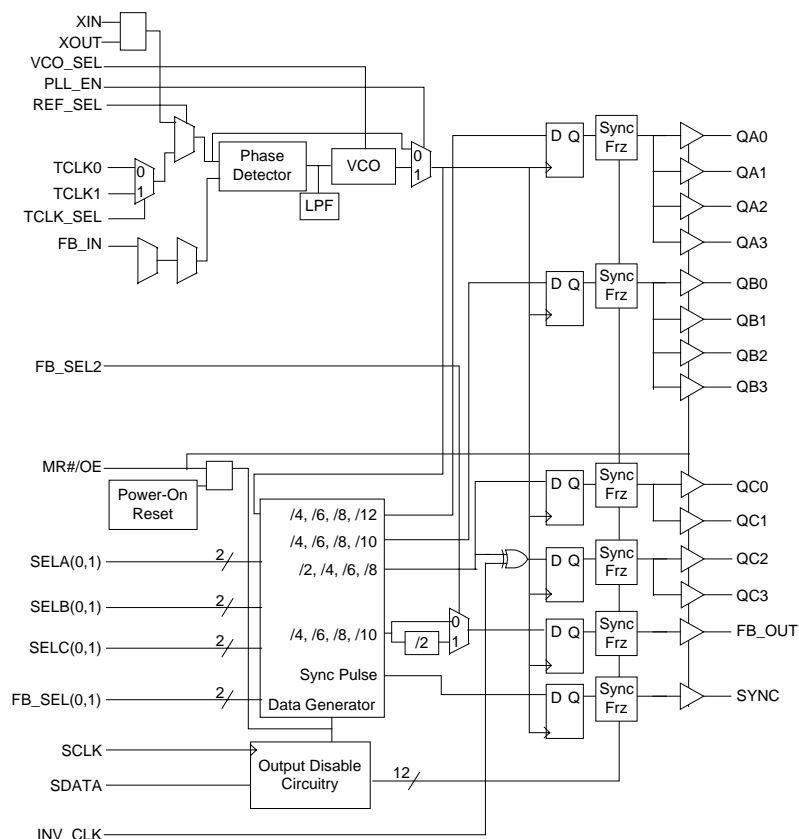
Z9972

3.3V, 125MHz, Multi-Output Zero Delay Buffer

Product Features

- Output Frequency up to 125MHz
- Supports PowerPC™, and Pentium™ Processors
- 12 Clock Outputs: Frequency Configurable
- Configurable Output Disable
- Two Reference Clock Inputs for Dynamic Toggling
- Oscillator or Crystal Reference Input
- Spread Spectrum Compatible
- Glitch-free Output Clocks Transitioning
- 3.3V Power Supply
- Pin Compatible with MPC972
- Industrial Temp. Range: -40°C to +85°C
- 52-Pin TQFP Package

Block Diagram



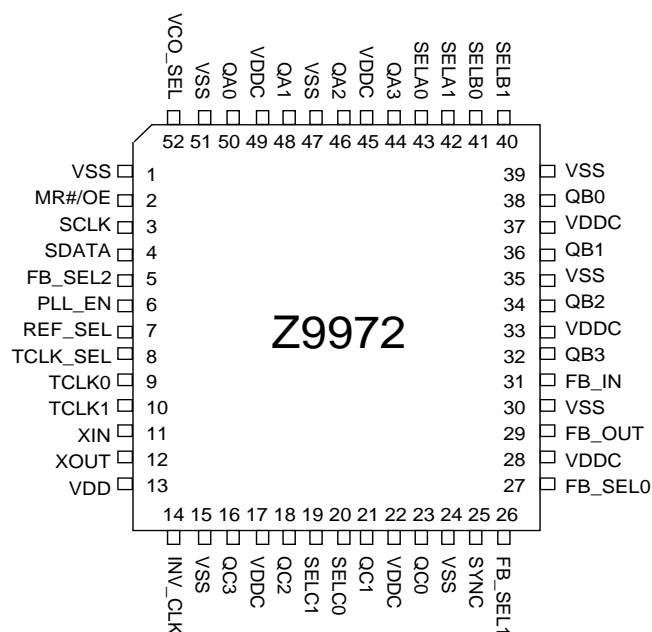
Frequency Table *

VCO_SEL	FB_SEL2	FB_SEL1	FB_SEL0	F _{VCO}
0	0	0	0	8x
0	0	0	1	12x
0	0	1	0	16x
0	0	1	1	20x
0	1	0	0	16x
0	1	0	1	24x
0	1	1	0	32x
0	1	1	1	40x
1	0	0	0	4x
1	0	0	1	6x
1	0	1	0	8x
1	0	1	1	10x
1	1	0	0	8x
1	1	0	1	12x
1	1	1	0	16x
1	1	1	1	20x

Table 1

* x = the reference input frequency, 200MHz < F_{VCO} < 480MHz.

Pin Configuration



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Pin Description

PIN	NAME	PWR	I/O	TYPE	Description
11	XIN		I		Oscillator Input. Connect to a crystal.
12	XOUT		O		Oscillator Output. Connect to a crystal.
9	TCLK0		I	PU	External Reference/Test Clock Input.
10	TCLK1		I	PU	External Reference/Test Clock Input.
44, 46, 48, 50	QA(3:0)	VDDC	O		Clock Outputs. See Table 2 for frequency selections.
32, 34, 36, 38	QB(3:0)	VDDC	O		Clock Outputs. See Table 2 for frequency selections.
16, 18, 21, 23	QC(3:0)	VDDC	O		Clock Outputs. See Table 2 for frequency selections.
29	FB_OUT	VDDC	O		Feedback Clock Output. Connect to FB_IN for normal operation. The divider ratio for this output is set by FB_SEL(0:2). See Frequency Table. A bypass delay capacitor at this output will control Input Reference/ Output Banks phase relationships.
25	SYNC	VDDC	O		Synchronous Pulse Output. This output is used for system synchronization. The rising edge of the output pulse is in sync with both the rising edges of QA (0:3) and QC(0:3) output clocks regardless of the divider ratios selected.
42, 43	SELA(1,0)		I	PU	Frequency Select Inputs. These inputs select the divider ratio at QA(0:3) outputs. See Table 2
40, 41	SELB(1,0)		I	PU	Frequency Select Inputs. These inputs select the divider ratio at QB(0:3) outputs. See Table 2
19, 20	SELC(1,0)		I	PU	Frequency Select Inputs. These inputs select the divider ratio at QC(0:3) outputs. See Table 2
5, 26, 27	FB_SEL(2:0)		I	PU	Feedback Select Inputs. These inputs select the divide ratio at FB_OUT output. See Table 1
52	VCO_SEL		I	PU	VCO Divider Select Input. When set low, the VCO output is divided by 2. When set high, the divider is bypassed. See Table 1
31	FB_IN		I	PU	Feedback Clock Input. Connect to FB_OUT for accessing the PLL.
6	PLL_EN		I	PU	PLL Enable Input. When asserted high, PLL is enabled. And when low, PLL is bypassed.
7	REF_SEL		I	PU	Reference Select Input. When high, the crystal oscillator is selected. And when low, TCLK (0,1) is the reference clock.
8	TCLK_SEL		I	PU	TCLK Select Input. When low, TCLK0 is selected and when high TCLK1 is selected.
2	MR#/OE		I	PU	Master Reset/Output Enable Input. When asserted low, resets all of the internal flip-flops and also disables all of the outputs. When pulled high, releases the internal flip-flops from reset and enables all of the outputs.
14	INV_CLK		I	PU	Inverted Clock Input. When set high, QC(2,3) outputs are inverted. When set low, the inverter is bypassed.
3	SCLK		I	PU	Serial Clock Input. Clocks data at SDATA into the internal register.
4	SDATA		I	PU	Serial Data Input. Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.
17, 22, 28, 33, 37, 45, 49	VDDC				3.3V Power Supply for Output Clock Buffers.
13	VDD				3.3V Supply for PLL
1, 15, 24, 30, 35, 39, 47, 51	VSS				Common Ground

A bypass capacitor (0.1μF) should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.



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Maximum Ratings

Input Voltage Relative to VSS:	VSS-0.3V
Input Voltage Relative to VDD:	VDD+0.3V
Storage Temperature:	-65°C to + 150°C
Operating Temperature:	-40°C to +85°C
Maximum Power Supply:	5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$VSS < (V_{in} \text{ or } V_{out}) < VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	VSS	-	0.8	V	
Input High Voltage	VIH	2.0	-	VDD	V	
Input Low Current (@ VIL = VSS)	IIL		-	-120	μA	Note 2
Input High Current (@ VIH = VDD)	IIH			10	μA	
Output Low Voltage	VOL			0.5	V	IOL = 20mA, Note 1
Output High Voltage	VOH	2.4			V	IOH = -20mA, Note 1
Quiescent Supply Current	IDDC	-	10	15	mA	All VDDC and VDD
PLL Supply Current	IDD		15	20	mA	VDD only
Input Pin Capacitance	Cin	-	-	4	pF	
VDD = VDDC = 3.3V ± 5%, TA = -40°C to +85°C						

Note 1: Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines.

Note 2: Inputs have pull-up resistors, which affect input current.



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AC Parameters¹

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	CONDITIONS
Tr / Tf	TCLK Input Rise / Fall				3.0	ns	
Fref	Reference Input Frequency		Note 2		Note 2	MHz	
Fxtal	Crystal Oscillator Frequency		10		25	MHz	See Table 3 for details
FrefDC	Reference Input Duty Cycle		25		75	%	
Fvco	PLL VCO Lock Range		200		480	MHz	
Tlock	Maximum PLL lock Time				10	ms	
Tr / Tf	Output Clocks Rise / Fall Time ³		0.15		1.2	ns	0.8V to 2.0V
Fout	Maximum Output Frequency		-		125	MHz	Q (÷2)
					120		Q (÷4)
					80		Q (÷6)
					60		Q (÷8)
FoutDC	Output Duty Cycle ³		TCYCLE/2 – 750		TCYCLE/2 + 750	ps	
tpZL, tpZH	Output Enable Time ³ (all outputs)		2		10	ns	
tpLZ, tpHZ	Output Disable Time ³ (all outputs)		2		8	ns	
TCCJ	Cycle to Cycle Jitter ³ (peak to peak)			+/- 100		ps	
TSKEW	Any Output to Any Output Skew ^{3,4}				350	ps	
Tpd	Propagation Delay ^{4,5}	TCLK0	-270	130	530	ps	QFB =(÷8)
		TCLK1	-330	70	470		
VDD = VDDC = 3.3V +/- 5%, TA = -40°C to +85°C							

VDD = VDDC = 3.3V +/- 5%, TA = -40°C to +85°C

Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production.

Note 2: Maximum and minimum input reference is limited by VCO lock range.

Note 3: Outputs loaded with 30pF each.

Note 4: 50Ω transmission line terminated into VDDC/2.

Note 5: Tpd is specified for a 50MHz input reference. Tpd does not include jitter.

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Description

The Z9972 has an integrated PLL that provides low skew and low jitter clock outputs for high performance microprocessors. Three independent banks of four outputs as well as an independent PLL feedback output, FB_OUT, provide exceptional flexibility for possible output configurations. The PLL is ensured stable operation given that the VCO is configured to run between 200 MHz to 480 MHz. This allows a wide range of output frequencies up to 125MHz.

The phase detector compares the input reference clock to the external feedback input. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by FB_SEL(0:2) and VCO_SEL select inputs, refer to Frequency Table. The VCO frequency is then divided down to provide the required output frequencies. These dividers are set by SELA(0,1), SELB(0,1), SELC(0,1) select inputs, see table 2 below. For situations where the VCO needs to run at relatively low frequencies and hence might not be stable, assert VCO_SEL low to divide the VCO frequency by 2. This will maintain the desired output relationships, but will provide an enhanced PLL lock range.

The Z9972 is also capable of providing inverted output clocks. When INV_CLK is asserted high, QC2 and QC3 output clocks are inverted. These clocks could be used as feedback outputs to the Z9972 or a second PLL device to generate early or late clocks for a specific design. This inversion does not affect the output to output skew.

VCO_SEL	SELA1	SELA0	QA	SELB1	SELB0	QB	SELC1	SELC0	QC
0	0	0	VCO/8	0	0	VCO/8	0	0	VCO/4
0	0	1	VCO/12	0	1	VCO/12	0	1	VCO/8
0	1	0	VCO/16	1	0	VCO/16	1	0	VCO/12
0	1	1	VCO/24	1	1	VCO/20	1	1	VCO/16
1	0	0	VCO/4	0	0	VCO/4	0	0	VCO/2
1	0	1	VCO/6	0	1	VCO/6	0	1	VCO/4
1	1	0	VCO/8	1	0	VCO/8	1	0	VCO/6
1	1	1	VCO/12	1	1	VCO/10	1	1	VCO/8

Table 2

Glitch-Free Output Frequency Transitions

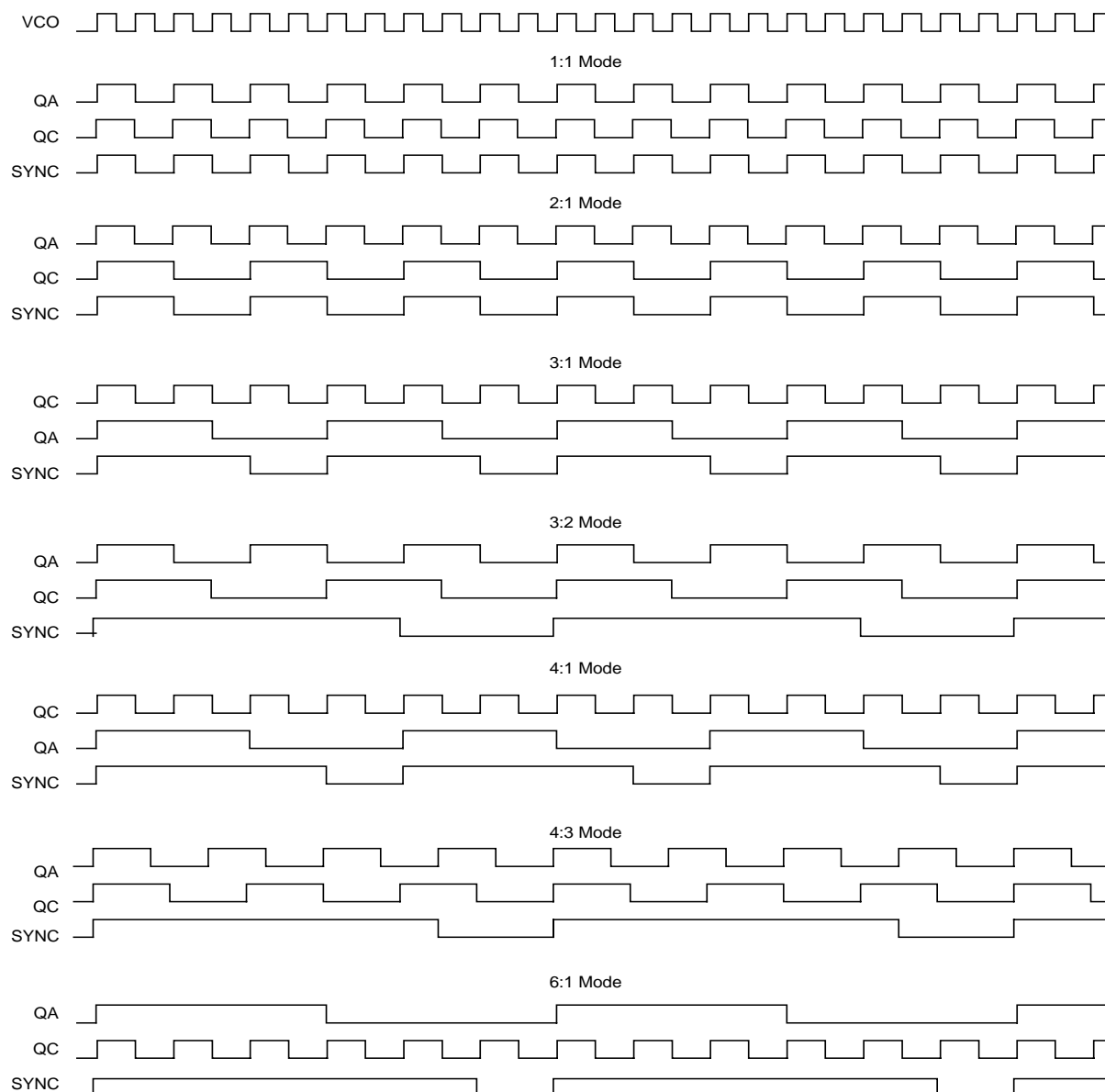
Customarily when output buffers have their internal counter's changed "on the fly" their output clock periods will:

- Contain short or "runt" clock periods. These are clock cycles in which the cycle(s) are shorter in period than either the old or new frequency that is being transitioned to.
- Contain stretched clock periods. These are clock cycles in which the cycle(s) are longer in period than either the old or new frequency that is being transitioned to.

This device specifically includes logic to guarantee that runt and stretched clock pulses do not occur if the device logic levels of any or all of the following pins changed "on the fly" while it is operating: SELA, SELB, SELC, and VCO_SEL.

SYNC Output

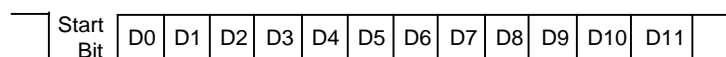
In situations where output frequency relationships are not integer multiples of each other the SYNC output provides a signal for system synchronization. The Z9972 monitors the relationship between the QA and the QC output clocks. It provides a low going pulse, one period in duration, one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse depend on the higher of the QA and QC output frequencies. The following timing diagram illustrates various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of the QA and QC outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.



Power Management

The individual output enable / freeze control of the Z9972 allows the user to implement unique power management schemes into the design. The outputs are stopped in the logic '0' state when the freeze control bits are activated. The serial input register contains one programmable freeze enable bit for 12 of the 14 output clocks. The QC0 and FB_OUT outputs can not be frozen with the serial port, this avoids any potential lock up situation should an error occur in the loading of the serial data. An output is frozen when a logic '0' is programmed and enabled when a logic '1' is written. The enabling and freezing of individual outputs is done in such a manner as to eliminate the possibility of partial "runt" clocks.

The serial input register is programmed through the SDATA input by writing a logic '0' start bit followed by 12 NRZ freeze enable bits. The period of each SDATA bit equals the period of the free running SCLK signal. The SDATA is sampled on the rising edge of SCLK.



D0-D3 are the control bits for QA0-QA3, respectively
D4-D7 are the control bits for QB0-QB3, respectively
D8-D10 are the control bits for QC1-QC3, respectively
D11 is the control bit for SYNC

Suggested Oscillator Crystal Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency Tolerance	T_C	-	-	+/-100	PPM	Note 1
Frequency Temperature Stability	T_S	-	-	+/- 100	PPM	(T_A -10 to +60C) Note 1
Aging	T_A	-	-	5	PPM/Yr	(first 3 years @ 25C) Note 1
Load Capacitance	C_L	-	20	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	80	Ohms	Note 2

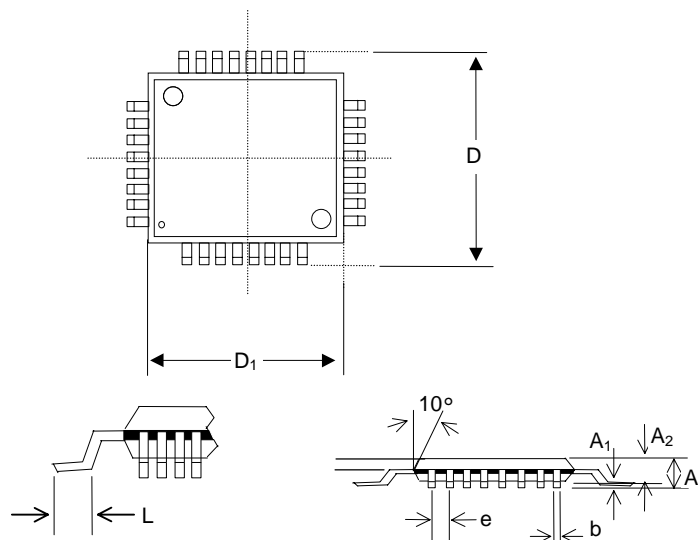
Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

Table 3

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Package Drawing and Dimensions (52 TQFP)



52 Pin TQFP Outline Dimensions

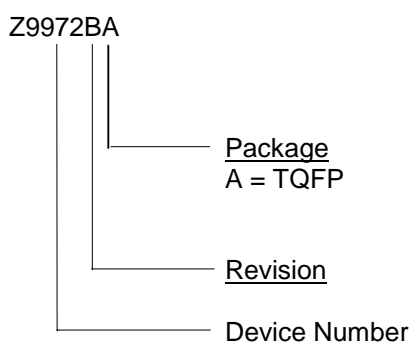
SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A ₁	0.002	-	0.006	0.05	-	0.15
A ₂	0.037	-	0.041	0.95	-	1.05
D	-	0.472	-	-	12.00	-
D ₁	-	0.394	-	-	10.00	-
b	0.009	-	0.015	0.22	-	0.38
e	0.026 BSC			0.65 BSC		
L	0.018	-	0.030	0.45	-	0.75

Ordering Information

Part Number	Package Type	Production Flow
Z9972BA	52 TQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: CYPRESS
Z9972BA
Date Code, Lot #



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