Z80S183

MIXED SIGNAL Z183 WEBSERVER

PB001201-0601

PRELIMINARY

PRODUCT BLOCK DIAGRAM

<table>
<tr><td>WDT</td><td colspan="2">8S180 CPU</td><td rowspan="2">8 ch, 10-Bit A/D</td></tr>
<tr><td>RTC</td><td colspan="2">MMU</td></tr>
<tr><td rowspan="2">24 I/O</td><td colspan="2">ZDI</td><td rowspan="3">10-Bit D/A</td></tr>
<tr><td>2C/T</td><td>2 DMA</td></tr>
<tr><td colspan="2">2 UART</td><td>CSIO</td></tr>
<tr><td colspan="2">1K ROM</td><td>2K SRAM</td><td>POG</td></tr>
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FEATURES

- Z8S180 Macrocell
  - Improved CPU performance. Extended instructions. Code-compatible with Z80 core.
  - Up to 33 Mhz speed
  - 5 V & 3.3 V operation
  - 2 DMA Channels
  - 2 Enhanced UARTs (512 Kbps)
  - 2 16-Bit Timers
  - CSIO
  - On-chip MMU (1 MByte)
  - Edge/Level Triggered Interrupt Controller
  - Wait State Generator
  - Low Power Modes
  - Low EMI modes
- 32-bit GPIO
- 8 Channels 10-bit A/D
- 8 Bit Programmable Output Generator (POG)
- 10 bit Digital to Analog Converter
- 2 K Static SRAM
- 1 K Boot ROM (Virtual Loader)
- Real Time Clock
- Watch-Dog Timer
- Economical 100-pin VQFP package

GENERAL DESCRIPTION

The Z80S183 is a highly integrated mixed signal webserver. It consists of the full-featured Z80S180 microprocessor, 32 bits of General Purpose I/O, an Analog-to-Digital channel with eight multiplexed inputs, Eight POG channels, a Digital to Analog converter, Watch-Dog Timer, 8 K SRAM, a Real-Time Clock, and 1 K Boot ROM.

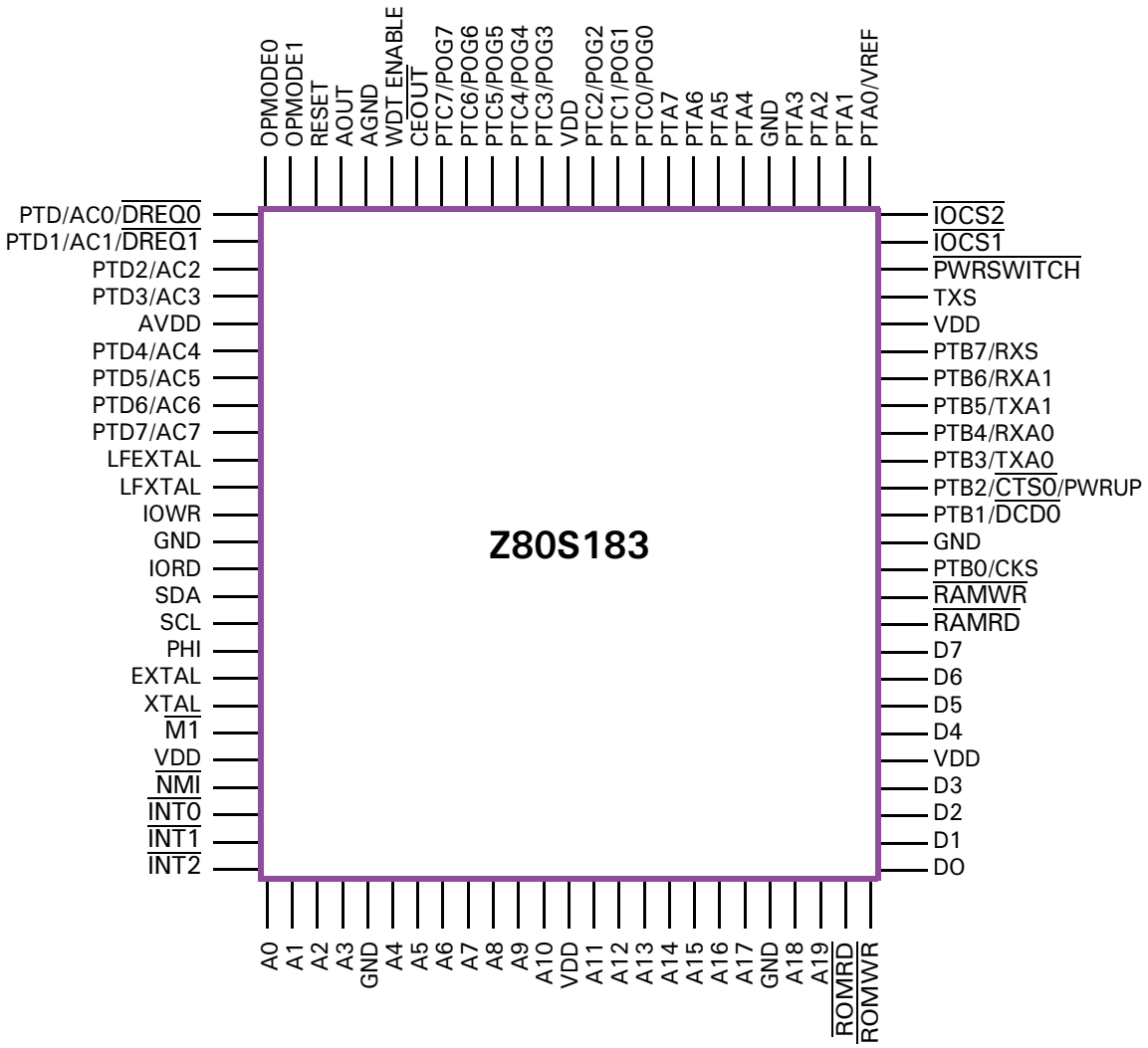
The Z80S183 is an economical 100-pin VQFP package.

DETAILED DESCRIPTION

Z8S180 MICROPROCESSOR CORE. The enhanced Z8S180™ significantly improves on the previous Z8S180 models while still providing full backward compatibility with existing ZiLOG Z80 devices. The Z8S180/Z8L180 offers faster execution speeds, power-saving modes, and EMI noise reduction.

Not only does the Z8S180 core consume less power during normal operations than the previous Z80180 models, it is designed with three modes intended to further reduce the power consumption. ZiLOG reduced I_{CC} power core consumption during STANDBY Mode to a minimum of 10µA by stopping the external oscillators and internal clock. The SLEEP mode reduces power by placing the CPU into a *stopped* state, thereby consuming less current while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a *stopped* mode, reducing power consumption even further.

PIN-OUTS AND PIN DIRECTION



Z80S183 Peripheral Description

2 FAST ASCI. With the addition of ESCC-like Baud Rate Generators (BRGs), the two ASCIs now have the flexibility and capability to transfer data asynchronously at rates of up to 512 Kbps. In addition, the ASCI receiver has added a 4-byte First In First Out (FIFO) which can be used to buffer incoming data to reduce the incidence of overrun errors.

2 DMA. The DMAs have been modified to allow for a chain-linking of the two DMA channels when set to take their DMA requests from the same peripherals device. This feature allows for non-stop DMA operation between the two DMA channels, reducing the amount of CPU intervention.

2 COUNTER/TIMERS. Two separate, 16-bit programmable reload counter/timers (PRT) are provided. PRT1 provides an optional output to allow for wave-form generation.

CSIO. The clock serial I/O provides a half-duplex serial transmitter and receiver. This channel can be used for simple high speed data connection to another microprocessor or microcomputer

32-BIT GENERAL PURPOSE I/O. Four 8- bit ports are provided for general purpose I/O. These pins are individually programmable for input or output mode. Each I/O is capable of sourcing and sinking 15mA

WATCH-DOG TIMER. A Watch-Dog timer is provided to prevent code runaway and possible result-

ing system damage. The range of time constants is up to 4s. The $\overline{\text{RESET}}$ input can be forced as an output upon the terminal count of the Watch-Dog Timer. This action allows external peripherals to be reset along with the Z80S183.

EIGHT CHANNEL ANALOG TO DIGITAL CONVERTERS. There is a single Analog to Digital converter that has eight multiplexed pins. The Analog to Digital Converter is a 10-bit half-flash converter that uses two references resistor ladders for its upper 5 bits (MSB) and lower 5 bits (LSB) conversion. Two reference voltage pins AVCC and AGND are provided for external reference voltage supplies. The minimum conversion time is 8µs

DIGITAL TO ANALOG CONVERTER. There is a 10-bit Digital to Analog converter on board to support applications that require an Analog input. The DAC is a 10-bit register string. The DAC out voltages settles after the internal data is latched into the DAC Data register.

POG. The POG is a memory-mapped programmable event generator which can be used to create complex wave forms, trigger A/D and D/A conversions, and generates processor interrupts. POG events are timed relative to a high-speed clock, creating high speed performance. The POG consumes minimal processor overhead. A POG event is generated by programming event data, a next- event address pointer, and an event timer into POG RAM.

The POG can handle up to 64 events. When a POG event begins, the POG event data and next address bytes are loaded into internal holding buffers and the POG even tim is loaded into the POG countdown timer. Once the timer counts to 0, the POG event occurs and POG next address points to the next PGO even block.

ZDI. A ZiLOG Debug Interface is included. ZDBI incorporates most of the functions of an In-Circuit Emulate on the IC. ZDBI allows the user (with an ICEBOX) to single step code, change registers, edit programs and view status of internal registers.

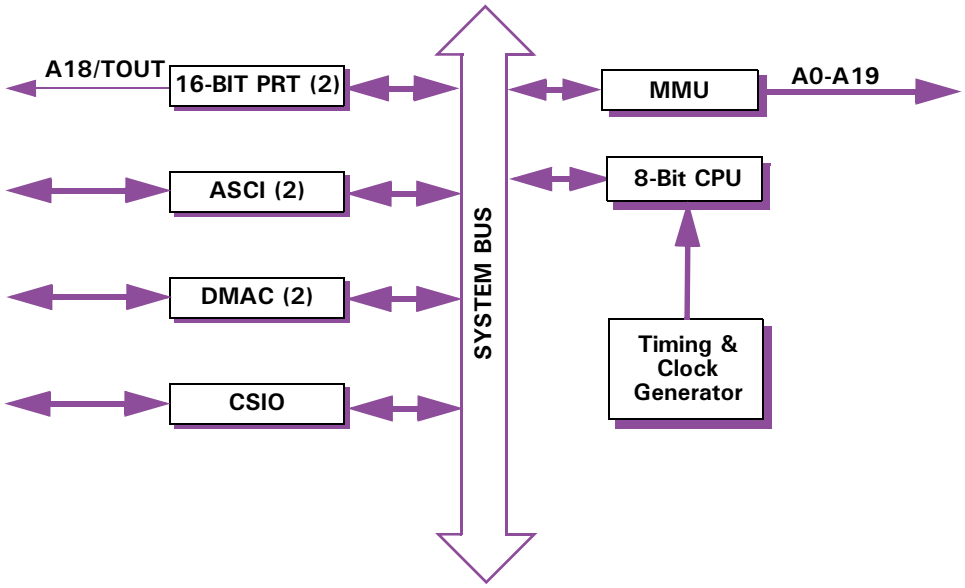
2K BYTES OF SRAM. There is 2K bytes of Static RAM. It resides at Address E000H-FFFFH. This RAM can be used for stack, read/write data storage, and POG events.

1K BOOT ROM. The Z80S183 contains 1K boot ROM.

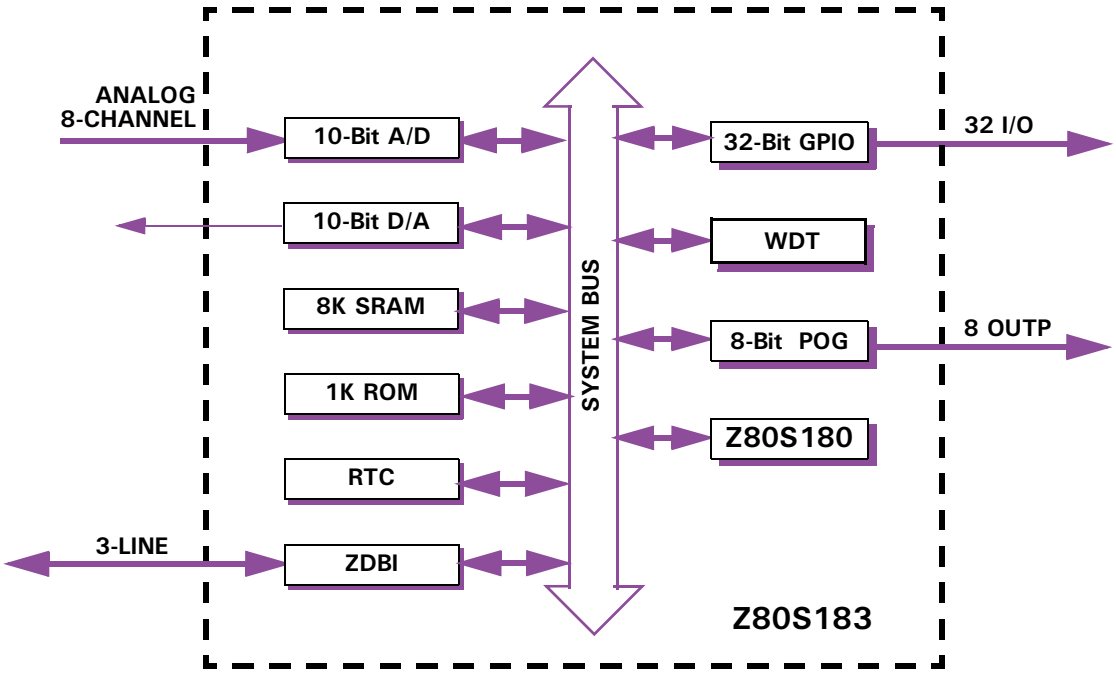
REAL TIME CLOCK. The Z80S183 RTC provides a time and calendar function of seconds, minutes, hours, 12/24, AM//PM, day of week, day of month, month and year. It features a 24 hour alarm facility capable of generating an interrupt.

POWER FAIL SENSING. A power-fail trigger is implemented by detecting missed mains frequency cycles. This feature ensures the earliest possible warning of power failure. Once this event occurs, the systems generate an NMI interrupt if enabled, as well as a status bit in the System Status Register. This feature allows the application software to provide a graceful shutdown.

BLOCK DIAGRAMS



Z8S180 CORE PROCESSOR BLOCK DIAGRAM



Z80S183 BLOCK DIAGRAM

Applications and Support Tools

The following development tools are available for the programming and debug of this device:

- Orion emulators
- ZiLOG Development Suite (ZDS)
- Numerous 3rd party software support (Visit http://www.zilog.com/support/z80_z185.html)

Related Products

Other Integrated Controllers of interest are:

Z84C00	Z80™ CPU (up to 20 MHz)
Z84C15	Z80™ + 2 SIO + 4x8 CTC + 2 PIO + WDT (up to 16 MHz)
Z80S180	Improved Z80 + 1MByte MMU + 2 DMA +2-16bit PRT + 2 UARTs + CSIO (up to 33MHz)
Z80181	Z8S180™ (see above) + SCC+CTC+ 16 GPIO
Z80182	Z8S180™ (see above) + 2 ESCC + 24 bit GPIO+ 16550 Mimic interface (up to 33MHz)
Z80189	Z8S180™ (see above) + 24 GPIO + 16550 Mimic interface (up to 33MHz)
Z80S190	eZ80™ enhanced CPU (single cycle instruction fetch, 16Mbyte Linear Address) + Multiply and Accumulate, 2 UARTs, 6 C/T, CSIO, 2 DMA, 32 GPIO. (Up to 40MHz). Available Q1, 00
Z84C00	Z80™ CPU (up to 20 MHz)

Electrical Features Summary

- 50 µA maximum Supply Current
- 4.75 V to 5.25 V Operating Range

Ordering Information

Part	PSI	Description
Analog 180	Z8S18333ASC	100 VQFP, Standard temp
Low voltage analog 180	Z80L18320ASC	100 VQFP, Standard temp, low power

Document Disclaimer

Pre-Characterization Product

The product represented by this Product Brief is newly introduced and ZiLOG has not completed the full characterization of the product. The Product Brief states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

Low Margin

Customer is advised that this product does not meet ZiLOG's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on ZiLOG liability stated on the front and back of the acknowledgment, ZiLOG makes no claim as to quality and reliability under the Product Brief. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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