Z86L78

IR/LOW-VOLTAGE MICROCONTROLLER

FEATURES

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86L78	16	493	16	2.0V to 3.9V

Note: *General-Purpose

- Low Power Consumption: 40 mW (Typical)
- Three Standby Modes (Typical)
  - STOP - 2 µA
  - HALT - 0.8 mA
  - Low Voltage ($<V_{LV}$)
- Programmable Watch-Dog/Power-On Reset Circuits
- All Digital Inputs are CMOS Levels
- Five Priority Interrupts
  - Three External
  - Two Assigned to Counter/Timers
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC (Mask Selectable), or External Clock Drive
- Mask Selectable Option to Enable 32 kHz Crystal Operation
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Mask-Selectable 200 KOhm Pull-Ups on Ports 0, 2, 3:
  - All Eight Port 2 Bits Individually Selected
  - Pull-Ups Automatically Disabled Upon Selecting an Output.

GENERAL DESCRIPTION

Zilog's Z86L78 is a low-voltage microcontroller, a member of the IR (Infrared) Family, with 16 KB of ROM and 493 bytes of general-purpose RAM. Manufactured in CMOS technology and offered in 20-pin DIP or SOIC styles packages, this cost-effective, low power consumption ROM-based device offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion.

The Z86L78 architecture is based on Zilog's 8-bit microcontroller core, with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z86L78 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

For applications demanding powerful I/O capabilities, the Z86L78 provides 16 pins dedicated to input and output. These lines are grouped into three ports, which are configurable under software control to provide timing, status signals and parallel I/O.

There are four basic address spaces available to support a wide range of configurations: Program Memory, Register File, Expanded Register File, and Extended Data RAM.

GENERAL DESCRIPTION (Continued)

The Register File is composed of 256 bytes of RAM, and it includes four I/O port registers, 16 control and status registers and the rest are General-Purpose registers. The Extended Data RAM adds 256 bytes of usable general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the system from coping with real-time tasks, such as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86L78 offers an innovative intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Additionally, the Z86L78 features a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

Notes: Signals with a preceding front slash, "/", are active Low, for example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

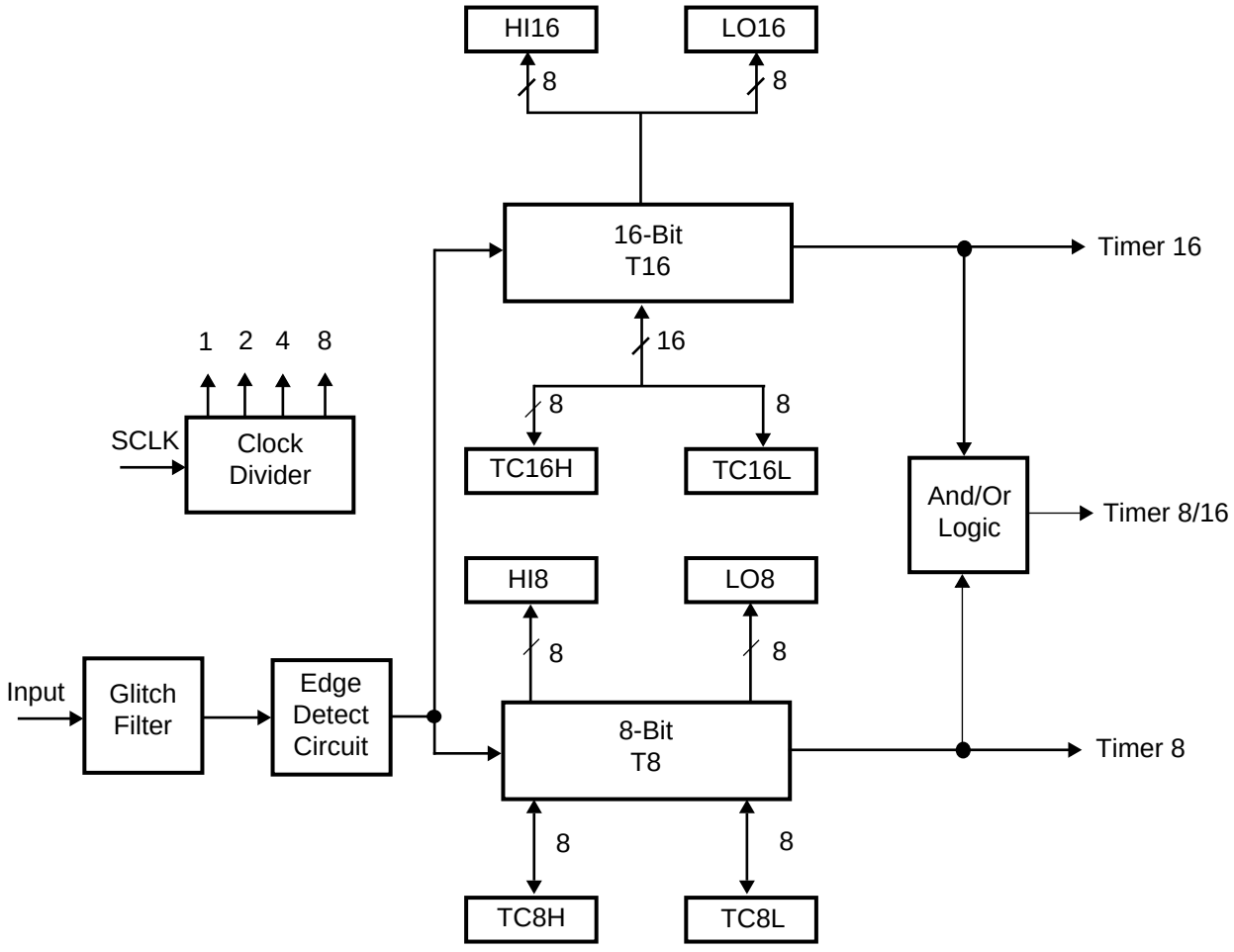


Figure 1. Counter/Timer Block Diagram

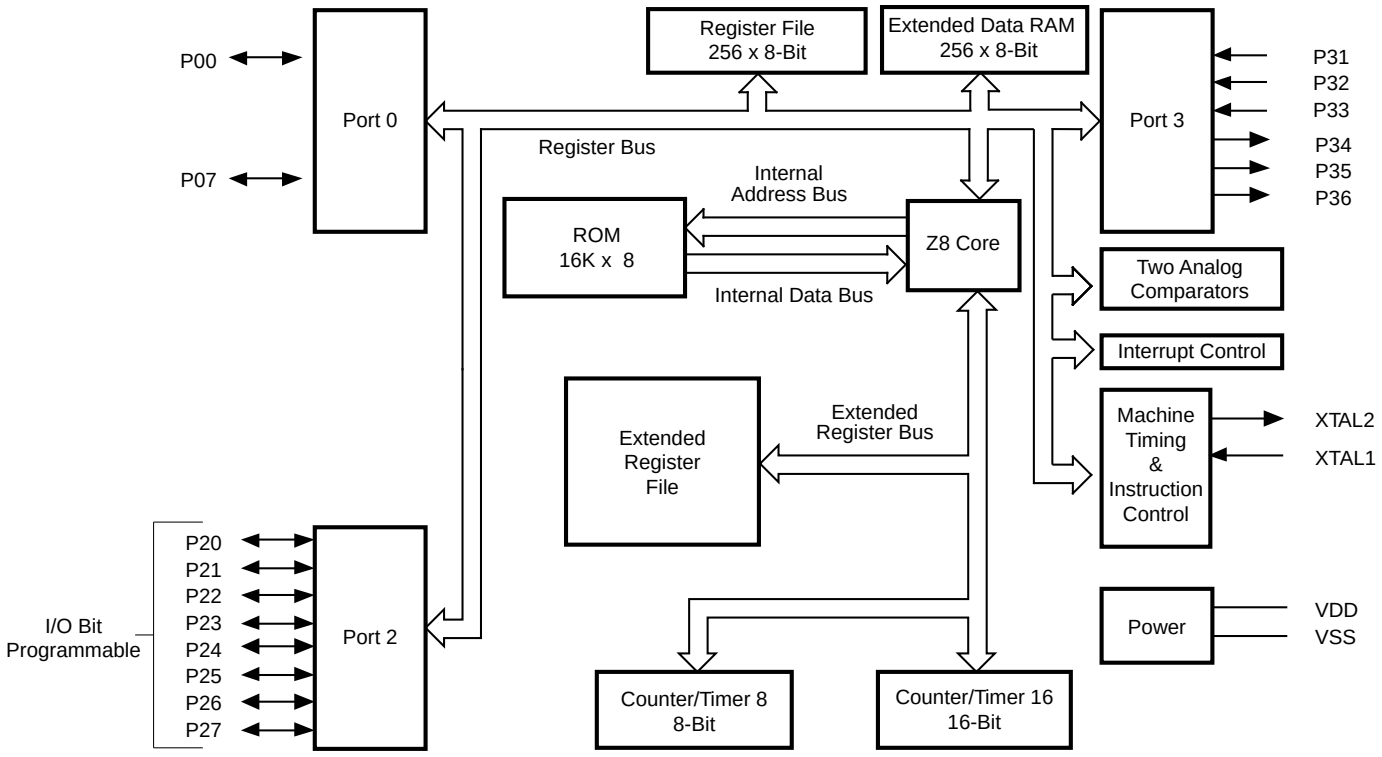


Figure 2. Functional Block Diagram

PIN DESCRIPTION

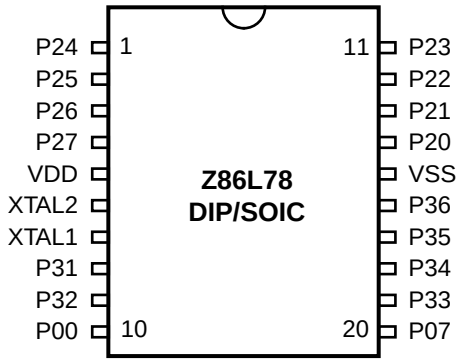


Figure 3. 20-Pin DIP/SOIC Pin Assignments

Table 1. 20-Pin DIP and SOIC Pin Identification

Pin No.	Symbol	Direction	Description
10	P00	Input/Output	Port 0 is Nibble Programmable.
11	P07	Input/Output	
17	P20	Input/Output	Port 2 pins are individually configurable as input or output
18	P21	Input/Output	
19	P22	Input/Output	
20	P23	Input/Output	
1	P24	Input/Output	
2	P25	Input/Output	
3	P26	Input/Output	
4	P27	Input/Output	
8	P31	Input	IRQ2/Modulator input
9	P32	Input	IRQ0
12	P33	Input	IRQ1
13	P34	Output	T8 output
14	P35	Output	T16 output
15	P36	Output	T8/T16 output
7	XTAL1	Input	Crystal, Oscillator Clock
6	XTAL2	Output	Crystal, Oscillator Clock
5	V_{DD}		Power Supply
16	V_{SS}		Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper. Ambient Temp.		†	C

Note:
* Voltage on all pins with respect to Ground.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 4).

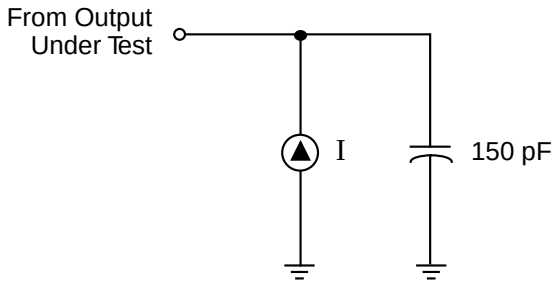


Figure 4. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to Ground.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Preliminary

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	2.0V		7		V	I_{IN} 250 µA	
		3.9V		7		V	I_{IN} 250 µA	
V_{CH}	Clock Input High Voltage	2.0V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
		3.9V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS} -0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
		3.9V	V_{SS} -0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	0.7 V_{CC}	V_{CC} + 0.3	1.3	V		
		3.9V	0.7 V_{CC}	V_{CC} + 0.3	2.5	V		
V_{IL}	Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5	V		
		3.9V	V_{SS} – 0.3	0.2 V_{CC}	0.9	V		
V_{OH1}	Output High Voltage	2.0V	V_{CC} – 0.4		1.7	V	I_{OH} = –0.5 mA	
		3.9V	V_{CC} – 0.4		3.7	V		
V_{OH2}	Output High Voltage (P36, P37)	2.0V	0.7			V	I_{OH} = –7 mA	
		3.9V	0.7			V		
V_{OL1}	Output Low Voltage	2.0V		0.4	0.2	V	I_{OL} = 1.0 mA	
		3.9V		0.4	0.1	V	I_{OL} = <4.0 mA	
V_{OL2}	Output Low Voltage	2.0V		0.8	0.3	V	I_{OL} = 2.0 mA	
		3.9V		0.8	0.5	V	3 Pin Max	
V_{RH}	Reset Input High Voltage	2.0V	0.8 V_{CC}	V_{CC}	1.5	V		
		3.9V	0.8 V_{CC}	V_{CC}	3.0	V		
V_{RI}	Reset Input Low Voltage	2.0V	V_{SS} - 0.3	0.2 V_{CC}	0.5			
		3.9V	V_{SS} - 0.3	0.2 V_{CC}	0.9			
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.9V		25	10	mV		
I_{IL}	Input Leakage	2.0V	-1	1	<1	µA	V_{IN} = O_V, V_{CC}	
		3.9V	-1	1	<1	µA	V_{IN} = O_V, V_{CC}	
I_{OL}	Output Leakage	2.0V	-1	1	<1	µA	V_{IN} = O_V, V_{CC}	
		3.9V	-1	1	<1	µA	V_{IN} = O_V, V_{CC}	
I_{IR}	Reset Input Current	2.0V		-45	-20	µA		
		3.9V		-55	-30	µA		
I_{CC}	Supply Current (WDT Off)	2.0V		10	4	mA	@ 8.0 MHz	4,5
		3.9V		15	10	mA	@ 8.0 MHz	
		2.0V		100	10	mA	@ 32 kHz	
		3.9V		300	10	mA	@ 32 kHz	

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (WDT OFF)	2.0V		3	1	mA	HALT Mode V_{IN}=0V, V_{CC} @ 8.0 MHz	1,2
		3.9V		5	4	mA	HALT Mode V_{IN}=0V, V_{CC} @ 8.0 MHz	
		2.0V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz	
		3.9V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz	
I_{CC2}	Standby Current (WDT Off)	2.0V		8	2	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	3,5
		3.9V		10	3	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	3,5
		2.0V		500	310	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	3,5
		3.9V		800	600	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	3,5
V_{ICR}	Input Common Mode Voltage Range	2.0V	0	V_{CC} - 1.0V		V		11
		3.9V	0	V_{CC} - 1.0V		V		
T_{POR}	Power-On Reset	2.0V	7.5	75	13	ms		
		3.9V	2.5	20	7	ms		
V_{rf1}	Voltage Reference		1.8	2.0		V	8 MHz max	4

Notes:

1. GND = 0V
2. 2.0V to 3.9V
3. All outputs unloaded, I/O pins floating, inputs at rail.
4. CL1 = CL2 = 100 pF
5. Same as note [4] except inputs at V_{CC}.
6. The Vrf1 increases as the temperature decreases.
7. Oscillator stopped
8. Two outputs at a time, independent to other outputs.
9. One at a time
10. 32 kHz clock driver input
11. For analog comparator, inputs when analog comparators are enabled.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

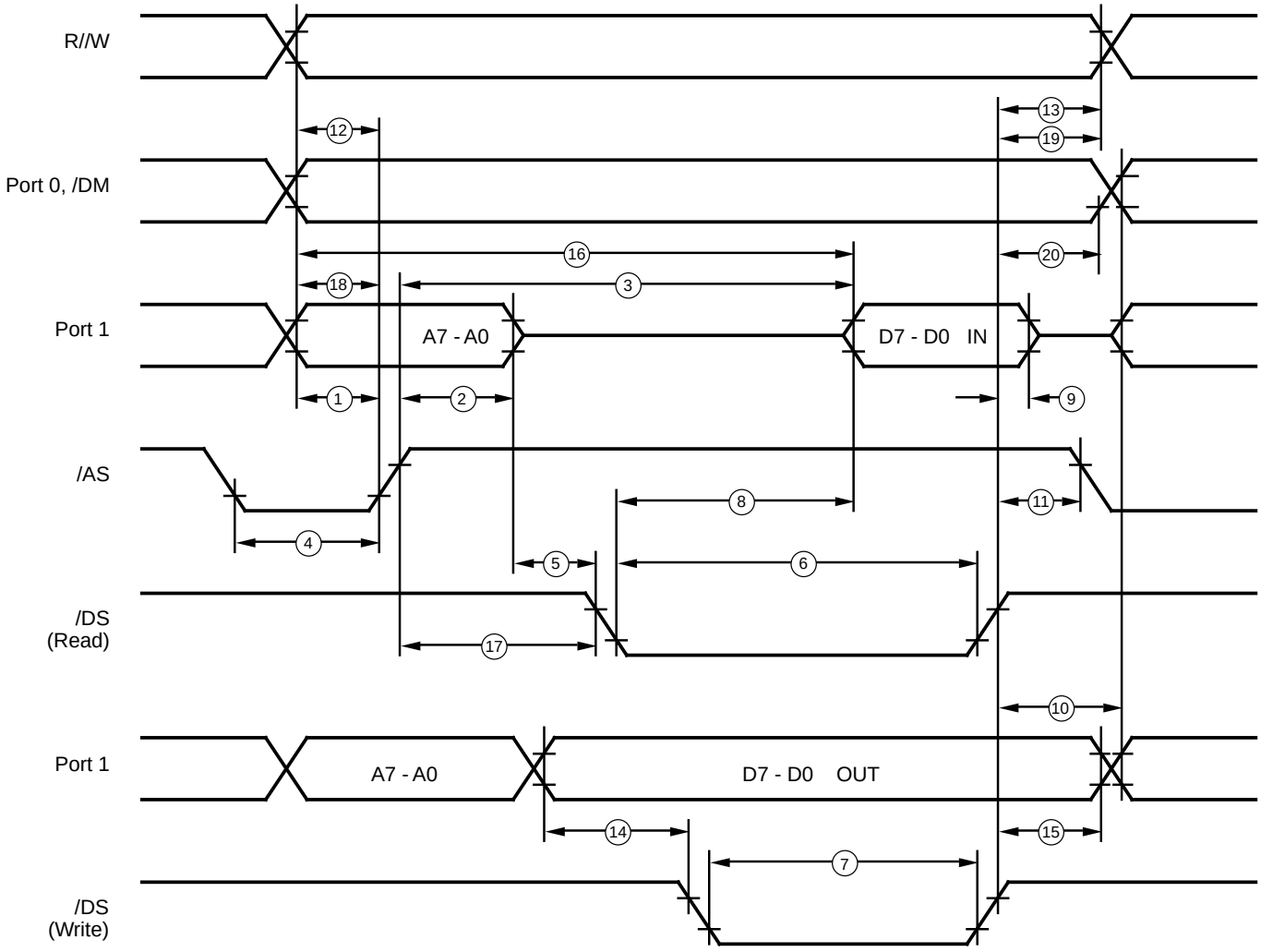


Figure 5. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

Preliminary

External I/O or Memory Read and Write Timing Table

				T_A = 0°C to +70°C			
No	**Sym**	**Parameter**	**V_{CC}**	**MIn**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS Rising Delay	2.0V 3.9V	55 55		ns ns	2
2	TdAS(A)	/AS Rising to Address Float Delay	2.0V 3.9V	70 70		ns ns	2
3	TdAS(DR)	/AS Rising to Read Data Required Valid	2.0V 3.9V		400 400	ns ns	1,2
4	TwAS	/AS Low Width	2.0V 3.9V	80 80		ns ns	2
5	Td	Address Float to /DS Falling	2.0V 3.9V	0 0		ns ns	
6	TwDSR	/DS (Read) Low Width	2.0V 3.9V	300 300		ns ns	1,2
7	TwDSW	/DS (Write) Low Width	2.0V 3.9V	165 165		ns ns	1,2
8	TdDSR(DR)	/DS Falling to Read Data Required Valid	2.0V 3.9V		260 260	ns ns	1,2
9	ThDR(DS)	Read Data to /DS Rising Hold Time	2.0V 3.9V	0 0		ns ns	2
10	TdDS(A)	/DS Rising to Address Active Delay	2.0V 3.9V	85 95		ns ns	2
11	TdDS(AS)	/DS Rising to /AS Falling Delay	2.0V 3.9V	60 70		ns ns	2
12	TdR/W(AS)	R//W Valid to /AS Rising Delay	2.0V 3.9V	70 70		ns ns	2
13	TdDS(R/W)	/DS Rising to R//W Not Valid	2.0V 3.9V	70 70		ns ns	2
14	TdDW(DSW)	Write Data Valid to /DS Falling (Write) Delay	2.0V 3.9V	80 80		ns ns	2
15	TdDS(DW)	/DS Rising to Write Data Not Valid Delay	2.0V 3.9V	70 80		ns ns	2
16	TdA(DR)	Address Valid to Read Data Required Valid	2.0V 3.9V		475 475	ns ns	1,2
17	TdAS(DS)	/AS Rising to /DS Falling Delay	2.0V 3.9V	100 100		ns ns	2
18	TdDM(AS)	/DM Valid to /AS Falling Delay	2.0V 3.9V	55 55		ns ns	2
19	TdDS(DM)	/DS Rise to /DM Valid Delay	2.0V 3.9V	70 70		ns ns	
20	ThDS(A)	/DS Rise to Address Valid Hold Time	2.0V 3.9V	70 70		ns ns	

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.

Standard Test Load

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS

Additional Timing Diagram

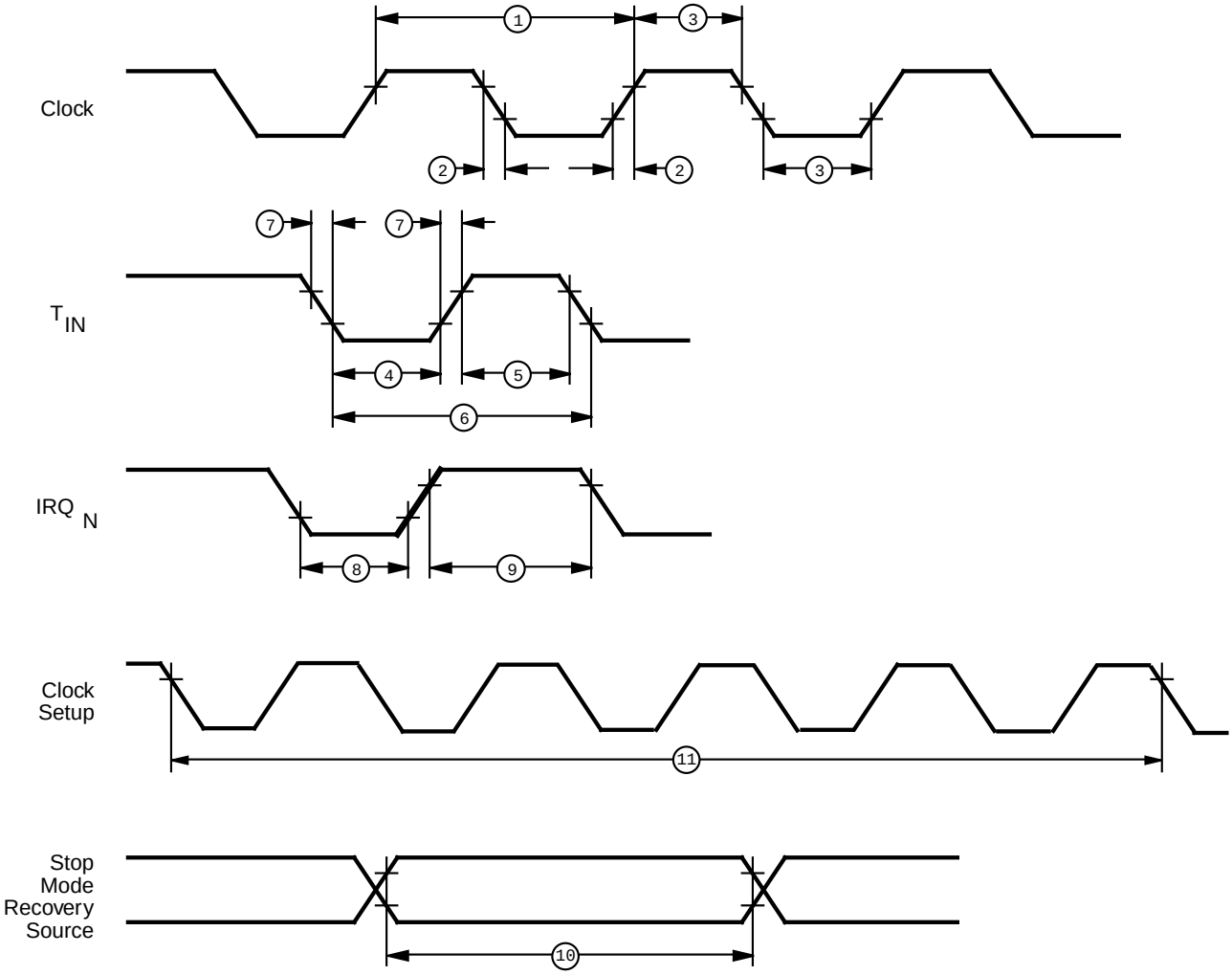


Figure 6. Additional Timing

AC CHARACTERISTICS

Preliminary

Additional Timing Table

				T_A = 0°C to +70°C 8.0 MHz			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	2.0V	121	DC	ns	1
			3.9V	121	DC	ns	1
2	TrC,TfC	Clock Input Rise	2.0V		25	ns	1
		and Fall Times	3.9V		25	ns	1
3	TwC	Input Clock Width	2.0V	37		ns	1
			3.9V	37		ns	1
4	TwTinL	Timer Input	2.0V	100		ns	1
		Low Width	3.9V	70		ns	1
5	TwTinH	Timer Input	2.0V	3TpC			1
		High Width	3.9V	3TpC			1
6	TpTin	Timer Input Period	2.0V	8TpC			1
			3.9V	8TpC			1
7	TrTin,TfTin	Timer Input Rise	2.0V		100	ns	1
		and Fall Timers	3.9V		100	ns	1
8A	TwIL	Interrupt Request	2.0V	100		ns	1,2
		Low Time	3.9V	70		ns	1,2
8B	TwIL	Int. Request	2.0V	5TpC			1,3
		Low Time	3.9V	5TpC			1,3
9	TwIH	Interrupt Request	2.0V	5TpC			1,2
		Input High Time	3.9V	5TpC			1,2
10	Twsm	Stop-Mode Recovery Width	2.0V	12		ns	5
		Spec	3.9V	12		ns	5
			2.0V	5TpC		ns	4
			3.9V	5TpC		ns	4
11	Tost	Oscillator Start-up Time	2.0V		5TpC		4
			3.9V		5TpC		4
12	Twdt	Watch-Dog Timer (5 ms)	2.0V	10	75	ms	
		Delay Time	3.9V	5	20	ms	
		(10 ms)	2.0V	30	150	ms	
			3.9V	10	40	ms	
		(15 ms)	2.0V	50	300	ms	
			3.9V	20	80	ms	
		(80 ms)	2.0V	200	1200	ms	
			3.9V	80	320	ms	

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Interrupt request through Port 3 (P30).
4. SMR – D5 = 0
5. SMR – D5 =1

AC CHARACTERISTICS

Handshake Timing Diagrams

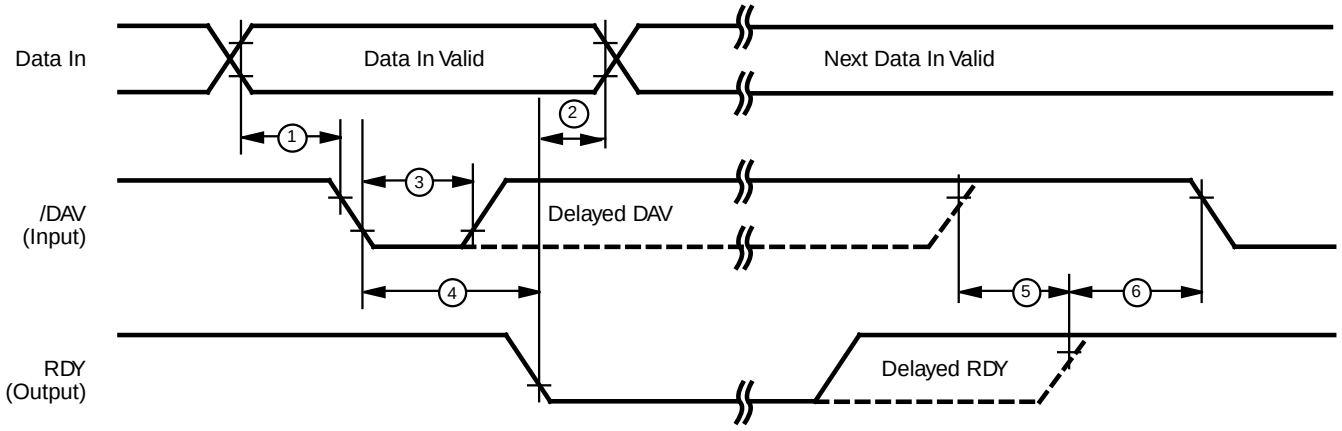


Figure 7. Input Handshake Timing

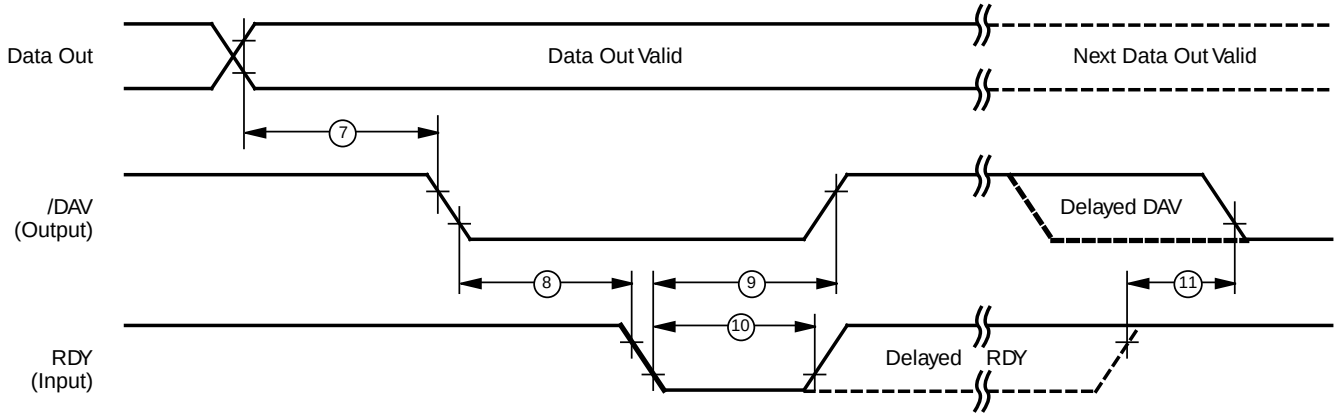


Figure 8. Output Handshake Timing

AC CHARACTERISTICS

Preliminary

Handshake Timing Table

				T_A = 0°C to +70°C 8 MHz		Data
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Direction**
1	TsDI(DAV)	Data In Setup Time	2.0V	0		IN
			3.9V	0		IN
2	ThDI(DAV)	Data In Hold Time	2.0V	160		IN
			3.9V	115		IN
3	TwDAV	Data Available Width	2.0V	155		IN
			3.9V	110		IN
4	TdDAVI(RDY)	DAV Falling to RDY	2.0V		160	IN
		Falling Delay	3.9V		115	IN
5	TdDAVId(RDY)	DAV Rising to RDY	2.0V		120	IN
		Falling Delay	3.9V		80	IN
6	TdRDYO(DAV)	RDY Rising to DAV	2.0V	0		IN
		Falling Delay	3.9V	0		IN
7	TdDO(DAV)	Data Out to DAV	2.0V	63		OUT
		Falling Delay	3.9V	63		OUT
8	TdDAV0(RDY)	DAV Falling to RDY	2.0V	0		OUT
		Falling Delay	3.9V	0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV	2.0V		160	OUT
		Rising Delay	3.9V		115	OUT
10	TwRDY	RDY Width	2.0V	110		OUT
			3.9V	80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV	2.0V		110	OUT
		Falling Delay	3.9V		80	OUT

Notes:

Writing or reading the Extended Data RAM is accomplished by using LDE instruction only.

PIN FUNCTIONS

XTAL1 Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

Port 0 (P07 and 00). Port 0 is an 2-bit, bidirectional, CMOS-compatible port. These two I/O lines are configured under software control, and the output drivers are push-pull.

If one or both bits are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional 200 KOhm pull-up is available as a mask option on P07 and P00.

These pull-ups are disabled when configured (bit by bit) as outputs.

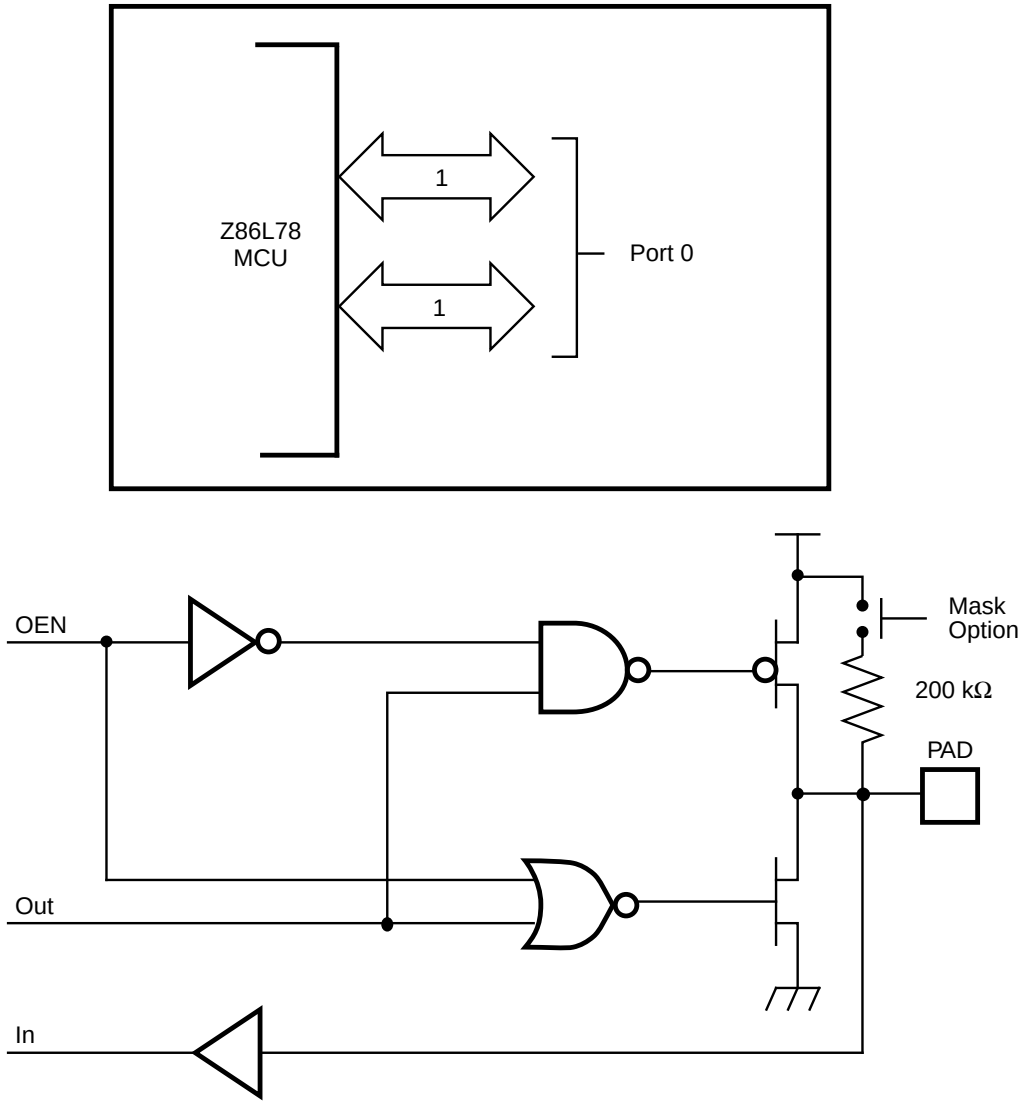


Figure 9. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight 200 KOhm (±50%) pull-up resistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The Z86L78 wakes up with the eight bits of Port 2 configured as inputs with open-drain outputs.

Port 2 also has an 8-bit input OR and an AND gate which can be used to wake up the part (Figure 33). P20 can be programmed to access the edge selection circuitry (Figure 10).

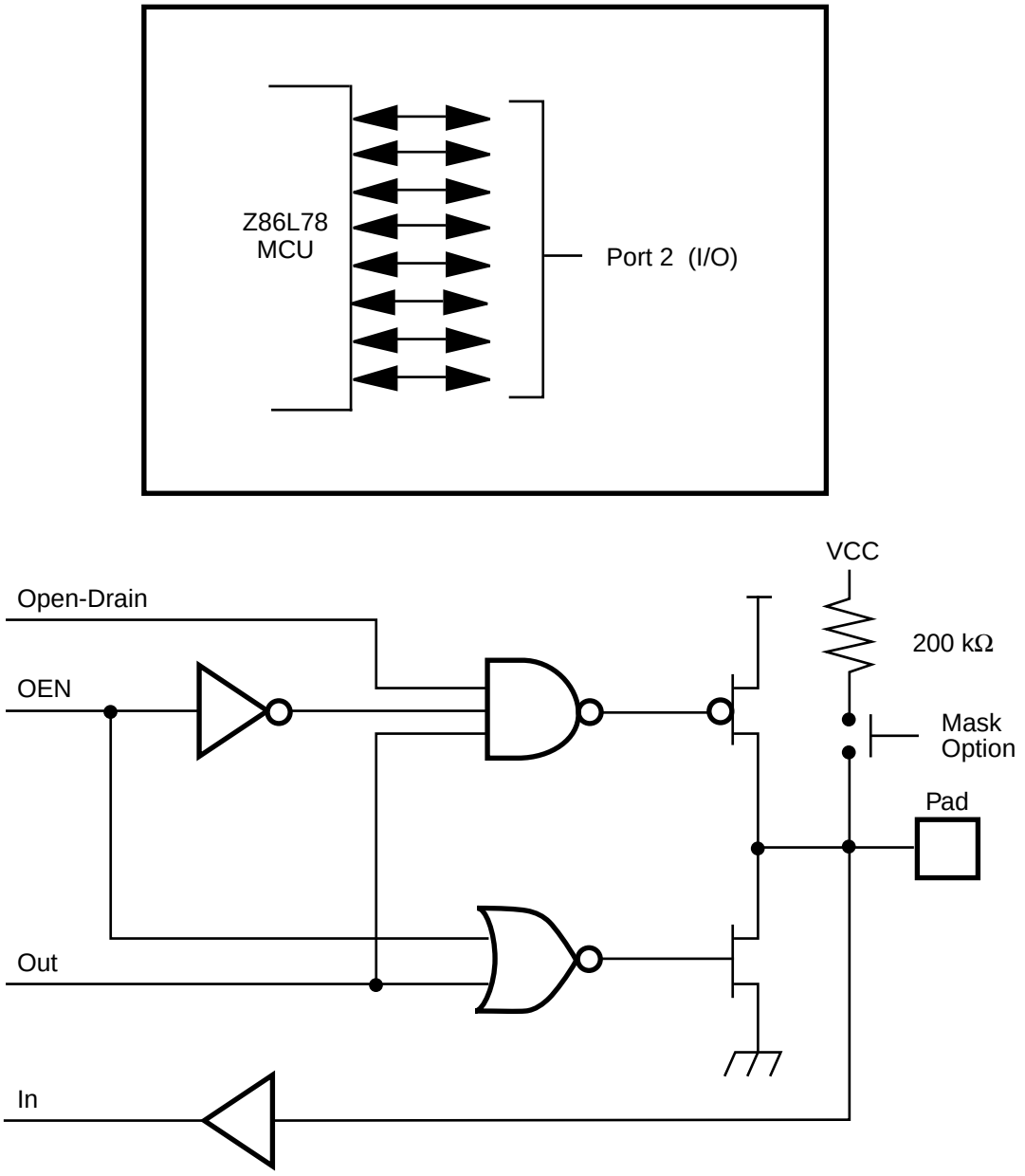


Figure 10. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P31). Port 3 is a 6-bit, CMOS-compatible three fixed input and four fixed output port. Port 3 and can be configured under software control for Input/Output, Interrupt, and output from the counter/timers. P31, P32, and P33 are standard CMOS inputs. Outputs P34, P35 are push-pull or open-drain depending on P3M D0. P36 is push-pull.

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage inputs. Access to the edge detection circuit is through P31 or P20. P33 will be in common to both comparators.

Port 3 provides output for each of the counter/timers and the AND/OR Logic. Control is performed by programming bits D5-D4 of CTRI, bit 0 of CTR0 and bit 0 of CTR2.

Table 2. Port 3 Pin Assignments

Pin	I/O	C/T	Comp.	Int.	P0 HS	P1 HS	P2 HS	Ext
Pref1	IN		RF1					
P31	IN	ISP	AN1	IRQ2			D/R	
P32	IN		AN2		D/R			
P33	IN		RF2	IRQ1		D/R		
P34	OUT	T8	A01			R/D		DM
P35	OUT	T16			R/D			
P36	OUT	T8/16					R/D	
P00	I/O							

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Comparator Inputs. In Analog Mode, Port 3, P31 and P32 have a comparator front end. The comparator reference voltages are on P33. The internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR. In this mode, any of the Stop-Mode Recovery sources can be used to toggle the P33 bit or generate IRQ1. In digital mode, P33 can be used as a Port 3 register input or IRQ1 for P33 (Figure 9).

Notes: Comparators are powered down by entering STOP Mode. For P33-P31 to be used as a STOP-mode recovery source, these inputs must be placed into digital mode.

Comparator Outputs. Comparator output of COMP1 can be programmed to output on P34 through the PCON register (Figure 8).

/RESET (Input, active Low). Initializes the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer; Stop-Mode Recovery, and Low Voltage detection. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the internal reset Low for the POR time.

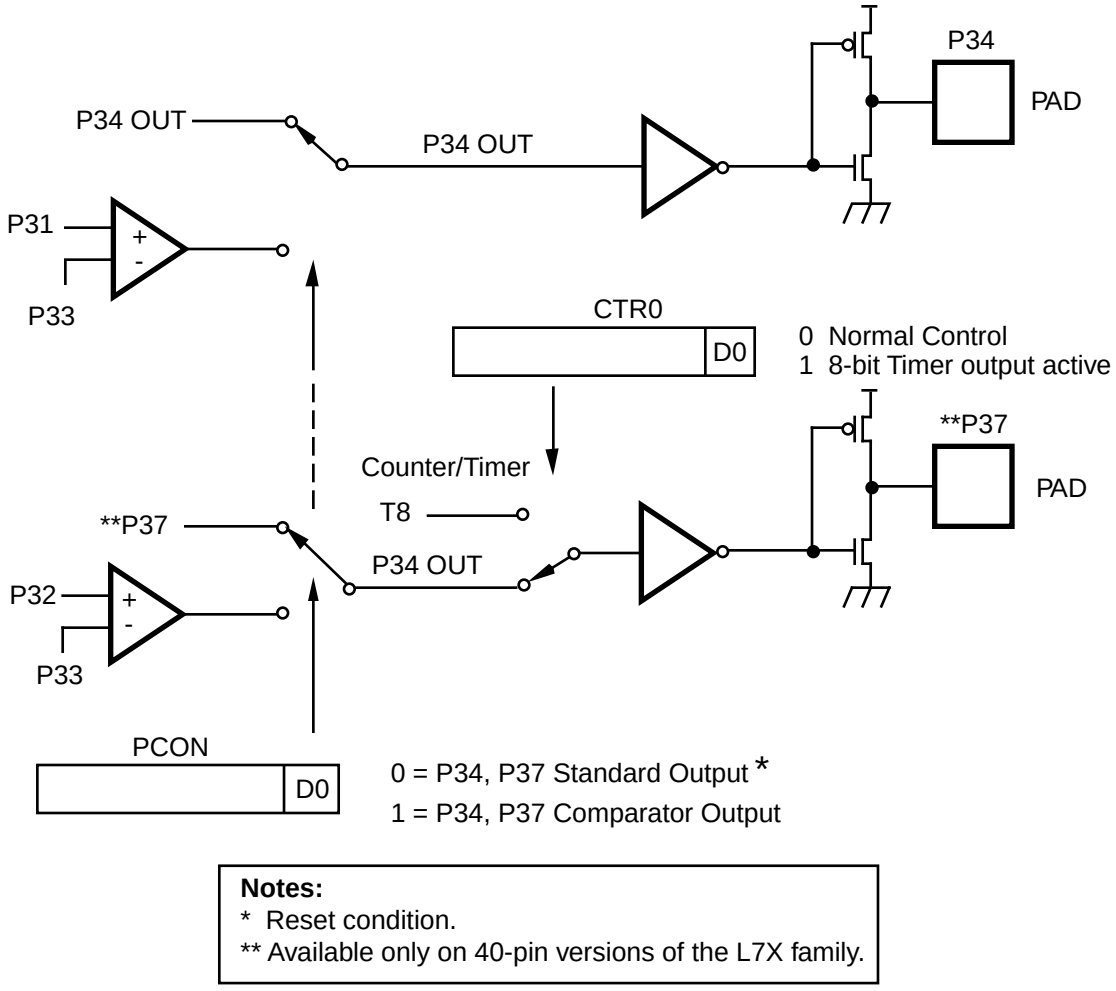


Figure 11. Port 3 Configuration

PIN FUNCTIONS (Continued)

Program execution begins at location 000CH, 5-10 TpC cycles after the RST is asserted. For Power-On Reset, the typical reset output time is 5 ms.

Note: The Z86L78 does not reset WDTMR, SMR, P2M, or P3M registers on a Stop-Mode Recovery operation.

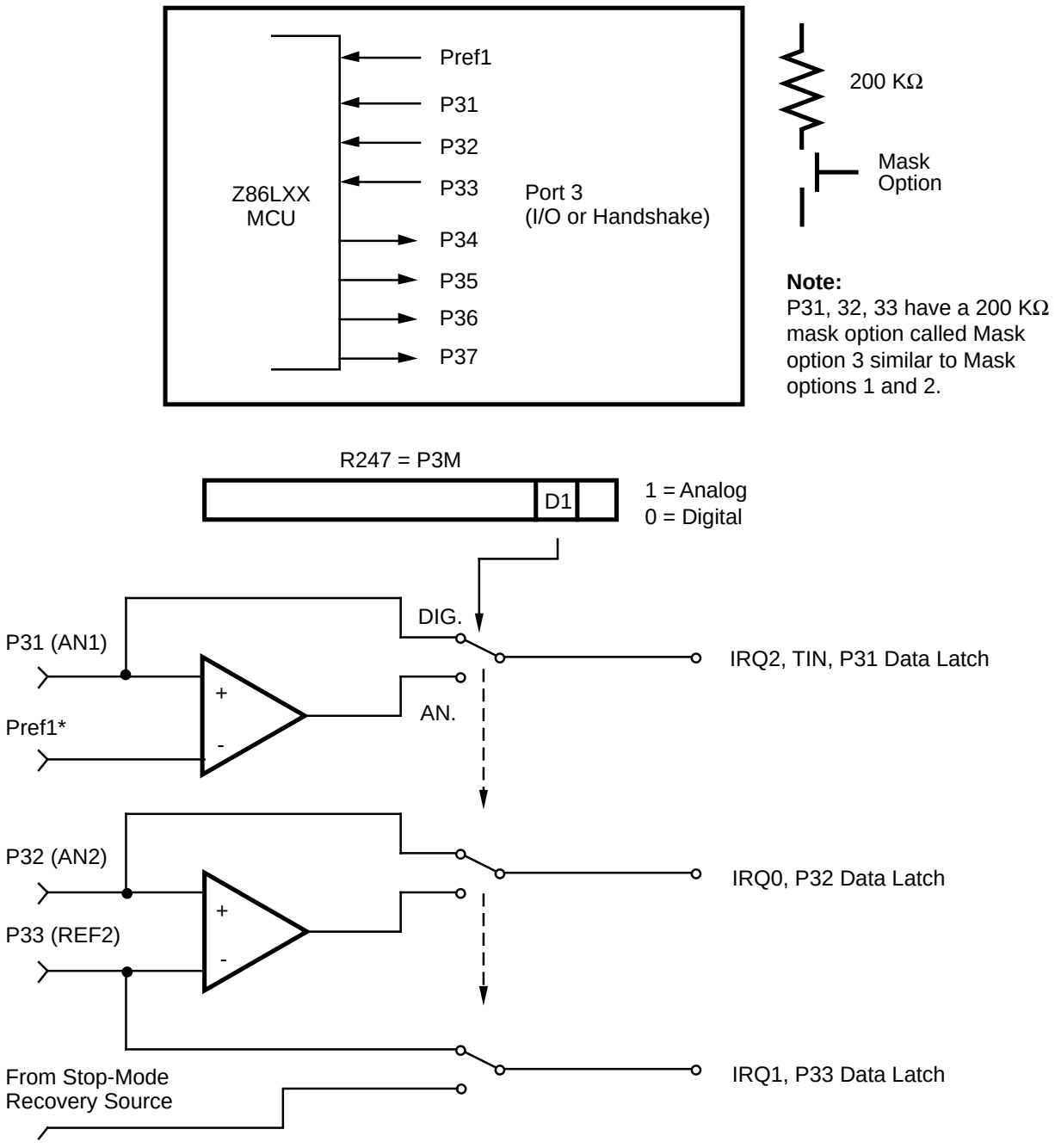


Figure 12. Port 3 Configuration

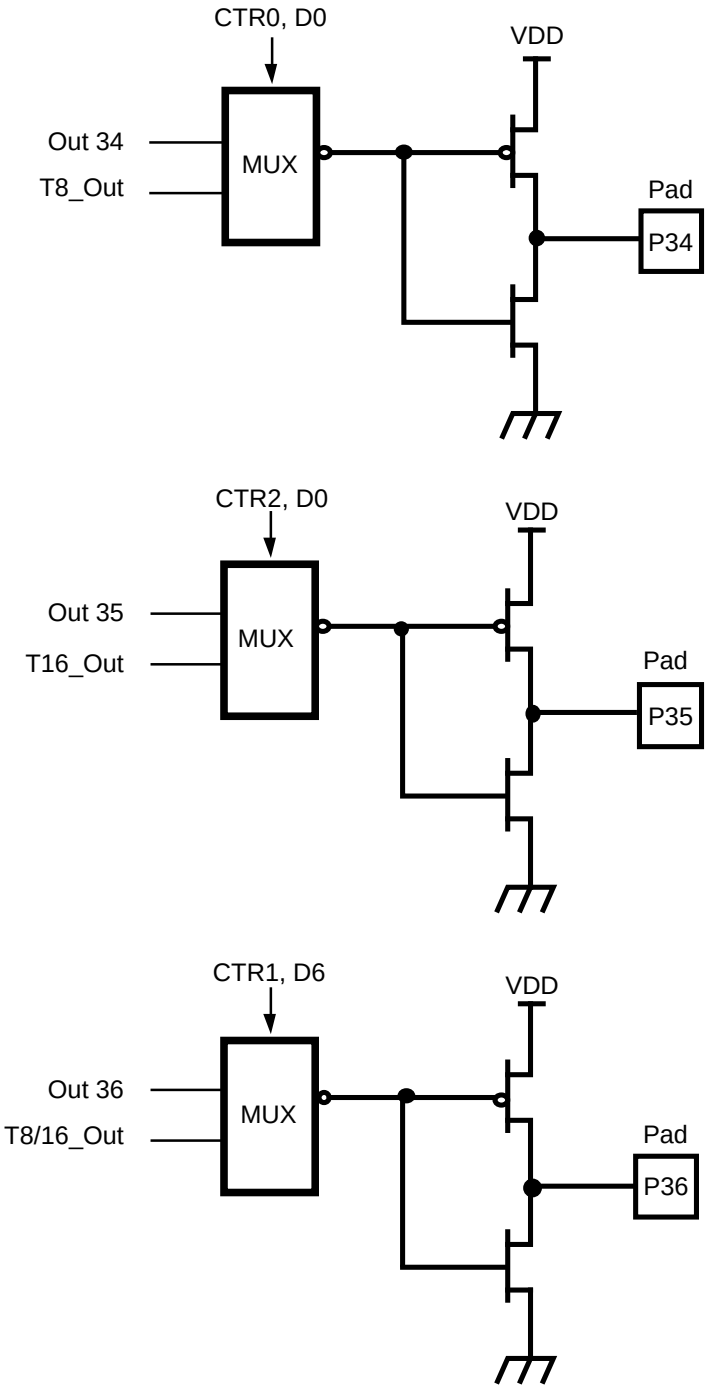


Figure 13. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The Z86L78 incorporates special features to enhance the standard Z8 core architecture to provide the user with increased design flexibility in the areas of consumer and battery operated applications.

Reset. The device is reset in one of the following conditions:

1. Power-On Reset
2. Watch-Dog Timer
3. Stop-Mode Recovery Source
4. Low Voltage Detection

Program Memory. The Z86L78 addresses up to 16 KB of internal program memory (Figure 14). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain five 16-bit vectors that correspond to the five available interrupts. Addresses to 16K consist of on-chip mask-programmed ROM.

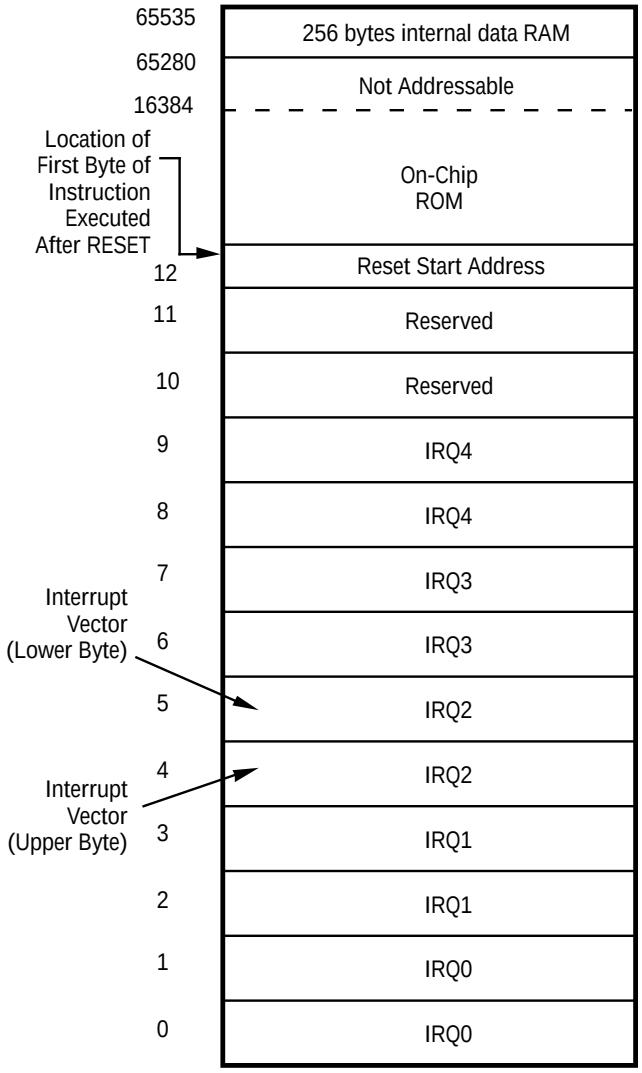


Figure 14. Program Memory Map

RAM. The Z86L78 has 512-bytes of RAM and 256 bytes make-up the Register file. The remaining 256 bytes make up the Extended Data RAM.

Extended Data RAM. The Extended Data RAM occupies the address range. FF00H-FFFFH (256 bytes). Accessing the Extended Data RAM is accomplished by using LDE instruction only.

Note: The Extended Data RAM cannot be used as Stack or instructions/code memory.

Expanded Register File (ERF). The standard Z8 register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has been implemented as 16 groups of 16 registers per group. These register groups are known as the Expanded Register File (ERF). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 16).

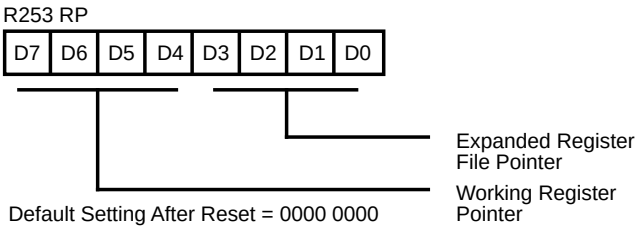


Figure 15. Register Pointer Register

The upper nibble of the register pointer (Figure 18) selects which group of 16 bytes in the register file, out of the full 256 bytes, will be accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86L78, Banks F and D are implemented. A 0H in the lower nibble will allow the normal register file to be addressed, but any other value from 1H to FH will exchange the lower 16 registers in favor of an expanded register group of 16 registers.

For example:

Z86L78: (See Figure 17)

R253 RP = 00H R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0DH R0 = CTRL0
R1 = CTRL1
R2 = CTRL2
R3 = Reserved

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

LD RP, #0DH Select ERF D for access and register Bank 0 as the working register group

LD R0,#xx access CTRL0

LD1, #xx access CTRL1

LDRP, #7DH Select expanded register group (ERF) group D for access and register Bank 7 as the working register bank

LDR1, 2 CTRL2 $\rightarrow$ register 71H

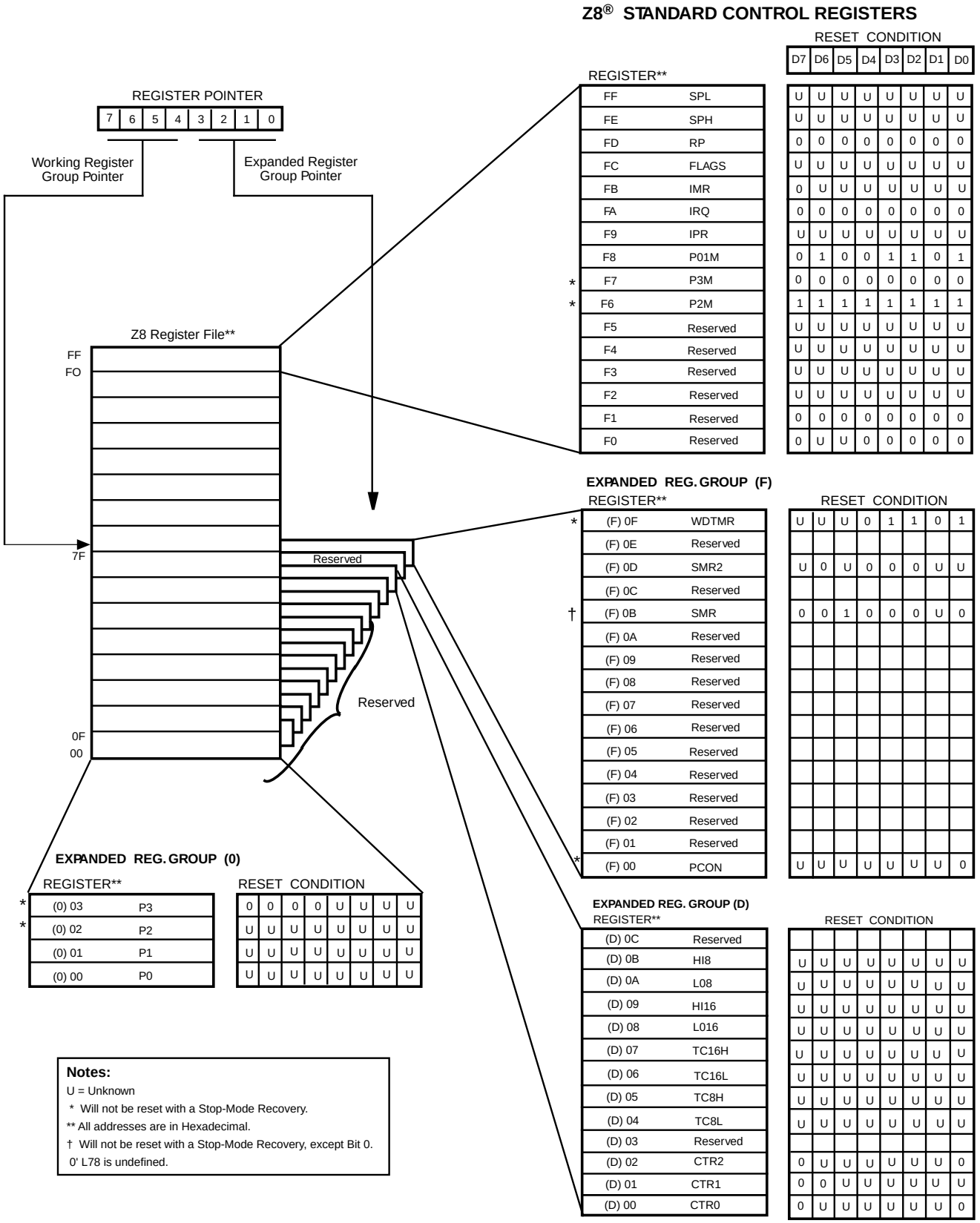


Figure 16. Expanded Register File Architecture

Register File. The register file (group 0) consists of four I/O port registers, 236 general-purpose registers, and 16 control and status registers (R0-R3, R4-R239, and R240-R255, respectively), Plus two expanded registers groups (Banks D and F). Instructions can access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 15). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group. **Note: Registers E0-EF of Bank 0 are only accessed through working registers and indirect addressing modes.**

Stack. The Z86L78 internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the general-purpose registers (R4-R239). SPH is used as a general-purpose register only when using internal stacks. Note: Only the lower 256 bytes of RAM may be used for stack operations.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH will be loaded into Port 0 whenever the internal stack is accessed.

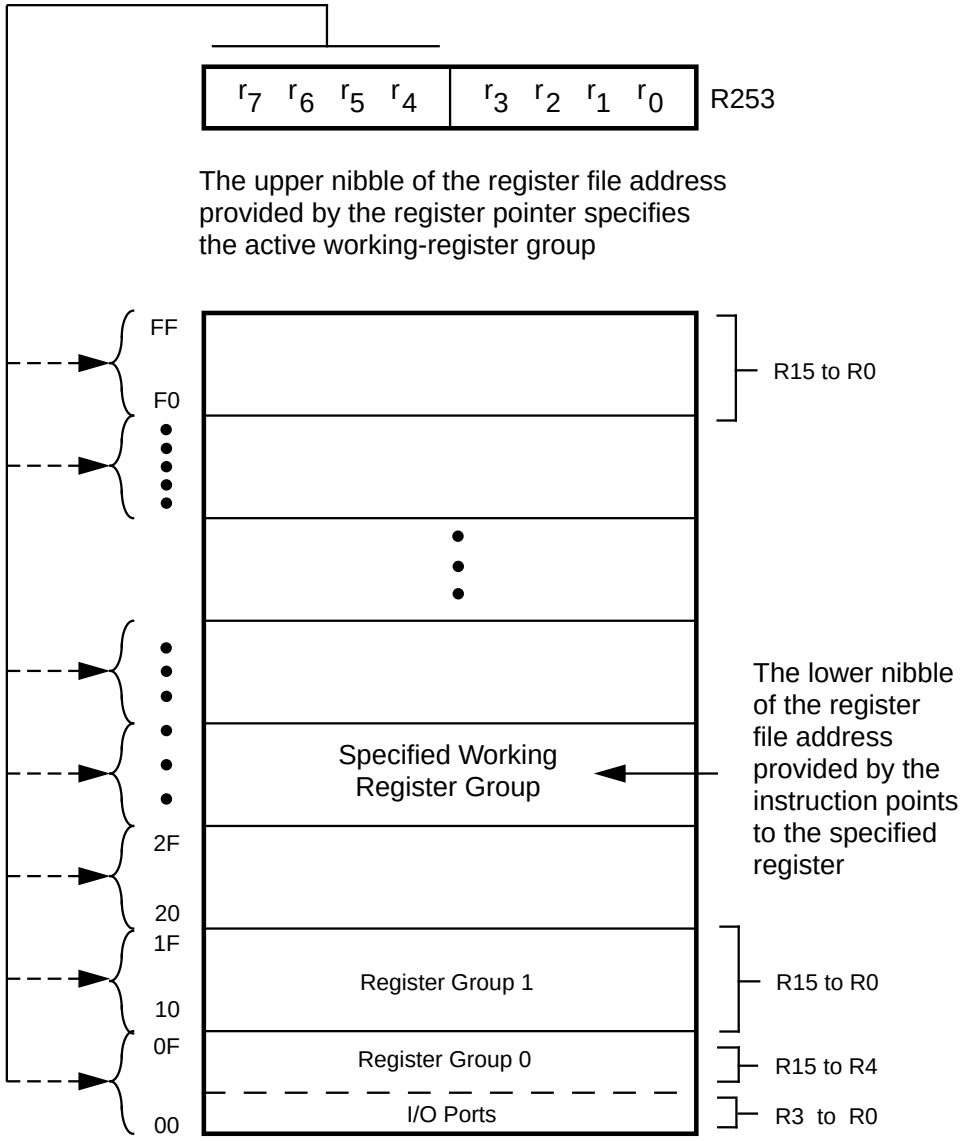


Figure 17. Register Pointer

Counter/Timer Register Description

Expanded Register Group D

(D)%0C	Reserved
(D)%0B	HI8
(D)%0A	LO8
(D)%09	HI16
(D)%08	LO16
(D)%07	TC16H
(D)%06	TC16L
(D)%05	TC8H
(D)%04	TC8L
(D)%03	Reserved
(D)%02	CTR2
(D)%01	CTR1
(D)%00	CTR0

Register Description

HI8(D)%0B: Holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	76543210	R W	Captured Data No Effect

L08(D)%0A: Holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	76543210	R W	Captured Data No Effect

HI16(D)%09: Holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	76543210	R W	Captured Data No Effect

L016(D)%08: Holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	76543210	R W	Captured Data No Effect

TC16H(D)%07: Counter/Timer2 MS-Byte Hold Register.

Field	Bit Position		Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)%06: Counter/Timer2 LS-Byte Hold Register.

Field	Bit Position		Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)%05: Counter/Timer8 High Hold Register.

Field	Bit Position		Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)%04: Counter/Timer8 Low Hold Register.

Field	Bit Position		Description
T8_Level_LO	76543210	R/W	Data

CTR0 (D)00: Counter/Timer8 Control Register.

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6------	R/W	0	Modulo-N
			1	Single Pass
Time-Out	--5-----	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1‘	Reset Flag to 0
T8_Clock	---43---	R/W	0 0	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P34_Out	-------0	R/W	0*	P34 as Port Output*
			1	T8 Output on P34

Note: *Indicates the value upon Power-On Reset

CTR0: Counter/Timer8 Control Register Description

T8 Enable. This field enables T8 when set (written) to 1.

Single/Modulo-N. When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Time-Out. This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 should be written to this location. This is the only way to reset this status condition, therefore, care should be taken to reset this bit prior to using/enabling the counter/timers.

Note: Care must be taken when utilizing the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers will be ORed or ANDed with the designated value and then written back into the registers. Example: When the status of bit 5 is 1, a reset condition will occur.

T8 Clock. Defines the frequency of the input signal to T8.

Capture_INT_Mask. Set this bit to allow interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask. Set this bit to allow interrupt when T8 has a time out.

P34_Out. This bit defines whether P34 is used as a normal output pin or the T8 output.

CTR1(D)%01: Controls the functions in common with the T8 and T16.

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	Transmit Mode
			1	Demodulation Mode
P36_Out/Demodulator_Input	-6------	R/W		Transmit Mode
			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/Edge Detect	--54----	R/W		Transmit Mode
			00	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/Glitch_Filter	----32--	R/W		Transmit Mode
			00	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	16 SCLK Cycle
Initial_T8_Out/Rising_Edge	------1-			Transmit Mode
			0	T8_OUT is 0 Initially
			1	T8_OUT is 0 Initially
				Demodulation Mode
			0	No Rising Edge
			1	Rising Edge Detected
			0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/Falling_Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 1 Initially
			1	T16_OUT is Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

CTR1 Register Description

Mode. If it is 0, the Counter/Timers are in the transmit mode, otherwise they are in the demodulation mode.

P36_Out/Demodulator_Input. In Transmit Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In Demodulation Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

T8/T16_Logic/Edge _Detect. In Transmit Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In Demodulation Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter. In Transmit Mode, this field defines whether T8 and T16 are in the "Ping-Pong" mode or in independent normal operation mode. Setting this field to "Normal Operation Mode" terminates the "Ping-Pong Mode" operation. When set to 10, T16 is immediately forced to a 0.

In Demodulation Mode, this field defines the width of the glitch that should be filtered out.

Initial_T8_Out/Rising_Edge. In Transmit Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When this bit is set to 1 or 0, T8_OUT will be set to the opposite state of this bit. This insures that when the clock is enabled a transition occurs to the initial state set by CTR1, D1.

In Demodulation Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge. In Transmit Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3, D2). When this bit is set, T16_OUT will be set to the opposite state of this bit. This insures that when the clock is enabled a transition occurs to the initial state set by CTR1, D0.

In Demodulation Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Note: Modifying CTR1, (D1 or D0) while counters are enabled will cause un-predictable output from T8/16_out.

CTR2 (D)%02: Counter/Timer16 Control Register.

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6------	R/W		Transmit Mode
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	---43---	R/W	00	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
				Enable Time-Out Int.
P35_Out	-------0	R/W	0	P35 as Port Output*
				T16 Output on P35

Note: * Indicates the value upon Power-On Reset.

CTR2 Description

T16_Enable. This field enables T16 when set to 1.

Single/Modulo-N. In Transmit Mode, when set to 0, the counter reloads the initial value when terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

In Demodulation Mode, when set to 0 , T16 captures and reloads on detection of all the edges; when set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode.

Time_Out. This bit is set when T16 times out (terminal count reached). In order to reset it, a 1 should be written to this location.

T16_Clock. Defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask. Set this bit to allow interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask. Set this bit to allow interrupt when T16 times out.

P35_Out. This bit defines whether P35 is used as a normal output pin or T16 output.

Port pins configured as outputs are ignored as an SMR2 recover source. For example, if NAND of P23-P20 is selected as the recover source and P20 is configured as output, then P20 is ignored as a recover source. The effective recover source in this case is NAND of P23-P21.

SMR2(F)%0D: Stop-Mode Recovery Register 2.

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0*	Low
			1	High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000*	A. POR Only
			001	B. NAND of P23-P20
			010	C. NAND of P27-P20
			011	D. NOR of P33-P31
			100	E. NAND of P33-P31
			101	F. NOR of P33-P31, P00,P07
			110	G. NAND of P33-P31,P00,P07
			111	H. NAND of P33-P31,P22-P20
Reserved	------10	00	Reserved (Must be 0)	

Note: * Indicates the value upon Power-On Reset.

Counter/Timer Functional Blocks

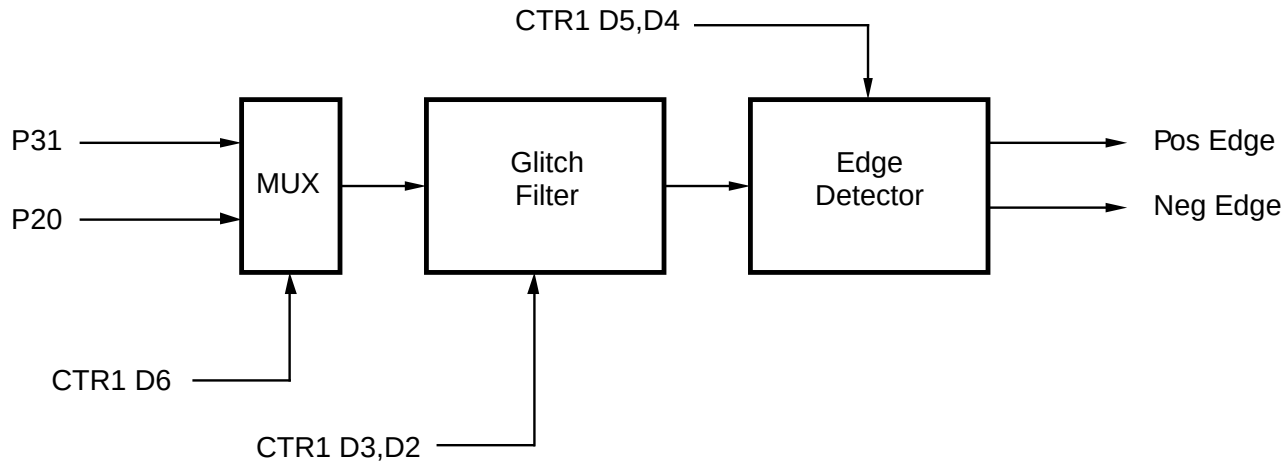


Figure 18. Glitch Filter Circuitry

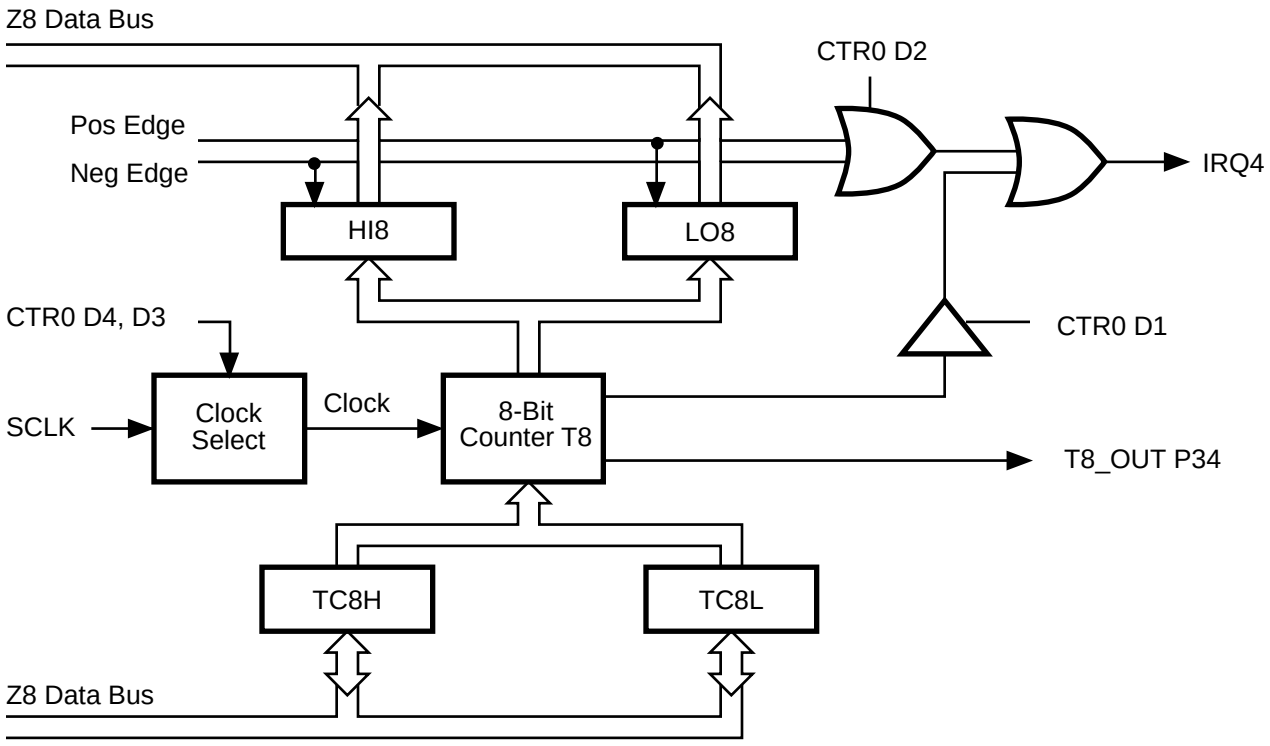


Figure 19. 8-Bit Counter/Timer Circuit

Input Circuit
The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5-D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal which have a width less than specified (CTR1 D3, D2) are filtered out.

T8 Transmit Mode
When T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1. If it is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded, otherwise TC8H is loaded into the counter. In Single-Pass Mode (CTR0 D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0 D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0 D1) (Figure 18). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. Then T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0 D5) and generates an interrupt if enabled (CTR0 D1) (Figure 19). This completes one cycle. T8 then loads from TC8H or TC8L according to the T8_OUT level, and repeats the cycle.

The user can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded. Care must be taken not to write these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. **An initial count of 1 is not allowed (a non-function will occur).** An initial count of 0 will cause TC8 to count from 0 to %FF to %FE (Note, % is used for hexadecimal values). Transition from 0 to %FF is not a time-out condition.

Note: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended. Two successive commands, first stopping the counter/timers, then resetting the status bits is necessary. This is required because it takes one counter/timer clock interval for the initiated event to actually occur.

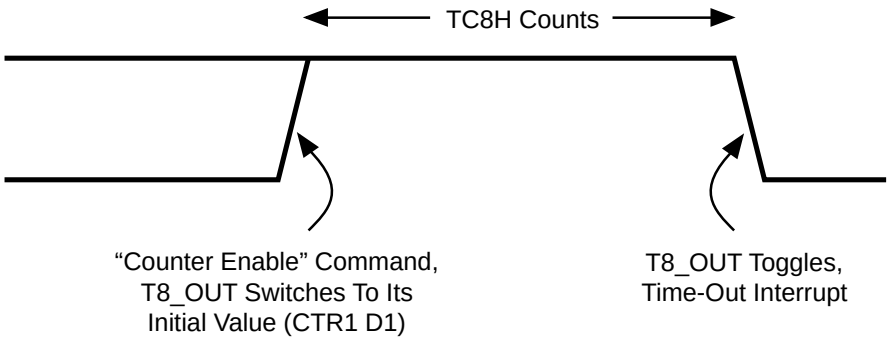


Figure 20. T8_OUT in SIngle-Pass Mode

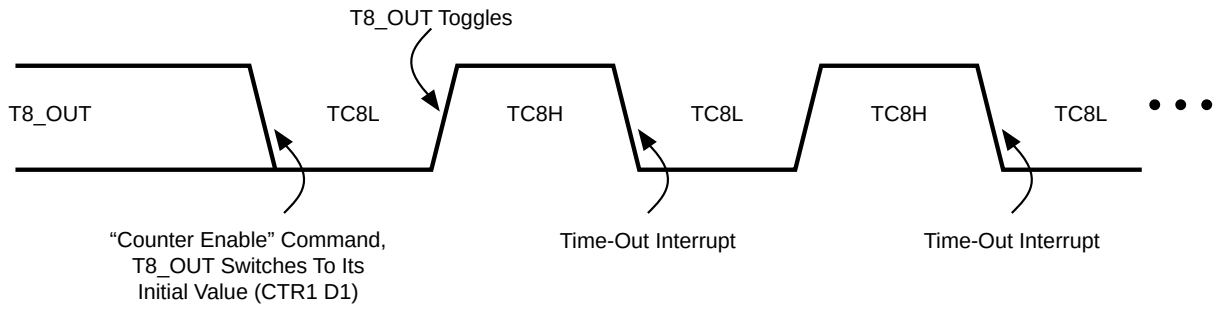


Figure 21. T8_OUT in Modulo-N Mode

FUNCTIONAL DESCRIPTION (Continued)

T8 Demodulation Mode

The user should program TC8L and TC8H to %FF. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8, if negative edge, HI8. One of the edge detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with %FF and starts counting again. Should T8 reach 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from %FF (Figure 23).

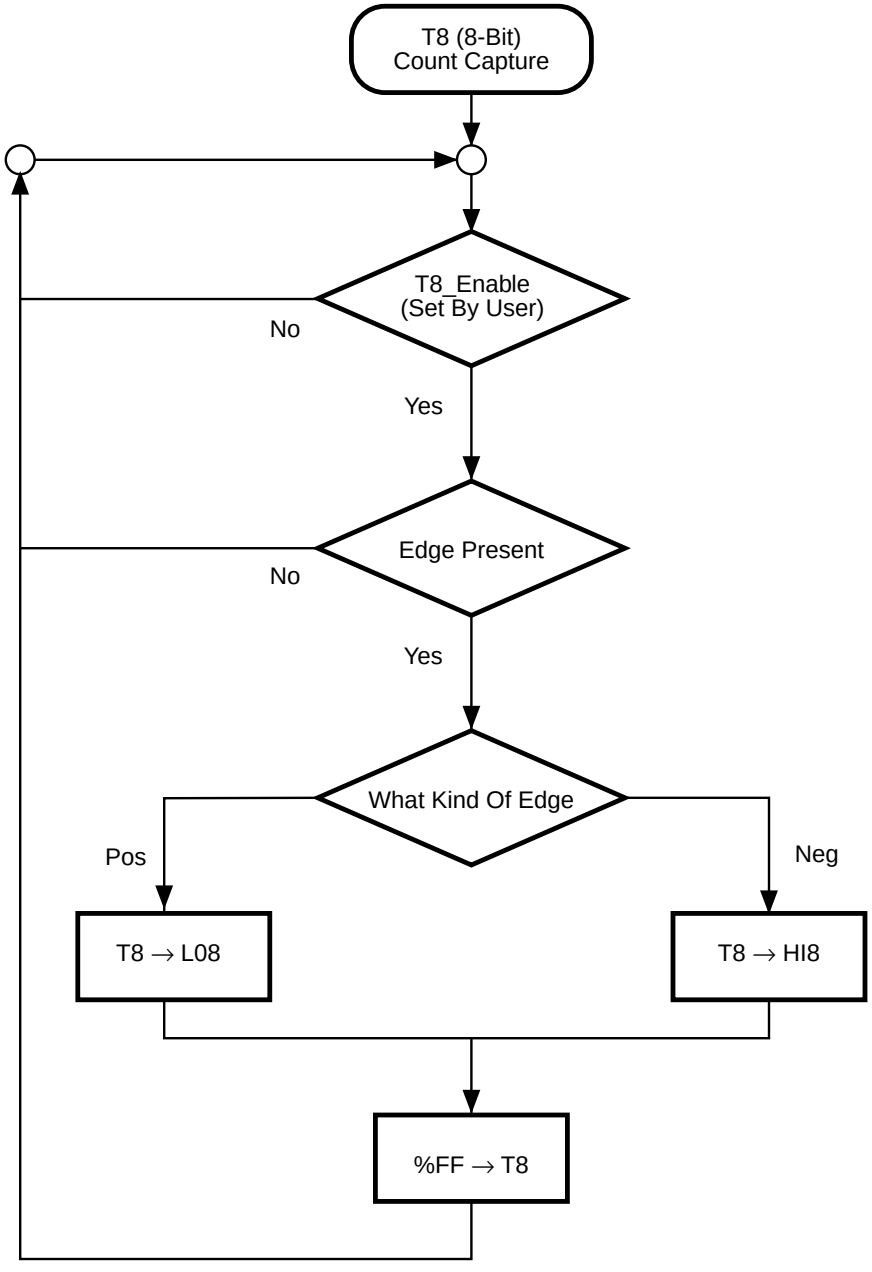


Figure 22. Demodulation Mode Count Capture Flowchart

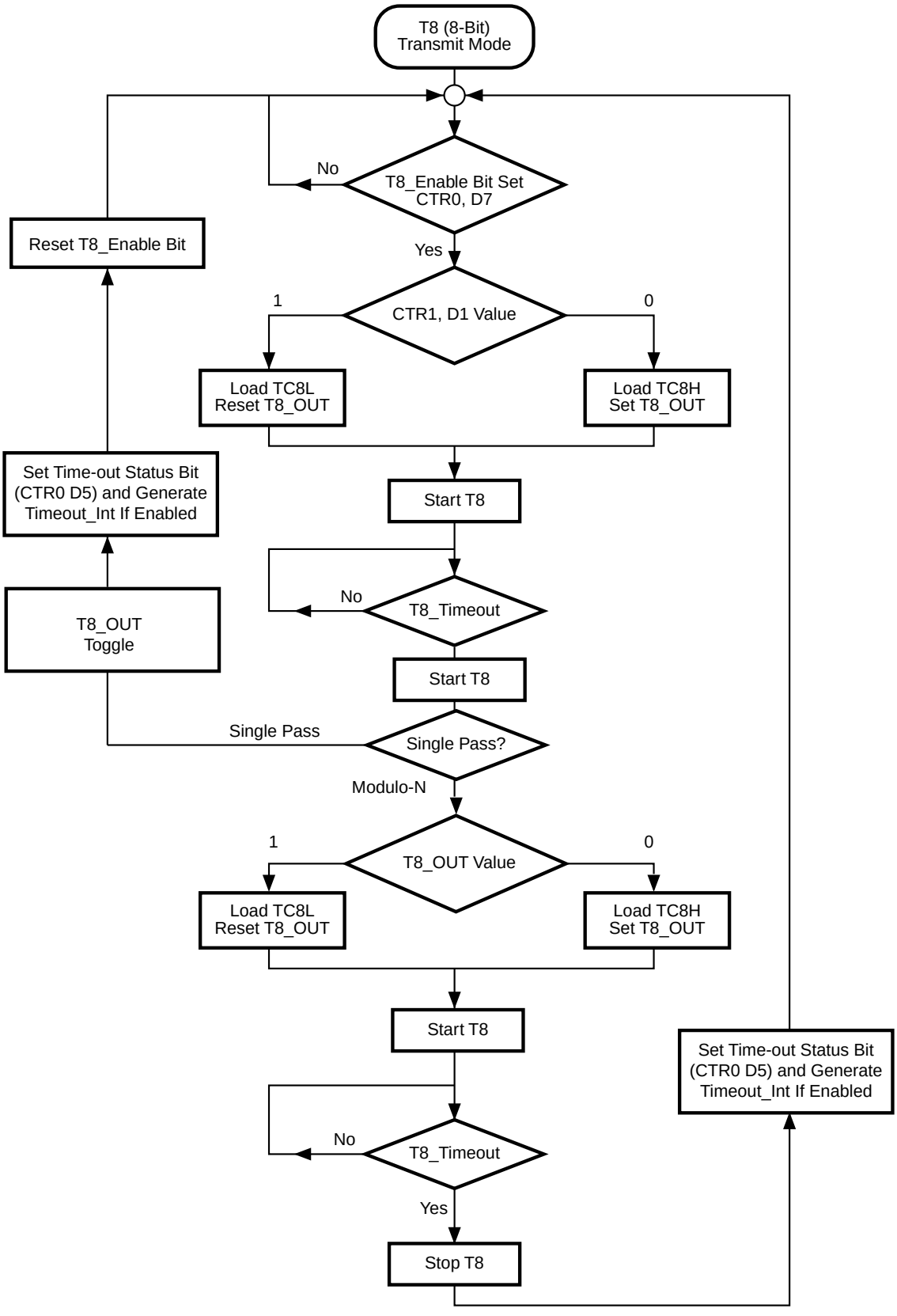


Figure 23. Transmit Mode Flowchart

FUNCTIONAL DESCRIPTION (Continued)

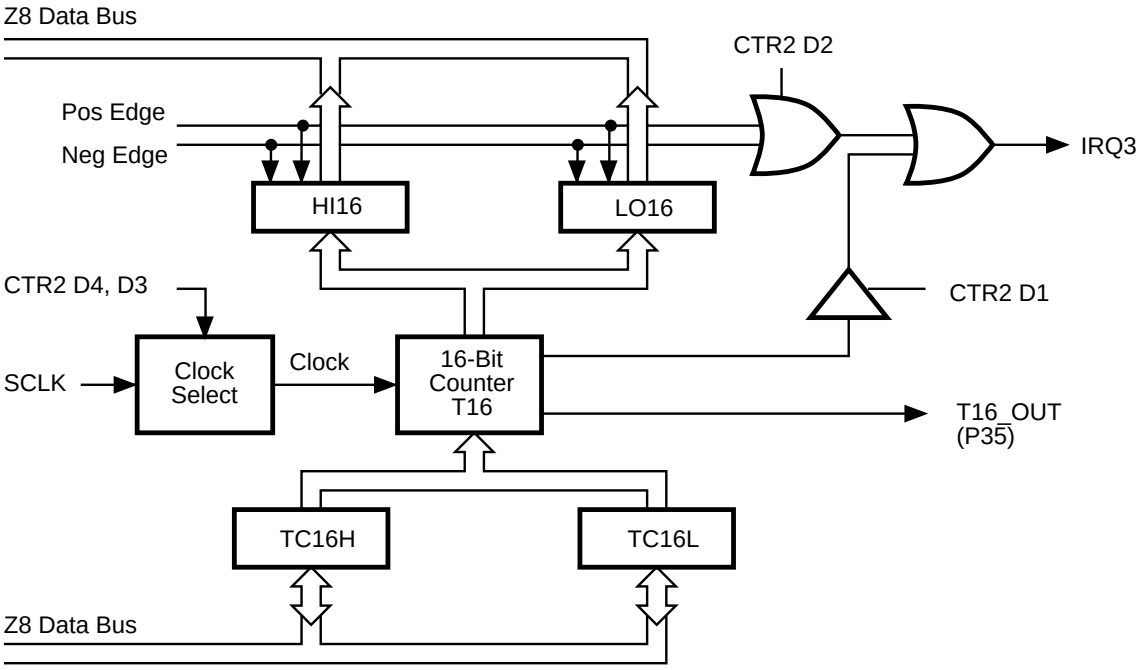


Figure 24. 16-Bit Counter/Timer Circuits

T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16 when not enabled is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. The user can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3, D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1 D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt is generated if enabled (CTR2 D1), and a status bit (CTR2 D5) is set. Note that global interrupts will override this function as described in the interrupts section. If T16 is in Single-Pass Mode, it is stopped at this point. If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L and the counting continues.

The user can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded. Care must be taken not to load these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 will cause T16 to count from 0 to %FFFF to %FFFE. Transition from 0 to %FFFF is not a time-out condition.

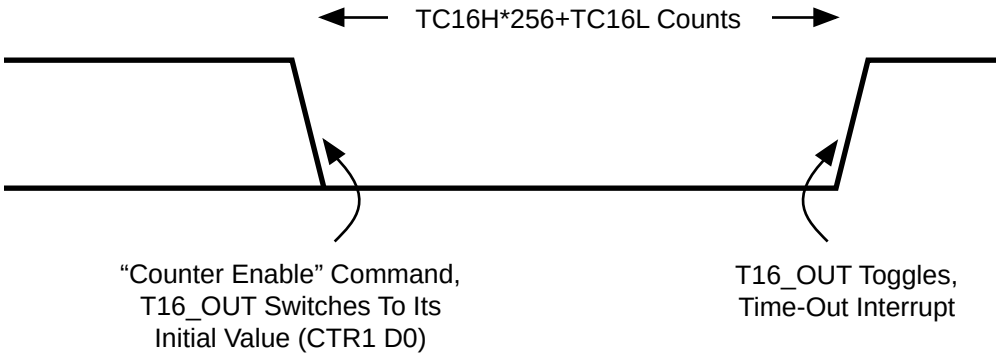


Figure 25. T16_OUT in Single-Pass Mode

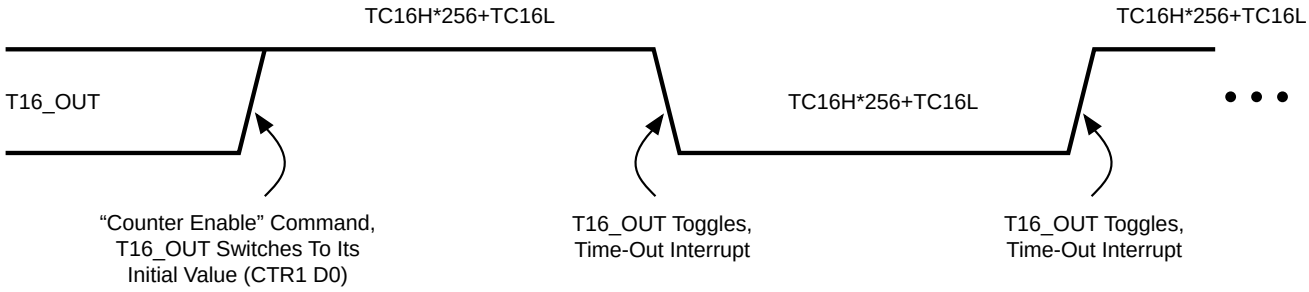


Figure 26. T16_OUT in Modulo-N Mode

T16 Demodulation Mode

The user should program TC16L and TC16H to %FF. After T16 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, T16 captures HI16 and LO16, reloads and begins counting.

If D6 of CTR2 is 0: When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current count in T16 is one's complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1 D1, D0) is set and an interrupt is generated if enabled (CTR2 D2). T16 is loaded with %FFFF and starts again.

If D6 of CTR2 is 1: T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 will cause T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 will capture and reload on the next edge (rising, falling, or both depending on CTR1 D5, D4) but continue to ignore subsequent edges.

Should T16 reach 0, it continues counting from %FFFF; meanwhile, a status bit (CTR2 D5) is set and an interrupt time-out can be generated if enabled (CTR2 D1).

FUNCTIONAL DESCRIPTION (Continued)

Ping-Pong Mode

This operation mode is only valid in Transmit Mode. T8 and T16 need to be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6) and Ping-Pong Mode needs to be programmed in CTR1 D3, D2. The user can begin the operation by enabling either T8 or T16 (CTR0 D7 or CTR2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1.

Note: Enabling Ping-Pong operation while the counter/timers are running may cause intermittent counter/timer function. Therefore, disable the counter/timers, then reset the status flags prior to instituting this operation.

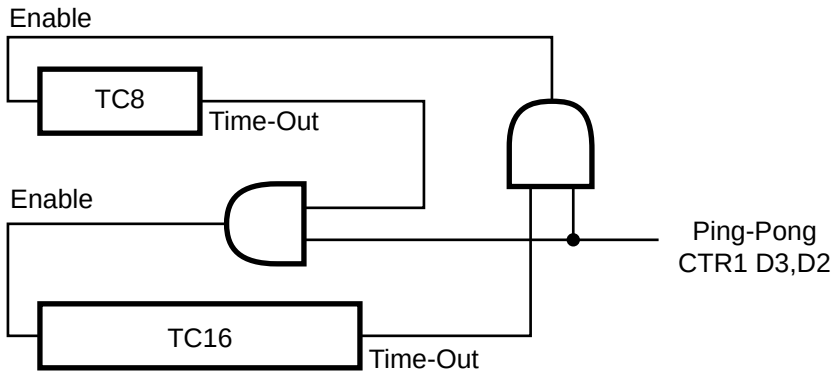


Figure 27. Ping-Pong Mode

To Initiate Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) will be cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) will be set every time the counter/timers reach the terminal count.

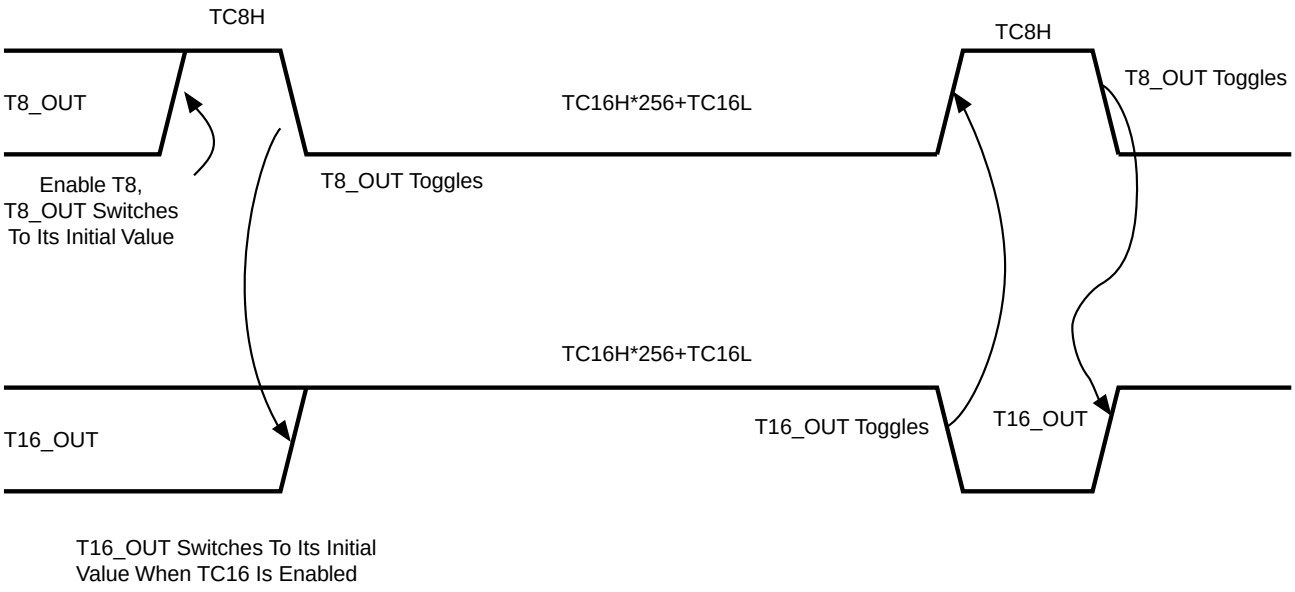


Figure 28. T8_OUT and T16_OUT in Ping-Pong Mode

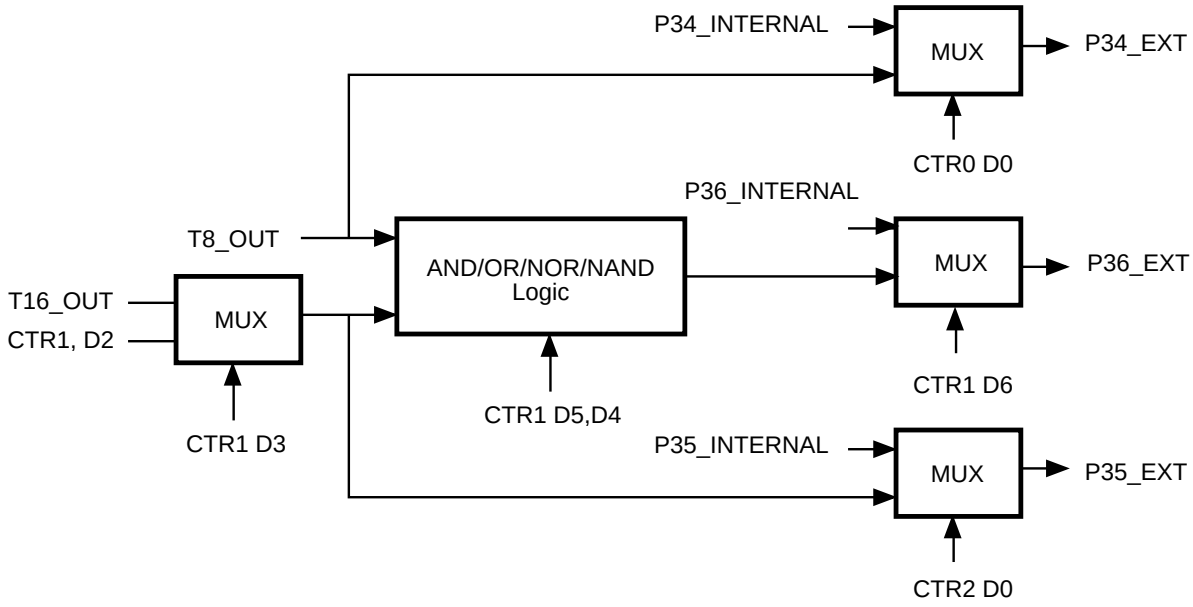


Figure 29. Output Circuit

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86L78 has five different interrupts, which are maskable and prioritized (Figure 30). The five sources are divided as follows: two are claimed by Port 3 lines P33, P31, one by the low voltage detect circuit (IRQ0) and the remaining two by the counter/timers (Table 5). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

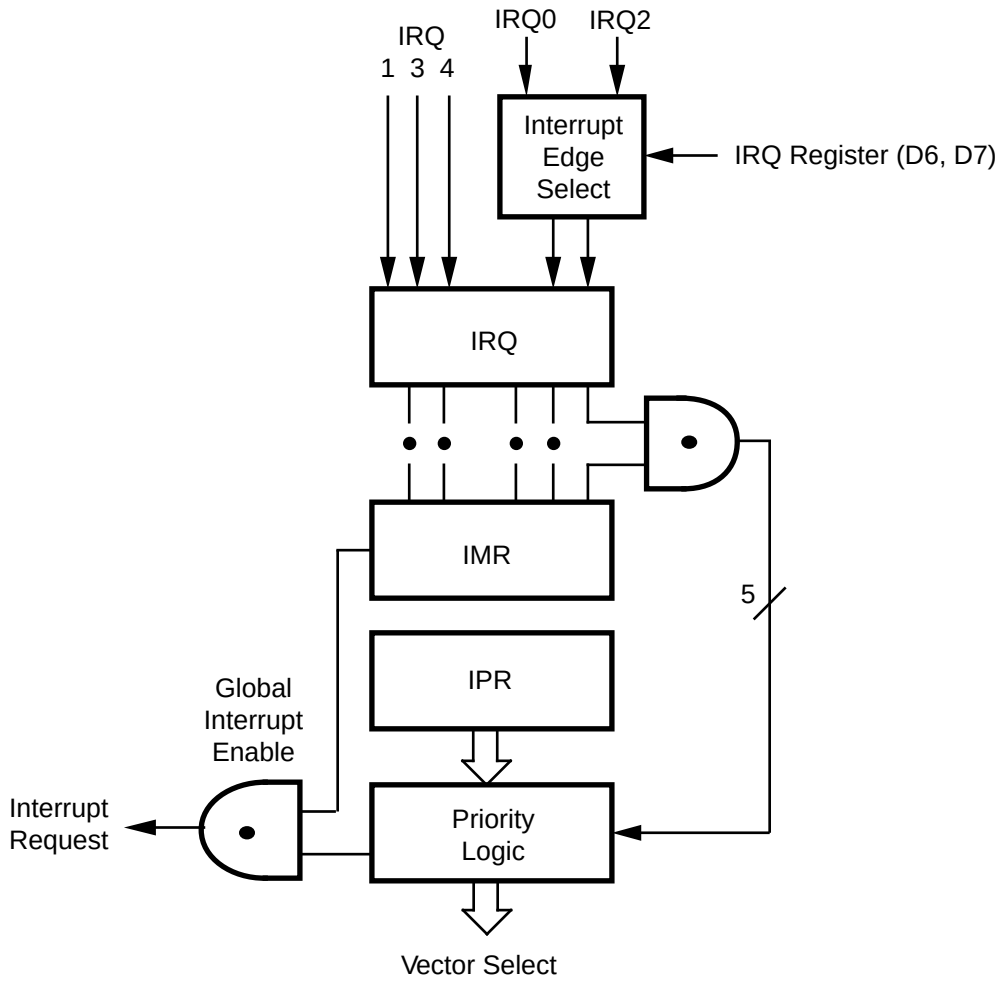


Figure 30. Interrupt Block Diagram

Table 3. Interrupt Types, Sources and Vectors

Name	Source	Vector Location	Comments
IRQ0	IRQ0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6, 7	Internal
IRQ4	T8	8, 9	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86L78 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 4.

Table 4. Interrupt Types, Sources, and Vectors

IRQ		Interrupt Edge	
D7	D6	IRQ2(P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Notes: In analog mode, the Stop-Mode Recovery sources selected by the SMR register are connected to the IRQ1 input. Any of the Stop-Mode Recovery sources for SMR (except P31,P32 and P33) can be used to generate IRQ1 (falling edge triggered).

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86L78 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86L7X on-chip oscillator may be driven with a cost-effective RC network or other suitable external clock source. For 32 kHz crystal operation a mask option is selected which disables the internal XTAL1/2 feedback resistor. The external components for using a 32 kHz crystal include a feedback (Rf) and serial (Rd) resistor as shown in Figure 33.

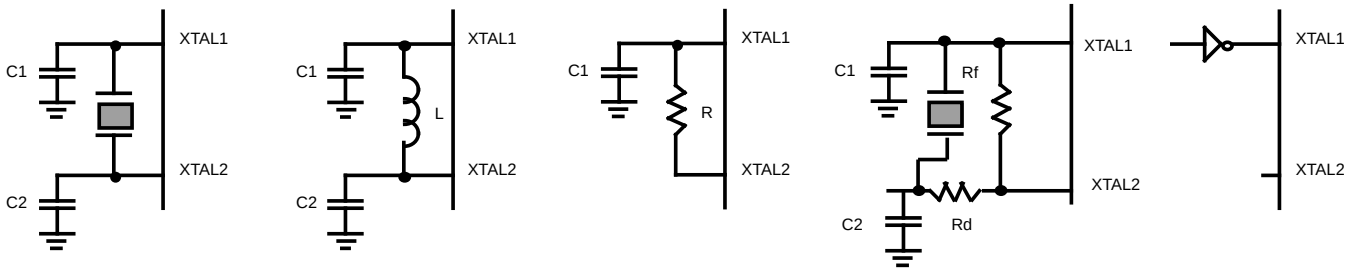
The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 32).

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power Fail to Power OK status.
2. Stop-Mode Recovery (if D5 of SMR = 1).
3. WDT Time-Out.

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, LC oscillators).



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz

* Preliminary value including pin parasitics

LC
C1, C2 = 22 pF

L = 130 µH *
f = 3 MHz *

RC
@ 3V VCC (TYP)

C1 = 33 pF *
R = 1K *

32 kHz XTAL
C1 = 20 pF, C = 33 pF
Rd = 56 - 470K
Rf =10 M

External Clock

Figure 31. Oscillator Configuration

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μA (typical) or less. STOP Mode is terminated only by a reset, such as WDT time-out, POR, SMR, or external reset. This causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate SLEEP instruction, i.e.,

```
FF    NOP     ; clear the pipeline
6F    STOP    ; enter STOP Mode
              or
FF    NOP     ; clear the pipeline
7F    HALT    ; enter HALT Mode
```

Port Configuration Register (PCON). The PCON register configures the comparator output on Port 3. It is located in the expanded register file at Bank F, location 00 (Figure 32).

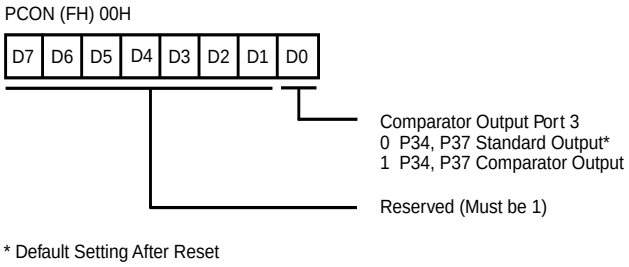
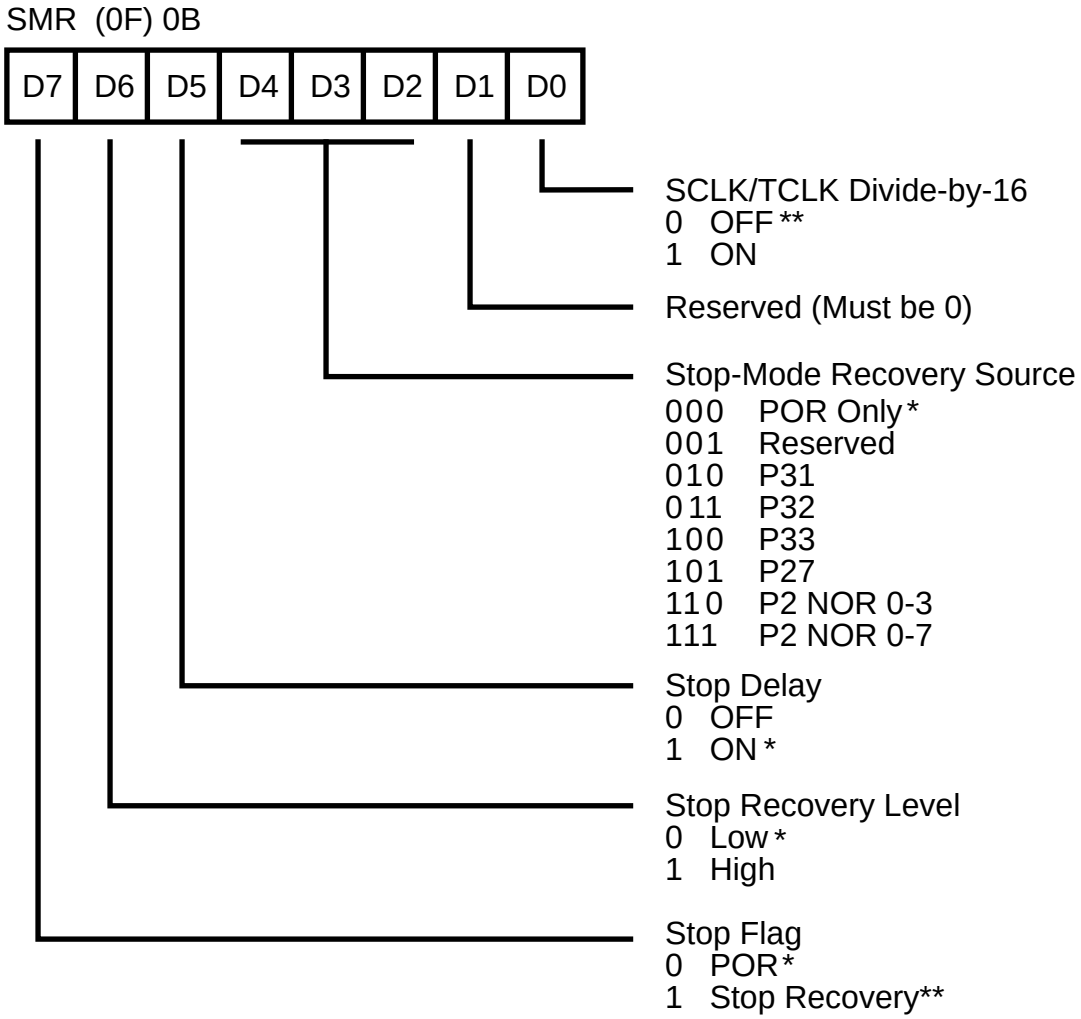


Figure 32. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0). Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

FUNCTIONAL DESCRIPTION (Continued)

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 33). All bits are Write Only except bit 7, which is Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4, of the Stop-Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not.



* Default Setting After Reset
** Default Setting After Reset and Stop-Mode Recovery

Figure 33. Stop-Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a Divide-by-16 prescaler of SCLK/TCLK (Figure 34). The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to a 0.

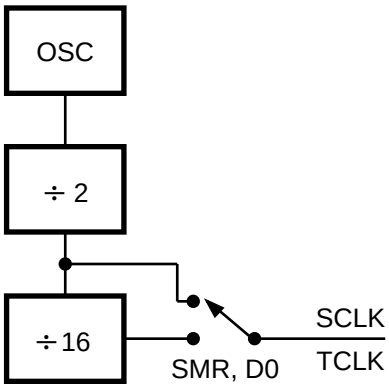


Figure 34. SCLK Circuit

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake up source of the STOP recovery (Figure 35 and Table 5).

Table 5. STOP-Mode Recovery Source

SMR: 432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note: Any Port 2 bit defined as an output will drive the corresponding input to the default state to allow the remaining inputs to control the AND/OR function. Refer to SMR2 register for other recover sources.

STOP-Mode Recovery Delay Select (D5). This bit, if Low, disables the 5 ms /RESET delay after Stop-Mode Recovery. The default configuration of this bit is one. If the "fast" wake up is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

STOP-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Z86L78 from STOP Mode. A 0 indicates Low level recovery. The default is 0 on POR (Figure 35).

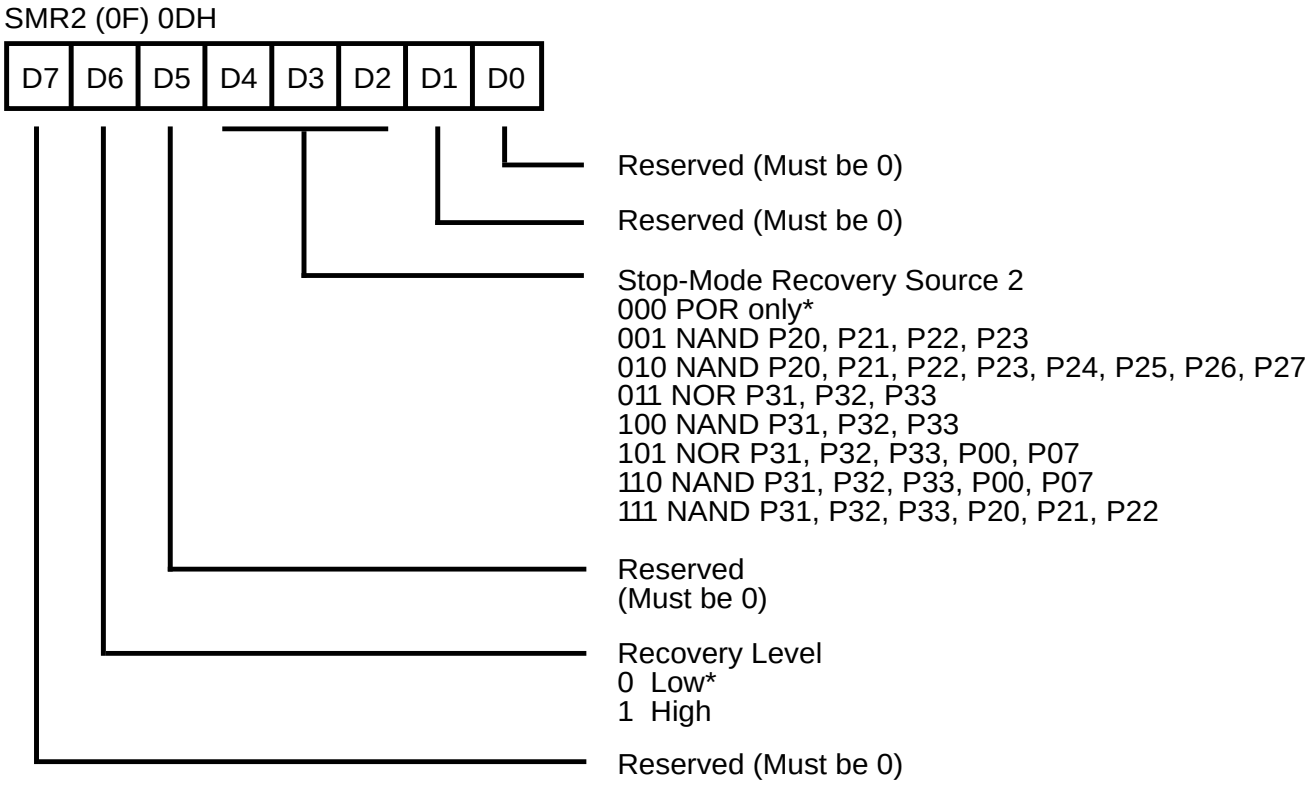
Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. It is a Read Only Flag bit. A 1 in D7 (warm) indicates that the device will awaken from a SMR source or a WDT while in STOP Mode. A 0 in this bit (cold) indicates that the device will be rest by a POR, WDT while not in STOP, or the device awakened from a low voltage standby mode.

Stop-Mode Recovery Register 2 (SMR2). This register determines the mode of stop mode recovery for SMR2 (Figure 36).

If SMR2 is used in conjunction with SMR, either of the specified events will cause a Stop-Mode Recovery.

Note: Port pins configured as outputs are ignored as a SMR or SMR2 recovery source. For example, if the NAND of P23-20 is selected as the recovery source and P20 is configured as an output then the remaining SMR pins (P23-P21) form the NAND equation.

FUNCTIONAL DESCRIPTION (Continued)



Note: If used in conjunction with SMR, either of the two specified events will cause a Stop-Mode Recovery.

*Default Setting After Reset

Figure 35. Stop-Mode Recovery Register 2 ((0F) DH: D2-D4, D6 Write Only

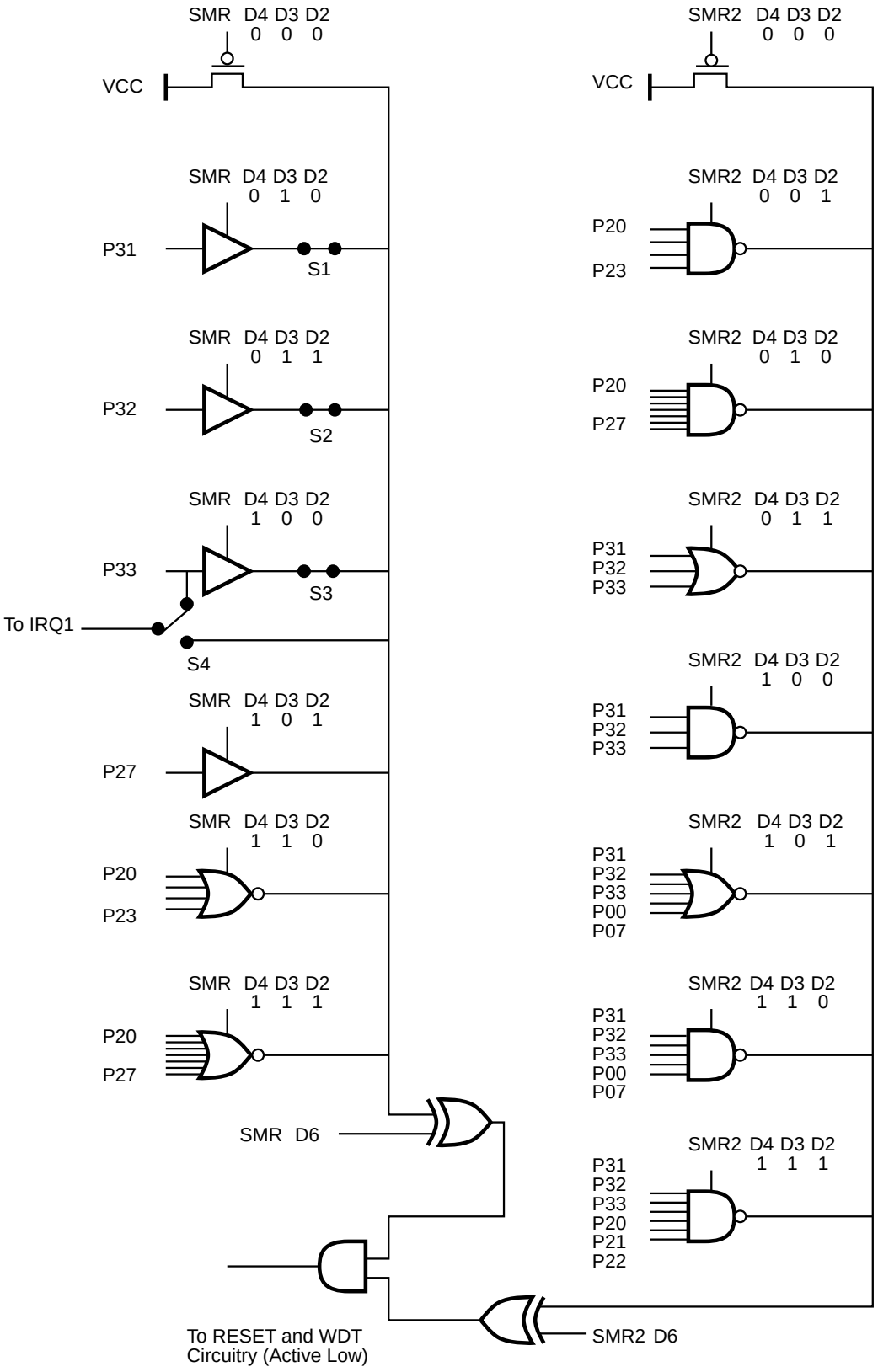
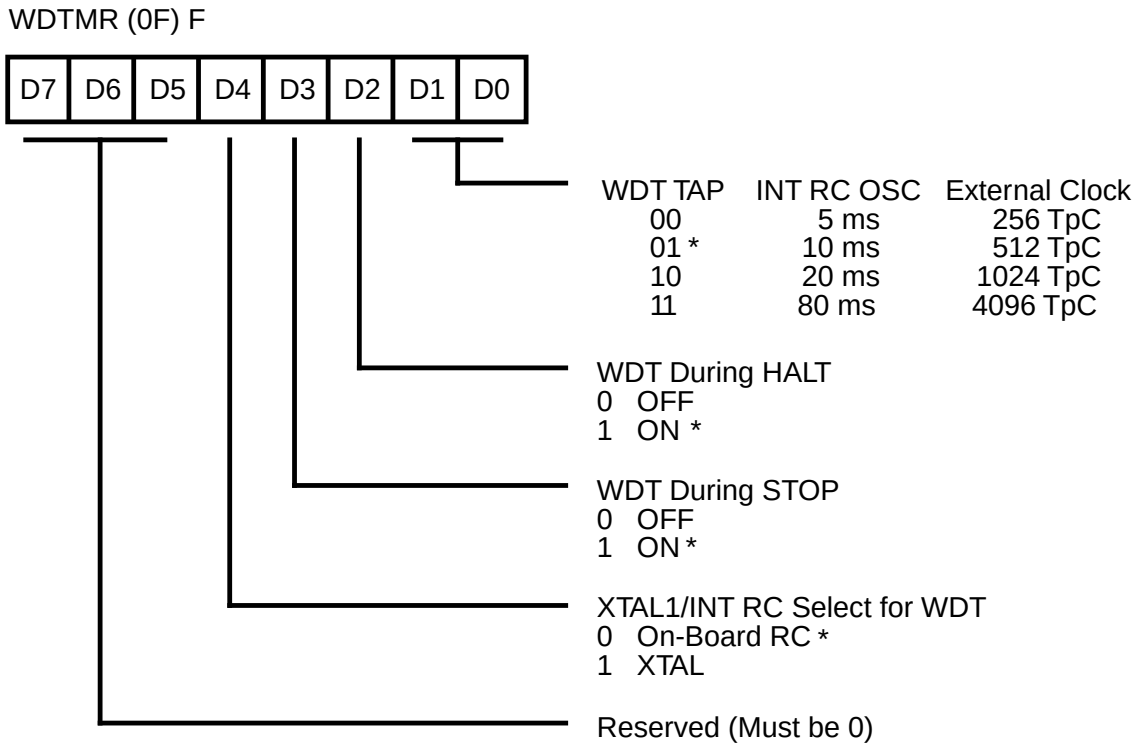


Figure 36. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Figure 38). This register is accessible only during the first 64 processor cycles (128 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 35). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as follows:



* Default Setting After Reset

Figure 37. Watch-Dog TImer Mode Register (Write Only)

WDT Time Select (D0, D1). Selects the WDT time period. It is configured as shown in Table 6.

Table 6. WDT TIme Select

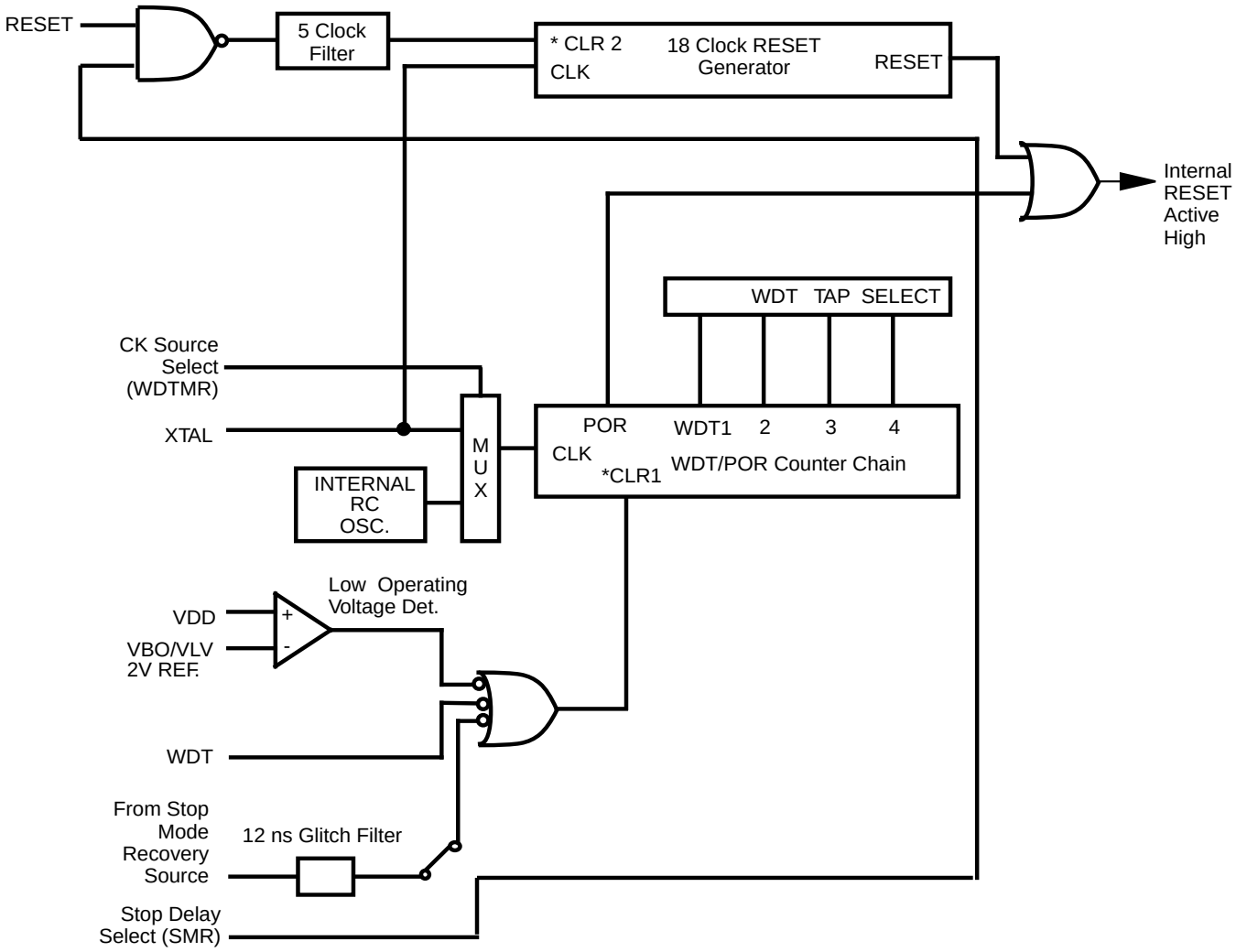
D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	10 ms min	512 TpC
1	0	20 ms min	1024 TpC
1	1	80 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 10 ms

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.



* /CLR1 and /CLR2 enable the WDT/POR and 18 Clock Reset timers upon a Low to High input translation.

Figure 38. Resets and WDT

FUNCTIONAL DESCRIPTION (Continued)

Reset Functional Operation. Reset is internally driven by four sources:

1. **POR.** (0 volts to operating voltage condition) usually occurs upon powering up the MCU.

2. **WDT.** The WDT counts down and generates a reset, usually to "wake" the part from a "sleep" condition.

3. **Low Voltage Detection/Standby.** An on-chip Voltage Comparator checks that the V_{CC} is at the required level for correct operation of the device. Reset is globally driven when V_{CC} falls below V_{LV} (Vrf1). A small further drop in V_{CC} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. Typical power consumption in this Low Voltage Standby mode (I_{LV}) is about 45 µA (varying with the number of Masks selectable options enabled). When the power level is returned to above V_{LV}, the device will perform a POR and function normally. If the V_{CC} is allowed to stay above 1.5V, the RAM content is preserved. Low Voltage Standby was designed to allow the device to draw power from board level decoupling capacitors during battery changes.

4. Stop Mode Recovery (Partial reset).

Low Voltage Protection. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below Vrf1.

Maximum (Vrf1) Conditions:

T_A = 0°C, +70°C Internal clock frequency equal to or less than 4.0 MHz

Note: The internal clock frequency is one-half the external clock frequency.

The device functions normally at or above Vrf1 under all conditions (Figure 39).

Mask Selectable Options. There are five Mask Selectable Options to choose from based on ROM code requirements. These are:

RC/Other	Clock Source
Port 0 Pull-ups	On/Off
Port 2 Pull-ups	On/Off
Port 3 Pull-ups	On/Off
32 kHz Option	On/Off

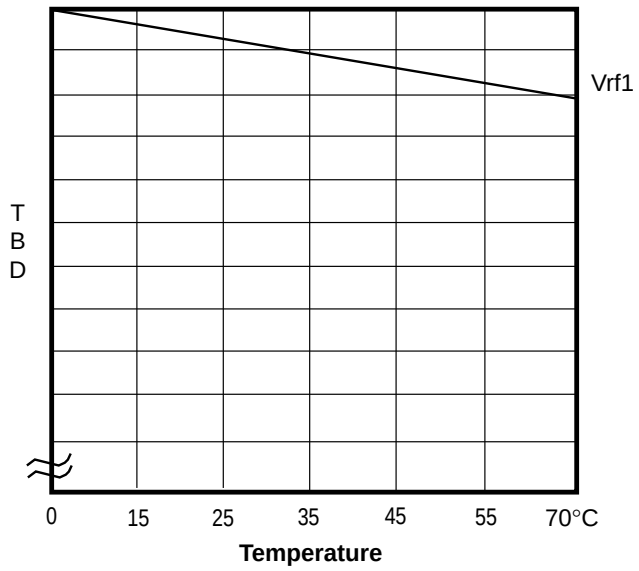


Figure 39. Z86L78 Low Voltage vs Temperature at 8 MHz

EXPANDED REGISTER FILE CONTROL REGISTERS (0D)

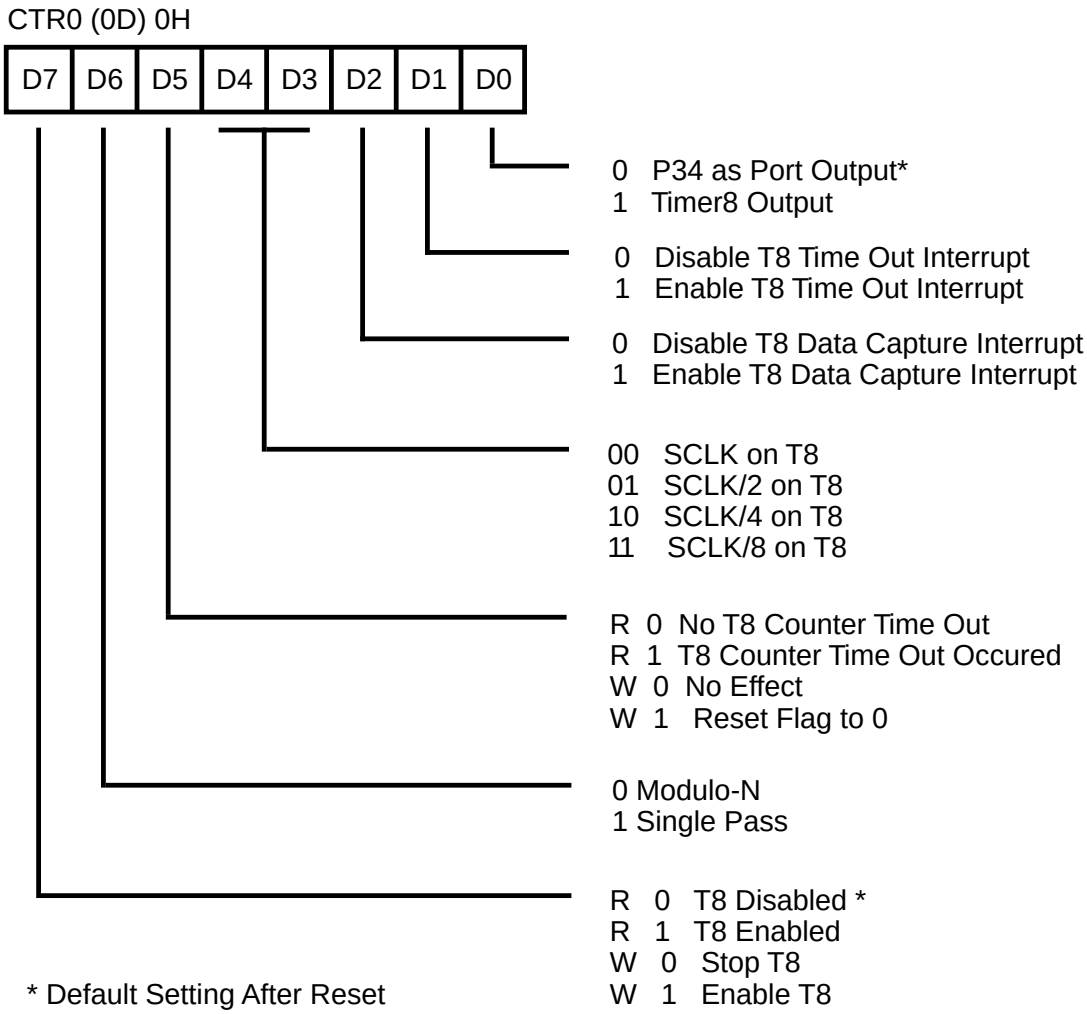
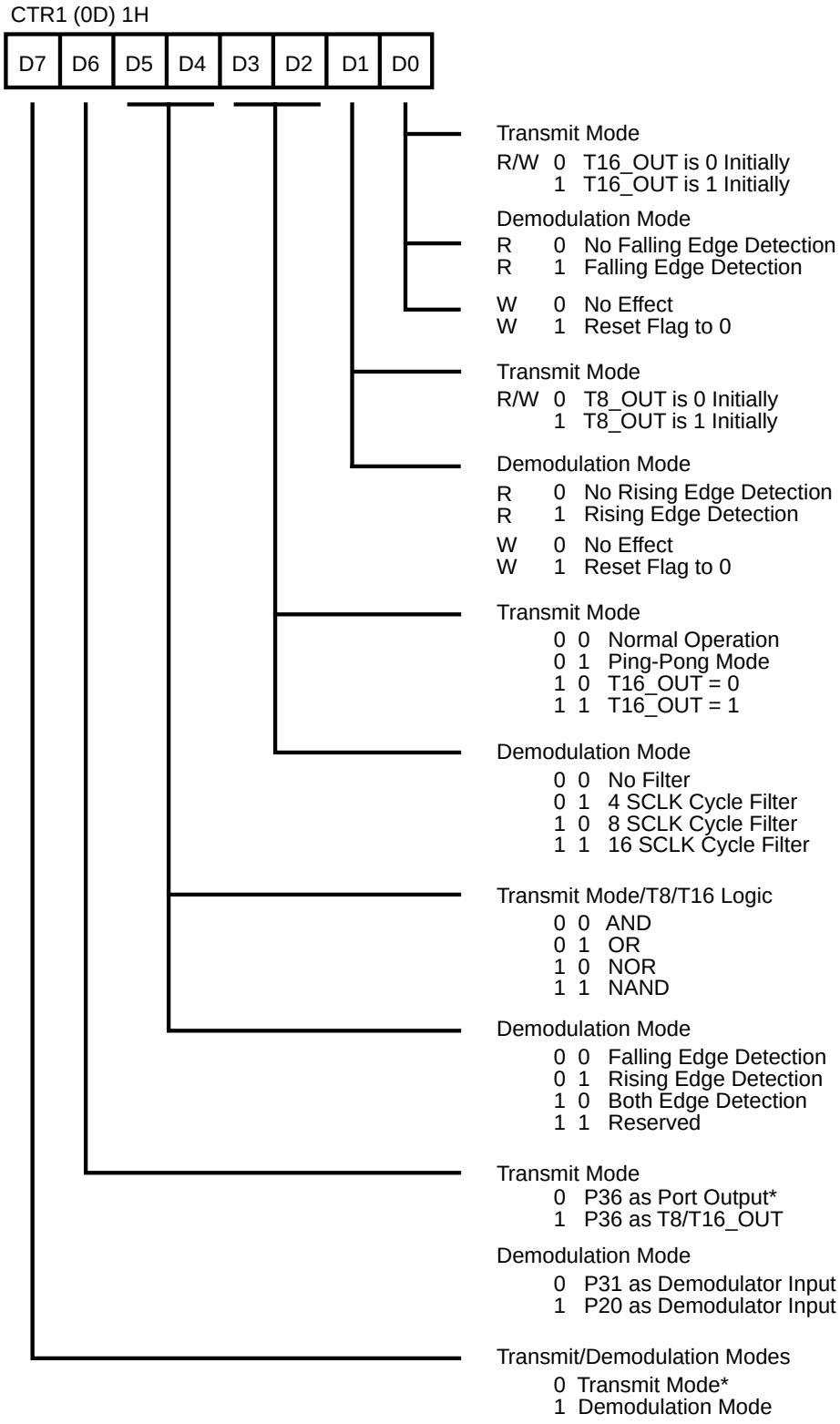


Figure 40. TC8 Control Register
((0D) 0H: Read/Write Accept Where Noted)



Note: Care must be taken in differentiating Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit will have different functions.

***Note:** Changing from one mode to another cannot be done without disabling the counter/timers.

Figure 41. T8 and T16 Common Control Functions ((0D) 1H: Read/Write)

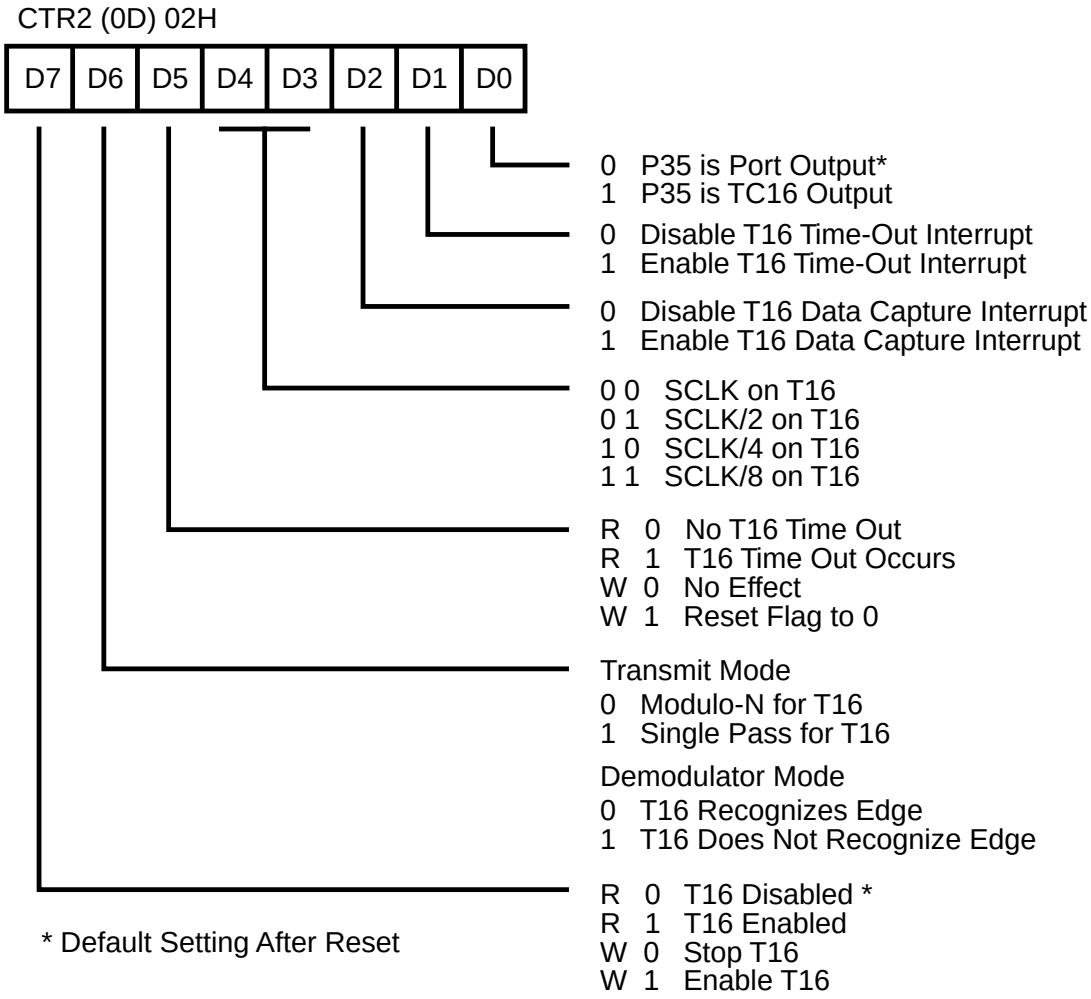
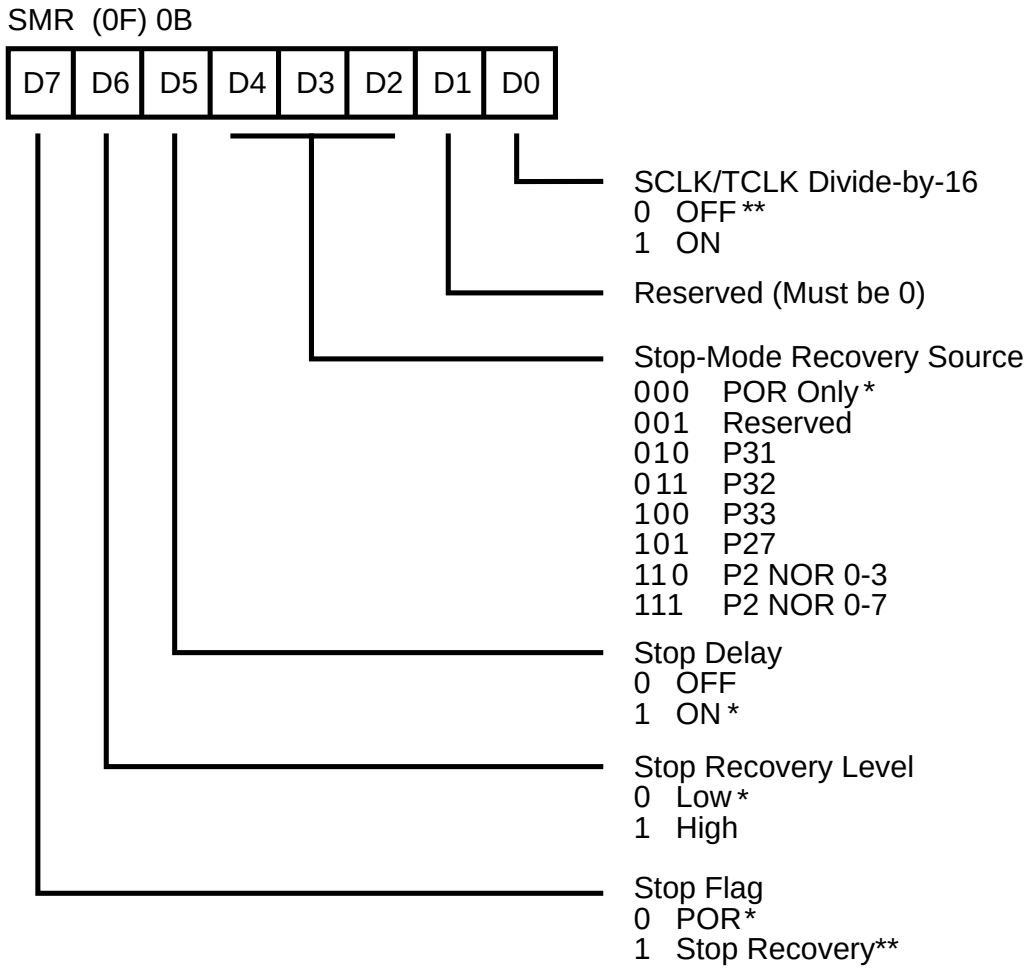


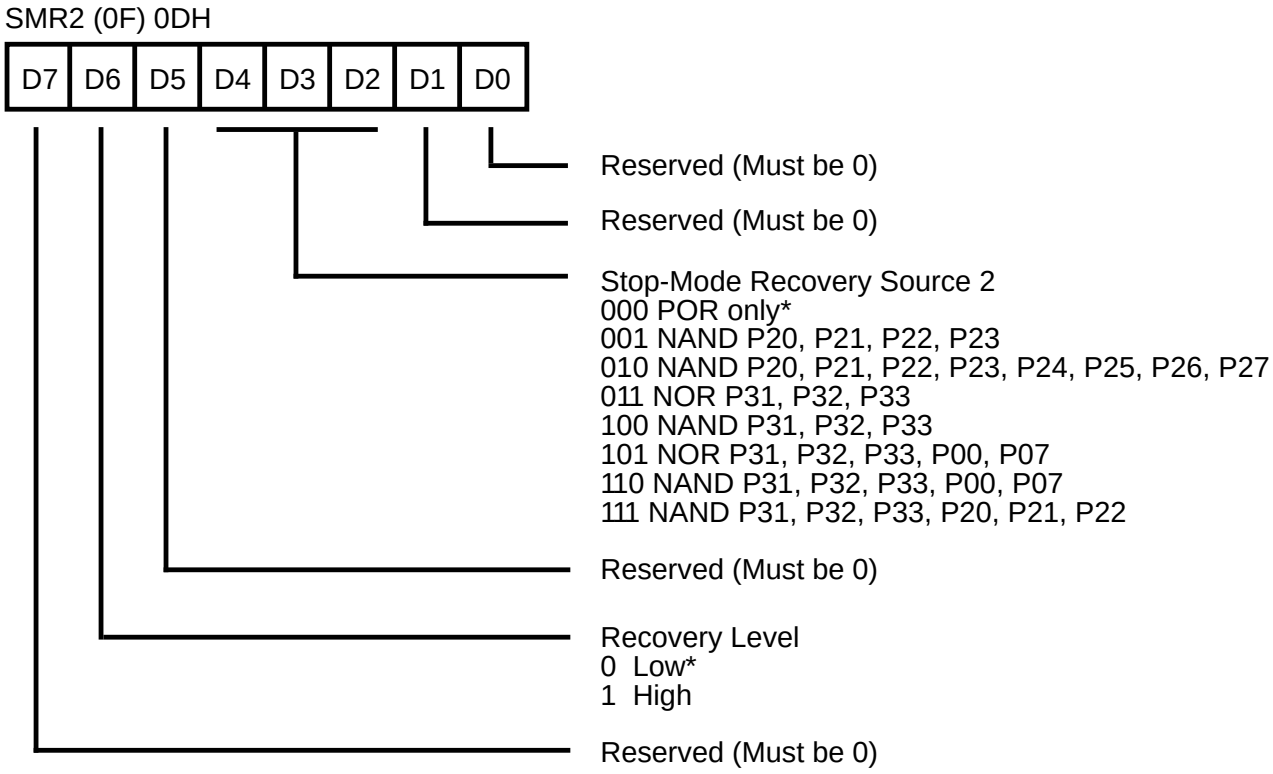
Figure 42. T16 Control Register
((0D) Read/Write Except Where Noted

EXPANDED REGISTER FILE CONTROL REGISTERS (0F)



* Default Setting After Reset
** Default Setting After Reset and Stop-Mode Recovery

Figure 43. Stop-Mode Recovery Register ((F) 0BH: D6-D0 = Write Only, D7=Read Only

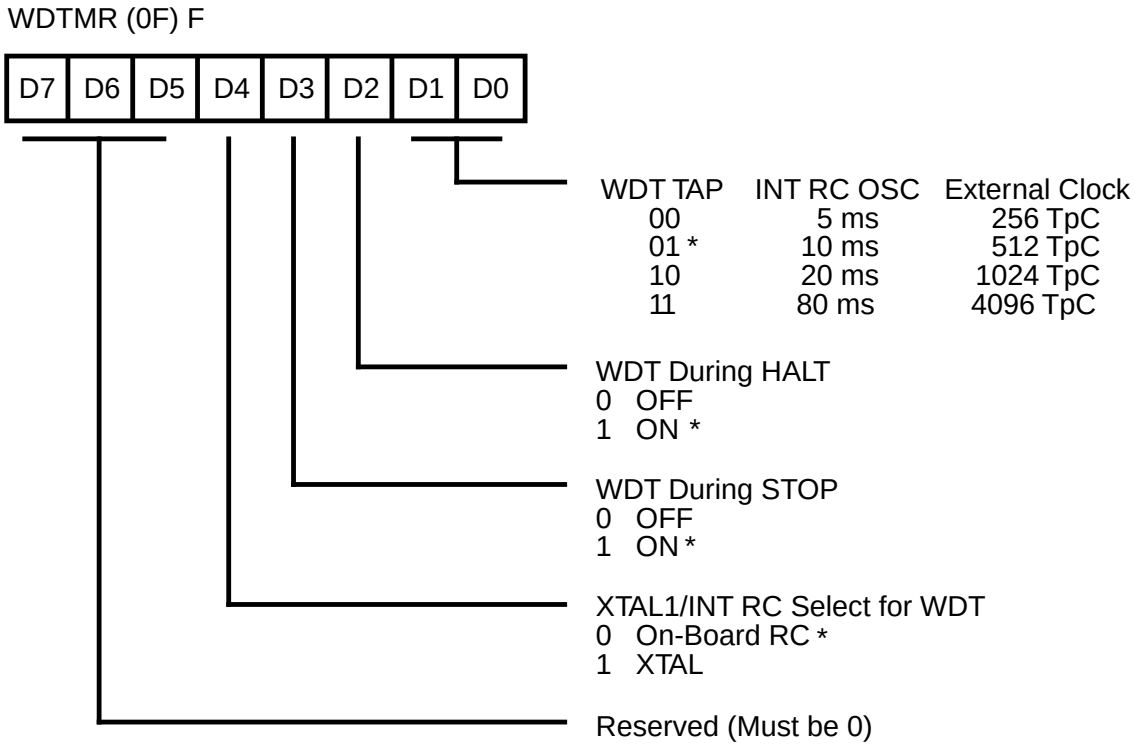


Note: If used in conjunction with SMR, either of the two specified events will cause a Stop-Mode Recovery.

*Default Setting After Reset

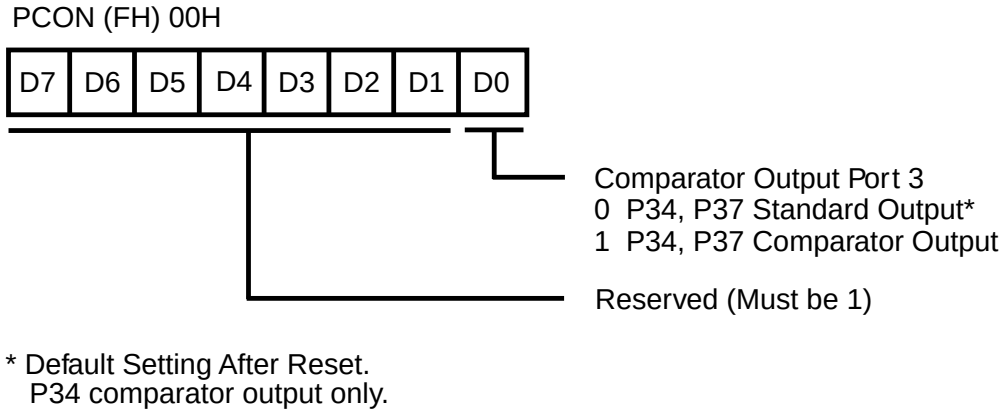
Figure 44. Stop-Mode Recovery Register 2 ((0F) DH: D2-D4, D6 Write Only)

EXPANDED REGISTER FILE CONTROL REGISTERS (0F) (Continued)



* Default Setting After Reset

Figure 45. Watch-Dog Timer Mode Register ((F) 0FH: Write Only)



* Default Setting After Reset.
P34 comparator output only.

Figure 46. Port Configuration Register (PCON) ((0F) 0H: Write Only)

Z8 STANDARD CONTROL REGISTER DIAGRAMS

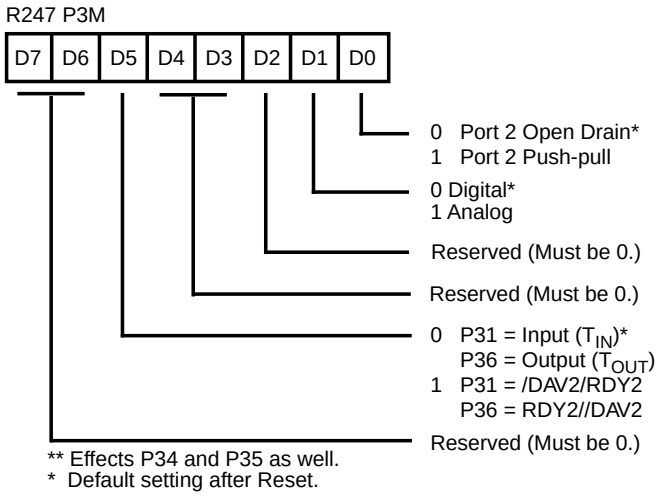


Figure 47. Port 3 Mode Register (F7H: Write Only)

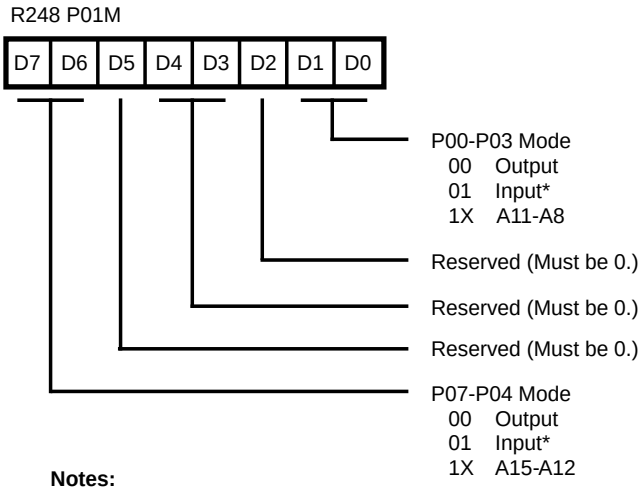


Figure 48. Port 0 and 1 Mode Register (F8H: Write Only)

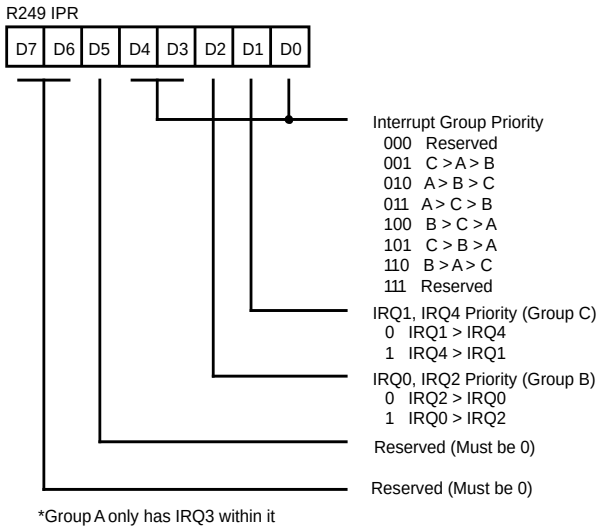


Figure 49. Interrupt Priority Registers ((0) F9H: Write Only)

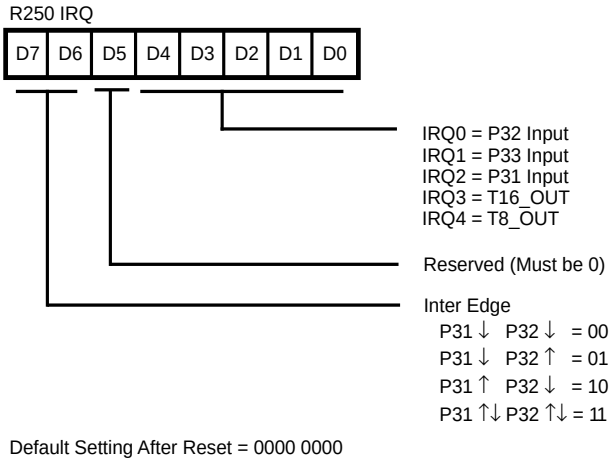


Figure 50. Interrupt Request Register ((0) FAH: Read/Write)

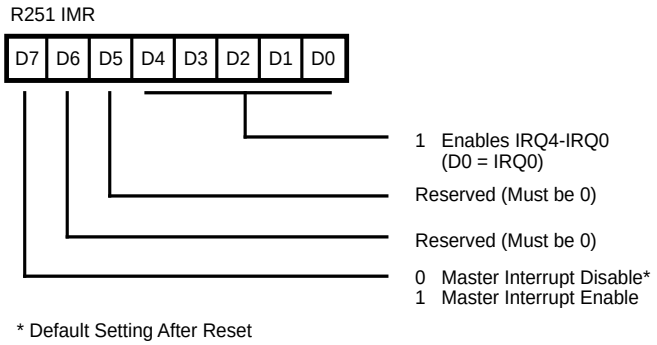


Figure 51. Interrupt Mask Register ((0(FBH: Read/Write)

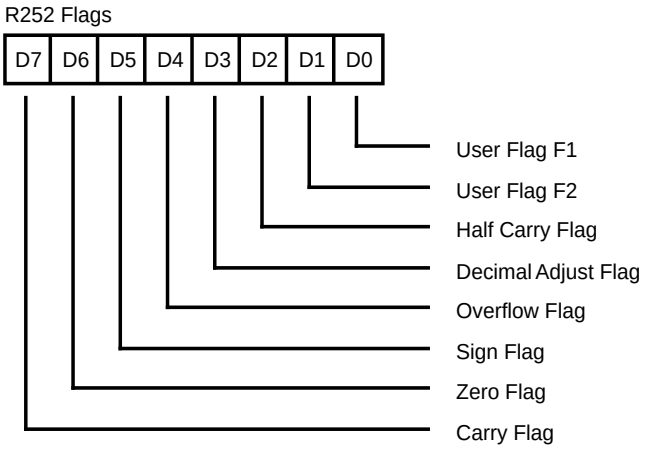


Figure 52. Flag Register ((0) FCH: Read/Write

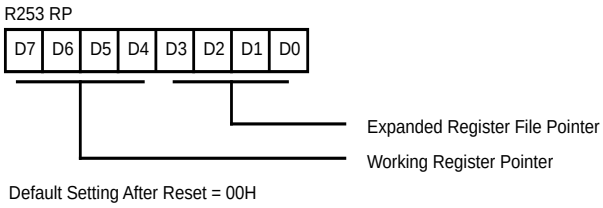


Figure 53. Register Pointer ((0) FDH: Read/Write)

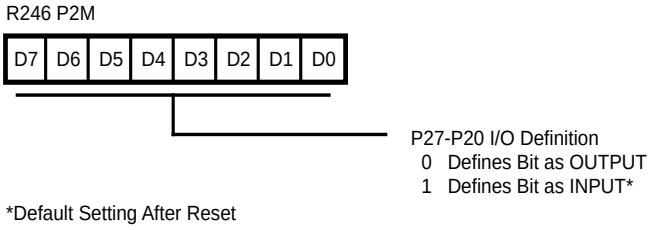


Figure 54. Port 2 Mode Register (F6H: Write Only)

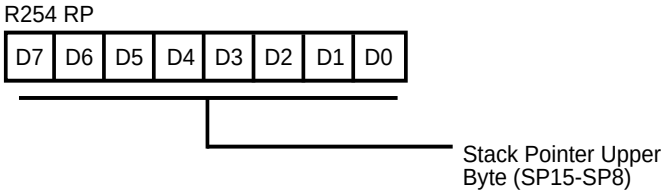


Figure 55. Stack Pointer High ((0) FEH: Read/Write)

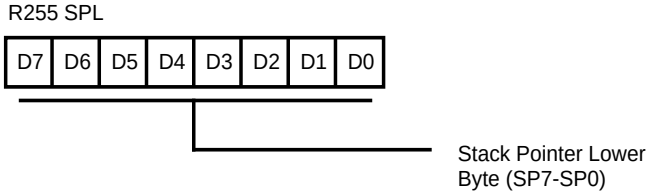
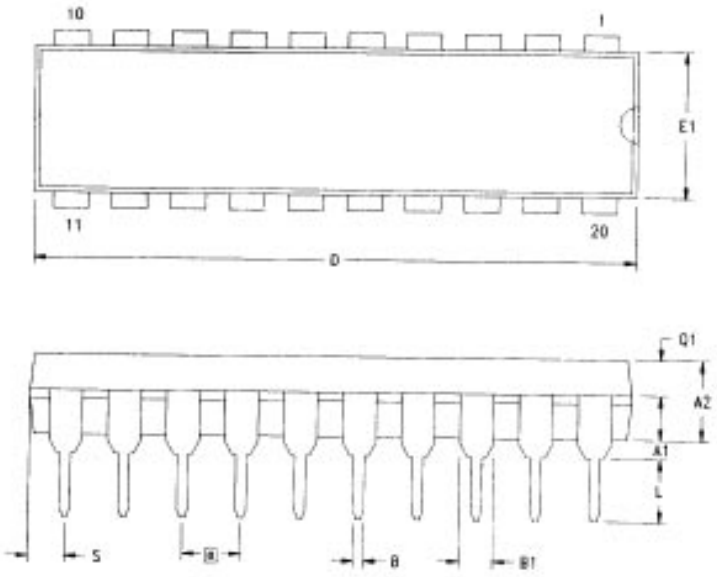


Figure 56. Stack Pointer Low ((0) FFH: Read/Write)

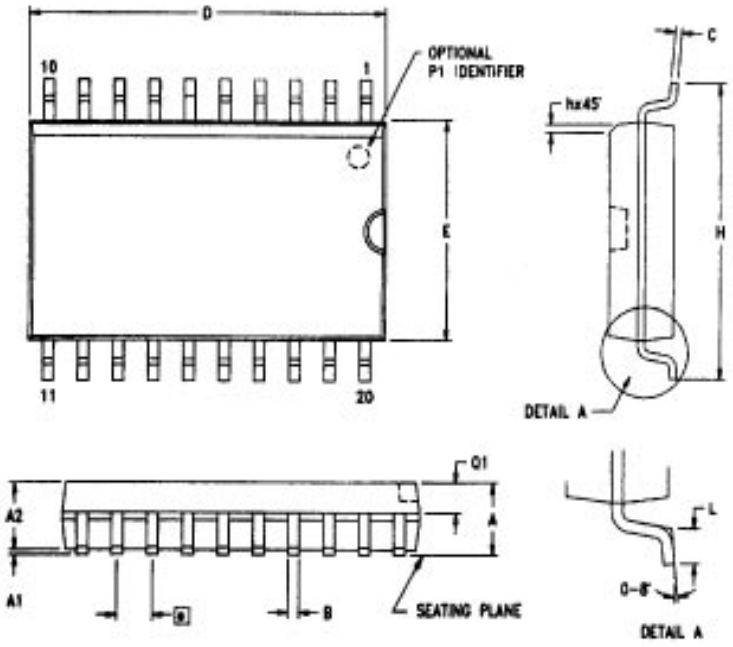
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
(e)	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

Figure 57. 20-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 58. 20-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86L78

8.0 MHz

20-pin DIP	**20-pin SOIC**
Z86L7808PSC	Z86L7808SSC

Codes

Package

P = Plastic DIP
S = SOIC (Small Outline Integrated Circuit)

Temperature

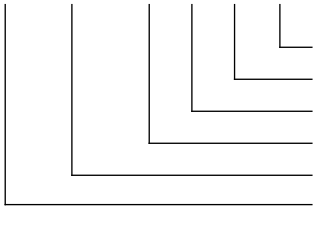
8 = 8.0 MHz

Environmental

C = Plastic Standard

Example:

Z 86L78 08 P S C is a Z86L78, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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