

Z08615

NMOS 8-BIT Z8[®] MCU KEYBOARD CONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Speed (MHz)
Z08615	4	124	32	5

Note: *General-Purpose

- Low Power Consumption - 750 mW
- Digital Inputs NMOS Levels with Internal Pull-Up Resistors
- Four Direct Connect LED Drive Ports
- Hardware Watch-Dog Timer (WDT)
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- On-Chip Oscillator that Accepts an RC (Capacitor On-Board), Crystal, Ceramic Resonator, or External Clock Drive (Mask Options)
- Clock Frequency:
RC = 8 to 10 MHz
Crystal = 4 to 5 MHz
- Low EMI Emission

GENERAL DESCRIPTION

The Z08615 Keyboard Controller is a member of the Z8[®] single-chip microcontroller family with 4 Kbytes of ROM. The device is housed in a 40-pin DIP and 44-pin PLCC package, and is manufactured in NMOS technology. The Z08615 microcontroller offers fast execution, efficient use of memory, sophisticated interrupt, input/output bit-manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z08615 architecture is characterized by a flexible I/O scheme, an efficient register, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z08615 provides 32 pins dedicated to input and output. These lines are grouped into four ports, each port consists of 8 lines, and are configurable under software control to provide timing, status signals, and serial or parallel I/O ports.

The Z08615 offers low EMI emission which is achieved by means of several modifications in the output drivers and clock circuitry of the device.

There are two basic address spaces which are available to support this wide range of configurations: Program Memory and 124 General-Purpose Registers.

The Z08615 offers two on-chip counter/timers with a large number of user-selectable modes. This unburdens the program from coping with real-time problems such as counting/timing (Figure 1).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

GENERAL DESCRIPTION (Continued)

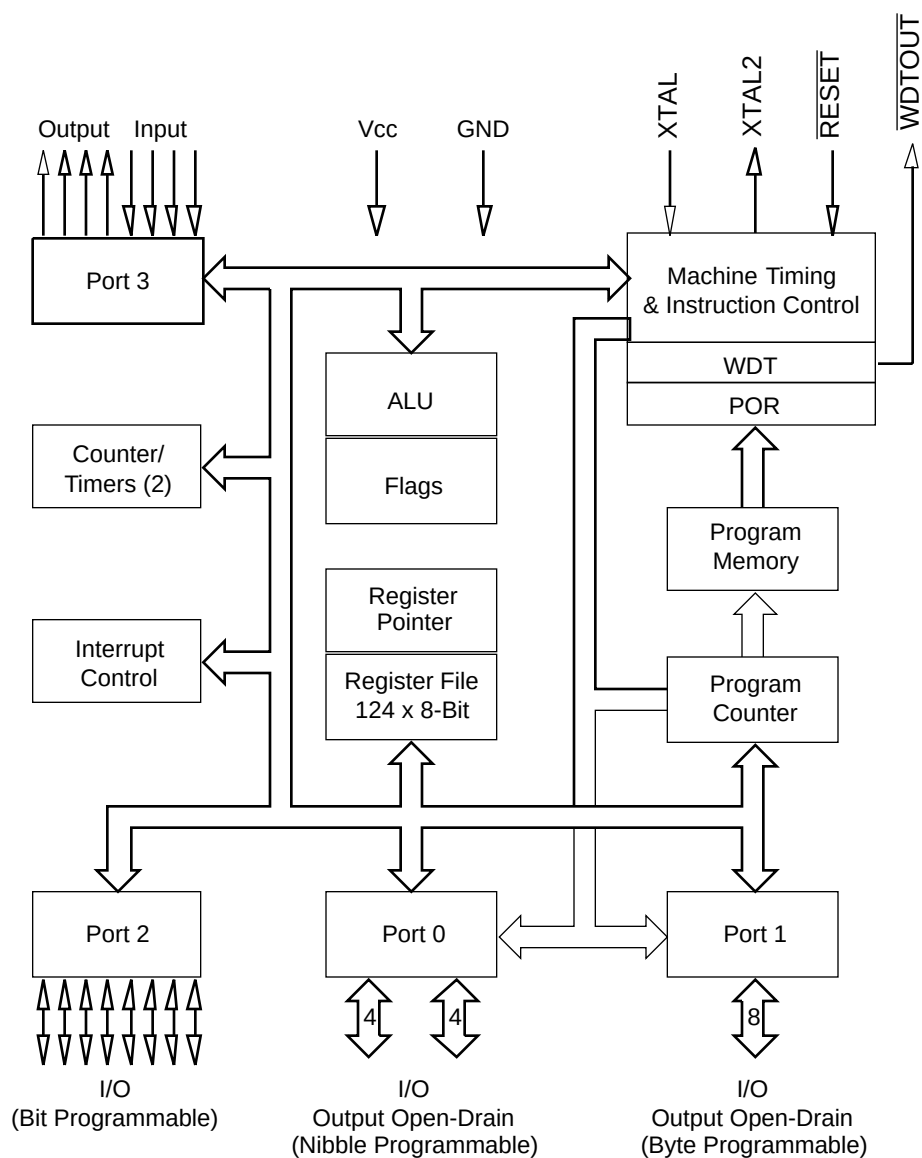
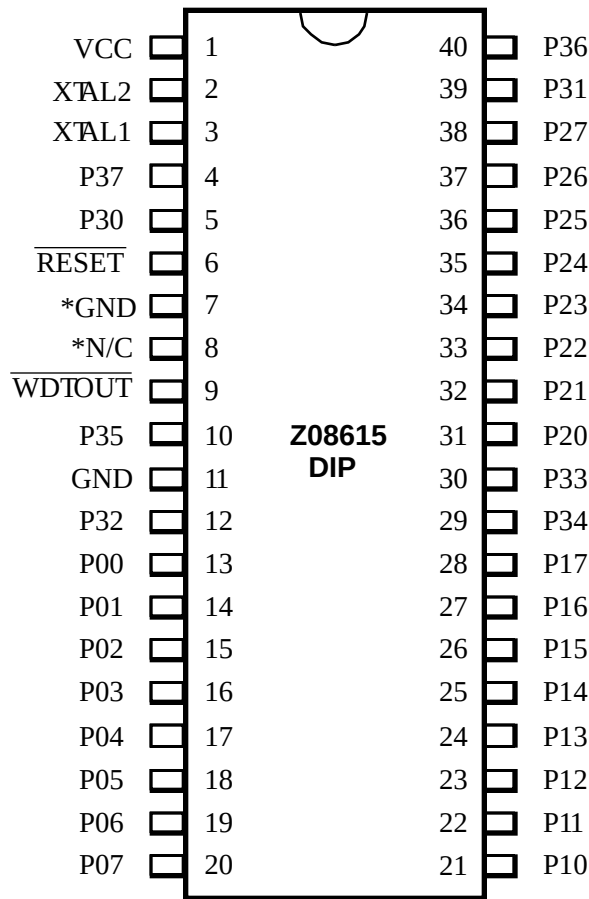


Figure 1. Z08615 Functional Block Diagram

PIN DESCRIPTIONS



Note:
* Pin 8 is connected to the chip, although used only for testing.
This pin *must* float. Pin 7 is a test pin and *must* be grounded.

Figure 2. Z08615 40-Pin DIP Pin Configuration

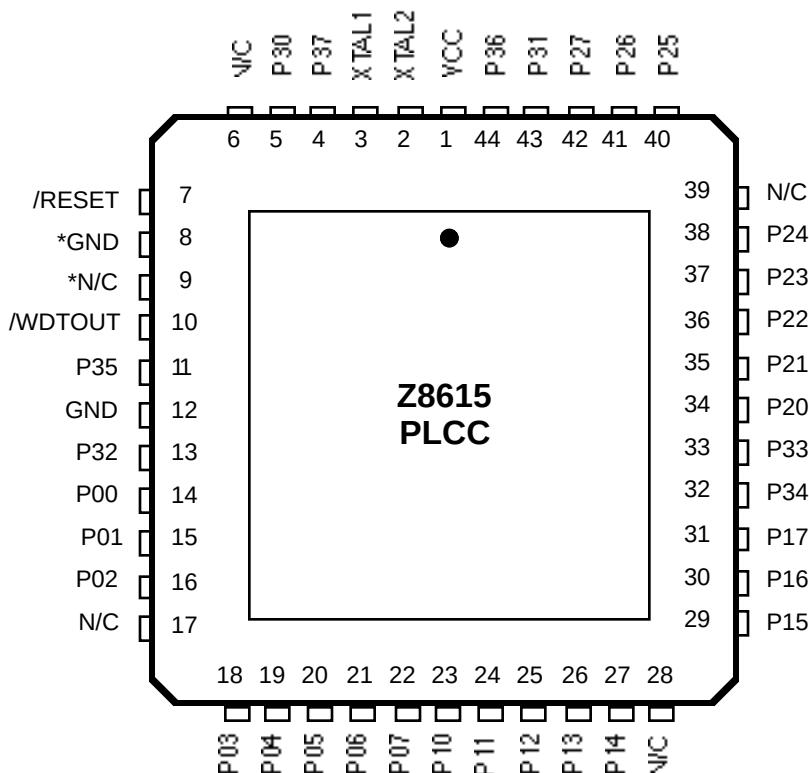
Table 1. Z08615 40-Pin DIP Identification

Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input
2	XTAL2	Crystal Oscillator Clock	Output
3	XTAL1	Crystal Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	RESET	Reset	Input
*7	GND	Ground	
*8	N/C	Not Connected	
9	WDTOUT	Watch-Dog Timer	Output

Table 1. Z08615 40-Pin DIP Identification

Pin #	Symbol	Function	Direction
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
21-28	P17-P10	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P27-P20	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

PIN DESCRIPTIONS (Continued)



Note:
* Pin 9 is connected to the chip, although used only for testing.
This pin **must** float. Pin 8 is a test pin and **must** be grounded.

Figure 3. Z08615 44-Pin PLCC Pin Configuration

Table 2. Z08615 44-Pin PLCC Pin Identification			
Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input
2	XTAL2	Crystal Oscillator Clock Output	
3	XTAL1	Crystal Oscillator Clock Input	
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	
7	RESET	Reset	Input
*8	GND	Ground	
*9	N/C	Not Connected	
10	WDTOUT	Watch-Dog Timer	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input
14-16	P02/P00	Port 0, Pins 0, 1, 2	In/Output
17	N/C	Not Connected	
18-22	P07-P03	Port 0, Pins 3, 4, 5, 6, 7	In/Output

Table 2. Z08615 44-Pin PLCC Pin Identification			
Pin #	Symbol	Function	Direction
23-27	P14-P10	Port 1, Pins 0, 1, 2, 3, 4	In/Output
28	N/C	Not Connected	
29-31	P17-P15	Port 1, Pins 5, 6, 7	In/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P24-P20	Port 2, Pins 0, 1, 2, 3, 4	In/Output
39	N/C	Not Connected	
40-42	P27-P25	Port 2, Pins 5, 6, 7	In/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

ABSOLUTE MAXIMUM RATINGS

Sym.	Parameter	Min.	Max.	Units
V _{DD}	Supply Voltage*	−0.3	+7	V
T _{STG}	Storage Temp.	−65°	+150°	C
T _A	Oper. Ambient Temp.	†	†	C

Note:
*Voltages on all pins with respect to Ground.
†See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 4).

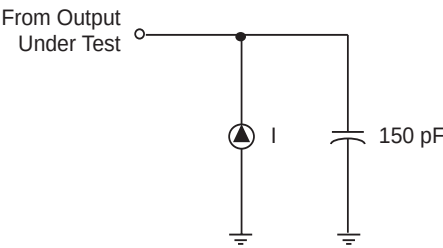


Figure 4. Test Load Diagram

CAPACITANCE

T_A = 25°C, VCC = GND = 0V, f = 1.0 MHz, unmeasured pins returned to ground.

Parameter	Min.	Max.
Input Capacitance	0	12 pF
Output Capacitance	0	12 pF
I/O Capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 4.75V$ to $5.25V$ @ $0^{\circ}C$ to $-55^{\circ}C$

Sym	Parameter	Min	Max	Typ*	Unit	Condition	Notes
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	-0.3	0.8		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0	V_{CC}		V		
V_{IL}	Input Low Voltage	-0.3	0.8		V		
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V		
V_{RL}	Reset Input Low Voltage	-0.3	0.8		V		
V_{OH}	Output High Voltage	2.0			V	$I_{OH} = -250 \mu A$ (Port 2 only)	
	Output High Voltage	2.4			V	$I_{OH} = -250 \mu A$ (Port 3 only)	
V_{OL}	Output Low Voltage		0.8		V	$I_{OL} = 10.0 \text{ mA}$	1
I_{IL}	Input Leakage	-10	10		μA	$V_{IN} = 0V, 5.25V$	3
I_{OL}	Output Leakage	-10	10		μA	$V_{IN} = 0V, 5.25V$	2
I_{IR}	Reset Input Current	-335	-775	-477	μA	$V_{IN} = 0V, 5.25V$	
I_{R1}	Input Current	-335	-775		μA	Pull-up resistor=10.4 Kohms, $V_{IN}=5.25V$	
I_{R2}	Input Current	-1.6	-2.9		mA	Pull-up resistor = 2.4 Kohms, $V_{IN}=0.0V$	
I_{CC}	VCC Supply Current		150		mA		
WDT	Watch-Dog Timer		2.0		mA	$V_{OL}=0.4 \text{ Volt}$	

Notes:

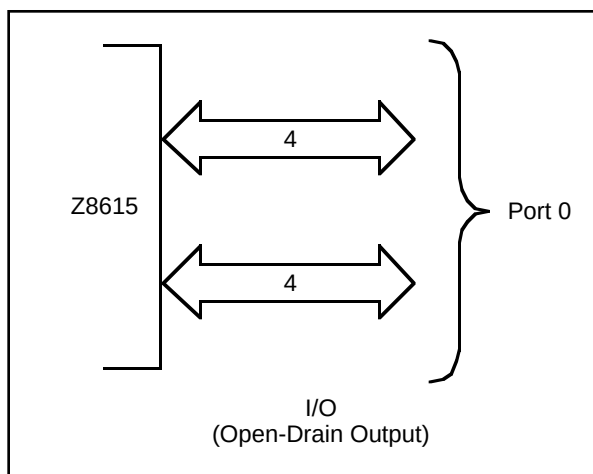
* Typical @ $25^{\circ}C$

1. Ports P37-P34 may be used to sink 12 mA at 2.8V. These may be used for LEDs or as general-purpose outputs requiring high sink current.
2. P00-P07, P10-P17, P20-P25, P30-P33 as output mode open-drain as a logic one.
3. P00-P07, P10-P17, P20-P25, P30-P33 as output mode open-drain as a logic one.

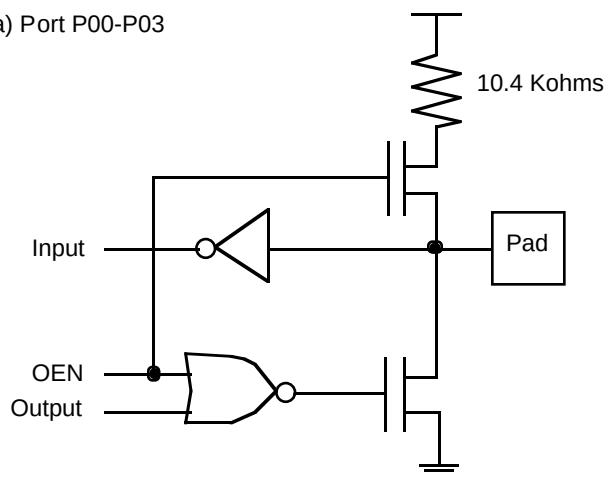
PIN FUNCTIONS

XTAL1, XTAL2. Crystal in, crystal out (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock to the on-chip clock oscillator and buffer.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bi-directional, NMOS compatible I/O port. These eight I/O lines can be configured under software control as a nibble input port, or as a nibble open-drain output port. When used as an I/O port, inputs are standard NMOS (Figure 5). Port P03-P00 has 10.4 Kohms ($\pm 35\%$) pull-up resistors when configured as inputs.



(a) Port P00-P03



(b) Port P04-P07

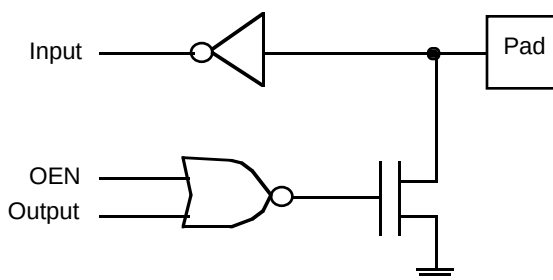


Figure 5. Port 0 Configuration

Port 1 (P17-P10) Port 1 is an 8-bit, byte programmable, bi-directional, NMOS compatible I/O port. These eight I/O lines are configured under software control program as a

byte input port or as an open-drain output port. When used as an I/O port, inputs are standard NMOS (Figure 6).

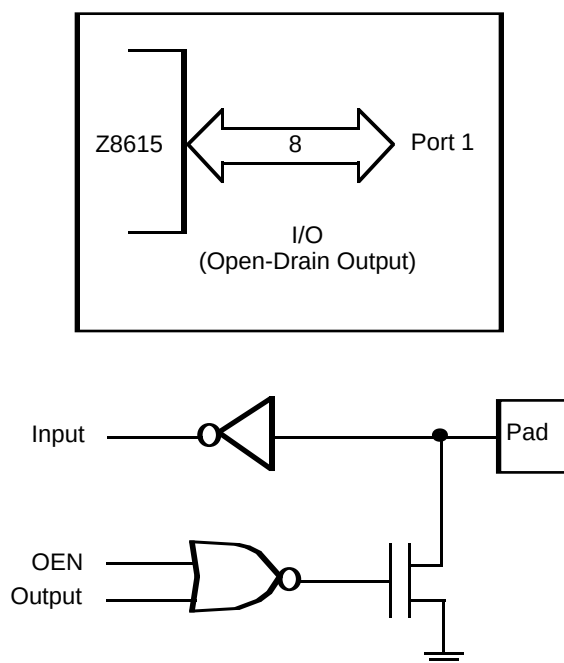


Figure 6. Port 1 P17-P10 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit-programmable, bi-directional, NMOS-compatible I/O port. These eight I/O lines are configured under the software control program for I/O. Port 2 can be programmed as bit-by-bit independently, as input or output, or configured to provide open-drain out-

puts (Figure 7). P26 and P27 have 2.4 Kohms ($\pm 25\%$) pull-up resistors and are capable of sourcing 2.4 mA. P24 and P25 have 10.4 Kohms ($\pm 35\%$) pull-up when configured as inputs.

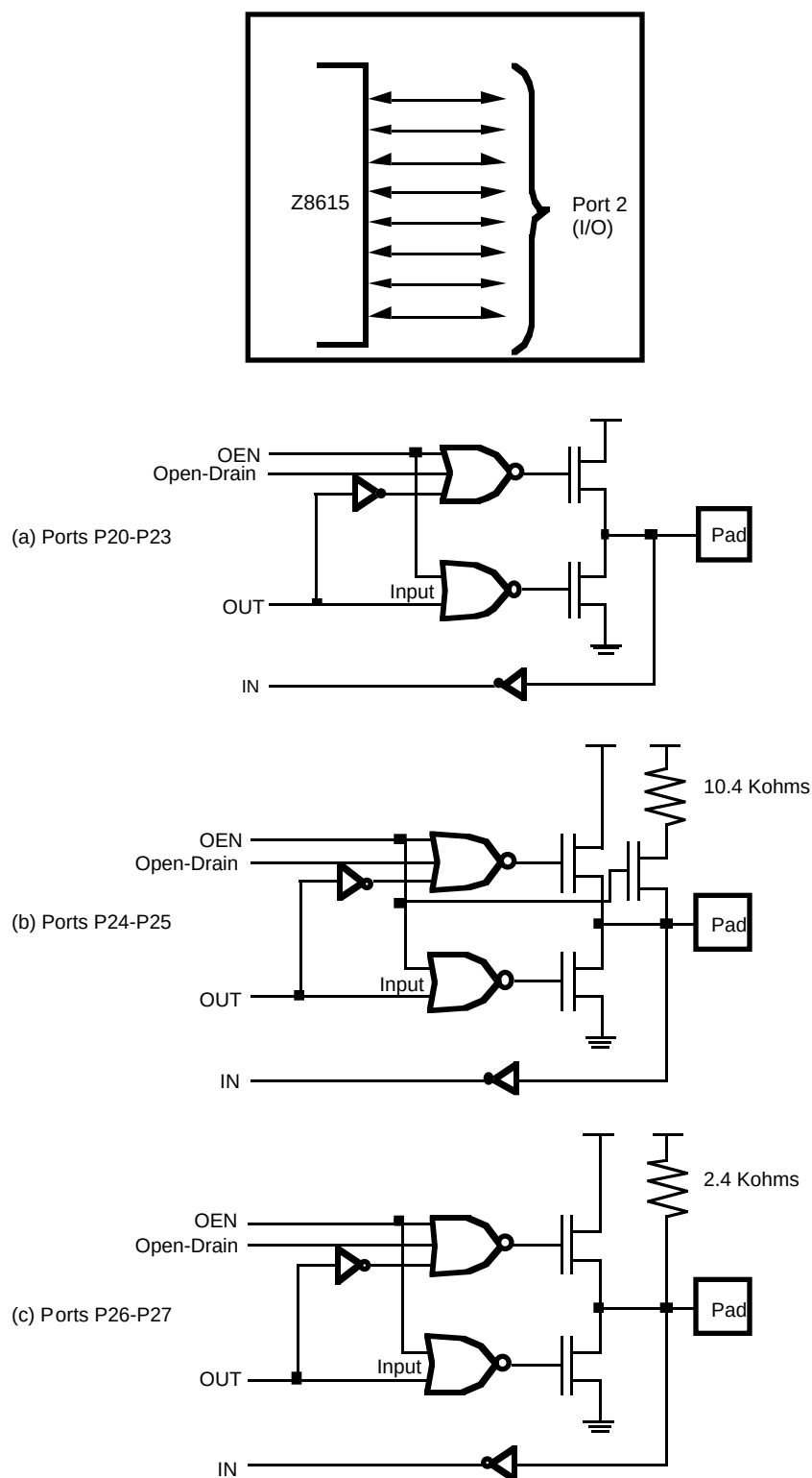


Figure 7. Port 2 P27-P20 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, NMOS compatible four-fixed-input and four-fixed-output I/O port. These eight I/O lines have four-fixed-input (P33-P30) and four-fixed-output (P37-P34) ports. Port 3 outputs have 10.4 Kohms ($\pm 25\%$) pull-up resistors and are capable of driving up to four LEDs.

Port 3 is configured under software control to provide the following control functions: four external interrupt request

signals (IRQ3-IRQ0); timer input and output signals (TIN and TOUT - Figure 8).

RESET (input, active Low). When activated, **RESET** initializes the Z08615. When **RESET** is deactivated, program execution begins from the internal program location at 000CH. Reset pin has a 10.4 Kohms pull-up resistor. Once this pin is pulled Low, it takes about 150 μ s for micro-controller initialization.

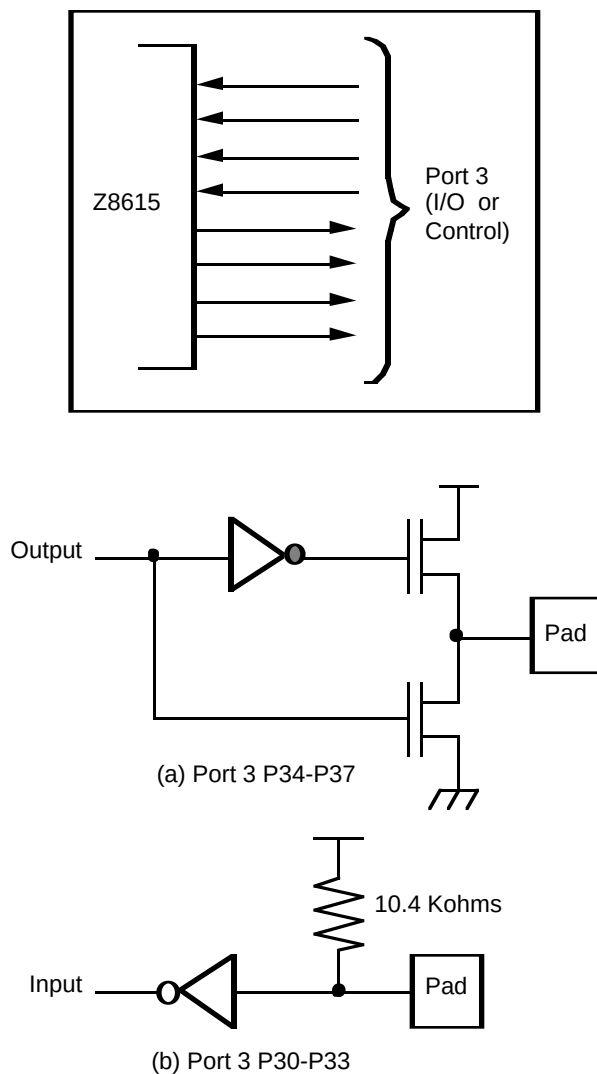


Figure 8. Port 3 P37-P30 Configuration

The device incorporates special functions to enhance Zilog's Z8 applications as a keyboard controller, scientific research and advanced technologies applications.

Program Memory. The 16-bit program counter addresses 4 KB of program memory space at internal locations (Figure 9).

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations have six 16-bit vectors that correspond to the six available interrupts.

Byte 12 to byte 4095 consists of on-chip, mask programmed ROM. Addresses 4096 and greater are reserved.

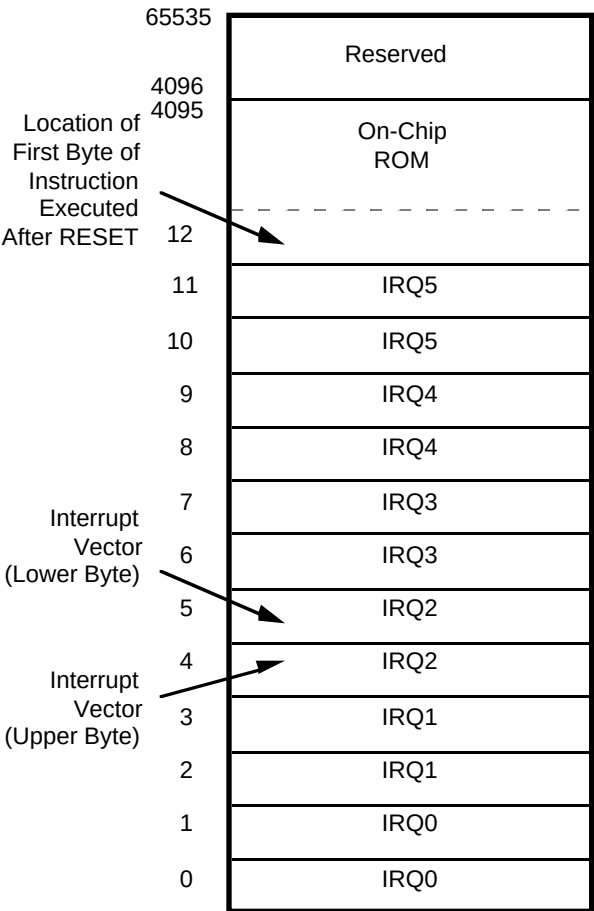


Figure 9. Program Memory Map

Register File. The register file (Figure 10) consists of four I/O port registers, 124 general-purpose registers and 16 control and status registers (R3-R0, R127-R4, and R255-R240, respectively). The instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addressing using the Register

LOCATION		IDENTIFIERS
R255	Stack Pointer (Bits 7-0)	SPL
R254	General-Purpose Register (Bits 7-0)	GPR
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 1-0 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PREQ
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Reserved	
	Not Implemented	
R127	General-Purpose Registers	
R4		
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

Figure 10. Register File

PIN FUNCTIONS (Continued)

Pointer (Figure 11). In the 4-bit mode, the register file is divided into nine working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Stack. The Z08615 internal register files are used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 124 general-purpose registers.

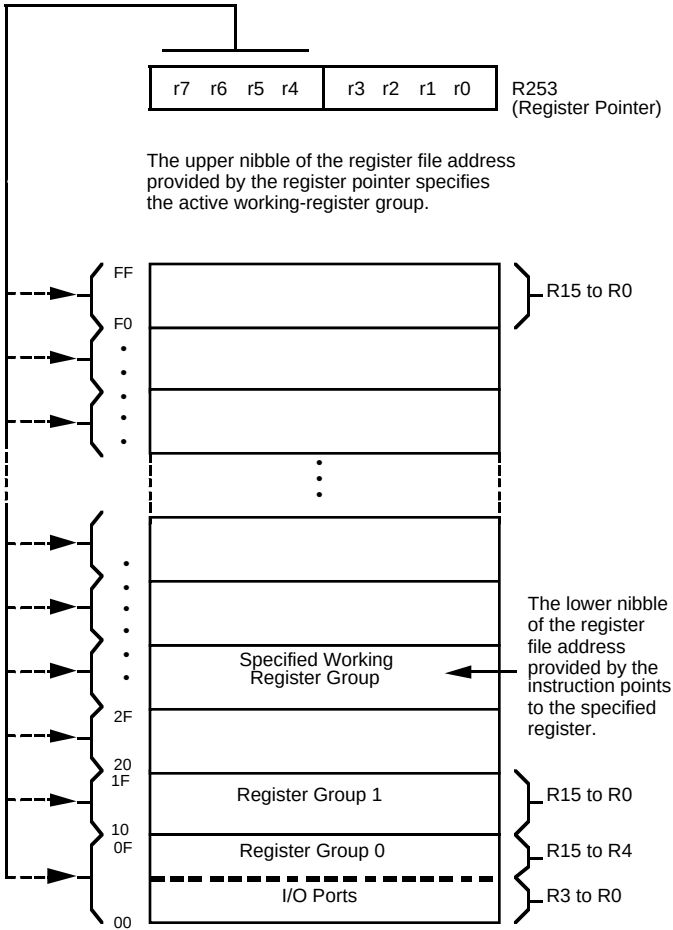


Figure 11. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 12).

The 6-bit prescalers can further divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its own counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counter and prescaler reach the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single

pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and are either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input as an external clock, a trigger input that can be retriggerable or non-triggerable, or as a gate input for the internal clock. The counter/timers can be programmable cascaded by connecting the T0 output to the input of T1. Port 3 lines P36 also serves as a timer output (TOUT) through which T0, T1 or the internal clock are output.

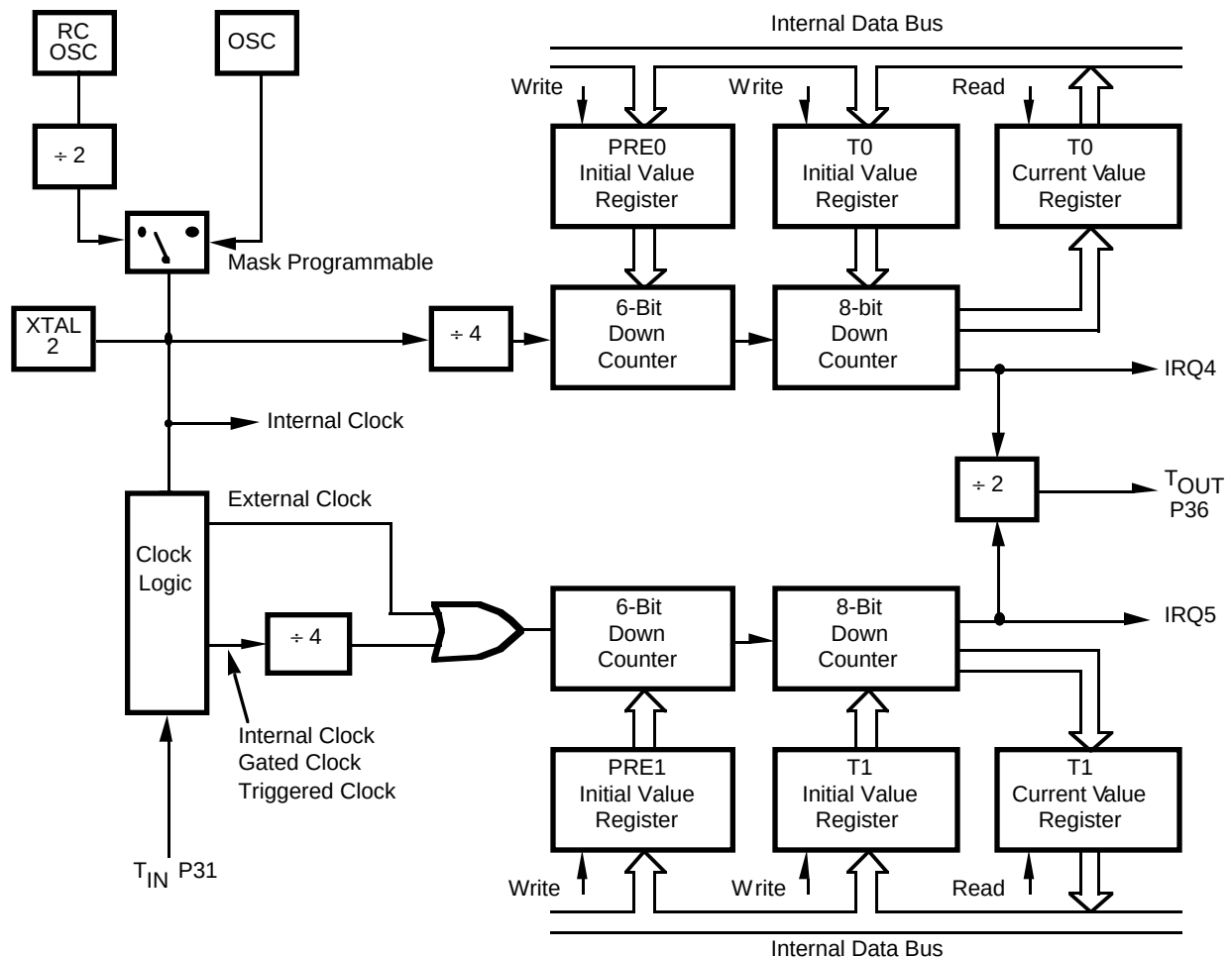


Figure 12. Counter/Timers Block Diagram

PIN FUNCTIONS (Continued)

Interrupts. The Z08615 has six different interrupts from six different sources. These interrupts are maskable and prioritized (Figure 13). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two are claimed by the counter/timers. The Interrupt Masked Register globally or individually enables or disables the six interrupts requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All interrupts are vectored through locations in the program memory. When

an interrupt machine cycle is activated an interrupt request is granted. This disables all of the subsequent interrupts, saves the Program Counter and status flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt request needs service.

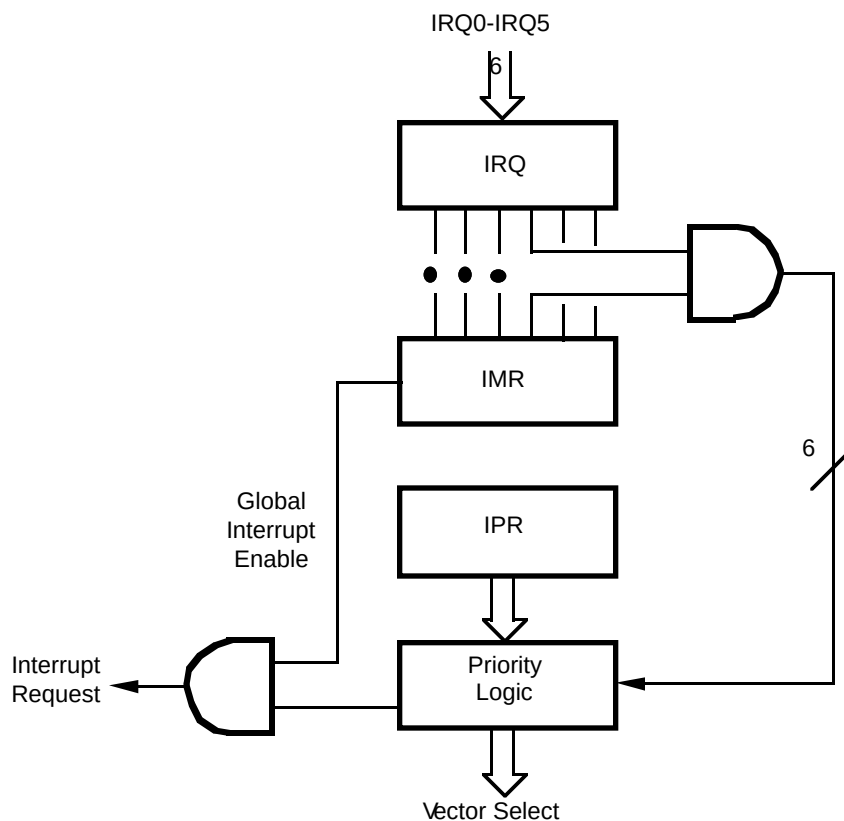


Figure 13. Interrupt Block Diagram

Clock. The Z08615 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The internal clock oscillates at the crystal frequency. The crystal should be AT cut, 5 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the supplier's recommended capacitors from each pin to ground (Figure 14). Capacitance is between

50 pF to 150 pF depending upon the manufacturer of crystal, ceramic resonator and PCB layout.

RC Oscillator. The Z08615 provides an internal capacitor to accommodate an RC oscillator configuration. A 1% precision resistor is necessary to achieve $\pm 10\%$ accurate frequency oscillation.

EMI. The Z08615 offers low EMI emission due to circuit modifications to improve EMI performance. The internal divide-by-two circuit has been removed to improve EMI performance.

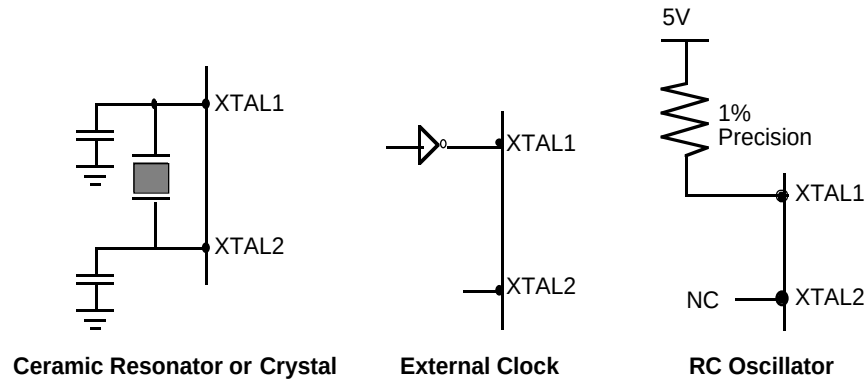


Figure 14. Oscillator Configuration

Watch-Dog Timer (WDT). The Z08615 is equipped with a hardware Watch-Dog Timer which will be turned on automatically by power-on (Figure 16). The Watch-Dog Timer must be refreshed at least once every 50 ms by executing the instruction WDT (Opcode = %5F), otherwise the Z08615 will reset itself if $\overline{\text{WDTOUT}}$ pin 9 is connected to $\overline{\text{RESET}}$ (Pin 6). Figure 16 shows the block diagram of WDT.

The Watch-Dog Timer is automatically enabled upon power-up of the microcontroller and $\overline{\text{RESET}}$ going High. The

$\overline{\text{WDTOUT}}$ pin can be connected to the $\overline{\text{RESET}}$ pin to provide an automatic reset upon WDT time-out. During WDT time-out, the $\overline{\text{WDTOUT}}$ pin goes Low for approximately 8-15 μs .

WDT Hot Bit. Bit 7 of the Interrupt Request Register (IRR register FAH) determines whether a hot start or cold start occurred. A cold start is defined as a reset occurring from the power-up of the Z08615 (bit 7 is set to zero upon power-up). A hot start occurs when a WDT time-out has occurred (bit 7 is set to 1). Bit 7 of the IRQ register is read-only and is automatically reset to 0 when accessed.

Power-On Reset. Upon power-up of the microcontroller, a reset condition is enabled. A delay of 150 ms $\pm 20\%$ is used to assist in initializing the microcontroller.

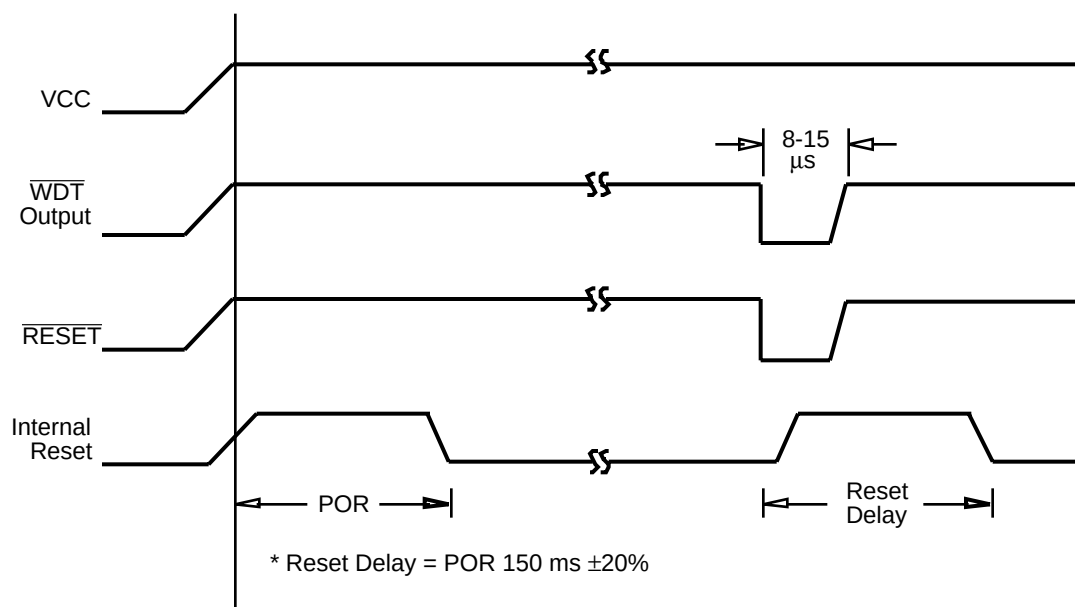


Figure 15. WDT Turn-on Timing After RESET

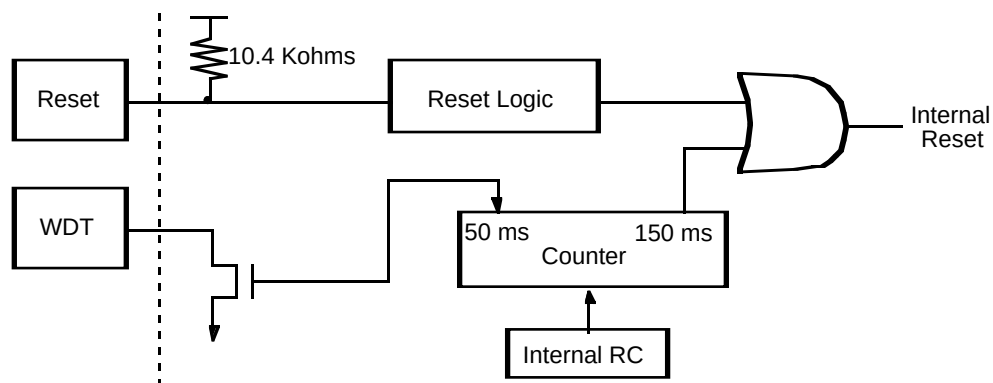
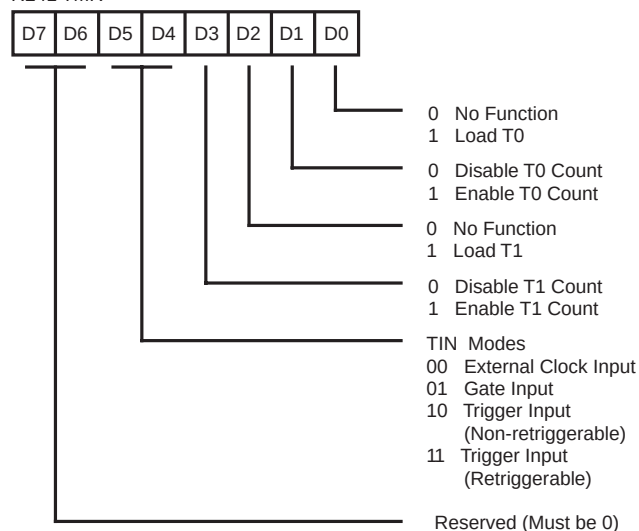


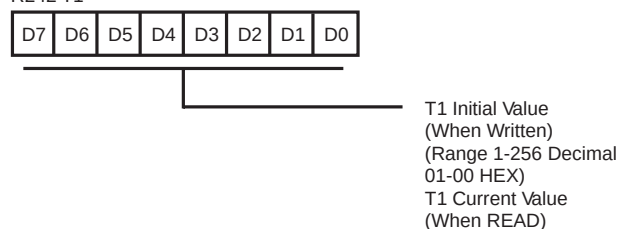
Figure 16. WDT Block Diagram

Z8 CONTROL REGISTERS

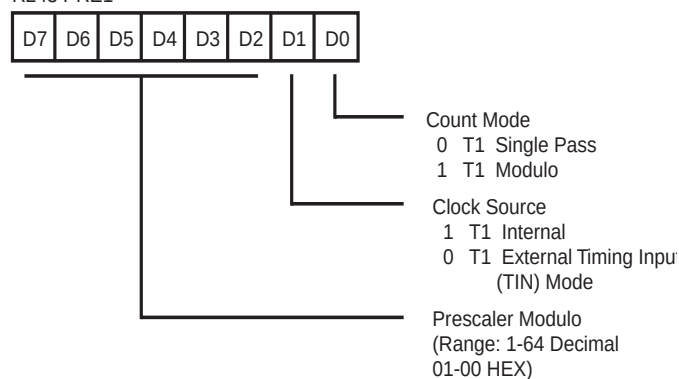
R241 TMR

Figure 17. Timer Mode Register (F1_H:Read/Write)

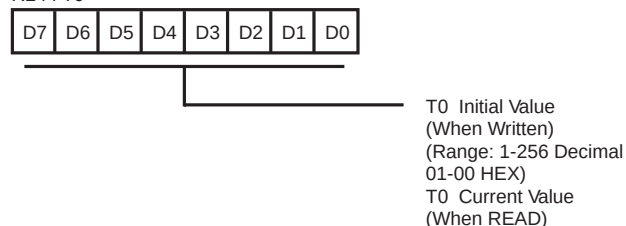
R242 T1

Figure 18. Counter Timer 1 Register (F2_H: Read/Write)

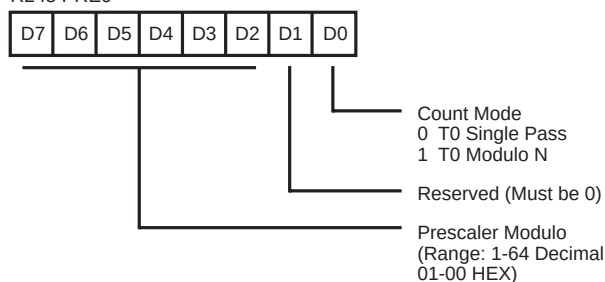
R243 PRE1

Figure 19. Prescaler 1 Register (F3_H:Write Only)

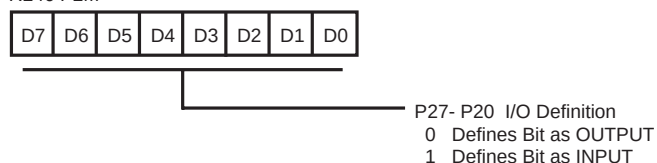
R244 T0

Figure 20. Counter Timer 0 Register (F4_H: Read/Write)

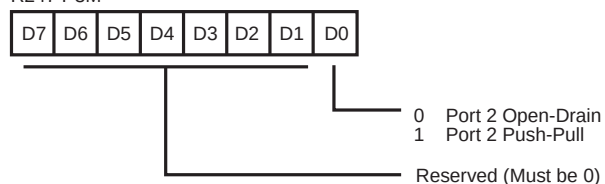
R245 PRE0

Figure 21. Prescaler 0 Register (F5_H: Write Only)

R246 P2M

Figure 22. Port 2 Mode Register (F6_H: Write Only)

R247 P3M

Figure 23. Port 3 Mode Register (F7_H: Write Only)

Z8 CONTROL REGISTERS (Continued)

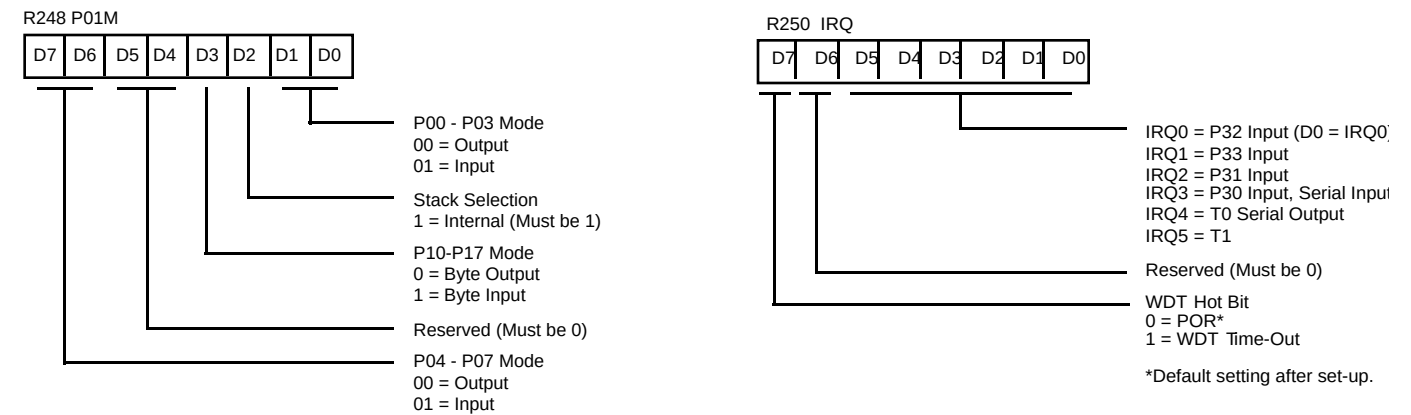


Figure 24. Port 0 and 1 Mode Register (F8H: Write Only)

Figure 26. Interrupt Request Register (FAH: Read/Write)

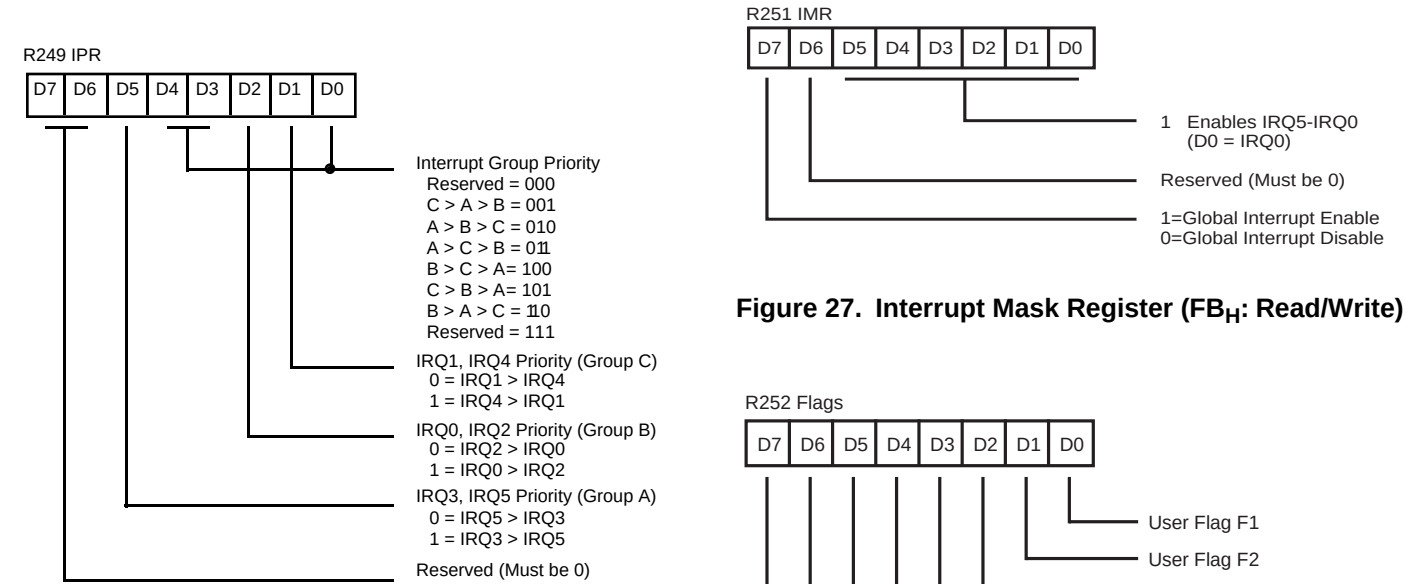


Figure 25. Interrupt Priority Register (F9H: Write Only)

Figure 27. Interrupt Mask Register (FBH: Read/Write)

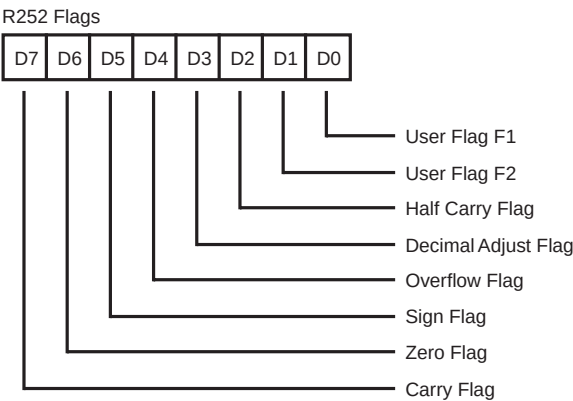


Figure 28. Flag Register (FCH: Read/Write)

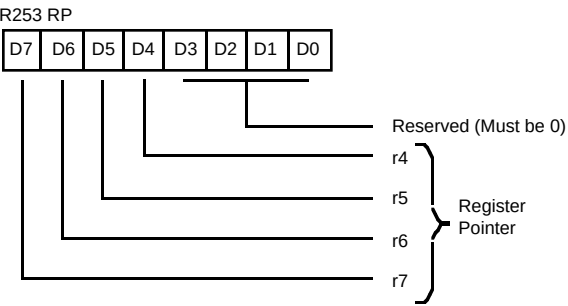


Figure 29. Register Pointer (FD_H: Read/Write)

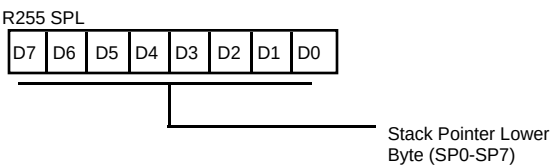


Figure 31. Stacker Pointer (FFH: Read/Write)

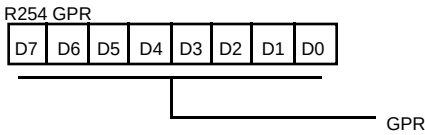


Figure 30. Stack Pointer (FFH: Read/Write)

PACKAGE INFORMATION

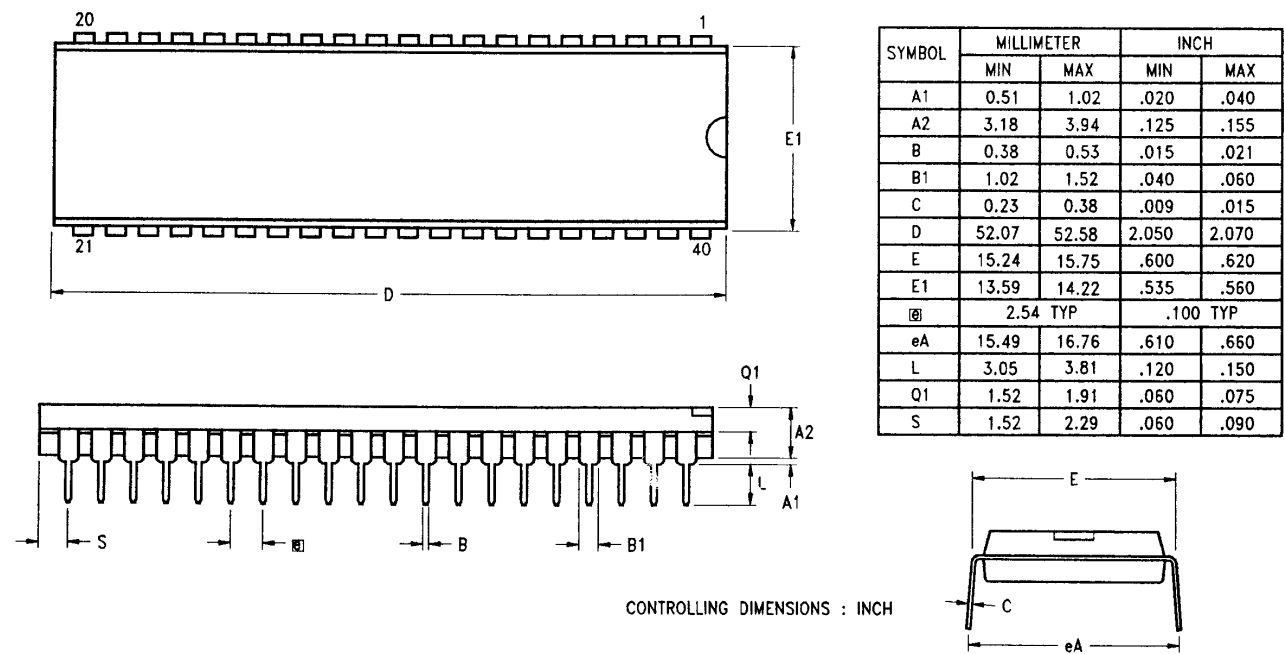


Figure 32. 40-Pin DIP Package Diagram

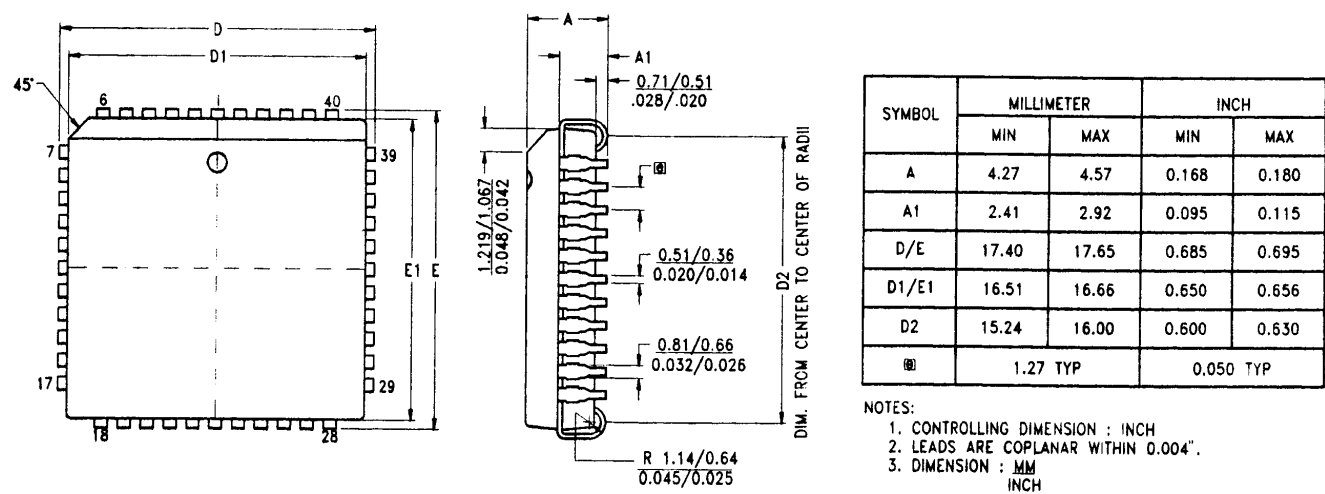


Figure 33. 44-Pin PLCC Package Diagram

ORDERING INFORMATION

Z08615	
5 MHz	5 MHz
Z0861505PSC	Z0861505VSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES**Preferred Package**

P = Plastic DIP

V = Plastic Leaded Chip Carrier

Speed

05 = 5 MHz

Environmental

C = Plastic Standard

Temperature

S = 0°C to +70°C (standard temp for the Z08615 is 0 to -55°C) For fast results, contact your local Zilog sales offices for assistance in ordering the part desired.

Example:

Z 08615 04 P S C is a Z08615, 5 MHz, DIP, 0°C to -55°C, Plastic Standard Flow

The diagram shows the part number Z 08615 04 P S C with lines connecting each part to its description:

- Z**: Zilog Prefix
- 08615**: Product Number
- 04**: Speed
- P**: Package
- S**: Temperature (standard temp for the Z08615 is 0 to -55°C)
- C**: Environmental Flow

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