ZipWire2

CN8980 HDSL2/SDSL Transceiver and Framer

Innovative, Symmetrical xDSL Modem Solution

The Conexant ZipWire2 chipset is a DSL transceiver which provides enhanced performance and better reach at a given data rate than existing symmetric transport systems based on 2B1Q or CAP modulation. ZipWire2 is designed to be fully compliant with the OPTIS based ANSI standard for HDSL2T1 transport and meets all the current requirements of the emerging ETSI standards for SDSL E1 transport. In particular, flexible control of the transmitted signal power spectral density results in enhanced spectral compatibility with other services such as ADSL, T1, E1, HDSL, and ISDN.

The ZipWire2 chipset goes beyond providing modems for T1 or E1 transport by offering on-chip circuits to facilitate variable data rate operation. These allow the user to trade-off data rate for reach performance. Any data rate between 144 Kbps to 4640 Kbps on 8 Kbps boundaries is supported. In addition, ZipWire2 devices provide a mode of operation supporting legacy HDSL1 (2B1Q) transport and framing so that system OEMs can offer Central Office equipment capable of operation with 2B1Q based (e.g., Bt8970/8953A) remote terminals. These CO terminals can be upgraded to OPTIS based HDSL2 through software alone.

Distinguishing Features

- Highly integrated two chip "system" solution
- Multi-rate operation from 144 Kbps to 4640 Kbps with on-chip programmable frequency synthesizer
- Operation in 2B1Q, OPTIS or Trellis coded PAM
- On chip framer and microcontroller
- Compliant to ANSI specifications
- Low power

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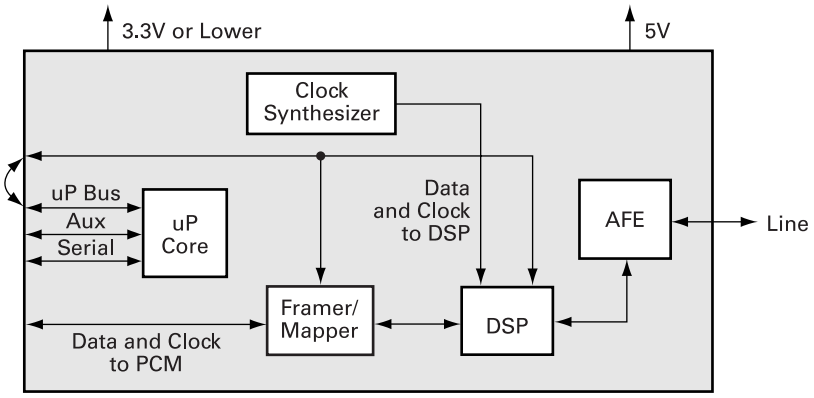
The ZipWire2 device has a two-chip architecture: analog-front-end and line driver in one chip and all digital functions in the other chip. Major functional blocks in the digital chip include:

- A bypassable Framer/Mapper function
- A Rate Adaptive Bit Pump DSP with trellis coding
- A high performance microprocessor core



Functional block diagram

The framer/mapper features a highly flexible bit-processing engine capable of almost any frame format. In particular, it supports the ANSI HDSL2 and ETSI HDSL1 frame formats. It performs EOC, overhead and payload insertion and extraction, data scrambling, bit stuffing and sync detection. The framer supports T1/E1 Primary Rate framed or unframed modes, synchronous or asynchronous payload mapping, and per time slot random or fixed data insertion. In addition, it has programmable external timeslot add/drop controls, bit error metering, and programmable payload mapping supporting 1, 2, 4 or 8 bit time slots.

The rate adaptive DSP is responsible for echo cancellation, line equalization and data coding. It is capable of 2, 4, 8 and 16 PAM coding and contains integrated, a software controlled, clock recovery and synthesis function. The on-chip 8051 compatible microprocessor core provides DSP control and sequencing but can also be used as a general purpose controller for peripheral components such as codecs or T1/E1 framers and to host network management software.

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