Migrating from the Hitachi HD64180 to ZiLOG's Z80180

TABLE OF CONTENTS

Acknowledgements

Project Lead Engineer:
Zhi Wong

Application and Support Engineers:
Craig MacKenna

System and Code Development:
N/A

INTRODUCTION

I. General Overview

To ensure a more reliable source of Z80-based products, and avoid product obsolescence, ZiLOG recommends that customers migrate from Hitachi's HD64180 devices to ZiLOG's Z80180 or Z8S180 embedded microprocessors. This Application Note documents the changes needed to seamlessly migrate from one chipset to the other.

ZiLOG's Z80180 is a pin-to-pin compatible part with Hitachi's HD64180. The device resets to a 64180-compatible state, so that no changes are required to software developed on the 64180. ZiLOG also offers the Z8S180, which is the enhanced static version of Z80180. Refer to the application note "Migrating from the Z80180 to Z8S180" on ZiLOG's website for more information.

SOFTWARE CHANGES

I. How to Configure the Z80180 to Function like the HD64180

Configuring the Z80180 to operate like the HD64180 is accomplished by writing the Operation Mode Control Register (OMCR), which controls the following:

- Operation of the /M1 signal
- Timing of the /IORQ and /RD signals
- RETI operation

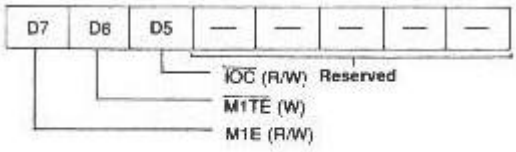

Figure 4. Operation Mode Control Register

To operate like the HD64180, write the Operation Mode Control Register (OMCR) with either a 111XXXXX binary or FF hexadecimal value (the default value at reset). To satisfy the Z80 peripheral (PIO, SIO, or CTC) requirements, however, the user must modify this programming of the Operation Mode Control Register (OMCR) to reflect either a 000XXXXX binary or 0F hexadecimal.

II. Bit Assignments and Register Changes

M1E (/M1 Enable):

This bit controls the M1 output and is set to a 1 during RESET.

When M1E=1, the /M1 output is asserted LOW during op code fetch cycles, /INT0 acknowledge cycles, and the first machine cycle of the /NMI acknowledge. This action also causes the /M1 signal to be active during both fetches of the RETI instruction sequence, causing possible corruption of the external interrupt daisy chain. Therefore, this bit should be set to 0 for the Z80180.

When M1E=0, the /M1 output is normally inactive and asserted LOW only during the re-fetch of the RETI instruction sequence and during the /INT0 acknowledge cycle.

M1TE (M1 Temporary Enable):

Controlling the temporary assertion of the /M1 signal, this bit is always read back and set to 1 during a RESET.

When M1E is set to 0 to accommodate specific external Z80 peripherals, that same device may require a pulse on M1 after programming certain registers in order to complete the programming function. For example, when a control word is written to the Z80 PIO, SIO, or CTC to enable interrupts, no enable actually takes place until the PIO, SIO, or CTC recognizes an active M1 signal.

When M1TE=1, there is no change in the operation of the /M1 signal, and M1E controls its function.

When M1TE=0, the M1 output will be asserted during the next op code fetch cycle regardless of the state programmed into the M1E bit. Additional reprogramming to 1 to disable the function is not needed because the action is only a one-time event (See Figure 5).

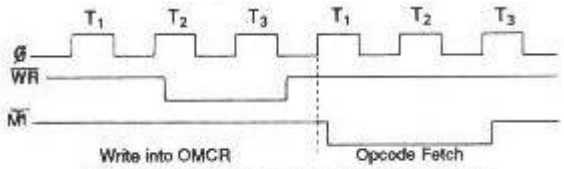

Figure 5. M1 Temporary Enable Timing

/IOC:

Controlling the timing of the /IORQ and /RD signals, this bit is set to 1 by a RESET.

When /IOC=1, the /IORQ and /RD signals function the same as the HD64180.

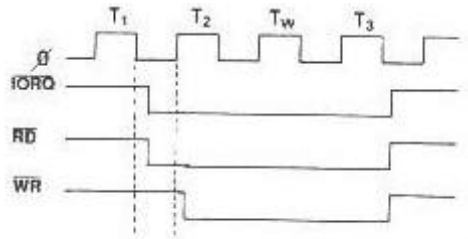

Figure 6. I/O Read and Write Cycles with $\overline{IOC}$ =1

SUMMARY

I. Conclusion

By following these simple instructions, users of Hitachi's HD64180 can now enjoy the features and benefits of ZiLOG's more robust Z80180 without encountering compatibility problems with their end-user applications.

II. Comparison Chart

Hitachi Part	Frequency (MHz)	Package	ZiLOG Part
HD64A180R0P	4	DIP-64	Z8018006PSC
HD64B180R0P	6		
HD64180ZP6	6		
HD64180R1P6	6		
HD64180ZP8	8		Z8018008PSC
HD64180R1P8	8		
HD64180ZP10	10		Z8018010PSC
HD64A180R0F	4	QFP-80	Z8018006FSC
HD64B180R0P	6		
HD64180ZFS6X	6		
HD64180RF6X	6		
HD64180RFS6X	6		
HD64180ZFS8X	8		Z8018008FSC
HD64180RF8X	8		
HD64180RFS8X	8		
HD64180ZFS10X	10		Z8018010FSC
HD64A180R0CP	4	PLCC-68	Z8018006VSC
HD64B180R0CP	6		
HD64180ZCP6X	6		
HD64180RCP6X	6		
HD64180ZCP8X	8		Z8018008VSC
HD64180RCP8X	8		
HD64180ZCP10X	10		Z8018010VSC

NOTES

Information Integrity

The information contained within this document has been verified according to the general principles of electrical and mechanical engineering. Any applicable source code illustrated in the document was either written by an authorized ZiLOG employee or licensed consultant. Permission to use these codes in any form besides the intended application must be approved through a license agreement between both parties. ZiLOG will not be responsible for any code(s) used beyond the intended application. Contact your local ZiLOG Sales Office to obtain necessary license agreements.

Document Disclaimer