MIGRATING FROM Z80180 TO Z8S180

INTRODUCTION

ZiLOG encourages customers to take advantage of static CMOS parts that offer higher-performance and lower-power consumption.

In line with this philosophy, ZiLOG now offers the Z8S180, the static version of the Z80180.

This application note describes the necessary steps to successfully migrate from the Z80180 to the Z8S180. The note includes minor software and hardware modifications required running a Z8S180-based system. In addition, it summarizes the differences between the Z80180 and Z8S180. For the remainder of this Application Note, the Z80180 will be referred to as the Z180, and the Z8S180 will be referred to as the S180.

The S180 is an improved version of the Z180. The S180 was designed to minimize the changes in the existing Z180 designs. Thus, the S180 pin layout is identical to the Z180. Moreover, the S180 supports the same instruction set as the Z180.

Section 2 outlines the features common to both the Z180 and the S180. Sections 3, 4 and 5 of this application note summarize the new features and enhancements to the S180. Section 6 describes these changes in more detail.

EXISTING Z180/S180 FEATURES

- Code Compatible with ZiLOG Z80 CPU
- Extended Instructions
- On-Chip Interrupt Controller
- On-Chip Wait-State Generators
- On-Chip Oscillator/Generator
- Expanded MMU Addressing (up to 1 MB)
- Clocked Serial I/O Port
- Two 16-Bit Counter/Timers
- Standard Operating Temperature Range: 0°C to +70°C
- Extended Operating Temperature Range: –40°C to +85°C
- Three Packaging Styles:
  - 68-Pin PLCC
  - 64-Pin DIP
  - 80-Pin QFP

NEW S180 FEATURES

- Additional power-down modes (STANDBY and IDLE) that reduce power consumption even further than the Z180
- A clock multiplier that allows the usage of lower cost crystals
- A low-noise crystal option that reduces the S180's internal oscillator drive
- The internal oscillator's default drive is reduced by 30%
- The I/O pins, with exception of the XTAL and EXTAL pins, are auto-latches

S180 ENHANCEMENTS

The Asynchronous Serial Communications Interface (ASCI) channels have the "ESCC-like" Baud Rate Generators (BRG). This BRG enables data transfer rates up to 512 Kbits/sec at 33 MHz, in addition to the Z180 style BRG.

The ASCI receiver and transmitter have deeper First In First Out (FIFO) buffers, four and two bytes respectively that increase the communication performance.

The Direct Memory Access (DMA) channels can be "chain-linked," which reduces the CPU intervention during a DMA transfer.

The S180 is a static part that reduces the overall power consumption.

The S180 operates up to 33 MHz at 5.0 Volts and 20 MHz at 3.3 Volts.

SUMMARY OF THE NEW S180 REGISTERS

Register Name	I/O Addr in Hex	Access
ASCI0 Extension Control Reg.	12	R/W
ASCI1 Extension Control Reg.	13	R/W
ASCI0 Time Constant Low	1A	R/W
ASCI0 Time Constant High	1B	R/W
ASCI1 Time Constant Low	1C	R/W
ASCI1 Time Constant High	1D	R/W
Clock Multiplier Reg.	1E	R/W
CPU Control Reg.	1F	R/W
DMA Memory Addr Register Ch 1B	2D	R/W

Register Name	I/O Addr in Hex	Access
ASCI0 Extension Control Reg.	12	R/W
ASCI1 Extension Control Reg.	13	R/W
ASCI0 Time Constant Low	1A	R/W
ASCI0 Time Constant High	1B	R/W
ASCI1 Time Constant Low	1C	R/W
ASCI1 Time Constant High	1D	R/W
Clock Multiplier Reg.	1E	R/W
CPU Control Reg.	1F	R/W
DMA Memory Addr Register Ch 1B	2D	R/W

DETAILED DESCRIPTION OF THE NEW S180 FEATURES

Additional Power-Down Modes

The S180 has several new modes designed to reduce power consumption. The S180 has 4 STANDBY modes, 1 IDLE mode, and a STANDBY/QUICK RECOVERY mode.

Standby Mode

The STANDBY/IDLE mode is selected by multiplexing D6 and D3 of the CPU Control Register (CCR, I/O Address = 1FH).

To enter STANDBY mode:

1. Set D6 and D3 to 1 and 0, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the device is in STANDBY mode, it behaves similar to the SYSTEM STOP mode as it exists on the Z80180, except that the STANDBY mode stops the external oscillator, internal clocks and reduces power consumption to 50 µA (typical).

Since the clock oscillator has been stopped, a restart of the oscillator requires a period of time for stabilization. An 18-bit counter has been added in the S180 to allow for oscillator stabilization. When the part receives an external IRQ or BUSREQ during STANDBY mode, the oscillator is restarted and the timer counts down 2^17 counts before acknowledgment is sent to the interrupt source.

The recovery source must remain asserted for the duration of the 2^17 count; otherwise standby will be resumed.

The following is a description of how the device exits STANDBY for different interrupts and modes of operation.

STANDBY Mode Exit with $\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ input must be asserted for a duration long enough for the crystal oscillator to stabilize, thereby exiting from the STANDBY mode. When $\overline{\text{RESET}}$ is deasserted, it

goes through the normal reset timing to start instruction execution at (logical and physical) address 0000H.

The clocking is resumed within the S180, and at the system clock output, after $\overline{\text{RESET}}$ is asserted when the crystal oscillator is restarted (but not yet stabilized).

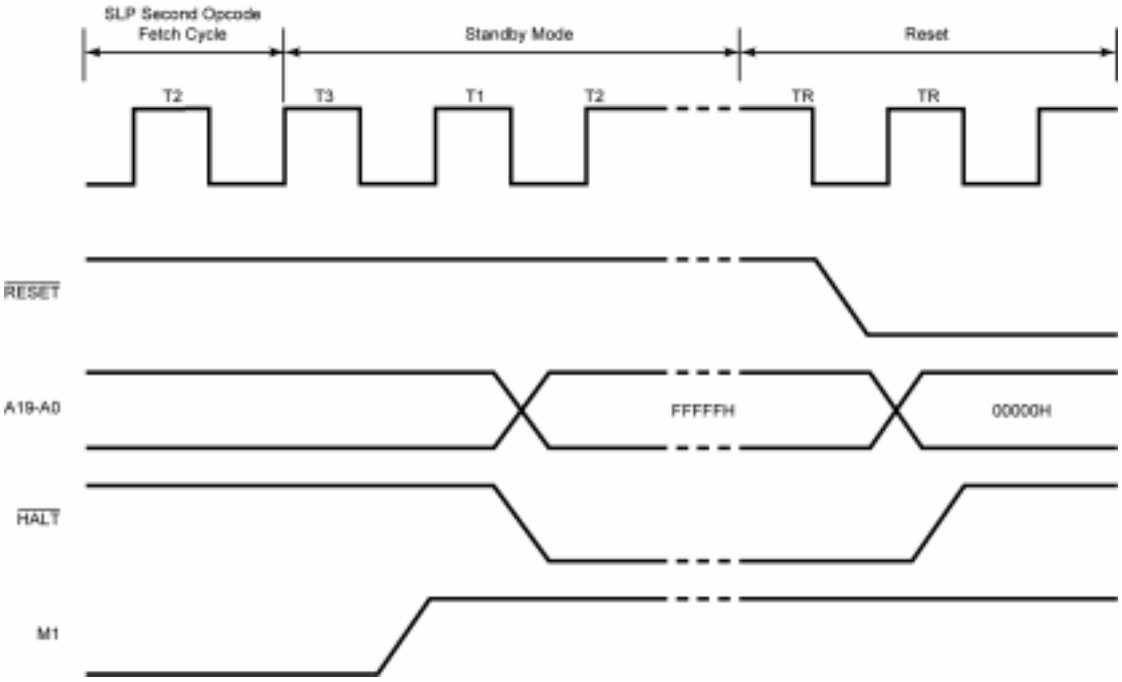

Figure 1. S180 STANDBY Mode Timing With RESET Exit

STANDBY Mode Exit with BUS REQUEST

Optionally, if the BREXT bit (D5 of CPU Control Register) is set to 1, the S180 exits STANDBY mode when the $\overline{\text{BUSREQ}}$ input is asserted; the crystal oscillator is then restarted. An internal counter automatically provides time for the oscillator to stabilize, before the internal clocking and the system clock output of the S180 are resumed.

The S180 relinquishes the system bus after the clocking is resumed by:

- Tri-State the address outputs A19 through A0
- Tri-State the bus control outputs $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, RD and $\overline{\text{WR}}$
- Asserting $\overline{\text{BUSACK}}$

The S180 regains the system bus when $\overline{\text{BUSREQ}}$ is deactivated. The address outputs and the bus control outputs are then driven High; the STANDBY mode is exited.

If the BREXT bit of the CPU Control Register (CCR) is cleared, asserting the $\overline{\text{BUSREQ}}$ will not cause the S180 to exit STANDBY mode.

If STANDBY mode is exited due to a reset or an external interrupt, the S180 remains relinquished from the system bus as long as $\overline{\text{BUSREQ}}$ is active.

DETAILED DESCRIPTION OF THE NEW S180 FEATURES (Continued)

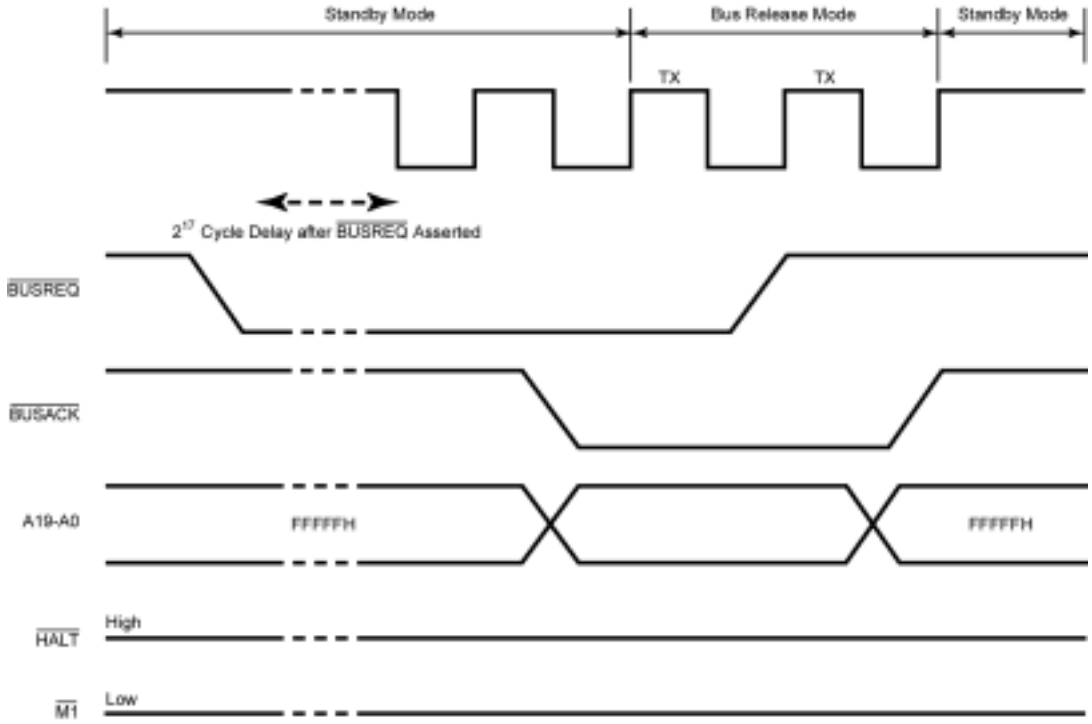

Figure 2. S180 STANDBY Mode Timing With BUS REQUEST

Standby Mode Exit with External Interrupts

STANDBY mode can be exited by asserting input $\overline{\text{NMI}}$. The STANDBY mode may also exit by asserting $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$, depending on the conditions specified in the following paragraphs.

$\overline{\text{INT0}}$ wake-up requires assertion throughout the duration of the clock stabilization time (2^17 clocks).

If exit conditions are met, the internal counter provides time for the crystal oscillator to stabilize before the internal clocking and the system clock output within the S180 are resumed.

1. Exit with Non-Maskable Interrupts

   If $\overline{\text{NMI}}$ is asserted, the CPU begins a normal NMI interrupt acknowledge sequence after clocking resumes.

2. Exit with External Maskable Interrupts

If an External Maskable Interrupt input is asserted, the CPU responds according to the status of the Global Interrupt Enable Flag IEF1 (determined by the ITE1 bit), and the settings of the corresponding interrupt enable bit of the Interrupt/Trap Control Register (ITC: I/O Address = 34H):

a. If an interrupt source is disabled in the ITC, asserting the corresponding interrupt input will not cause the S180 to exit STANDBY mode. This situation is true regardless of the state of the Global Interrupt Enable Flag IEF1.

b. If the Global Interrupt Flag IEF1 is set to 1, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input causes the S180 to exit STANDBY mode. The CPU performs an interrupt acknowledge sequence appropriate to the input being asserted when clocking is resumed if:

   - The interrupt input follows the normal interrupt daisy-chain protocol
   - The interrupt source is active until the acknowledge cycle is completed

c. If the Global Interrupt Flag IEF1 is disabled (in other words, reset to 0), and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input will still cause the S180 to exit STANDBY mode. The CPU will proceed to fetch and execute instructions that follow the SLEEP instruction when clocking is resumed.

If the External Maskable Interrupt input is not active until clocking resumes, the S180 will not exit STANDBY mode. If the Non-Maskable Interrupt ($\overline{NMI}$) is not active until clocking resumes, the S180 still exits the STANDBY mode even if the interrupt sources go away before the timer times out, because $\overline{NMI}$ is edge-triggered. The condition is latched internally when $\overline{NMI}$ is asserted Low.

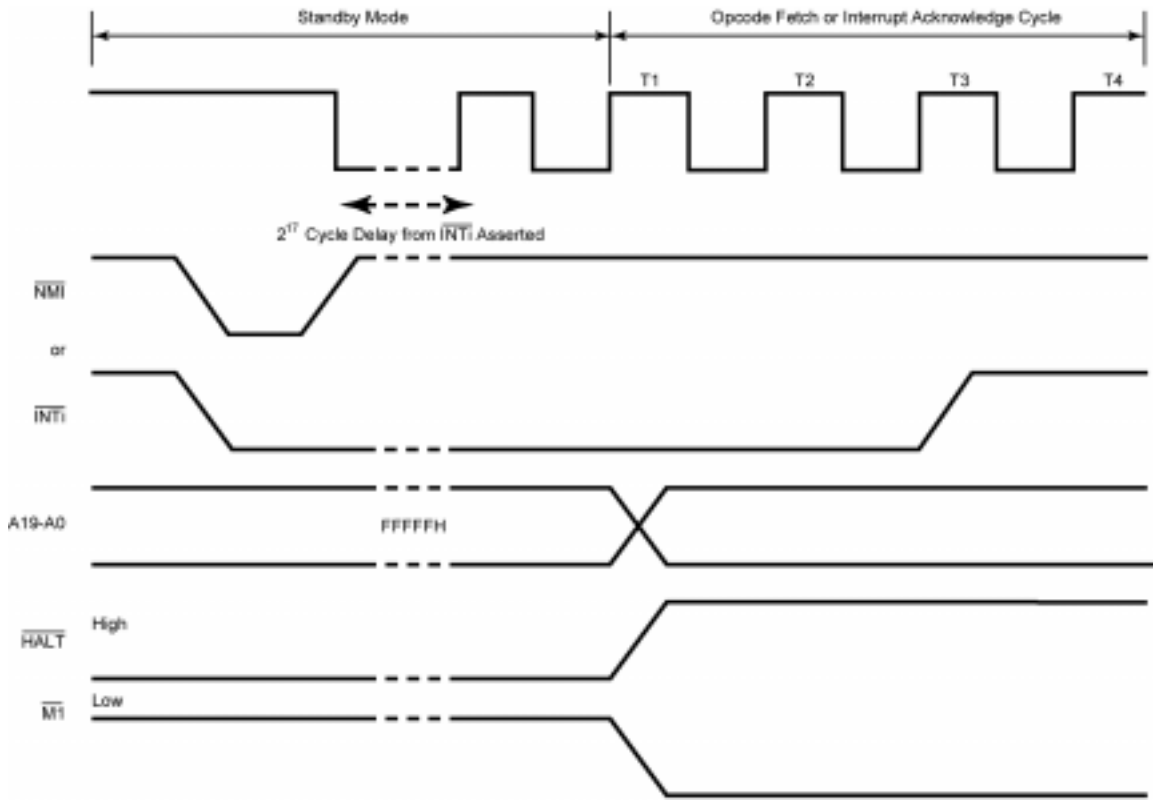

Figure 3. Z8S180 Standby Mode Exit with External Interrupts

IDLE Mode

IDLE mode is another power-down mode offered by the S180. To enter IDLE mode:

1. Set D6 and D3 to 0 and 1, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in IDLE mode, the clock oscillator is kept oscillating, but the clock to the rest of the internal circuit, including the CLKOUT, is stopped completely. IDLE mode is exited in a similar way as STANDBY mode. In other words, RESET, BUS REQUEST or EXTERNAL INTERRUPTS, except that the 2^17 bit wake-up timer is bypassed. All control signals are asserted eight clock cycles after the exit conditions are gathered.

Standby-Quick Recovery Mode

STANDBY-QUICK RECOVERY mode is an option offered in STANDBY mode to reduce the clock recovery time in STANDBY mode from 2^17 clock cycles (6.5 ms at 20 MHz) to 26 clock cycles (3.2 µs at 20 MHz). This feature can only be used when providing an oscillator as the clock source.

To enter STANDBY-QUICK RECOVERY mode:

1. Set D6 and D3 to 1 and 1, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY-QUICK RECOVERY mode, the operation is identical to STANDBY mode except when exit conditions are gathered (in other words, RESET, BUS REQUEST or EXTERNAL INTERRUPTS). The clock and

DETAILED DESCRIPTION OF THE NEW S180 FEATURES (Continued)

other control signals are recovered sooner than the STAND-BY mode.

Power-Down Modes	CPU Core	On-Chip I/O	OSC.	CLKOUT	Recovery Source	Recovery Time (Minimum)
SLEEP	Stop	Running	Running	Running	RESET, Interrupts	1.5 Clock
I/O STOP	Running	Stop	Running	Running	By Programming	—
SYSTEM STOP	Stop	Stop	Running	Running	RESET, Interrupts	1.5 Clock
IDLE	**Stop**	**Stop**	**Running**	**Stop**	**RESET, Interrupts, BUSREQ**	**8 +1.5 Clock**
STANDBY	**Stop**	**Stop**	**Stop**	**Stop**	**RESET, Interrupts, BUSREQ**	**See Notes 1,2,3**

Notes:
1. 2^17 +1.5 Clock (Normal Recovery; 2^6 +1.5 Clock (Quick Recovery).
2. The minimum recovery time can be achieved if INTERRUPT is used as the Recovery Source.
3. New features appear in **boldface type.**

Note: If STANDBY-QUICK RECOVERY is enabled, the user must make sure stable oscillation is obtained within 64 clock cycles.

Clock multiplier that allows the usage of lower cost crystals

A new clock-doubler feature has been implemented in the S180 device that allows the programmer to double the internal clock from that of the external clock. A systems cost savings results by allowing the use of lower cost, lower frequency crystals instead of the higher cost, and higher speed oscillators.

Table 1. Clock Multiplier Register (S180 MPU Address 1EH)

7	6	5	4	3	2	1	0
0	0	1	1	1	1	1	1

Bit	Default	Description
7	0	X2 Clock Multiplier
6	0	Low Noise Crystal
5	1	Reserved
4	1	Reserved
3	1	Reserved
2	1	Reserved
1	1	Reserved
0	1	Reserved

Bit 7: X2 Clock Multiplier Mode

When this bit is set to 1, the programmer is allowed to double the internal clock from that of the external clock. This feature will only operate effectively with frequencies of 10–16 MHz (20–32MHz internal).

Low noise crystal option that reduces the S180's internal oscillator drive

When this bit is set to 0, the S180 device will operate in normal mode. Upon power-up, this feature is disabled.

Bit 6: Low Noise Crystal Option

Setting this bit to 1 will enable the low noise option for the EXTAL and XTAL pins. This option reduces the gain, in addition to reduction the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications where the oscillator may drive the crystal too hard. Setting this bit to 0 will select for normal operation of the EXTAL and XTAL pins. The default for this bit is 0.

Note: Operating restrictions for device operation are listed below. If the low noise option is required, and normal device operation is also required, use the clock multiplier feature.

Low Noise ADDR 1E, bit 6=1	Normal ADDR 1E, bit 6=0
20 MHz @ 4.5V, 100°C	33 MHz @ 4.5V, 100°C
10 MHz @ 3.0V, 100°C	20 MHz @ 3.0V, 100°C

Internal oscillator's default drive reduced by 30%
The power gain across XTAL and EXTAL pins has been reduced by 30%. In other words, the voltage gain has been reduced by ÷3.

The I/O pins, with exception of the XTAL and EXTAL pins, are auto-latches (weak-latches)
The I/O pins are "auto latches;" the maximum leakage current is 10 µA, with exception of XTAL and EXTAL. Thus, strong pull-ups are recommended for the I/O pins.

I/O port bits that are configurable as inputs are protected against open circuit conditions using Auto Latches. An Auto Latch is a circuit which, in the event of an open circuit condition, latches the input at a valid CMOS level. As a result, the tendency of the input transistors to self-bias in the forward active region is inhibited, thus drawing excessive supply current. A simplified schematic of the CMOS S180 I/O circuit is shown in Figure 4.

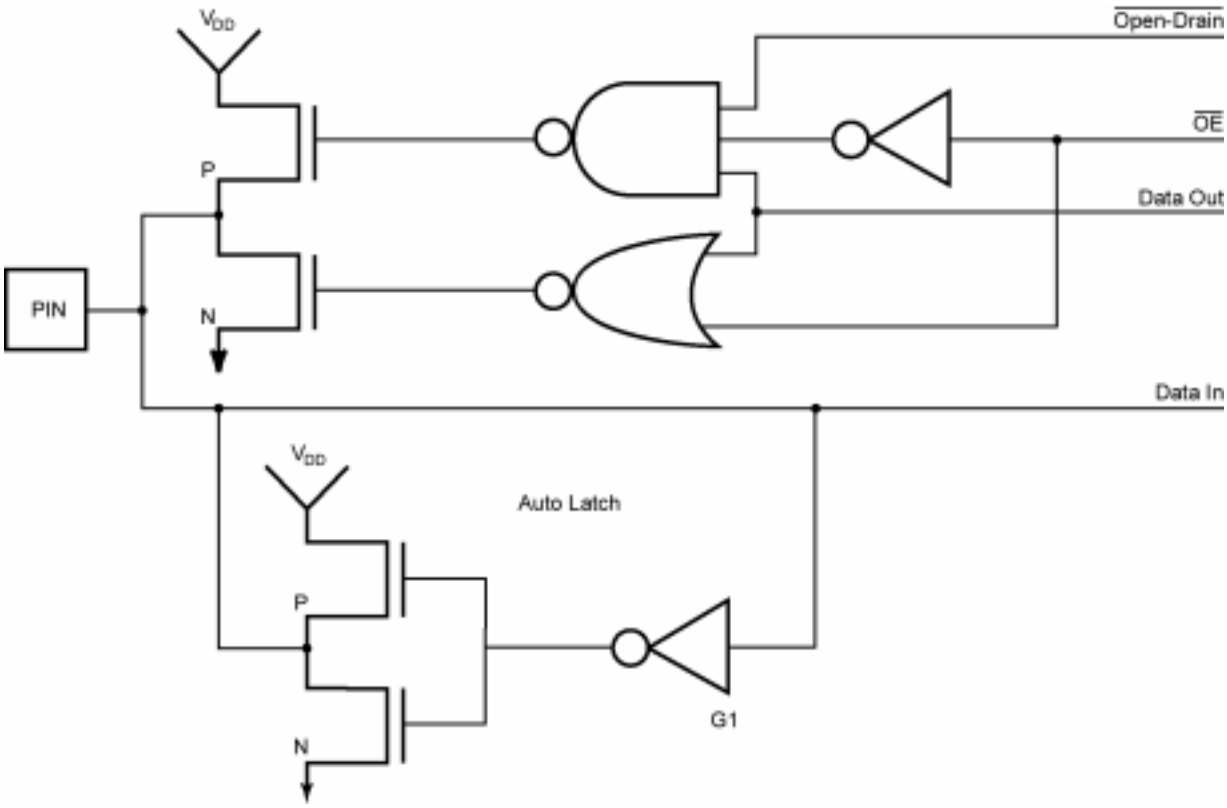

Figure 4. CMOS S180 I/O Circuit

The operation of the Auto Latch circuit is straightforward. Assume the input pad is latched at +5V (Logic 1). The inverter (G1) inverts the bit, turning the P-channel FET ON and the N-channel FET OFF. The output of the circuit is effectively shorted to V_{DD}, returning +5V to the input. If the pad is then disconnected from the +5V source, the Auto Latch will hold the input at the previous state. If the device is powered up with the input floating, the state of the Auto Latch will be at either supply; however, predictability is indeterminable. There are four operating conditions, which will activate the Auto Latches. The first, which occurs when the input pin is physically disconnected from any source, is the most obvious. The second occurs when the input is connected to the output of a device with tri-state capability.

The Auto Latch will also activate when the input voltage at the pin is not within 200 microvolts of either supply rail. In this case, the circuit will draw current, which is not significant compared to the I_{CC} operating current of the device; however, this circuit will increase ICC2 STOP Mode current of the device dramatically.

The fourth condition occurs when the I/O bit is configured as an output. Referring to the output section of Figure 5, there are two ways of tri-stating the port pin. The first is by

DETAILED DESCRIPTION OF THE NEW S180 FEATURES (Continued)

configuring the port as an input, which disables the $\overline{OE}$ signal, turning both transistors off. The second can be achieved in output mode by writing a "1" to the output port, then activating the open-drain mode. Again, both transistors are off, and the port bit is in a high impedance state. The Auto Latches then pull the input section toward V_{DD}.

Auto Latch Model:

The Auto Latch's equivalent circuit is shown in Figure 5. When the input is High, the circuit consists of a resistance R_P from V_{DD} (the P-channel transistor in its ON state) and a much greater resistance R_H to GND. Current I_{AO} flows from V_{DD} to the output. When the input is Low, the circuit may be modeled as a resistance R_P from GND (the N-channel transistor in the ON state) and a much greater resistance R_H to V_{DD}. Current I_{AO} now flows from the input to ground. The Auto Latch is characterized with respect to I_{AO}, so the equivalent resistance R_P is calculated according to $R_P = (V_{DD} - V_{IN})/I_{AO}$. The worst case equivalent resistance R_P (min) may be calculated at the worst case input voltage, $Vi = V_{IH(MIN)}$.

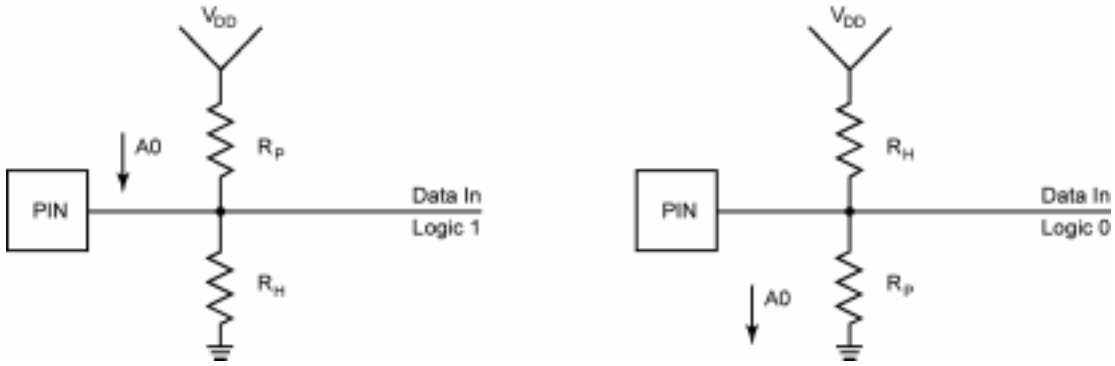

Figure 5. Auto Latch Equivalent Circuit

Design Considerations

For circuits in which the Auto Latch is active, consider the loading constraints of the Auto Latches.

Example: With weak values of V_{IN}, close to $V_{IH(MIN)}$ or $V_{IL(MAX)}$, pull-up or pull-down resistances must be calculated using Ref = R/R_P. For best case STOP mode operation, the inputs should be within 200 mV of the supply rails.

In output mode, if a port bit is forced into a tri-state condition, the Auto Latches will force the pad to V_{DD}. If there is an external pull-down resistor on the pin, the voltage at the pin may not switch to GND due to the Auto Latch. As shown in Figure 6, the equivalent resistance of the Auto Latch and external pull-down form a voltage divider, and if the external resistor is large, the voltage developed across it will exceed $V_{IL(MAX)}$. For worst case:

$$V_{IL(MAX)} > V_{DD} [R_{EXT} / (R_{EXT} + R_P)]$$

$$R_{EXT(MAX)} = [(V_{IL(MAX)} / V_{DD})R_P] / [1-(V_{IL(MAX)} / V_{DD})]$$

For V_{DD} = 5.0V and I_{AO} = 5 µA, $V_{IH(MAX)}$ = 0.8V

$$R_{EXT(MAX)} = (0.16 / 1M) / (1-0.16) = 190\ K\Omega$$

R_P increases rapidly with V_{DD}, so increased V_{DD} will relax the requirement on R_{EXT}.

In summary, the CMOS S180 Auto Latch inhibits excessive current drain in S180 devices by latching an open input to either V_{DD} or GND. A current I_{AO} and a resistor R_P, whose value is V_{DD}/I_{AO}, may model the effect of the Auto Latch on the I/O characteristics of the device.

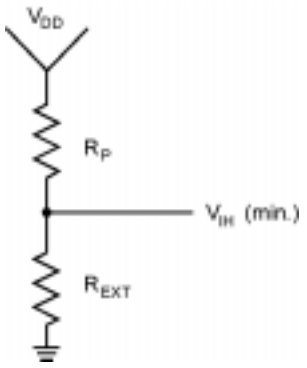

Figure 6. Effect of Pull-Down Resistors on Auto Latches

Detailed Description of the S180 Enhancements

ASCI channels

The Asynchronous Serial Communications Interface (ASCI) channels have the "ESCC-like" Baud Rate Generators (BRG) which enable data transfer rates up to 512 Kbits/sec at 33 MHz.

The Baud Rate Generator (BRG) has two modes. The first is the same as in the Z180. The second is a 16-bit down counter that divides the processor clock by the value in a 16-bit time constant register, and is identical to the ESCC BRG. As a result, a common baud rate of up to 512 Kbps can be selected. The BRG can also be disabled in favor of an external clock on the CKA pin.

The Receiver and Transmitter will subsequently divide the output of the BRG (or the signal from the CKA pin) by 1, 16 or 64, under the control of the DR bit in the CNTLB register, and the X1 bit in the ASCI Extension Control Register. To compute baud rate, use the following formulas.

If ss2,1,0 = 111, baud rate = fCKA / Clock mode

else if BRG mode baud rate = fPHI / (2 * (TC+2) * Clock mode)

else baud rate = fPHI / ((10 + 20*PS) * 2^ss * Clock mode)

Where:

- BRG mode is bit 3 of the ASEXT register
- PS is bit 5 of the CNTLB register
- TC is the 16-bit value in the ASCI Time Constant registers

The TC value for a given baud rate is:

TC = (fPHI / (2 * baud rate * Clock mode)) – 2

Table 2. ASCI Extension Control Register 0 (ASEXT0: S180 MPU Address 12H)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bit	Default	Description
7	0	RDRF0 DI
6	0	Disable DCD0
5	0	Disable CTS0
4	0	X1
3	0	BRG0 Mode
2	0	Enable Break
1	0	Break
0	0	Send Break

Table 3. ASCI Extension Control Register 1 (ASEXT1: S180 MPU Address 13H)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bit	Default	Description
7	0	RDRF1 DI
6	0	Reserved
5	0	Reserved
4	0	X1
3	0	BRG1 Mode
2	0	Enable Break
1	0	Break
0	0	Send Break

RDRF Interrupt Disable (bit 7). If this bit is 1, an ASCI does not request receive data interrupts. This bit should be set to 1 when a DMA channel is used to handle an ASCI's receive data.

DCD0 Disable (bit 6, ASCI0 only). If bit 0 of the Interrupt Edge Register is 0 to select the DCD0 function for the DCD0/CKA1 pin (and this bit is 0), then the DCD0 pin "auto-enables" the ASCI0 receiver, such that when the pin is negated/high, the Receiver is held in a reset state. If bit 0 of the IER is 0 and this bit is 1, the state of the DCD0 pin has no effect on receiver operation. In either state of this bit, software can read the state of the DCD0 pin in the STAT0 register, and the receiver will interrupt on a rising edge of DCD0 if its RIE bit is 1.

DETAILED DESCRIPTION OF THE NEW S180 FEATURES (Continued)

CTS0 disable (bit 5, ASCI0 only). If bit 5 of the System Configuration Register is 0 to select the CTS0 function of the CTS0/RxS pin (and this bit is 0), then the CTS0 pin "auto-enables" the ASCIO transmitter. When the CTS0 pin is negated/high, the TDRE bit in the STAT0 register is forced to 0. If bit 5 of the System Configuration Register is 0 (and this bit is 1), the state of the CTS0 pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the CTS0 pin in the CNTLB0 register.

X1 (bit 4). If this bit is 1, the clock from the Baud Rate Generator or CKA pin is taken as a "1X" bit clock (sometimes termed "isochronous" mode). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in the CNTLB register to obtain the actual bit rate. In this mode, receive data on the RxA pin does not require synchronization to a clock.

BRG Mode (bit 3). If the SS2–0 bits in the CNTLB register are not 111, and this bit is 0, the ASCI's Baud Rate Generator divides PHI by 10 or 30 depending on the DR bit in CNTLB. Then, by a power of two selected by the SS2–0 bits, the DR bit can obtain the clock that is presented to the transmitter and receiver allowing it to be an output on the CKA pin. If SS2–0 are not 111, and this bit is 1, the Baud Rate Generator divides PHI by the quantity (twice the 16-bit value programmed into the Time Constant Registers, plus two). This mode is identical to the operation of the baud rate generator in the ESCC.

Break Enable (bit 2). If this bit is 1, the receiver will detect Break conditions and report them in bit 1, allowing the transmitter to send Breaks under the control of bit 0.

Break Detect (bit 1). The receiver sets this read-only bit to 1 when an all-zero character with a Framing Error becomes the oldest character in the Rx FIFO. The bit is cleared when the software writes a 0 to the EFR bit in CNTLA register, by a Reset, by IOSTOP Mode, and for ASCIO (if the DCD0 pin is auto-enabled and is negated high).

Send Break (bit 0). If this bit (and bit 2) are both 1, the transmitter holds the TXA pin Low to send a Bread condition. The duration of the Bread is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.

ASCI0 Time Constant Register Low (S180 MPU Address 1AH)
ASCI0 Time Constant Register High (S180 MPU Address 1BH)
ASCI1 Time Constant Register Low (S180 MPU Address 1CH)
ASCI1 Time Constant Register Low (S180 MPU Address 1DH)

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

If the SS2–0 bits in the CNTLB register are 111, and the multiplexed CKA pin is selected for the CKA function, then the pin is used as a clock input, dividing the sampling rate by the receiver and transmitter:

bits/second = fCKAin / Sampling Rate

If the SS2–0 bits are not 111, and the BRG Mode bit in the ASEXT register is 0, then the baud rate generator divides PHI for serial clocking.

bits/second = fPHI/ ((10+20*PS) *2^SS2–0 *Sampling Rate)

where PS selects between a "prescaler" of 10 and 30, and 2^SS2–0 is a power of two between 1 and 64. If the multiplexed CKA pin is selected for the CKA function, it outputs the clock before the final division by the Sampling Rate:

fCKAout = fPHI/((10+20*PS)*2^SS2–0)

If the SS2–0 bits are not 111, and the BRG Mode bit is 1, the baud rate generator divides PHI for serial clocking as on the ESCC:

bits/second = fPHI/(2*(TC+2)*Sampling Rate)

Where TC is the 16-bit value programmed into the TC High and Low registers. If the multiplexed CKA pin is selected for the CKA function, it outputs the clock before the final division by the Sampling Rate:

fCKAout = fPHI/(2*(TC+2))

To find the TC value for a particular serial bit rate:

TC = (fPHI / (2*bits/second*Sampling Rate)) – 2

The ASCI Receiver and Transmitter

The ASCI receiver and transmitter have deeper First In First Out (FIFO) buffers (four and two bytes, respectively), that increase the communication performance.

ASCI Transmit Shift Register 0, 1 (TSR0, 1)

When the ASCI Transmit Register receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for transmission, TSR idles by outputting a continuous High level. This register is not program accessible.

ASCI Transmit Data Register 0, 1 (TDR0, 1:I/O Address = 06H, 07H).
Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as it is empty. Data can be written while the TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered.

Data can be written into and read from the ASCI Transmit Data Register. If data is read from the ASCI Transmit Data Register, the ASCI data transmit operation will not be affected by the read operation.

ASCI Receive Shift Register 0, 1 (RSR0, 1)
This register receives data shifted in on the RXA pin. When a character has been received, it is automatically transferred to the ASCI FIFO, if the FIFO is not full. If the FIFO is full when the next incoming data byte is completed, an overrun error occurs. This register is not program accessible.

ASCI Receive Data FIFO 0, 1 (RDR0, 1:I/O Address = 08H, 09H).
The ASCI Receive Data Register is a read-only register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4-character Receive Data First-In First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. Thus, the ASCI receiver is well buffered.

ASCI Status FIFO
This 4-entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the status registers as described below.

ASCI Status Register 0, 1 (STAT0, 1)
Each channel status register allows interrogation of ASCI communication, error and modem control signal status, and enabling or disabling of ASCI interrupts.

Direct Memory Access (DMA) channels

The Direct Memory Access (DMA) channels can be "chain-linked" to reduce the CPU intervention during a DMA transfer. If both channels are programmed to survive the same high-speed device, special request-routing logic can be enabled to switch the request between them as each completes a data buffer. This feature allows the processor software to program a new buffer address and byte count into one channel as the other is operating, making it possible to handle very fast and demanding I/O devices.

Table 4. DMA I/O Address Register Channel 1 (S180 MPU Address 2DH)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bit	Default	Description
7	0	AltE
6	0	AltC
5	0	Reserved
4	0	Reserved
3	0	TOUT/DREQ
2	0	Req1Sel
1	0	Req1Sel
0	0	Req1Sel

AltE: Alternating Channel Enable (Bit 7). The alternating channel enable bit should be set to 1 only when both DMA channels are programmed for the same I/O device. When this bit is 1, a "channel end" condition (byte count = zero) on channel 0 sets bit 6 (AltC), which then routes the device's Request signal to channel 1 rather than channel 0. Similarly, a channel end condition on channel 1 clears bit 6 (AltC), which then routes the device's Request to channel 0 rather than channel 1.

AltC (Bit 6). When bit 7 (AltE) is 1, and this bit is 0, the Request signal selected by bits 2–0 is not presented to channel 1, but channel 0's Request operates normally. When AltE is 1, and this bit is 1, the Request selected by SAR18–16 or DAR18–16 is not presented to channel 0, but channel 1's request operates normally. This bit can be written by software, but should be performed only when both channels are stopped (both DE1 and DE0 are zero), to select which channel operates first.

TOUT/DREQ (Bit 3). If this bit is 0, as it is after a Reset, the TOUT/DREQ pin acts as a DREQ input. When this bit is 1, the pin carries the TOUT output from PRT channel 1.

Req1Sel (Bit 2). These 3 bits select which Request signal is presented to DMA channel 1:

000 External TOUT/DREQ

001 ASCI 0 Request (TDRE or RDRF)

010 ASCI 1 Request (TDRE or RDRF)

011 ESCC Request

111 Bidirectional Centronics Request

The I/O pins, with exception of the XTAL and EXTAL pins, are auto-latches (weak-latches). Thus, strong pull-ups are recommended for the I/O pins.

APPENDIX A: A SUMMARY OF THE S180 ADVANTAGES

Commercial Advantages of the S180	
Feature	**Benefit**
Lower Device Price	Lower System Cost
Pin-to-Pin Compatible to Z80180	Drop-in Replacement
Code Compatible	Same Support Tools
Static Part	Lower Power Consumption

Technical Advantages of the S180	
Feature	**Benefit**
Faster Clock Speeds (33 MHz)	Higher Performance
Additional Power Down Modes	Less Power Consumption
Clock Multiplier Option (x2)	Inexpensive Crystals
Low Noise Crystal Option (30%)	Reduced EMI
Faster UART (512 Kbits/sec at 33 MHz)	Higher Performance
Deeper UART FIFO (2 Tx, 4 Rx)	Higher Performance
Chain-linked DMA	Higher Performance
Low Power Option (3.3 V at 20 MHz)	Compact Designs

ZiLOG, Inc.
910 East Hamilton Avenue, Suite 110
Campbell, CA 95008
Telephone (408) 558-8500
FAX 408 558-8300
Internet: http://www.zilog.com