MPEG-1 SYSTEM and VIDEO DECODER

Features

- Single chip MPEG-1 System and Video Decoder, conforming to the MPEG-1 standard (ISO 11172-1,2)
- Highly integrated device:
  - Parses the MPEG-1 system bitstream and performs real-time decoding of video bitstreams at SIF resolution, (352x240 pixels at 30 fps or 352x288 pixels at 25 fps)
  - Synchronizes the MPEG-1 audio and video data
  - Includes the circuitry required for minimal-glue interfacing to host buses, and supports DMA or programmed I/O data transfer, 8 or 16 bits wide
- High quality of decoded video:
  - Accepts up to 5Mbits/second MPEG-1 system bitstream
  - Accepts up to 3Mbits/second MPEG-1 video bitstream
- Flexible video output formats:
  - Supports NTSC and PAL video timing standards
  - Provides progressive SIF-size or interlaced CCIR-size output
  - Provides several video output formats with optional pixel interpolation and field repetition: 24-bit RGB, 16-bit RGB (5,5,5 or 5,6,5), 16-bit YUV 4:2:2, 12-bit YUV 4:1:1
- Full support for stand-alone CD-ROM MPEG-1 applications:
  - Optional on chip sync generation
  - Provides outputs compatible with industry-standard digital video encoders
- On-chip support for synchronization of audio and video:
  - Decodes audio and video time stamps from the MPEG-1 multiplexed system bitstream
  - Provides programmable compensation for the total delays of the audio and video reconstruction chains
  - Maintains synchronization during freeze, single step and slow motion playback of video
  - Two serial output ports provide audio and private bitstreams to external decoders
- Includes special display modes and operating features:
  - Freeze, single step and random access
  - Slow motion, with slowdown factors of 2 to 7
  - Decodes special high-resolution still-image sequences (352x480 NTSC, 352x576 PAL)
  - Performs frame rate conversion from all common MPEG picture rates to standard NTSC or PAL display frame rates, including 3/2 pulldown as a special case
- Interfaces directly to DRAM:
  - Requires 4Mbits of 80ns or faster DRAM
  - Supports two configurations, 256Kx16 or 4x256Kx4
- Occupies minimal PCB area:
  - Available in a 128 pin small-outline PQFP

Applications

- Entertainment and games
- Interactive training/education tools
- Video kiosks and karaoke systems
- Movie players
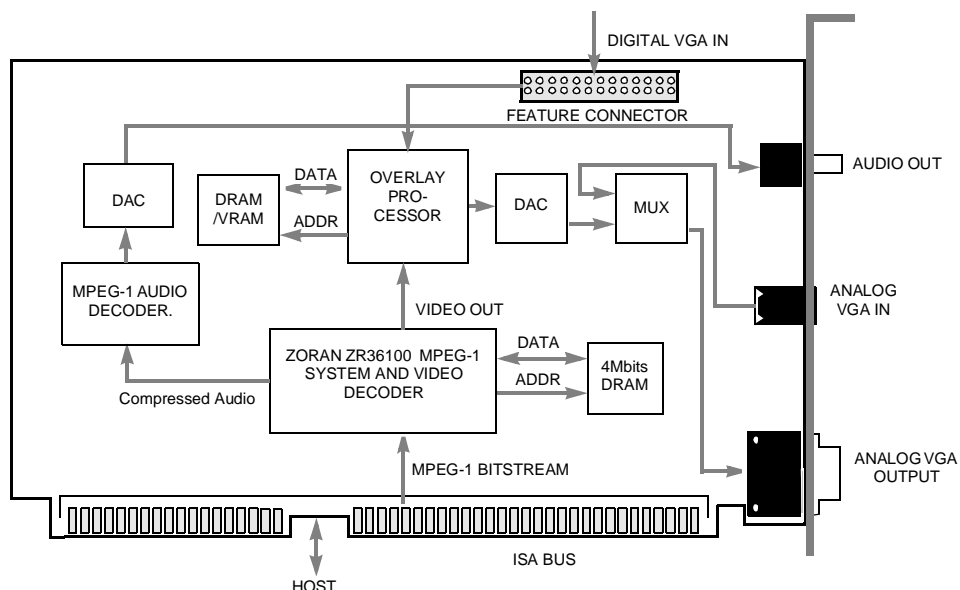- Video-enhanced presentations
- Multimedia books and reference materials

Figure 1. Block Diagram of a Typical MPEG-1 Playback Card

INTRODUCTION

Zoran's ZR36100 MPEG 1 System and Video Decoder is targeted to the needs of developers of cost-sensitive MPEG 1 full-motion video playback products, both personal computer add-in cards and stand-alone consumer Video CD players.

In addition to being a full-motion MPEG 1 video decoder, the ZR36100 is an MPEG 1 system-layer decoder and audio-video synchro-nizer. In this capacity, it demultiplexes the MPEG system bitstream, extracts the time stamps from the individual video and audio bitstreams, buffers both the compressed audio and video data, and provides the audio data to the input of an external audio decoder, all while maintaining full synchronization of audio and video, and compensating for any differences in processing delay of the audio and video decoders. Support from a host controller is minimal, confined mainly to initialization of the ZR36100 for decoding of the desired MPEG bitstream. During the decoding itself, the host controller is only required to feed the bitstream to the decoder while monitoring its status, and optionally giving it on-line commands to enter one of the special decoding modes, but is not required to perform any parsing of the bitstream.

A block diagram of a personal computer MPEG add-in board employing the ZR36100 is shown in Figure 1. This application typifies the interconnection of components in an MPEG decoding system featuring the ZR36100. In this example, the host controller for the ZR36100 is the personal computer's CPU, which initializes the decoder and transfers the bitstream to it. If the host system has a DMA controller, this can be used for the bitstream data transfer, thus reducing the load on the CPU to a minimum.

The decoded video, including appropriate sync signals, is sent to a display control circuit, in this case the overlay processor, where it is scaled to fit a window in the computer's graphics display and provided to the DAC with appropriate timing derived from the graphics card's syncs and pixel clock. The output of the DAC is multiplexed with the analog output of the graphics card to create the effect of MPEG video in a graphics window. Alternatively, the video output of the ZR36100 can be connected directly to a video encoder whose composite video output is suitable for display on a television monitor.

The MPEG audio stream, extracted from the multiplexed bitstream and correctly synchronized with the displayed video by the ZR36100, is passed in bit-serial form to the audio decoder. The analog audio can be connected directly to an audio amplifier and speakers, or to the auxiliary input of the computer's sound system.

FUNCTIONAL DESCRIPTION

Figure 2 is a simplified block diagram of the ZR36100, showing the major functional blocks and their interfaces to the host controller, video display, audio decoder and external DRAM.

Host Interface

The MPEG bitstream is transferred to the ZR36100 through its host bus, a parallel interface typically connected to a host microprocessor. The host interface is also used for initialization of the device prior to starting the MPEG decoding, for on-line commands from the host to start decoding and while decoding is in progress, and for status readout during the initialization and decoding phases.

The host interface has a flexible configuration that allows it to be connected with minimal glue logic to a variety of bus types. It has a 16-bit data bus and two address lines. The byte order on the 16-bit bus is selectable, to conform with either the Intel or Motorola conventions. The bus can also be configured to operate with a width of 8 bits. Two handshake modes are supported for the bitstream transfer, a programmed I/O mode in which the bitstream port is addressed directly by the host CPU, and a mode suitable for DMA. Initialization, on-line commands and status readout always use the programmed I/O mode of access.

System Bitstream Demultiplexing

The System Bitstream Demultiplexer separates the MPEG-1 stream into its elementary streams - the video and audio streams and an optional private data stream. These elementary streams are stored in buffers in the DRAM: one buffer for the video stream data and two buffers for any combination of audio or private data. In addition to MPEG system bitstreams, the system bitstream demultiplexer can be configured to deal with input from the host interface consisting of an MPEG video-only or audio-only elementary bitstream. In these cases, it clearly does not have to perform any demultiplexing, but only stores the incoming data in the DRAM buffer.

The video and audio (or private) elementary streams are extracted concurrently from the buffers in DRAM by the Video Decoder and Audio Synchronizer, respectively.

Video Decoding

The Video Decoder computes the motion vectors, and the Huffman-decoded transform coefficients subsequently undergo dequantization, rescaling, inverse discrete cosine transformation, and motion compensation. Reconstructed pictures are buffered as needed in the DRAM, to be read out later in the correct display order, which is in general not the same as the order of the encoded pictures in the bitstream, because of the presence of B-pictures which require bidirectional prediction.

Video Post Processing

The reconstructed pictures are stored in DRAM in the native progressive SIF 4:2:0 format of MPEG-1, in which each 2 x 2 array of luminance samples is associated with one chrominance sample pair. Before being output through the video interface, they are post-processed by the Video Post Processor and, optionally, the Color Space Convertor, to produce video in one of a number of commonly used pixel representations and one of two raster size options.

The video format (size and representation) options are:

- Progressive SIF-size, with 16-bit YUV 2:1:1 (2:1:1 is the same pixel format as 4:2:2, but for a SIF-size picture), 24-bit RGB, 16-bit RGB (5,6,5), or 15-bit RGB (5,5,5) pixels
- Interlaced CCIR-size, with 16-bit YUV 4:2:2, 12-bit YUV 4:1:1, 24-bit RGB, 16-bit RGB (5,6,5), or 15-bit RGB (5,5,5) pixels

The term "CCIR-size" is used here to denote a video frame whose vertical and horizontal dimensions are each twice that of the original MPEG picture. Typically but not necessarily, the pixel clock frequency and number of pixel clocks per line are as specified in CCIR601. The term is used interchangably for square-pixel or other similar (non-CCIR601) formats.

When interlaced CCIR-size output is selected, the SIF-size pictures are doubled in size horizontally, and (except when performing frame rate conversion, see below) the same picture is output in both fields. Conversion from the native 4:2:0 pixel format to any of the supported representations entails reconstruction of missing rows of chrominance samples; this is done by duplication of the existing rows. In all cases for which missing samples must be reconstucted to double the size horizontally, this can optionally be done by duplication or by interpolation using a two-tap filter. This inlcudes reconstruction of chrominance samples for the RGB representation, which is always 4:4:4, and reconstruction of chrominance and luminance for the doubling to CCIR-size fields.

Video Timing and Sync Generation

The video sync signals have two functions in the ZR36100: the horizontal and vertical sync signals provide the timing for the post-processed video output; the vertical sync signal also determines the rate at which the pictures are decoded from the bitstream.

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The sync signals can be configured as inputs, in which case they are driven by an external sync generator. More commonly, the ZR36100's internal sync generator is used as the master sync generator, and the sync signals are configured as outputs. The sync generator is highly programmable, and is capable of generating the standard interlaced NTSC and PAL raster formats, as well as a wide variety of other interlaced and progressive formats.

The ZR36100 supports cropping of the decoded picture, so that the active displayed region can optionally be smaller than the decoded picture. With the exception of some necessary restrictions, the active region can be positioned anywhere within the display raster defined by the vertical and horizontal sync signals. The display region outside the active region, except for the horizontal and vertical blanking regions, is filled with a user-specified background color.

Video decoding in the ZR36100 is tightly synchronized to the vertical sync signal. That is, it decodes pictures from the video stream, and thus consumes the video stream (and consequently the whole MPEG system bitstream), at a rate which bears a fixed relationship to the video frame rate. Nominally, this picture decoding rate is the same as the video frame rate. When, however, the video interface is configured for interlaced CCIR-size output, the ZR36100 is also capable of performing conversions from commonly used picture rates to the standard PAL and NTSC frame rates. A simple example of rate conversion supported is 3/2 pulldown, in which a 23.976 pictures/sec video bitstream is decoded, and output at the NTSC rate of 29.97 frames/sec, by displaying each decoded picture during two or three fields in an alternating sequence. This achieves the required ratio of four decoded pictures for every five output frames.

One consequence of the tight coupling of the bitstream consumption rate to the vertical sync rate is that, if the bitstream is provided to the ZR36100 at a constant rate over which it has no control, the master video clock of the ZR36100 should be locked to the bitstream clock to ensure continuous operation without glitches. On the other hand, in a computer environment, where the bitstream can be provided on request, there is no such requirement to lock the clocks.

Serial Ports

The audio or private data from each of the buffers in the DRAM is assigned to one of the two serial output ports. The data is read out of the buffer and output from the serial port at a constant user-programmed rate, which, in the case of an audio stream, is equal to the audio bit rate. The audio decoder connected to the serial port must be able to accept and decode the serial stream at the rate provided by the ZR36100. Since the ZR36100 decodes the video, and consumes the system bitstream, at a rate which is determined by the vertical sync frequency, this usually means that the audio decoder's output sampling clock frequency must be locked to the ZR36100's video clock frequency.

Synchronization of audio and video is achieved by timing the start of audio bitstream output from the serial port, relative to the start of video decoding. The starting time is computed from the time stamps embedded in the MPEG system bitstream. Thereafter, synchronization is maintained automatically by virtue of the constant rates of video decoding and audio bitstream output.

Microcoded Architecture

The ZR36100 comprises a number of hard-wired functional units operating in conjunction with, and under control of, a programmable microcoded unit. Microcode for all the modes and options contained in this data sheet is provided by Zoran. Users are also advised to consult the ZR36100 microcode release notes for information on new features that are added from time to time.

To initialize the ZR36100 for decoding, the host system must load the microcode, and also a 128-byte array of set-up parameters that configure the hard-wired functional units and microcode.

On-line Commands and Special Playback Modes

Once it is initialized, the behavior of the ZR36100 is controlled by the host by means of on-line commands. The commands supported are for the basic playback functions of starting, pausing, continuing and ending decoding, and also the following special playback modes:

- *Single step:* step to the next picture and pause
- *Decode to first I picture:* decode and display until the next I picture is displayed, then pause
- *Decode to next I picture:* freeze the displayed picture and continue decoding until the next I picture, then display it and pause
- *Slow motion:* decode and display with a slowdown factor of 2 to 7
- *Random access:* start or restart decoding at a random location in the bitstream

The ZR36100 can also be configured (by the appropriate set-up parameters) for decoding of specially-encoded high-resolution still-image sequences. These sequences have each still image encoded as a pair of consecutive pictures, of up to the maximum (SIF) picture size supported for normal bitstreams, which can be interlaced in the conventional way to produce an image with double the vertical resolution of standard SIF. The video post-processor and output interface are configured for interlaced CCIR-size operation. The image is doubled horizontally as for a normal MPEG sequence, but the two fields of the display contain the two separate pictures comprising the image. Advancing to the next image is the same as a single step of a normal MPEG sequence.
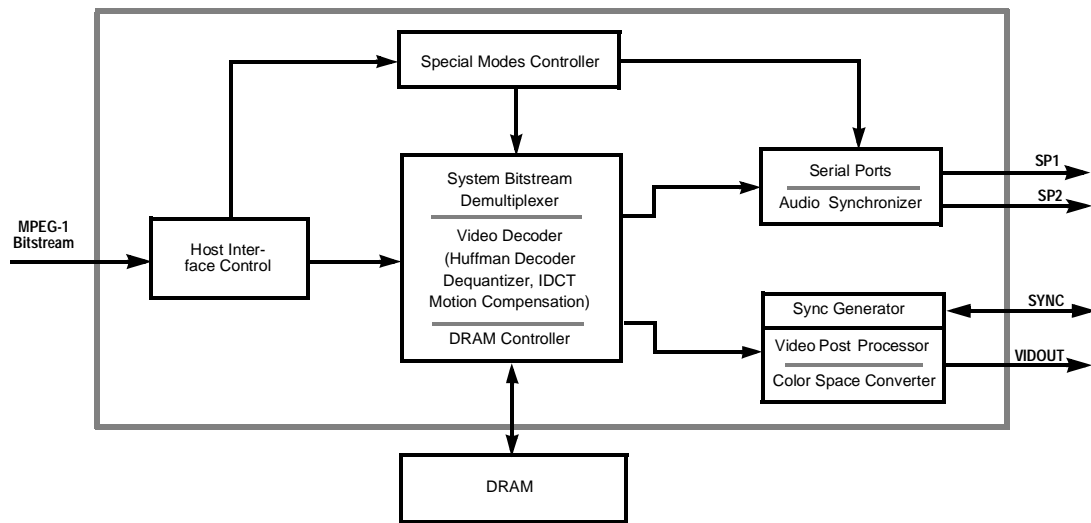
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Figure 2. Simplified Block Diagram

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SIGNAL DESCRIPTION

Name	Type	Description
VCC (5V)	S	5 volt power supply inputs.
VSS (0V)	S	Power supply ground inputs.
GCLK	I	General Clock input. Used by the internal PLL to generate the ZR36100's internal processing clock (PCLK). When $\overline{MB4}$ is low, the PLL multiples GCLK by 4, and the allowed frequency range of GCLK is 13.5MHz to 14.75MHz. When $\overline{MB4}$ is high, the PLL multiples GCLK by 9/2, and the allowed frequency range of GCLK is 12.0MHz to 13.1MHz. In most applications, the VCLK and GCLK pins can be tied together. If the internal crystal oscillator is used, with a crystal connected between GCLK and XT, a 20pF capacitor must be connected between GCLK and VSS.
XT	O	Crystal oscillator output. Instead of using an external clock generator connected to GCLK, a parallel resonant crystal of the required frequency may be connected between GCLK and XT for clock generation. If a crystal is not used, this pin should be left unconnected. If a crystal is used, a 20pF capacitor must be connected between XT and VSS.
$\overline{MB4}$	I	Input signal used to select the multiplication ratio of the PLL. Low selects a ratio of 4 and high selects a ratio of 9/2.
PCLK	O	Output signal used to monitor the ZR36100's internal processing clock. Used for test purposes only.
$\overline{RESET}$	I	Active low reset input. Reset operation is described in the *Reset and Standby Power* section of this document.
$\overline{STDBY}$	I	Active low input that drives the chip to the Standby state, forcing all output signals to float. In Standby the chip consumes a minimal amount of power. For operating restirictions when $\overline{STDBY}$ is activated, see the *Reset and Standby Power* section of this document. *Note*: If $\overline{RESET}$ is activated together with $\overline{STDBY}$, the power consumption is higher than the Standby power, as long as $\overline{RESET}$ is active.
IDLE	O	An active high output signal, activated by the ZR36100 with activation of $\overline{RESET}$ or after the decoding of a sequence has ended. The ZR36100 deactivates the IDLE signal after receiving the **GO** on-line command.
VIDOUT (23:0)	O	24-bit output bus used to output the video data. The data has one of several sizes and formats with different color space, width, and sub-sampling configurations.
VCLK	I	Video clock input. Synchronizes the VIDOUT bus and video sync signals (HSYNC, VSYNC, FI_EN). VCLK is the pixel clock when the video output mode is Interlaced CCIR-size and also in the special Enabled video output mode. VCLK can optionally be configured to be the pixel clock when the video output mode is Progressive SIF-size. When a serial port clock is configured as an output, it is derived by integer division from VCLK.
QCLK_V	O	In the normal video output modes, this is an output clock signal derived by dividing VCLK by 4. QCLK_V can optionally be configured to be the pixel clock when the video output mode is Progressive SIF-size. In the special Enabled video output mode, this is an active high signal indicating that the video output FIFO contains at least 8 valid pixels.
HSYNC	I/O	A signal indicating the beginning of a line on the VIDOUT bus. HSYNC can be configured to be active high or active low, short or long, input or output.
VSYNC	I/O	A signal indicating the beginning of a field or frame on the VIDOUT bus. VSYNC can be configured to be active high or active low, short or long, input or output.
FI_EN	I/O	This signal can be programmed for one of three functions. It can be an input or output signal that indicates the field (Field I or Field II, see note 1) being output. This signal is relevant only for interlaced video output. It can be an output, active low, composite blanking signal. In the Enabled video output mode, this signal is an input, used as an enable signal for the video output.
BUSDAT (15:0)	B	16-bit host interface bus. The MPEG bitstream, set-up parameters, microcode and on-line commands are all transferred to the ZR36100 over this bus. Status is read back to the host using bits 7 and 3:0. Lines 15:8, and 6:4 are input only (they float and are pulled down when read). Lines 7 and 3:0 are bidirectional.

Name	Type	Description
BUSADD (1:0)	I	2-bit input host address bus.
DREQ	O	Active high output control signal requesting data transfer from the host in DMA mode.
$\overline{DACK}$	I	Active low input control signal acknowledging the request of data transfer from the host in DMA mode.
$\overline{BUSWR}$	I	Host interface write strobe.
$\overline{BUSRD}$	I	Host interface read strobe.
$\overline{BUSCS}$	I	Host interface chip select.
READY	O	Active high output host bus control signal permitting data transfer from the host in I/O mode.
RAMDAT (15:0)	B	16-bit bidirectional bus used to transfer data between the ZR36100 and the external DRAM.
RAMADD (8:0)	O	9-bit output bus used by the ZR36100 for addressing the external DRAM.
$\overline{RAS}$	O	Active low output control signal used by the ZR36100 to specify the DRAM row address and enable the transfer of data between the ZR36100 and the DRAM.
$\overline{CAS}$	O	Active low output control signal used by the ZR36100 to specify the DRAM column address and initiate the transfer of data between the ZR36100 and the DRAM.
$\overline{WE}$	O	Active low output control signal used by the ZR36100 to specify whether the transfer of data between the ZR36100 and the external DRAM buffer is a write operation ($\overline{WE}$ low) or a read operation ($\overline{WE}$ high).
SP1DAT	O	Output signal for serial port 1 data. Serial port 1 data can be assigned to an audio stream, or one of the two private bitstreams.
SP1CLK	I/O	Serial port 1 clock. Can be programmed to be either an input or an output.
SP1FRM	O	Output frame synchronization signal for data output from serial port 1.
SP1CMD	O	Output signal used by the ZR36100 to send commands to the receiver of serial port 1 data.
SP2DAT	O	Output signal for serial port 2 data. Serial port 2 data can be assigned to an audio stream, or one of the two private bitstreams.
SP2CLK	I/O	Serial port 2 clock. Can be programmed to be either an input or an output.
SP2FRM	O	Output frame synchronization signal for data output from serial port 2.

Key to signal types: S - power supply; I - input only; O - output only; B - bi-directional bus; I/O - configurable as input or output.

Note 1: When referring to the fields of an interlaced frame, Field I is defined to be the field that starts at the beginning of a line, while Field II is defined to be the field that starts at the middle of a line.

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TYPICAL CIRCUIT DIAGRAM

Figure 3 is a generic schematic showing the connections of the ZR36100 to a host microcontroller, video display circuit, decoders of serial port data, DRAM, clock generator, and general system control circuits.
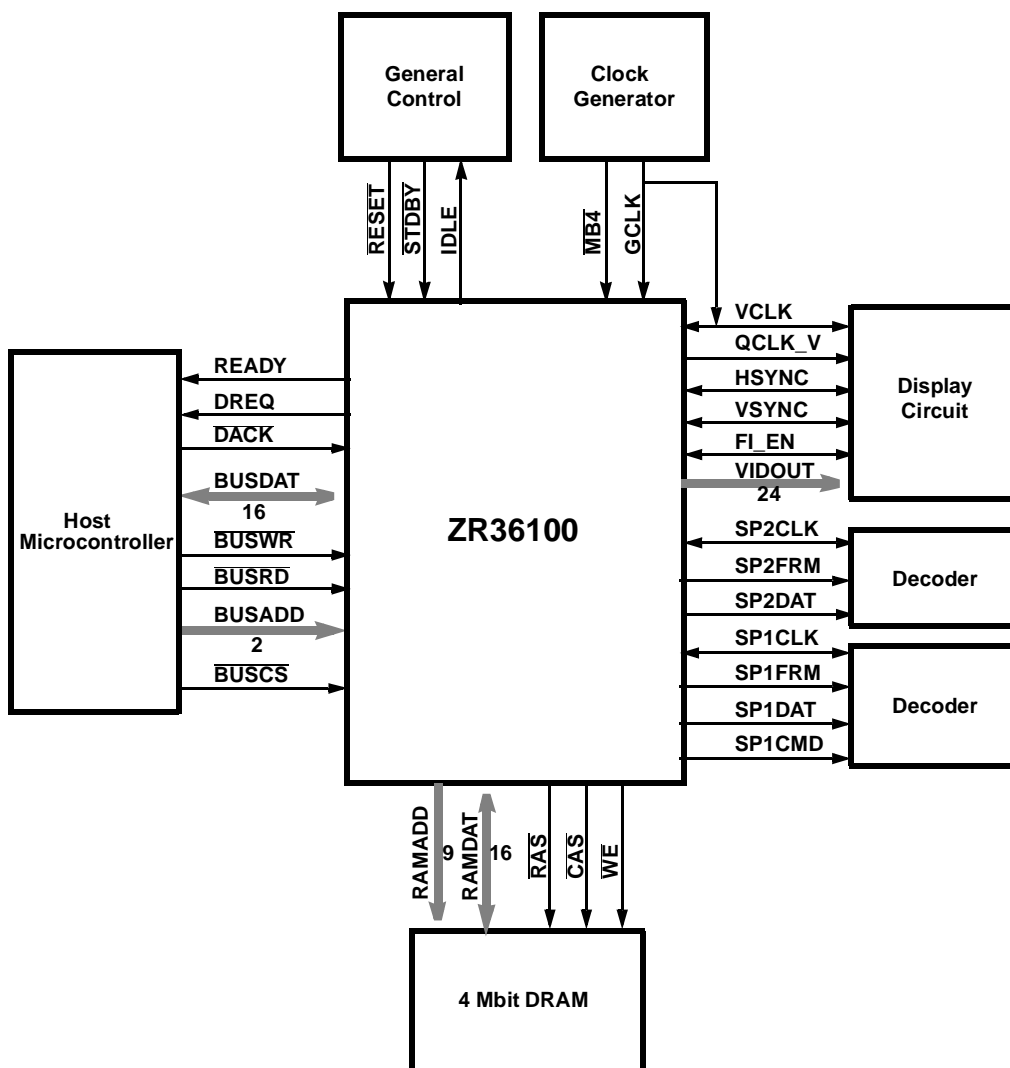

Figure 3. Generic ZR36100 Schematic Diagram

An actual implentation could differ from this in a number of typical ways:

■ Only one serial port is typically used, connected to an audio decoder.

■ The video sync signals, HSYNC and VSYNC, are either outputs or inputs, depending on whether the ZR36100's internal or an external sync generator is used. Depending on the video interface mode, a subset of the 24 bits of the VIDOUT bus may be used, and QCLK_V may be unused.

■ DREQ and DACK are only used if the bitstream is transferred by the host in DMA mode.

■ 8 bits of the BUSDAT bus are unused if the host interface is operated in its 8-bit configuration.

■ The READY and IDLE signals may be unused since their states are available to the host via a status register.

■ VSYNC is typically provided as an interrupt to the host controller, to maintain synchronization of the host software with the decoding of the MPEG bitstream.

SUPPORTED BITSTREAMS

The ZR36100 can be configured to accept the MPEG bitstream in one of three forms:

- System bitstream, with multiplexed video and/or audio and/or private bitstream packets, as defined in ISO 11172-1,2,3
- Video-only bitstream, that is, containing only the elementary video bitstream data, as defined in ISO 11172-2
- Audio-only bitstream, that is, containing only audio bitstream data

The bitstream must be byte-aligned as supplied by the host. For the bitstream to be decoded properly, it must obey the following restrictions.

System (multiplexed) bitstream

The ZR36100 decodes any legal MPEG-1 system bitstream which conforms to the ISO 11172-1 standard and obeys the following restrictions.

System Header

1. rate_bound - Less than or equal to 13107 (in 50 bytes/sec units, equivalent to 5Mbits/sec).

2. STD_buffer_size_bound -

   - Less than or equal to 32 if STD_buffer_size_scale is 0 and the preceding stream_id is "1011 1000". This is equivalent to 4Kbytes bound on the size of the input buffer for each audio or private-1 bitstream.
   - Less than or equal to 46 if STD_buffer_size_scale is 1 and the preceding stream_id is "1011 1001". The above is equivalent to 46Kbytes input buffer for the video bitstream.

Pack Header

3. mux_rate - Less than or equal to 13107 (in 50bytes/sec units, equivalent to 5 Mbits/sec).

Packet Header

4. STD_buffer_size -

   - Less than or equal to 32 if STD_buffer_scale is 0 and the preceding stream_id is "110x xxxx" (They always go together in the packet header). This is equivalent to 4Kbytes input buffer for the audio or private-1 bitstream.
   - Less than or equal to 46 if STD_buffer_scale is set and the preceding stream_id is "1110 xxxx" (They always go together in the packet header). This is equivalent to 46Kbytes input buffer for the video bitstream.
5. The packet rate must be less than or equal to 300 per second.

6. Requirements for audio-video synchronization:

   - The difference between the initial **SCR** and the initial video **PTS**, and between the initial **SCR** and each of the initial **PTS**s (presentation time stamps) of the streams assigned to the serial ports, must be less than 65536.

The concepts "initial SCR," "initial video DTS" and "initial PTS" are defined in the *Playback Operation* section.

Video bitstream (video-only, or the elementary video stream multiplexed in a system bitstream)

The ZR36100 decodes any legal MPEG-1 video bitstream which conforms to the ISO 11172-2 standard and obeys the following restrictions.

Sequence Header

1. horizontal_size - Less than or equal to 352. Minimum value is 32. With certain restrictions, horizontal_size values of 368 and 384, found in some CD-I sequences, are also supported. Details are contained in the ZR36100 microcode release notes.

2. vertical_size - Less than or equal to 288 if the picture_rate is 25 (PAL). Less than or equal to 240 if the picture_rate is 29.97 (NTSC). Minimum value is 32.

3. picture_rate - The picture rate codes supported are: 0001 (23.976 pps), 0010 (24 pps), 0011 (25 pps), 0100 (29.97 pps), 0101 (30 pps).

4. bit_rate - Less than or equal to 7865 in 400 bits/sec units, equivalent to 3 Mbits/sec.

5. vbv_buffer_size - Less than or equal to 20 in 16Kbits units, equivalent to 40Kbytes.

Picture Header

6. picture_coding_type - Not equal to 4, i.e. no sequences with D-pictures.

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Audio bitstream multiplexed in a system bitstream

The ZR36100 passes through its serial port, to the audio decoder device, any audio bitstream which obeys the following restrictions: The bitrate_index, layer and sampling_frequency parameters of all frames must have the same values as in the first frame. Free bit rate, that is, bitrate_index=0, is not allowed.

Audio-only bitstream

The ZR36100 passes through its serial port, to the audio decoder device, any audio bitstream which obeys the following restrictions: The bit rate must be constant, and less than or equal to 448 kbits/sec.

Private1 bitstream (multiplexed in a system bitstream)

The ZR36100 passes through its serial port any legal MPEG-1 private1 bitstream which conforms to the ISO 11172-1 standard and obeys the following restrictions.

7. Constant bit rate, which is less than or equal to the maximum bit rate allowed for audio bitstreams in ISO 11172-3.

SET-UP PARAMETERS

The set-up parameters of the ZR36100 consist of 128 bytes of data, divided up as follows:

- 7 single-byte parameters, six of which are further divided into single-bit or multi-bit sub-fields, configure the decoding system and interfaces
- 22 parameters (38 bytes) control the display (syncs and video output)
- 8 parameters (19 bytes) control timing and delays
- 2 parameters (4 bytes) control frame rate conversion
- 3 parameters (3 bytes) control video and audio stream selection
- 57 additional bytes, here designated as reserved. Some of these may be assigned to new functions implemented in the microcode and not described in this data sheet; the most current parameter assignments are specified in the ZR36100 microcode release notes. If unused, the reserved bytes must be loaded with the value zero.

The complete 128-byte array must always be loaded whenever a change to any parameter is required, for example when a sequence has ended and a new sequence with different MPEG parameters must be decoded.

Some of the parameter fields have default values, which are preset to a given value during a cold reset (cold reset is defined in the *Reset and Standby Power* section). The only parameters that have default values are those needed to specify signal directions for bidirectional lines to avoid contention, and to define the initial configuration of the host interface.

Some of the parameters and bit fields, designated "fixed parameter", or "fixed bit," may not be changed without a cold reset. These parameters pertain generally to the overall system configuration. All parameters with default values are also defined to be "fixed" in this sense.

The set-up parameters are listed in Table 1.

Table 1. Set-up parameters

Byte No. (Hex)	Symbol	Brief description
00	BUSMODE	Host bus mode
01	BUSOFF	Request off timing (in DMA mode)
02	SYSMODE	Decoding system mode
03	VIDMODE	Video output mode
04	SYNMODE	Video synchronization mode
05	SP1MODE	Serial port 1 mode
06	SP2MODE	Serial port 2 mode
07		Reserved
08	NAP (m.s.)	Number of active pixels per line
09	NAP (l.s.)	Number of active pixels per line
0A	NOP (m.s.)	Number of offset pixels per line
0B	NOP (l.s.)	Number of offset pixels per line
0C	NTP (m.s.)	Number of total pixels per line
0D	NTP (l.s.)	Number of total pixels per line
0E	NBP (m.s.)	Number of blank pixels per line
0F	NBP (l.s.)	Number of blank pixels per line
10	NBPF (m.s.)	Number of front blank pixels per line
11	NBPF (l.s.)	Number of front blank pixels per line
12	NDP (m.s.)	Number of delay pixels per line
13	NDP (l.s.)	Number of delay pixels per line
14	NAL (m.s.)	Number of active lines per picture
15	NAL (l.s.)	Number of active lines per picture
16	NOL (m.s.)	Number of offset lines per picture
17	NOL (l.s.)	Number of offset lines per picture
18	NTL (m.s.)	Number of total lines per frame
19	NTL (l.s.)	Number of total lines per frame
1A	NBL (m.s.)	Number of blank lines per field [frame]
1B	NBL (l.s.)	Number of blank lines per field [frame]
1C	NBLF (m.s.)	Number of front blank lines per field [frame]
1D	NBLF (l.s.)	Number of front blank lines per field [frame]
1E	NDL (m.s.)	Number of delay lines per field [frame]
1F	NDL (l.s.)	Number of delay lines per field [frame]
20	HSW	Width of horizontal sync signal (in pixels)

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Table 1. Set-up parameters (continued)

Byte No. (Hex)	Symbol	Brief description
21	VSW	Width of vertical sync signal (in lines)
22	BGRV	R or V component of the background color
23	BGGY	G or Y component of the background color
24	BGBU	B or U component of the background color
25	FIL	Value output on bits 23:16 of VIDOUT
26	CRV (m.s.)	V to R color space conversion coefficient
27	CRV (l.s.)	V to R color space conversion coefficient
28	CBU (m.s.)	U to B color space conversion coefficient
29	CBU (l.s.)	U to B color space conversion coefficient
2A	CGV (m.s.)	V to G color space conversion coefficient
2B	CGV (l.s.)	V to G color space conversion coefficient
2C	CGU (m.s.)	U to G color space conversion coefficient
2D	CGU (l.s.)	U to G color space conversion coefficient
2E	SP1BR (m.s.)	Serial port 1 bit rate ratio
2F	SP1BR	Serial port 1 bit rate ratio
30	SP1BR (l.s.)	Serial port 1 bit rate ratio
31	SP2BR (m.s.)	Serial port 2 bit rate ratio
32	SP2BR	Serial port 2 bit rate ratio
33	SP2BR (l.s)	Serial port 2 bit rate ratio
34	SP1CD (m.s.)	Divisor of VCLK for SP1CLK
35	SP1CD (l.s.)	Divisor of VCLK for SP1CLK
36	SP2CD (m.s.)	Divisor of VCLK for SP2CLK
37	SP2CD (l.s.)	Divisor of VCLK for SP2CLK
38	SP1DL (m.s.)	Serial port 1 delay
39	SP1DL (l.s.)	Serial port 1 delay
3A	SP2DL (m.s.)	Serial port 2 delay
3B	SP2DL (l.s.)	Serial port 2 delay
3C	VOD (m.s.)	Video output delay
3D	VOD (l.s.)	Video output delay
3E	VCLK (m.s.)	VCLK rate (Hz)
3F	VCLK	VCLK rate (Hz)
40	VCLK (l.s.)	VCLK rate (Hz)
41	Reserved	
42	Reserved	

Table 1. Set-up parameters (continued)

Byte No. (Hex)	Symbol	Brief description
43	R (m.s.)	Parameter used in frame rate conversion
44	R (l.s.)	Parameter used in frame rate conversion
45	M (m.s.)	Parameter used in frame rate conversion
46	M (l.s.)	Parameter used in frame rate conversion
47	SELMODE	Stream selection mode
48	VSID	Video stream_id
49	ASID	Audio stream_id
50 - 7F	Reserved	

Key: l.s. indicates the least significant byte, m.s. indicates the most significant byte of a multi-byte parameter.

Configuration Parameters

BUSMODE

This byte configures the host interface. It contains the following sub-fields.

■ BSWD (bit 7) - host bus width.

This bit defines the active width of the host bus, either 8 bits or 16 bits.

0 - The host bus width is 8 bits

1 - The host bus width is 16 bits

Default is 0, 8 bits bus width.

■ BSOR (bit 6) - Order of bytes on the host bus.

This bit defines the byte order of the data on the host bus, when the active width of the host bus is 16 bits. It defines which byte of the host data bus contains the earlier byte of the bitstream, the lower-numbered byte of the set-up parameters or microcode, or the MSB (most significant byte) of an on-line command. When the active width is 8 bits, the data are always on bits 7:0 and BSOR must be 0.

0 -"Motorola" style. Bits 15:8 of the host bus contain the earlier byte, lower-numbered byte or MSB.

1 - "Intel" style. Bits 7:0 of the host bus contain the earlier byte, lower-numbered byte or MSB.

Default is 0. When BSWD is 0 (8-bit bus width), BSOR is not applicable and must be 0.

■ BSTM (bit 5) - bitstream transfer mode.

BSTM specifies whether the MPEG-1 bitstream is transferred using programmed I/O or DMA. Microcode, set-up parameters, on-line commands and status reads always use programmed I/O.

0 - programmed I/O

1 - DMA

Default is 0, programmed I/O.

■ BSLN (bits 4:0) - burst length.

This is part of the mechanism that regulates the MPEG bitstream data transfer over the host bus interface. The same mechanism is used also during loading of the set-up parameters.

In programmed I/O transfer and set-up parameter loading, this bit field specifies the maximum number of write cycles that the host can perform after checking READY, before it must again check READY.

In DMA transfer mode, this field specifies the maximum number of DMA write cycles for which the DREQ signal will remain active before being de-activated.

For 8-bit host bus width, the allowed range for BSLN is 2 to 30, even numbers only. For 16-bit host bus width, the allowed range for BSLN is 1 to 15.

Default value is 16.

BUSOFF

This parameter is used to regulate the utilization of the host bus in DMA transfer mode. It is an unsigned integer which, when multiplied by 16, defines the minimum time, in PCLK periods, for which the ZR36100 will refrain from requesting the host bus, that is, not activate DREQ, after deactivating DREQ. Minimum value is 1 (16 PCLK periods). Must be zero in programmed I/O transfer mode.

SYSMODE

This byte configures the decoding system. It contains the following sub-fields.

- CODE (bit 7) - Bitstream type.
  This bit is not currently used. However, for compatibility with existing implementations of host software, it is recommended to set it as follows:
  1 - For a video-only bitstream.
  0 - For any other bitstream (system or audio-only)
- VIDS (bit 6) - Frame rate conversion control.
  Used in conjunction with the R and M parameters, as described below under Frame Rate Conversion Parameters.
  This parameter must be fixed.
- VIDB (bit 5) - Video interface mode.
  This bit configures the video interface for the special Enabled mode, described in the *Video Interface* section.
  0 - Normal video interface mode.
  1 - Enabled video interface mode.
  This parameter must be fixed.
- VSTL (bit 4) - High-resolution still images decoding mode.
  This bit configures the ZR36100 for decoding the special high-resolution still images.
  0 - Bitstream is normal moving-picture MPEG or audio-only.
  1 - Bitstream contains special high-resolution still images.
- Reserved (bits 3-1) - Must be 0.
- LPIC (bit 0) - Display after sequence end.
  This bit defines what is displayed on the video output bus after the ZR36100 decodes a sequence_end_code in the bitstream, and the last picture of the sequence has been displayed.
  0 - The background color is displayed after the last picture.
  1 - The last decoded picture is displayed indefinitely.
  When VIDB is 1 (for Enabled video interface mode), LPIC is not relevant and must be 0.

VIDMODE

This byte configures the video post-processor and output interface. See Tables 10 and 11 in the *Video Interface* section for the allowed combinations of VIDMODE's sub-fields.

- VSIZ (bit 7) - Video output size and scan mode selection.
  This bit defines the video output (display) scan mode and size option: either interlaced CCIR-size, or progressive SIF-size.
  0 - Video output is interlaced CCIR-size.
  1 - Video output is progressive SIF-size.
  This parameter must be fixed.
  If the Enabled video interface mode is used, VSIZ must be 1. If the special still-images mode is used, VSIZ must be 0.
- VINT (bit 6) -Video horizontal interpolation.
  This bit defines whether the reconstruction of the U and V samples from the native MPEG SIF picture format, and/or the horizontal size doubling, are done by replication or by linear interpolation.
  0 - Interpolation.
  1 - Replication.
- VCLR (bit 5) - Video output color space selection.
  This bit defines the color space of the video output: either YUV or RGB.
  0 - Video output color space is YUV
  1 - Video output color space is RGB
  If the Enabled video interface mode is used, VCLR must be 0.

■ VIWD (bits 4,3) - Video output color depth.

For RGB color space, these bits define the color depth (in bits) of the video output.

00 - RGB width is 24 bits

01 - RGB width is 16 bits (5,6,5)

10 - RGB width is 15 bits (5,5,5)

11 - Reserved

When the output color space is YUV, VIWD must be 00.

■ VSMP (bit 2) - Video output component sub-sampling structure.

This bit specifies 4:1:1 or 4:2:2 video output sub-sampling for interlaced CCIR-size video output, when YUV color space is selected.

0 -YUV format is 4:2:2

1 -YUV format is 4:1:1

This parameter must be fixed.

If the video output mode is not interlaced CCIR-size, or if the output color space is RGB, VSMP must be 0.

■ VBUV (bit 1) - Video output with biased U and V.

This bit defines whether the U and V video outputs for YUV color space are un-biased (i.e. in the range 0 to 255) or biased (i.e. in the range -128 to 127). The values for the biased case are the values of the unbiased case with 128 subtracted.

0 - U and V are un-biased

1 - U and V are biased

If the output color space is RGB, VBUV must be 0.

■ VBLN (bit 0) - Composite blanking output signal.

This bit defines whether the FI_EN signal, when output, is field index indicator or a composite blanking signal.

0 - FI_EN is field index

1 - FI_EN is composite blanking

This parameter must be fixed.

If the sync signals are defined to be inputs, or if the Enabled video interface mode is used, VBLN must be 0.

SYNMODE

This byte configures the video synchronization signals. It contains the following sub-fields. Note: Bits 2 to 6 must be set properly even when the SYNC signals are input.

■ SDIR (bit 7) - Video sync signals direction.

This bit determines whether the video sync signals (VSYNC, HSYNC, FI_EN) are input or output (i.e. generated by the ZR36100).

0 - Sync signals are input

1 - Sync signals are output

When the Enabled video interface mode is used (VIDB = 1), SDIR must be 1. In this mode, VSYNC and HSYNC are outputs, and FI_EN is an input even though SDIR = 1.

Default is 0 (the sync signals are input).

■ HSHL (bit 6) - HSYNC signal level.

This bit defines whether the HSYNC signal is active high or active low.

0 - HSYNC is active low

1 - HSYNC is active high

This parameter must be fixed.

■ VSHL (bit 5) - VSYNC signal level.

This bit defines whether the VSYNC signal is active high or active low.

0 - VSYNC is active low

1 - VSYNC is active high

This parameter must be fixed.

■ FIHL (bit 4) - FI_EN signal level.

This bit defines whether the FI_EN, when used as a field index signal, is high or low during field I. During field II the level is the complement of the level during field I.

0 - FI_EN is low during field I.

1 - FI_EN is high during field I.

This parameter must be fixed. If VIDB=1 or VBLN=1, FIHL must be 0.

■ HSLN (bit 3) - HSYNC signal length selection.

This bit defines the length of the HSYNC signal: Either short (Sync) or long (Blanking). The length of HSYNC is HSW pixels when short, or NBP+NBPF pixels when long (HSW, NBP and NBPF are defined below).

0 - HSYNC is short (Sync pulse)

1 - HSYNC is long (Blanking pulse)

This parameter must be fixed.

If the Enabled video interface mode is used, HSLN must be 1.

■ VSLN (bit 2) - VSYNC signal length.

This bit defines the length of the VSYNC signal: Either short (Sync) or long (Blanking). The length of VSYNC is VSW*NTP pixels when short, or (NBL+NBLF)*NTP+NBP+NBPF pixels when long (VSW, NTP, NBL, NBLF, NBP and NBPF are defined below).

0 - VSYNC is short (Sync pulse)

1 - VSYNC is long (Blanking pulse)

This parameter must be fixed.

If the Enabled video interface mode is used, VSLN must be 1.

■ VFAC (bit 1) - First field active video output.

This bit defines whether (for interlaced CCIR-size output) the first field of an active video frame is field I or field II. Note: If the NBL set-up parameter (see below) specifies an integer number of lines (as required for NTSC), field I is the top field and field II is the bottom field. If the NBL set-up parameter specifies a non-integer number of lines (as required for PAL), field I is the bottom field and field II is the top field.

0 - Field I is the first field

1 - Field II is the first field

This parameter must be fixed.

If the video output mode is not interlaced CCIR-size, VFAC must be 0.

■ VCRS (bit 0) - Video clock frequency range.

This bit defines whether, for progressive SIF-size output, VCLK or QCLK_V (1/4 the frequency of VCLK) is used as the pixel clock. See Table 5 in the *Video Interface* section.

0 -VCLK is the pixel clock.

1 - QCLK_V is the pixel clock.

This parameter must be fixed.

If the video output mode is interlaced CCIR-size, VCRS must be 0. If the Enabled video interface mode is used, VCRS must be 1.

SP1MODE, SP2MODE

The SP1MODE parameter configures serial port 1. SP2MODE (with sub-fields S2FT, S2CD, S2BS and S2AC) has exactly the same function for serial port 2. Only SP1MODE is described below. For restrictions on selection of these parameters, see the *Serial Ports Interface* section.

■ Reserved (bits 7,6) - Must be 0.

■ S1FT (bit 5) - SP1FRM signal type.

This bit defines whether the SP1FRM signal type is pulse or transition. The signal types are specified in the *Serial Ports Interface* section.

0 - SP1FRM signal is pulse type

1 - SP1FRM signal is transition type

This parameter must be fixed.

If the serial port is not active, (S1AC=0), S1FT must be 0.

■ S1CD (bit 4) - SP1CLK signal direction.

This bit defines whether the SP1CLK clock signal is an input or an output.

0 - SP1CLK clock signal is an input

1 - SP1CLK clock signal is an output

Default is 0, input clock.

If the serial port is not active, (S1AC=0), S1CD must be 0.

■ S1BS (bit 3-1) - Serial port 1 stream selection.

This field selects the source of the data assigned to serial port 1.

000 - Serial port 1 is assigned the first audio stream encountered

001 - Serial port 1 is assigned the second audio stream encountered

010 - Serial port 1 is assigned the private-1 bitstream

011 - Reserved

100 - Serial port 1 is assigned the private-2 bitstream

101 - Reserved

110 - Reserved

111 - None

The SELMODE and ASID parameters permit selection of a specific audio stream, from an MPEG system stream containing two or more audio streams. These parameters override S1BS. This feature is described below under Stream Selection Parameters.

Note that the same stream can not be output on both serial ports. That is, S1BS and S2BS may not have the same value except 111.

If the serial port is not active, (S1AC=0), S1BS must be 111.

■ S1AC (bit 0) - Serial port 1 active selection.

This bit specifies whether serial port 1 is active or not.

0 - Inactive

1 - Active

When a video-only bitstream is decoded, both serial ports must be inactive (S1AC = S2AC = 0). Whenever a serial port is unused, it must be configured to be inactive.

Display Control Parameters

The first four display parameters define the "active region" of the decoded picture, the portion of the picture that is actually displayed. Refer to Figure 4 and Table 18 in the *Video Interface* section.

NAP

Defines the width in pixels of the active region of the decoded picture.

NAL

Defines the height in lines of the active region of the decoded picture.

NOP

Defines the offset in pixels of the active region from the left side of the decoded picture.

NOL

Defines the offset in lines of the active region from the top of the decoded picture.

The following eight parameters specify the positioning of the active and background video in the display, relative to the raster defined by the sync signals. These parameters have different interpretations for the two display sizes and formats: interlaced CCIR-size or progressive SIF-size, as illustrated in Figures 12 and 13. For the restrictions on the values of these parameters, see Tables 19, 20 and 21 in the *Video Interface* section.

Note: Unless otherwise indicated, the values of these parameters must be set properly even when the sync signals are input.

NTP

Defines the number of pixels per displayed line, (i.e. the number of VCLK or QCLK_V periods, depending on the video output format; see the discussion of the pixel clock in the *Video Interface* section) between the leading edges of two consecutive HSYNC pulses. These 2 bytes are treated as a 16-bit unsigned integer.

This parameter must be fixed.

NTL

Defines the number of lines per frame, i.e. the number of HSYNC activations between the leading edges of consecutive VSYNC pulses (for progressive SIF-size output) or alternate VSYNC pulses (for interlaced CCIR-size output). These 2 bytes are treated as a 16-bit unsigned integer.

This parameter must be fixed.

NBP

Specifies the blanking region (number of blank pixels) at the beginning of each line.These 2 bytes are treated as a 16-bit unsigned integer. Not applicable for long input HSYNC, and must be set to 0 in this case. For long input HSYNC, the blanking region at the beginning of each line ends with the deactivation of HSYNC. Also, for long output HSYNC, NBP+NBPF specifies the width of the HSYNC pulse.

This parameter must be fixed.

NBL

Specifies the blanking region (number of blank lines) at the beginning of each field or frame. These 2 bytes are treated as a 16-bit unsigned fraction, with 15 integer bits and 1 bit after the binary point (that is, NBL specifies the number of blank lines with a resolution of one-half line). Not applicable for long input VSYNC, and must be set to 0 in this case. For long input VSYNC, the blanking region at the beginning of each field or frame ends with the deactivation of VSYNC. Also, for long output VSYNC, NBL+NBLF lines plus NBP+NBPF pixels specifies the width of the VSYNC pulse.

This parameter must be fixed.

NBPF

Specifies the blanking region (number of blank pixels) at the end of each line. These 2 bytes are treated as a 16-bit unsigned integer. Not applicable and must be 0 for long input HSYNC. Also, for long output HSYNC, NBP+NBPF specifies the width of the HSYNC pulse.

This parameter must be fixed.

NBLF

Specifies the blanking region (number of blank lines) at the end of each field or frame. These 2 bytes are treated as a 16-bit unsigned fraction, with 15 integer bits and 1 bit after the binary point (that is, NBLF specifies the number of blank lines with a resolution of one-half line). Not applicable and must be 0 for long input VSYNC. Also, for long output VSYNC, NBL+NBLF lines plus NBP+NBPF pixels specifies the width of the VSYNC pulse.

This parameter must be fixed.

NDP

Defines the number of background pixels on each line prior to (that is, to the left of) the active region. The 2 bytes of NDP are treated as a 16-bit unsigned integer.

NDL

Defines the number of background lines prior to (that is, above) the active region per field or frame. These 2 bytes are treated as a 16-bit unsigned integer.

The next two parameters specify the width of the video sync signals when they are output and short. Restrictions on the values of these parameters can be found in Table 20 in the *Video Interface* section. See also Figures 5 and 8.

HSW

Specifies the width of the horizontal sync signal (HSYNC), in pixels, when it is a short output. This byte is treated as an unsigned integer.

This parameter must be fixed.

VSW

Specifies the width of the vertical sync signal (VSYNC), in lines, when it is a short output. This byte is treated as an 8-bit unsigned fraction with 7 integer bits and 1 bit after the binary point.

This parameter must be fixed.

The next four parameters define background color, and the value of the upper byte of the video bus for 16-bit, 15-bit and 12-bit video output (see Tables 12, 13, 15 and 16). The background color values are not modified by the color space conversion (parameter VCLR), or the biasing of U and V (VBUV), so they must be specified in the output color space, and with the desired bias if applicable. They are, however, post processed according to the settings of VSMP and VIWD when applicable.

BGRV

The value of the R component of the background color if VCLR = 1, or the value of the V component of the background color, if

VCLR =0.

BGGY

The value of the G component of the background color if VCLR = 1, or the value of the Y component of the background color, if VCLR =0.

BGBU

The value of the B component of the background color if VCLR = 1, or the value of the U component of the background color, if VCLR =0.

FIL

The value output on bits [23:16] of the VIDOUT bus when one of the YUV or 16-bit RGB formats is used.

The following four parameters define the color space conversion coefficients. The conversion formulas are specified in the *Video Interface* section.

CRV

Defines the value of the V to R color space conversion coefficient. These two bytes are treated as a 16-bit two's complement fraction with 6 integer bits and 10 fractional bits.

Minimum value is 0. Maximum value is (2-1/1024). Note: CCIR 601 value is 1.402.

CBU

Defines the value of the U to B color conversion coefficient. These two bytes are treated as a 16-bit two's complement fraction with 6 integer bits and 10 fractional bits.

Minimum value is 0. Maximum value is (2-1/1024). Note: CCIR 601 value is 1.772.

CGV

Defines the value of the V to G color conversion coefficient. These two bytes are treated as a 16-bit two's complement fraction with 6 integer bits and 10 fractional bits.

Minimum value is -1. Maximum value is 0. Note: CCIR 601 value is -0.714.

CGU

Defines the value of the U to G color conversion coefficient. These two bytes are treated as a 16-bit two's complement fraction with 6 integer bits and 10 fractional bits.

Minimum value is -1. Maximum value is 0. CCIR 601 value is -0.344.

Note: If the output color space is YUV (VCLR=0), the values of the conversion coefficients must be zero.

Timing Parameters

The following parameters define the timing of the serial ports, presentation delays of the video and serial port data, and the frequency of VCLK.

SP1CD, SP2CD

The integer divisors of VLCK, used to specify the frequency of SP1CLK and SP2CLK respectively, when they are outputs.

The resulting serial port clock rates should be equal to or above the bit rates of the streams specified for the serial ports.

These are 2-byte parameters, treated as 16-bit unsigned integers. Minimum value is 4. Maximum value is 1023 (the most significant 6 bits must always be zero). If a serial port is inactive (S1AC=0 or S2AC=0), or the serial clock is an input (S1CD=0 or S2CD=0), the corresponding divisor value must be 0.

SP1BR, SP2BR

These parameters specify the ratios of bit rate to clock rate for serial ports 1 and 2 respectively. The ZR36100 maintains average bit rates as defined by these two parameters if the clock rates, generated by using SP1CD or SP2CD (or the external clocks), are equal to or higher than the bit rates specified for the serial ports.

These are 3-byte parameters treated as 24-bit unsigned fractions with 5 integer bits and 19 fractional bits. Minimum value is 1/64.

Maximum value is 1.0 (i.e., the most significant 4 bits must be zero). If a serial port is inactive, the corresponding value of SP1BR or SP2BR must be zero.

These parameters must be chosen so that the actual serial port bit rate is equal (to within the available precision) to the desired bit rate, which is usually equal to the bit rate of the audio stream assigned to the serial port. For example, if ABR is the bit rate of the audio stream assigned to serial port 2, F_{VCLK} is the frequency of VCLK, and the serial port clock is configured to be an output so that its frequency is F_{VCLK} / SP2CD,

$$SP2BR = (ABR * SP2CD) / F_{VCLK}$$

SP1DL, SP2DL

These parameters specify the delays in the audio decoders (or other processors) connected to serial port 1 and serial port 2. The delay is defined as the time between the reception of the first bit of the code of a presentation unit and the output of the first sample of this presentation unit to the user. The ZR36100 compensates for this delay when timing the output of the serial port, to maintain synchronization with the video relative to the perception of the user.

These two-byte parameters (treated as 16-bit unsigned integers) measure the delay in units of 90KHz clock. The value of the parameter must be zero when its serial port is inactive.

These parameters must be fixed.

VOD

This parameter specifies the delay in a possible display processor connected to the video output, between reception of the first sample of a presentation unit into that device and the output of the first sample of this presentation unit to the user. The ZR36100 compensates for this delay when timing the output of the serial ports, to maintain synchronization with the video relative to the perception of the user. The value of the parameter must be zero when neither serial port is active.

This 2-byte parameter (treated as a 16-bit unsigned integer) measures the delay in units of 90 KHz clock.

This parameter must be fixed.

VCLK

This parameter must be set to the nominal frequency of the video input clock (VCLK). VCLK is 3-byte parameter treated as a 24-bit unsigned integer, representing the frequency of the VCLK input signal in units of Hertz.

The VCLK parameter is used in the transformation of the time stamps and delay information from a 90KHz clock to a clock derived from VCLK.

This parameter must be fixed.

Frame Rate Conversion Parameters

Frame rate conversion is supported only when the video interface configuration is interlaced CCIR-size (when the VSIZ bit of VIDMODE is 0; see also the *Video Interface* section). Thanks to the frame rate conversion feature, the ZR36100 can produce NTSC-compatible (29.97 frames/sec) or PAL-compatible (25 frames/sec) video display, when the bitstream picture rate is any of the following: 23.976, 24, 25, 29.97, 30.

The parameters R and M, together with the VIDS bit of SYSMODE, are used to control the frame rate conversion, and should be set to the values shown in Table 2 (the values are given in decimal representation).

Table 2. Frame Rate Conversion Parameters

Display Frame Rate	Parameter	Bitstream Picture Rate				
		23.976	24	25	29.97	30
29.97 (NTSC)	R	0	1001	24	0	1001
	M	0	1001	1001	0	1001
	VIDS	0	0	0	1	1
25 (PAL)	R	6	6	0	6	6
	M	1200	6	0	1200	6
	VIDS	0	0	1	1	1

*Note*s:

1. When performing PAL to NTSC conversion, that is, when the bitstream picture height is greater than 240 lines and the display frame rate is 29.97, the frequency of GCLK must be 13.5 MHz and the $\overline{MB4}$ pin must be at a logic high.

2. When frame rate conversion is used, the video interface must be configured for interlaced CCIR-size mode (VSIZ = 0 in the VIDMODE parameter).

3. Only the timing of decoding and display of pictures is affected by the frame rate conversion. The pixel aspect ratio is not changed, that is, the aspect ratio at the video output is the same as that of the pictures in the bitstream. Thus, when pictures with vertical size of 240 are displayed with PAL (625 line) output, the picture does not fill the display vertically. If vertical scaling is required, it must be done by the display device. Similarly, when pictures with vertical size of 288 are displayed with NTSC (525 line) output, the active region of the displayed picture must be cropped vertically.

Stream Selection Parameters

When playing back an MPEG system bitstream that contains multiple video and/or multiple audio streams, the video stream to be decoded and/or the audio stream to be output on a serial port can be selected by specifying their stream_id numbers, by means of the following set-up parameters.

SELMODE

When bit 0 of SELMODE is 1, the video stream specified by VSID (see below) is selected for decoding. When bit 0 of SELMODE is 0, the first video stream encountered is decoded.

When bit 1 of SELMODE is 1, the audio stream specified by ASID (see below) is selected for output from the active serial port. When bit 1 of SELMODE is 0, the audio stream is selected as specified by the SP1BS or SP2BS fields of the SP1MODE or SP2MODE parameters, respectively.

VSID

The video stream_id. The valid range of values for VSID is 0xE0 to 0xEF.

ASID

The audio stream_id. The valid range of values for ASID is 0xC0 to 0xDF.

Audio stream selection by means of ASID is supported only when there is only one active serial port

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ON-LINE COMMANDS

Once it has been initialized, by the procedure described in the *Initialization* section, subsequent behavior of the ZR36100 is controlled by the host by means of on-line commands. On-line commands are written into the ZR36100 via an I/O port reserved for this purpose, as described in the *Host Interface* section.

An on-line command always consists of two bytes, of which the most significant is always zero. Note that when the host interface operates in 16-bit mode (BSWD=1), the byte order of the command must match the setting of the BSOR set-up parameter. Also note that when the host interface operates in 8-bit mode (BSWD=0), the command must be written with no intervening bitstream data transfers between the two bytes of the command. This restriction must be observed in both modes of bitstream transfer, DMA and programmed I/O.

Table 3 lists the supported on-line commands, with the least significant byte of the code for each command. All least significant byte values not listed in the table are reserved, and may be assigned functions in future releases of microcode. The most current assignments are documented in the ZR36100 microcode release notes.

Table 3. On-line commands

Command Name	Least Significant Byte Value
Go	0000 0000
Freeze	0001 0000
Decode to First I-Picture	0010 0000
Single Step	0011 0000
Decode to Next I-Picture	0100 0000
Slow Motion	0101 0sss
End Decoding	1000 000d
Continue	1001 0000

The ZR36100 maintains an internal 4-slot queue for on-line commands from the host. If the host writes to the on-line command port while the queue is full, the access is ignored and the command is lost. The status register (described in the *Host Interface* section) contains a bit (bit 7) that indicates to the host whether the queue is full or not.The host may enter commands at intervals of not less than 150 GCLK periods, if there is space in the queue.

The commands are executed from the queue, in the sequence they were received. Once per frame, the queue is checked and if it contains a command, the command is retrieved and executed.

The following is a concise description of the behavior in response to each of the on-line commands. More detailed information can be found in the *Playback Operation* section.

Go

Commands the ZR36100 to start consuming and decoding the bitstream. The Go command is allowed only when the decoder is idle (as indicated by the IDLE signal or status register bit), and is the only command allowed when the decoder is idle.

The Go command is a special case with respect to the on-line command queue, since it is executed immediately when received, and effectively does not occupy a slot in the queue.

Freeze

When the ZR36100 executes the Freeze on-line command, it pauses video decoding and serial port output, and displays the current picture indefinitely (that is, until another command is executed).

Decode to First I-Picture

When it executes this command, the ZR36100 continues until the next I-picture. That is, it continues normal decoding and display until it begins to display an I-picture.Then, when it has completed decoding of the picture that was being decoded when display of the I-picture started, it pauses as for the Freeze command, and displays the I-picture indefinitely.

Single Step

When it executes this command, the ZR36100 steps to the next picture. That is, it resumes decoding, decodes and displays one picture, then pauses, and displays the new picture indefinitely.

Decode to Next I-Picture

When it executes this command, the ZR36100 steps to the next I-picture. That is, it resumes decoding, but without changing the picture being displayed, until display of the next I-Picture is scheduled to begin. Then, when it has completed decoding of the picture that was being decoded at this time, it pauses, and displays the new I-picture indefinitely.

Slow Motion

When the ZR36100 executes this command, it decodes the pictures from the bitstream at a rate that is slowed down from the nominal by an integer factor, given by the "sss" field of the command word. This is implemented by stepping to the next picture, pausing for sss-1 frames, stepping again and pausing for sss-1 frames, and so on indefinitely.

Continue

When the ZR36100 executes this command, it resumes normal decoding.

End Decoding

When the ZR36100 executes this command, it terminates decoding, and when the last picture has been displayed, activates the IDLE signal and status bit, and goes into the idle state. The content of the display after this is specified by the "d" bit of the command word:

d=0, display the last picture

d=1, display the background color,

Note that this specification overrides the LPIC bit of the SYSMODE set-up parameter, if the video sequence happened to end at the same time.

Synchronization of video and serial port outputs

When the Go on-line command is executed, the ZR36100 goes through a phase of decoding start-up, and, if a system bitstream is being decoded and a serial port is active, synchronization of the serial output stream with the video display. The mechanism of start-up and synchronization is described in the *Playback Operation* section. Here, it is sufficient to note that once synchronization is established, it is maintained automatically.

Whenever decoding is suspended during execution of an on-line command, serial port output is also suspended. And when normal decoding resumes, whether indefinitely as after a Continue command, or transiently as in the Single Step, Slow Motion and Decode to Next I-Picture commands, serial port output also resumes. Synchronization is maintained during execution of all on-line commands.

On-Line Command Order

There are restrictions on the allowed order of on-line commands. Table 4 shows which commands are allowed to succeed each command; X indicates a legal succession. The table can also be used to determine which commands are allowed to precede any given command.

Table 4. On-Line Command Order

	Succeeding Command							
	Go*	End Decoding	Freeze	Continue	Single Step	Slow Motion	Decode to First I-Picture	Decode to Next I-Picture
Preceding Command								
Go			X				X	
End Decoding	X							
Freeze		X		X	X	X		
Continue			X				X	
Single Step		X		X	X	X		
Slow Motion		X		X	X	X		
Decode to First I-Picture		X		X	X	X		X
Decode to Next I-Picture		X		X	X	X		X

* A Go command is allowed only when the ZR36100 is idle, as indicated by the IDLE signal and status register bit.

Random Access

After a Go command, the ZR36100 is capable of starting up and synchronizing when the bitstream is fed to it starting either at the beginning of the stream, as defined in the ISO-11172 standard, or at any randomly chosen byte-aligned entry point. Also, when the ZR36100 goes idle after an End Decoding command, all remaining data in the video and serial port stream buffers is flushed. This can be used to implement a random access or seek function in the host software driver, by terminating decoding with an End Decoding command, and then when the device is idle, restarting it with a Go command, feeding the bitstream from the desired entry point.

Serial Port 1 Commands

The ZR36100 supports a special method of transferring commands to an external decoder connected to serial port 1. An audio or private data decoder that has a second input serial port can use this port, if it is programmed to respond appropriately to the serial port 1 commands from the ZR36100.

As described in the *Serial Ports Interface* section, serial port 1 has a second data line (SP1CMD) to transfer serial port on-line commands from the ZR36100 to the external decoder. The SP1CMD line uses the same clock and frame sync as the SP1DAT line.

The commands are "change state" commands, in that they are issued only once. Subsequent words on the SP1CMD line until the next new command are all zeroes. Commands may be issued on the SP1CMD line even if there is no simultaneous valid serial port data. Invalid SP1DAT is indicated by bit 3 of the command word being 1. When the serial port has valid data, a valid data word is transferred with the command and indicated by bit 3 of the command being 0. Bits 2:0 of the command word contain the command code. Bits 15:4 are always 0.

Table 5 lists the serial port commands, the corresponding command codes and the intended effect on an audio decoder connected to serial port 1. Codes not listed in the table are reserved.

Table 5. Serial Port 1 on-line commands

Command	Code	Intended Effect
Null	000	No change from last command
Start	001	A new audio sequence is about to begin
Finish	010	The current audio sequence is finished
Freeze	011	Suspend decoding and mute the output
Resume	110	Restart decoding after Freeze, and output without muting
Resume-and-Mute	111	Restart decoding after Freeze, and mute the output

Note: If an audio decoder does not respond to the serial port 1 commands, it is recommended to connect it to serial port 2. This will prevent the audio decoder from attempting to decode to serial port 1 frames that have a command, but no valid data (see the *Serial Port Interface* section).

Table 6 shows the serial port 1 commands that are issued as a consequence of the execution of each of the host on-line commands.

Table 6. Serial Port 1 Commands Corresponding to Host On-Line Commands

Host On-Line Command	Serial Port 1 Command(s)
Go	Start
End Decoding	Finish (when idle)
Freeze Frame	Freeze
Continue	Resume
Single Step	Resume-and-Mute, Freeze
Slow Motion	Freeze, Resume-and-Mute
Decode to First I-Picture	Freeze
Decode to Next I-Picture	Resume-and-Mute, Freeze

HOST INTERFACE

The host interface is used for the following functions:

- Microcode load
- Set-up parameters load
- On-line commands
- MPEG bitstream transfer
- Status readout

Two mechanisms are available for the bitstream transfer, programmed I/O and DMA. Microcode load, set-up parameters load and on-line commands use programmed I/O writes. Status is read from the ZR36100 back to the host using programmed I/O read. The I/O and DMA cycles are compatible with the ISA bus, but can operate at a much faster rate.

Host Interface Signals

The host interface comprises a 16-bit data bus (BUSDAT), a two-bit address bus (BUSADD), and 6 control signals: $\overline{BUSRD}$, $\overline{BUSWR}$, $\overline{BUSCS}$, DREQ and $\overline{DACK}$. The host interface operates asynchronously with the clocks of the ZR36100.

Host Interface Configuration

Table 7 shows the six legal combinations of the three sub-fields of the BUSMODE parameter used to configure the host bus interface. The default configuration after a cold reset is 8 bit, programmed I/O transfer. Note that all host interface write transactions (microcode load, set-up parameters load and on-line commands, as well as bitstream transfer), are affected by BSWD and BSOR.

In the 16 bit modes, the order of the bytes can be either "Motorola" or "Intel" style, which in effect determines which byte of the host data bus carries the earlier byte in the bitstream, the lower-numbered byte of the microcode or set-up parameters, or the most significant byte of an on-line command. For Motorola style, bits 15:8 of the host bus contain this byte. For Intel style, bits 7:0 of the host bus contain this byte. In the 8 bit modes, only bits (7:0) of the host bus are used; note that in this mode, the most significant byte of an on-line command precedes the least significant byte. Status is always read on bits (7:0).

Table 7. Host Interface

BSWD	BSOR	BSTM	Host Interface Configuration
0	0	0	8 bit, programmed I/O bitstream transfer [1]
0	0	1	8 bit, DMA bitstream transfer
1	0	0	16 bit, Motorola style, programmed I/O bitstream transfer
1	0	1	16 bit, Motorola style, DMA bitstream transfer
1	1	0	16 bit, Intel style, programmed I/O bitstream transfer
1	1	1	16 bit, Intel style, DMA bitstream transfer

1. Default mode after cold reset

I/O Write

The host performs programmed I/O writes by activating the $\overline{BUSCS}$ signal, and specifying the destination of the data with BUSADD (1:0). The falling edge of the $\overline{BUSWR}$ signal latches $\overline{BUSCS}$ and BUSADD. Data is then strobed into the ZR36100 using the rising edge of the $\overline{BUSWR}$ signal. See the "I/O Write Timing" diagram in the *AC Characteristics* section.

The two BUSADD bits define four write ports, which have different purposes during the initialization phase (when the ZR36100 is idle, that is, after a cold reset, or after decoding of a sequence has ended and IDLE is active) and the playback phase (between the Go on-line command and activation of IDLE). This is shown in Table 8.

Loading of microcode and set-up parameters is described in the *Initialization* section of this document.

When transferring the MPEG bitstream using programmed I/O (in I/O-only mode), the ZR36100 and the host employ a handshaking mechanism which regulates the rate that data is loaded in to the ZR36100. This handshaking mechanism uses the READY status bit (or the equivalent READY signal), and the 5-bit BSLN field of the BUSMODE set-up parameter. When the READY status bit (or the READY signal) is active (high), this indicates that the ZR36100 is ready to accept a burst of data. BSLN defines the maximum burst length, that is, the number of write cycles the host can perform after detecting READY active, before checking READY again.

Note: $\overline{DACK}$ must not be active when $\overline{BUSCS}$ is active.

Note: After finishing the transfer of a system bitstream in 8-bit modes, the host must transfer one more byte of any value, unless it can be assured that the length of the bitstream was an even number of bytes.

Table 8. Write ports defined by BUSADD

Phase of Operation	BUSADD(1:0)	Destination of Port Data
Initialization Phase	00	set-up parameters
	01	Go on-line command
	10	first part of microcode
	11	second and third parts of microcode
Playback Phase	00	MPEG bitstream in I/O-only mode, not used in mixed mode
	01	on-line commands
	10	not used
	11	not used

DMA Transfers

In DMA mode, the ZR36100 requests the bitstream by activating DREQ continuously for at most BSLN DMA write cycles. The host responds to DREQ by activating $\overline{DACK}$ and writing the data using the rising edge of $\overline{BUSWR}$. A single DMA cycle is illustrated in the "DMA Timing" diagram in the *AC Characteristics* section of this document. $\overline{DACK}$ is sampled by the ZR36100 only on the falling edge of $\overline{BUSWR}$, and a write cycle is completed on the rising edge of $\overline{BUSWR}$ without regard to $\overline{DACK}$, so $\overline{DACK}$ may remain active or pulse between bus cycles as desired. The BUSOFF parameter ensures that the ZR36100 does not monopolize the host bus in DMA transfer mode, by forcing it to refrain from re-activating DREQ for at least the specified amount of time after each de-activation of DREQ.

Note: DREQ may remain active after the last byte of a normally ending bitstream (the last byte of an iso_11172_ end_code or a sequence_end_code) has been transferred. This can happen if the last burst of data was shorter than BSLN. The work around for this is for the DMA controller to continue to supply data, of any value, until the ZR36100 deactivates DREQ. If playback is stopped by an End Decoding command, in rare cases DREQ can remain active even though the playback has ended and the ZR36100 has activated IDLE. If this happens, DREQ can only be forced inactive by a cold reset. If a cold reset is undesirable, a work around is for the DMA controller to ignore DREQ if IDLE is active. After the next GO command, it can respond to DREQ as if it had been activated normally.

Status Read (I/O Read)

To read the STATUS register, the host selects the ZR36100 by activating $\overline{BUSCS}$ and then reads the status using $\overline{BUSRD}$. The leading edge of $\overline{BUSRD}$ latches $\overline{BUSCS}$. The trailing edge can be used to latch the data. Reading the status register does not require the specification of an address.

The STATUS register (Table 9) is a five-bit register connected to BUSDAT(3:0) and BUSDAT(7). STATUS(7) indicates that there is at least one empty space in the internal on-line commands queue (described in the on-line commands section). STATUS(3) mirrors the READY signal and STATUS(2) mirrors the IDLE signal. Two bits, STATUS(1) and STATUS(0), are reserved for testing. Following

a cold reset, these bits are at logic high; if one of these bits ever goes low, it can only be restored to high by means of a cold reset. When reading status, BUSDAT(15:8) and BUSDAT(6:4) are not driven, and remain floating with weak pulldown resistors.

Table 9. Status Register

Bus Bit	Symbol	Description
7	OLC_RDY	Active low. When active, indicates that ZR36100 is ready to accept an on-line command.
3	READY	Mirrors the READY signal
2	IDLE	Mirrors the IDLE signal
1	TEST1	"1" after a cold reset. "1" if loading of program to address "11" passed. "0" if loading of program to address "11" failed.
0	TEST2	"1" after a cold reset. "1" if loading of program to address "10" passed. "0" if loading of program to address "10" failed.

VIDEO INTERFACE

The video interface consists of a 24 bit output data bus (VIDOUT), three bidirectional video synchronization signals (HSYNC, VSYNC and FI_EN) and two clock signals: one input (VCLK), and one output (QCLK_V).

Video Interface Configurations

In both the interlaced CCIR-size and progressive SIF-size configurations, the video interface operates as a conventional digital video source, with HSYNC and VSYNC defining the raster, the VIDOUT bus being driven continuously by the ZR36100, and the data being provided at a constant pixel clock rate along each line.

The video interface can also be configured to operate in a special Enabled video output mode, in which the ZR36100 drives the bus and provides the data in bursts, whose timing is controlled from the outside. This allows the VIDOUT bus to be shared. The Enabled mode is described in detail later in this section.

The parameter settings for each of the configurations are summarized in Table 10. The color space, bus width, and sub-sampling can be any of those shown in Table 11.

The interlaced CCIR-size configuration of the video interface must also be used when decoding a high-resolution still image sequence (see the *High-Resolution Still Images* section).

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Table 10. Legal set-up parameters for video interface configurations

Configuration	VSIZ[6]	VIDB[4]	VINT[6]	VCLR[6]	VIWD[6]	VSMP[6]	VBUV[6]	VCRS[7]	SDIR[7]	HSLN[7]	VSLN[7]	VBLN[6]	VFAC[7]
Interlaced CCIR-size	0	0	0/1	Any of formats 1, 2, 3, 4, 5 in Table 11				0	0	Input syncs[1]		0[3]	0/1
									1	Output syncs[2]		0/1	
Progressive SIF-size	1	0	0/1	Any of formats 1, 3, 4, 5 in Table 11				0/1	0	Input syncs[1]		0	0
									1	Output syncs[2]		0/1	
Enabled	1	1	0	0	0	0	0/1	1	1	1	1	0[5]	0

Note 1: Any combination of [HSLN, VSLN] except [0,1].
Note 2: Any combination of [HSLN, VSLN].
Note 3: When the syncs are inputs in interlaced CCIR-size, the field index FI_EN is also required.
Note 4: Parameter field is located in SYSMODE set-up parameter
Note 5: FI_EN is an input which enables the video output.
Note 6: Parameter field is located in VIDMODE set-up parameter.
Note 7: Parameter field is located in SYNMODE set-up parameter.

Video Data Bus Format Options

Prior to being output on the VIDOUT bus, the active region of the decoded picture is translated from the native format into one of the color space, component sub-sampling, and color depth formats shown in Table 11. The table summarizes the legal setup parameter combinations for each video data format. For YUV color spaces, the VBUV set-up parameter determines whether the U and V components will be output in a biased or unbiased format. For RGB color spaces, the conversion between YUV and RGB is performed using the coefficients in the CRV, CBU, CGV, and CGU set-up parameters. The conversion formulas are as follows, where U and V are in the unbiased representation:

R = Y + CRV*(V-128)
B = Y + CBU*(U-128)
G = Y + CGV*(V-128) + CGU*(U-128)

Format 2 is supported only in the interlaced CCIR-size configuration. In the Enabled configuration, only format 1 is supported.

Table 11. Video data formats

Video Data Format	VCLR	VIWD	VSMP	VBUV	Description		
					Color Space	Component Sub-Sampling	Color Depth (bits)
1	0	00	0	0/1	YUV	4:2:2	16
2	0	00	1	0/1	YUV	4:1:1	12
3	1	00	0	0	RGB	4:4:4	24
4	1	01	0	0	RGB	4:4:4	16 (5,6,5)
5	1	10	0	0	RGB	4:4:4	15 (5,5,5)

Note: 5,5,5 and 5,6,5 RBG are obtained by truncation of 8,8,8 (24-bit) RGB.

The sample arrangements on the video data bus for the five video data formats are given in the following tables. The most significant bit of each color component is aligned with the MSB of the VIDOUT sub-field on which it is output. A special case is the bit alignment for the UV color components in video format 2; this is shown in Table 13.

Table 12. Video format 1: YUV 4:2:2

VIDOUT bus	Pixel time slot							
	0	1	2	3	4	5	6	7
bits 23:16	FIL*							
bits 15:8	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
bits 7:0	U0	V0	U2	V2	U4	V4	U6	V6

* The value in the FIL setup parameter is output on bits 23:16.

Table 13. Video format 2: YUV 4:1:1

VIDOUT bus	Pixel time slot							
	0	1	2	3	4	5	6	7
bits 23:16	FIL							
bits 15:8	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
bit 7	U0,7	U0,5	U0,3	U0,1	U4,7	U4,5	V4,3	V4,1

Note: V0,7 indicates bit 7 of V component; sample 0.

Table 13. Video format 2: YUV 4:1:1

VIDOUT bus	Pixel time slot							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
bit 6	U0,6	U0,4	U0,2	U0,0	U4,6	U4,4	V4,2	V4,0
bit 5	V0,7	V0,5	V0,3	V0,1	V4,7	V4,5	V4,3	V4,1
bit 4	V0,6	V0,4	V0,2	V0,0	V4,6	V4,4	V4,2	V4,0
bits 3:0	Zero							

Note: V0,7 indicates bit 7 of V component; sample 0.

Table 14. Video format 3: 24 bit RGB

VIDOUT bus.	Pixel time slot							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
bits 23:16	R0	R1	R2	R3	R4	R5	R6	R7
bits 15:8	G0	G1	G2	G3	G4	G5	G6	G7
bits 7:0	B0	B1	B2	B3	B4	B5	B6	B7

Table 15. Video format 4: 16 bit RGB

VIDOUT bus	Pixel time slot							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
bits 23:16	FIL							
bits 15:11	R0	R1	R2	R3	R4	R5	R6	R7
bits 10:5	G0	G1	G2	G3	G4	G5	G6	G7
bits 4:0	B0	B1	B2	B3	B4	B5	B6	B7

Table 16. Video format 5: 15 bit RGB

VIDOUT bus	Pixel time slot							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
bits 23:16	FIL							
bit 15	Zero							
bits 14:10	R0	R1	R2	R3	R4	R5	R6	R7
bits 9:5	G0	G1	G2	G3	G4	G5	G6	G7
bits 4:0	B0	B1	B2	B3	B4	B5	B6	B7

Video Clocks (VCLK, QCLK_V)

In the interlaced CCIR-size interface configuration, VCLK is the pixel clock, and the video data bus and video sync signals are synchronized to the rising edge of VLCK.

In the progressive SIF-size configuration, there are two options: with parameter VCRS = 0, VCLK is the pixel clock, and the video bus and sync signals are synchronized to the rising edge of VLCK; with VCRS = 1, QCLK_V is the pixel clock, and the video bus and sync signals are synchronized to the rising edge of QCLK_V.

In the Enabled configuration, pixels are output in bursts at the VCLK rate and synchronized to VCLK. As far as the sync generator is concerned, however, the pixel clock frequency is effectively VCLK/4 and this should be used as the pixel rate when determining values for the display timing parameters.

Table 17 specifies the maximum VCLK frequency allowed in each configuration.

Table 17. Maximum VCLK frequency

Configuration	Max. VCLK Frequency	Pixel Rate
Interlaced CCIR-size	PCLK/4	VCLK
Progressive SIF-size (VCRS=0)	PCLK/16	VCLK
Progressive SIF-size (VCRS=1)	PCLK/4	1/4 VCLK (in sync with QCLK_V)
Enabled	PCLK/4	VCLK[*]

[*] Note, however, that in the Enabled video interface Configuration, the sync generator is clocked at a frequency of VCLK/4.

Active Region of the Decoded Picture

The decoded picture can be cropped to an "active region" prior to being displayed, as illustrated in Figure 4.

The size of the decoded picture is defined by the horizontal size (HS) and vertical size (VS) parameters given in the sequence header of the video stream. The active region of the decoded picture (the subregion within the decoded picture which will be post processed

and output on the VIDOUT bus) is defined by the NAP, NAL, NOP, and NOL set-up parameters. Restrictions on legal values for these parameters are given in Table 18.

Table 18. Legal NAP, NAL, NOP, NOL values

Parameter	Description	Representation	Video Interface Configuration	Restictions		
				Minimum value	Maximum value	Other
NAP	Width in pixels of the active region of the decoded picture	16-bit unsigned integer	All except Enabled		4*int(HS/4)	Multiple of 4
			Enabled	16		Multiple of 8
NAL	Height in lines of the active region of the decoded picture	16-bit unsigned integer	All		VS	none
NOP	Offset in pixels of the active region from the beginning of each line of the decoded picture	16-bit unsigned integer	All	0	4*int(HS/4)-NAP	Multiple of 4
NOL	Offset in lines of the active region from the beginning (top) of the decoded picture	16-bit unsigned integer	All	0	Smaller of VS-NAL, or 255	Even
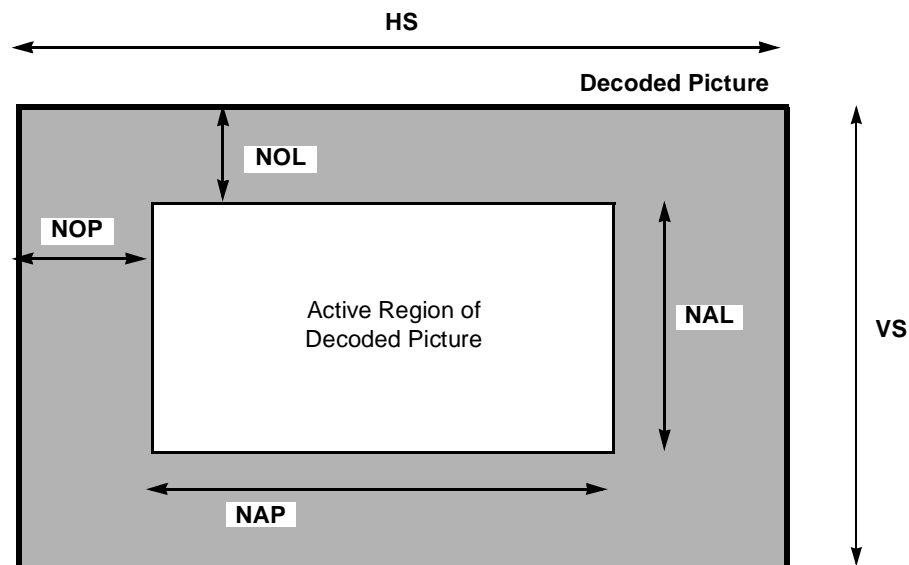
Figure 4. Decoded Picture and Active Region

Note: HS = Horizontal size
      VS = Vertical size
       HS and VS are found in the video sequence header

Video Sync Signals

Note: In all the diagrams in this section, those specifying the timing of the sync signals and those illustrating their interrelationships, active low sync signals are depicted. These diagrams apply equally well, with reversed polarity of the wave forms, to active high sync signals.

The HSYNC and VSYNC signals are both either inputs or outputs, as specified by the VDIR set-up parameter. The polarities of the HSYNC and VSYNC signals are selected independently using the HSHL and VSHL set-up parameters respectively. HSYNC and VSYNC are selected independently to be short (sync) or long (blanking) waveforms using the HSLN and VSLN fields of the VIDMODE parameter, respectively; but note that the combination of short input HSYNC and long input VSYNC is not allowed.

The set-up parameters NTP, NTL, NBP, NBPF, NDP, NBL, NBLF, NDL, HSW and VSW specify the sync signal waveforms. Table 19, Table 20 and Table 21, at the end of this subsection, show the restrictions on the values of these parameters. These restrictions are required to ensure that the parameters are consistent with one another, and with the other parameters that control the video display. Note that the parameters that specify horizontal timing are always specified in units of pixel periods (for the pixel period effective in each of the interface configurations, see above under *Video Clocks*).

The timing for a short, active low, output HSYNC is given in Figure 5. In this figure, HSYNC is active for HSW pixel periods. The timing for a long, active low, output HSYNC is given in Figure 6. In this figure, HSYNC is active for NBP + NBPF pixels. HSYNC has a period of NTP pixels.

Figure 7 shows the HSYNC signal when it is a short or long input. HSYNC must have a period of NTP pixels.

The timing for a short, active low output VSYNC is given in Figure 8. In this figure VSYNC is low for VSW lines. The timing for a long, active low, output VSYNC is given in Figure 9. In this figure VSYNC is low for (NBL + NBLF) lines + (NBP + NBPF) pixels. VSYNC has a period of NTL/2 lines for the interlaced CCIR-size configuration, and NTL lines for the progressive SIF-size or Enabled configurations.

Figure 10 shows the timing for short or long input VSYNC. VSYNC must have a period of NTL/2 lines for the interlaced CCIR-size configuration, and NTL lines for the progressive SIF-size configuration.

Whenever the edges of long input HSYNC and long input VSYNC should ideally coincide, the edges of VSYNC must not jitter outside the active part of HSYNC.

Note that in order to generate and receive sync signals which comply with the interlaced NTSC and PAL standards, the width of the VSYNC pulse can be defined with resolution of half a line.
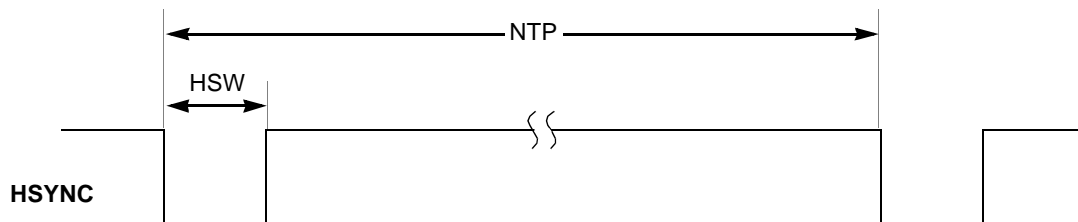
Figure 5. Short output HSYNC
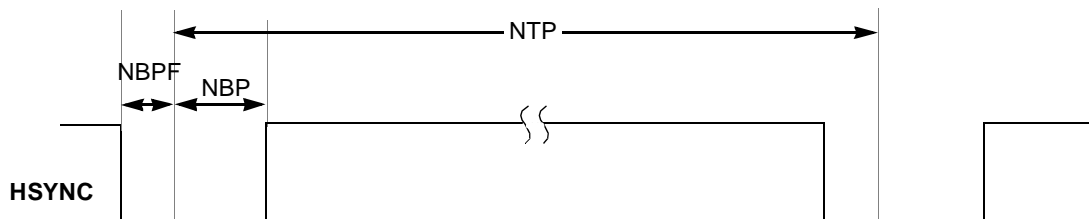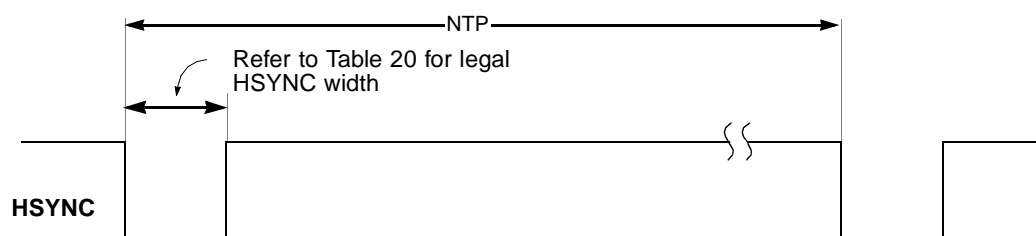

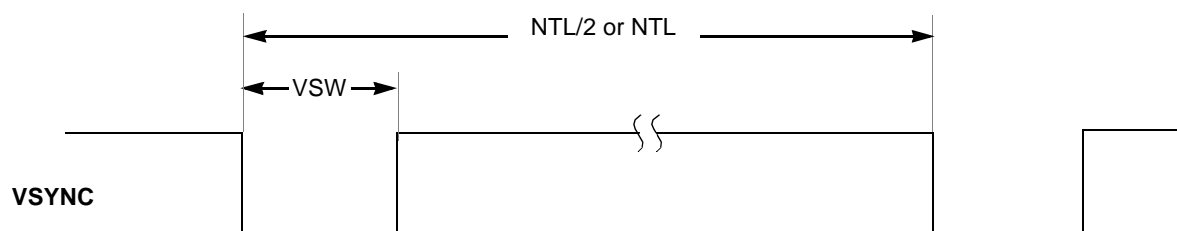**Figure 6. Long output HSYNC**

Figure 7. Input HSYNC

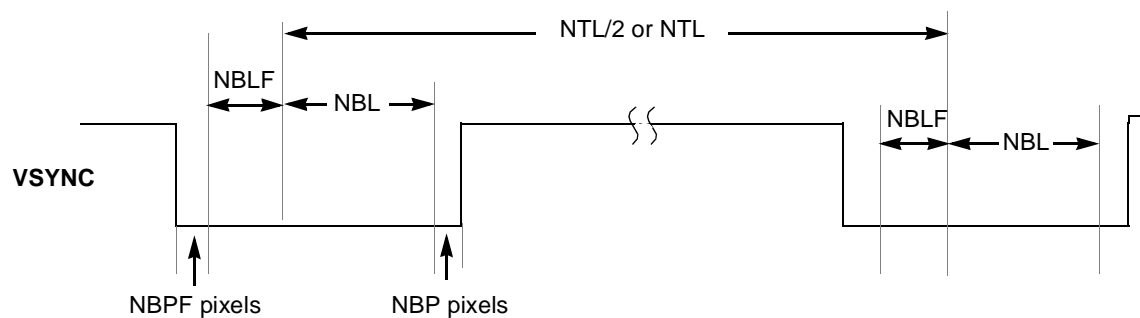**Figure 8. Short output VSYNC**

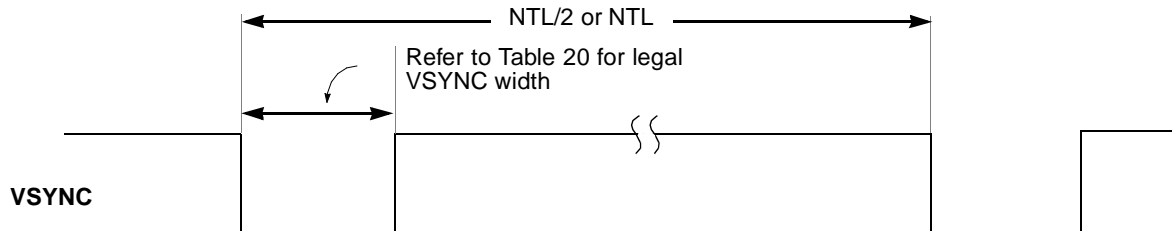**Figure 9. Long output VSYNC**

Figure 10. Input VSYNC

Table 19. Restrictions on legal values for NTP and NTL

Parameter	Definition	Interface Configuration	Restrictions		
			Minimum	**Maximum**	**Other**
NTP[1]	number of pixels per horizontal sync cycle	Interlaced CCIR-size; Output HSYNC	NBPF+NBP+NDP+ 2*NAP	1023	must be even
		Interlaced CCIR-size; Input HSYNC	Number of pixels between leading edges of two HSYNCs (maximum of 1023)		must be even
		Progressive SIF-size or Enabled; Output HSYNC	NBPF+NBP+NDP+NAP	1023	none
		Progressive SIF-size; Input HSYNC	Number of pixels between leading edges of two HSYNCs (maximum of 1023)		none
NTL[1]	number of lines per frame	Interlaced CCIR-size; Output VSYNC	2*(NBLF+NBL+NDL+ NAL)	1023	must be odd
		Interlaced CCIR-size; Input VSYNC	Number of lines between leading edges of alternate VSYNCs (maximum of 1023)		must be odd
		Progressive SIF-size or Enabled; Output VSYNC	NBLF+NBL+NDL+NAL	1023	none
		Progressive SIF-size; Input VSYNC	Number of lines between leading edges of consecutive VSYNCs (maximum of 1023)		none

1 NTP*NTL*FPS=VCLK rate (or QCLK_V rate if VCRS = 1), where FPS is the display frame rate.

Table 20 specifies the restrictions on the relevant setup parameters for the output sync combinations.

Table 20. Restrictions on legal values for output sync parameters

Sync Combination	Parameters							
	NBP	NBPF	HSW	NDP	NBL	NBLF	VSW	NDL
H-short V-short	a	e	b	f	c, i	i, k	g	h
H-short V-long	a	e	b	f	j, i	i, k	=0	h
H-long V-short	d	e	=0	f	c, i	i, k	g	h
H-long V-long	d	e	=0	f	i, j	i, k	=0	h
Enabled	d	e	=0	=0	i, j	i, k	=0	=0

For the following notes, the notation ( ), [ ] signifies the restrictions relevant to (interlaced CCIR-size), [progresive SIF-size or Enabled] configurations. When a restriction is shown without brackets or parentheses, it applies to all video interface configurations.

a. Minimum = HSW, maximum = NTP/2 or (NTP-2*NAP), [NTP-NAP] whichever is smaller.

b. Minimum = 4, maximum = NBP.

c. Minimum = 2.0 or VSW, whichever is larger. Maximum = (int (NTL/2)-NAL), [NTL-NAL].

d. Minimum = 4, maximum = NTP/2 or (NTP-2*NAP), [NTP-NAP] whichever is smaller.

e. Minimum = 2. maximum = NTP/2 or (NTP-2*NAP-NBP), [NTP-NAP-NBP], whichever is smaller.

f. Multiple of 4, minimum = 0, maximum = (NTP-2*NAP-NBP-NBPF), [NTP-NAP-NBP-NBPF].

g. Minimum = 2.0. Maximum = NBL.

h. Minimum = 0, maximum = (int (NTL/2)-NAL-NBL-NBLF), [NTL-NAL-NBL-NBLF].

i. The sum of NBL and NBLF is restricted to be an integer.

j. Minimum = 2.

k. Minimum = 1, maximum = (int (NTL/2)-NAL-NBL), [NTL-NAL-NBL].

Table 21 specifies the restrictions on the relevant set-up parameters for the input sync combinations.

Table 21. Restrictions on legal values for input sync parameters

Sync Combination	Parameters							
	NBP	NBPF	HSW	NDP	NBL	NBLF	VSW	NDL
H-short V-short	a	d	=0	e	b, c	c, f	=0	g
H-long V-short	=0	=0	=0	e	b, c	c, f	=0	g
H-long V-long	=0	=0	=0	e	=0	=0	=0	g

For the following notes, the notation ( ), [ ] signifies the restrictions relevant to (interlaced CCIR-size), [progresive SIF-size] configurations. When a restriction is shown without brackets or parentheses, it applies to all video interface configurations.

a. Minimum = width of input HSYNC, maximum = NTP/2 or (NTP-2*NAP), [NTP-NAP] whichever is smaller.

b. Minimum = actual width of input VSYNC or 2, whichever is larger. Maximum = (int (NTL/-2)-NAL), [NTL-NAL].

c. The sum of NBL and NBLF is restricted to be an integer.

d. Minimum = 2. Maximum = NTP/2 or (NTP-2*NAP-NBP), [NTP-NAP-NBP], whichever is smaller.

e. Multiple of 4. Minimum = 0. Maximum = NTP-2*NAP-NBP-NBPF, [NTP-NAP-NBP-NBPF].

f.   Minimum =1. Maximum = (int (NTL/2)-NAL-NBL), [NTL-NAL-NBL]).

g.   Minimum = 0. Maximum = (int (NTL/2)-NAL-NBL-NBLF), [NTL-NAL-NBL-NBLF].

Note also: The restrictions on the actual widths of input HSYNC and VSYNC pulses are identical to those for output HSYNC and VSYNC, as specified in the notes to Table 20.

Effective Blanking Interval and Extended Blanking Interval

The specification of the Video Display regions in the next subsection requires the definition of the following terms:

■ Effective Blanking Interval
  - The Effective Blanking Interval is related to VSYNC. For a short VSYNC signal, the effective blanking interval begins NBLF lines before the active edge of VSYNC, and continues for NBL lines following the active edge of VSYNC. For long VSYNC, the effective blanking interval is the same as the active period of the VSYNC signal.
■ Complete line
  - A Complete Line is all the VCLKs between leading edges of two successive HSYNC signals.
■ Extended Blanking Interval.
  - The Extended Blanking Interval is derived from the effective blanking interval as follows. When the effective blanking interval ends in the middle of a complete line (e.g. because of odd NTL in interlaced output, or non-integer NBL) it is extended until the end of the complete line. When the effective blanking interval starts in the middle of a complete line (for the same reasons), and the VSYNC is other than the long input case, the effective blanking interval is extended to cover also the preceding part of the complete line. This is illustrated in Figure 11.

a) Extended Blanking Interval:
All cases except long input VSYNC

b) Extended Blanking Interval:
Long input VSYNC
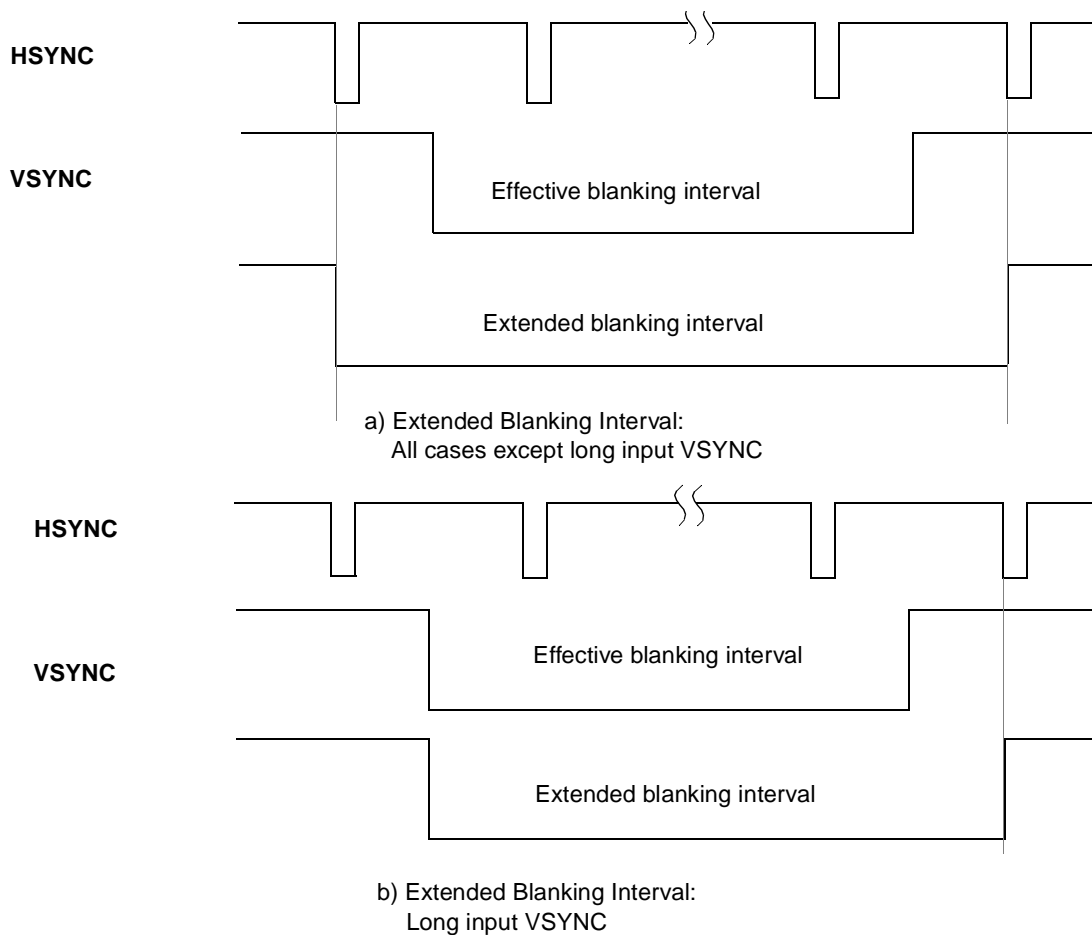
Figure 11. Extended blanking interval derivation from effective blanking interval

Video Display Regions

There are three data regions within a field or frame defined for the VIDOUT data: Active Region, Blanking Region, and Background Color Region. For interlaced CCIR-size configuration, refer to Figure 12. For progressive SIF-size or Enabled configuration, refer to Figure 13.

The set-up parameters NBP, NBPF, NBL, and NBLF define the Blanking Region (except when the sync signals are long inputs, in which case the horizontal and vertical blanking regions are defined by the actual widths of the sync signals respectively). The VIDOUT bus is driven to zero in this region.

The set-up parameters NDP and NDL define the horizontal and vertical offsets from the end of the Blanking Region to the start of the Active Region. The Active Region is 2xNAP (for interlaced CCIR-size) or NAP (for progressive SIF-size or Enabled) pixels wide by NAL lines high. The VIDOUT bus is driven with active picture data in the active region.

The Background Color Region is the region between the Blanking Region and the Active Region. The VIDOUT bus is driven with the values specified in the BGRV, BGGY, BGBU set-up parameters.

A special condition exists when HSYNC is a long input. In this case, the Blanking Region is extended by four pixels following the rise of the HSYNC signal. NDP is counted after these four pixels. Also, the first four pixels following the fall of HSYNC will be background color. If VCRS = 1, this delay is two pixels instead of 4.
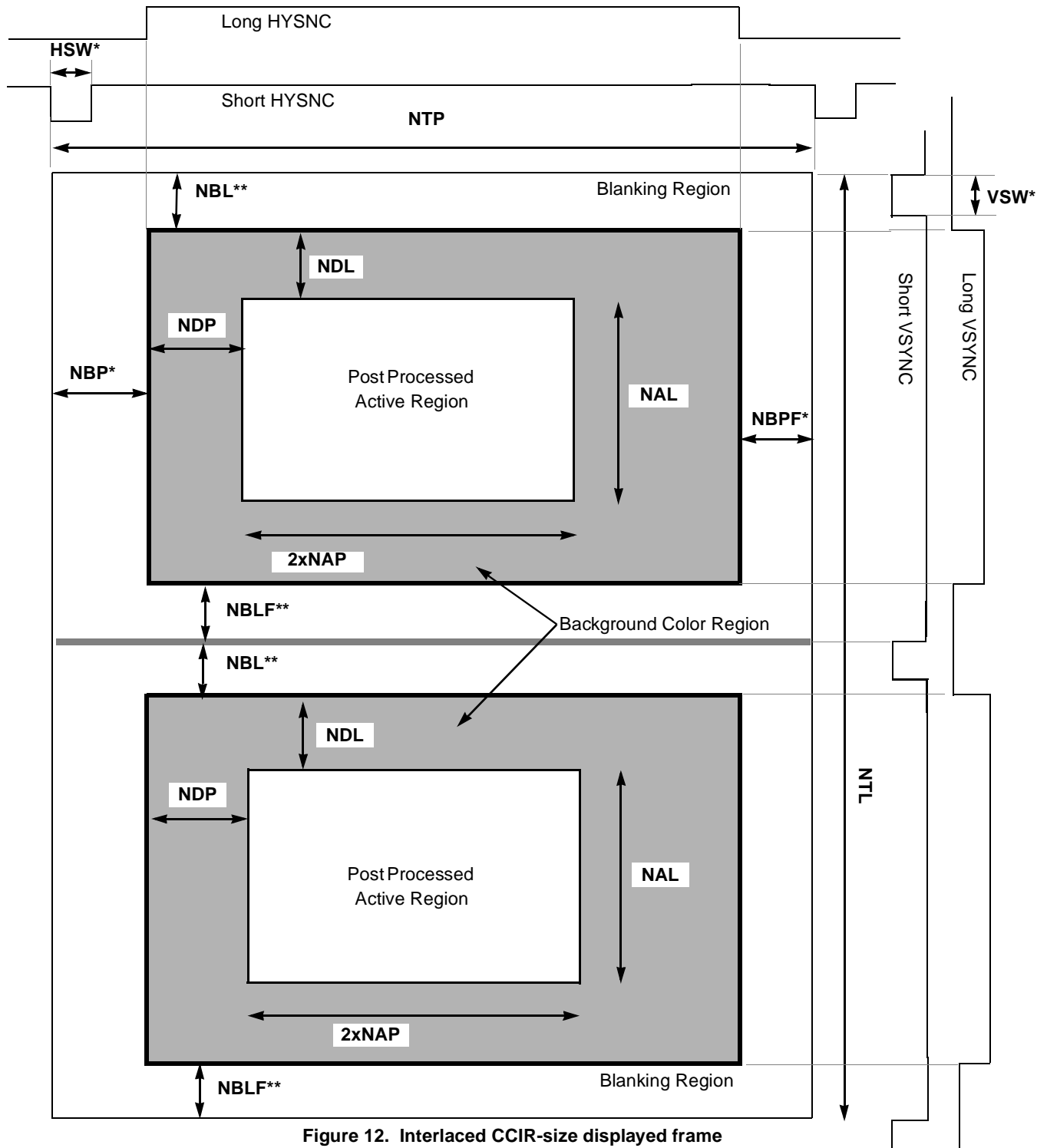
ZORAN

Figure 12. Interlaced CCIR-size displayed frame

* Not applicable when HSYNC signal is long input. In this case, these parameters are set to zero and the HSYNC waveform is determined by the source.
** Not applicable when VSYNC signal is long input. In this case, these parameters are set to zero and the VSYNC waveform is determined by the source.
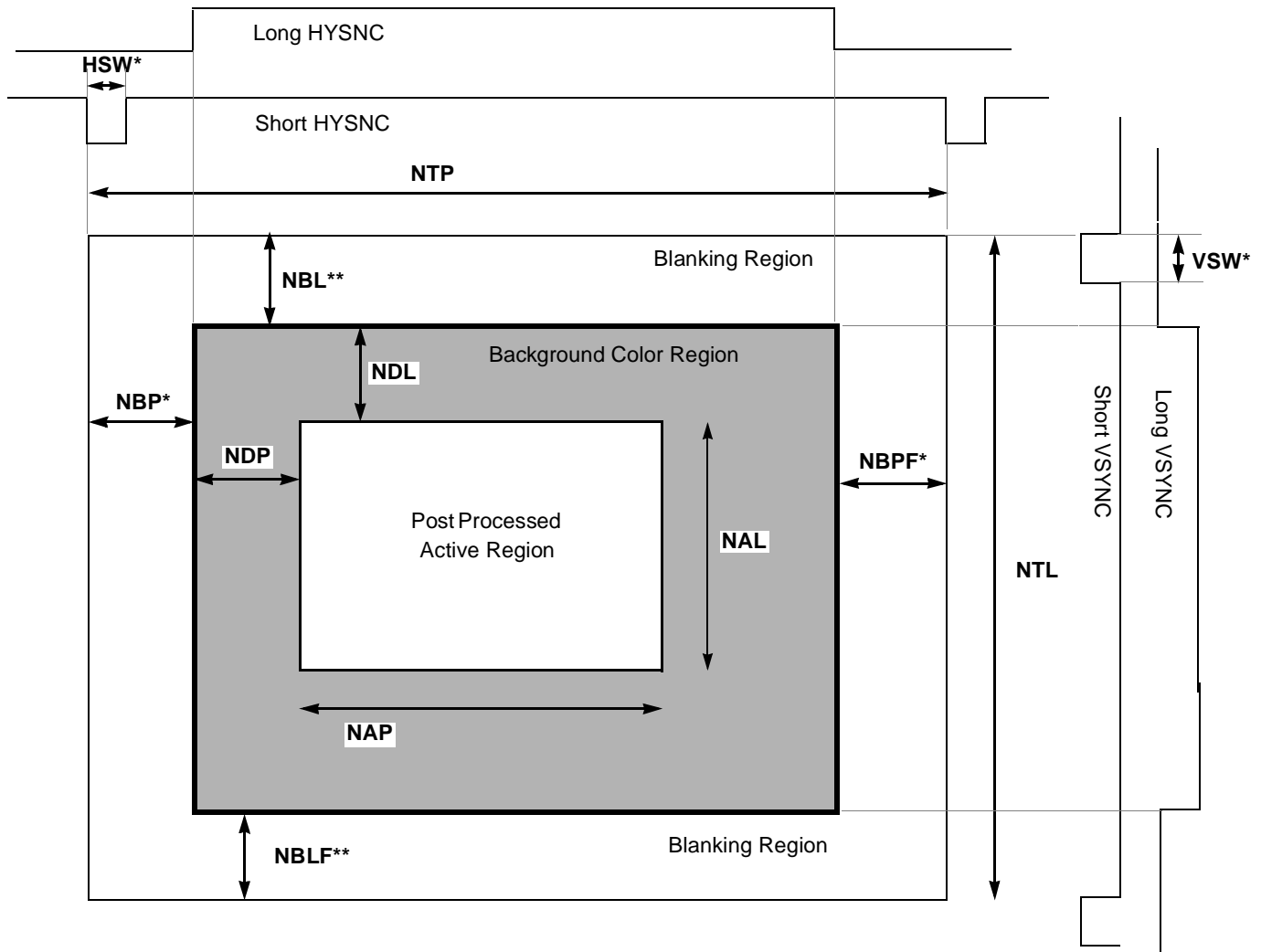Note also that the vertical parameters NBL, NBLF or the long input VSYNC are the extended versions, as described above.

Figure 13. Progressive SIF-size or Enabled mode displayed frames

* Not applicable when HSYNC signal is long input. In this case, these parameters are set to zero and the HSYNC waveform is determined by the source.

** Not applicable when VSYNC signal is long input. In this case, these parameters are set to zero and the VSYNC waveform is determined by the source.

Note also that the vertical parameters NBL, NBLF or the long input VSYNC are the extended versions, as described above.

The FI_EN signal

For interlaced CCIR-size configuration with output syncs, FI_EN can be either a field index or a composite blanking signal, as determined by the VBLN set-up parameter. With input syncs it is required to be a field index.

When FI_EN is defined to be a composite blanking signal, it is driven active in the Blanking region defined in Figure 12, that is, during the horizontal blanking interval and during the extended vertical blanking interval.

When FI_EN is defined to be a field index signal, it is active during field I and inactive during field II. When the sync signals are output, FI_EN is driven by the ZR36100; when the sync signals are inputs, FI_EN must be driven externally. (Recall that field I is defined to be the field that starts at HSYNC, while field II is defined to start in the middle of a line.)

Figures 14 through 21 show the relation of FI_EN (as a field index) and VSYNC to HSYNC under several different conditions. The conditions depend on the type of HSYNC and VSYNC (long or short) being used, and on whether non integer NBL/NBLF (e.g., for NTSC) or integer NBL/NBLF (e.g., for PAL) output video format is being used. All these examples show active-low syncs, and FI_EN low during Field I, but apply equally well to the complementary cases.

Enabled Video Interface Configuration

In Enabled configuration, the video output is progressive and SIF-sized with YUV 4:2:2 pixel format (this combination of SIF size and 4:2:2 pixel format is sometimes referred to as 2:1:1), and HSYNC and VSYNC must be outputs and long. The U and V components can be selected to be either biased or unbiased.

The FI_EN signal is an input which enables the video output. The active region of the decoded picture is output with the original size. Video is output only when enabled by the FI_EN input signal, starting one VCLK cycle following the activation of FI_EN. When FI_EN is de-activated, the VIDOUT bus floats, starting one VCLK cycle following the de-activation of FI_EN. Whenever there are at least 8 valid pixels in the video output FIFO, the QCLK_V signal is driven high, and 8 pixels can be read out in a burst by enabling FI_EN, before QCLK_V needs to be checked again.

All the pixels of the picture must be read out in the interval between the trailing edge of VSYNC and the leading edge of the next VSYNC; HSYNC can be disregarded. It is the responsibility of the circuits which generate the enable signal to make sure that the average pixel rate is maintained over the frame, when the averaging period is a quarter of the frame. The receiver of the video output data must count the number of active pixels per line and number of active lines to determine when all data of a picture have been read out.
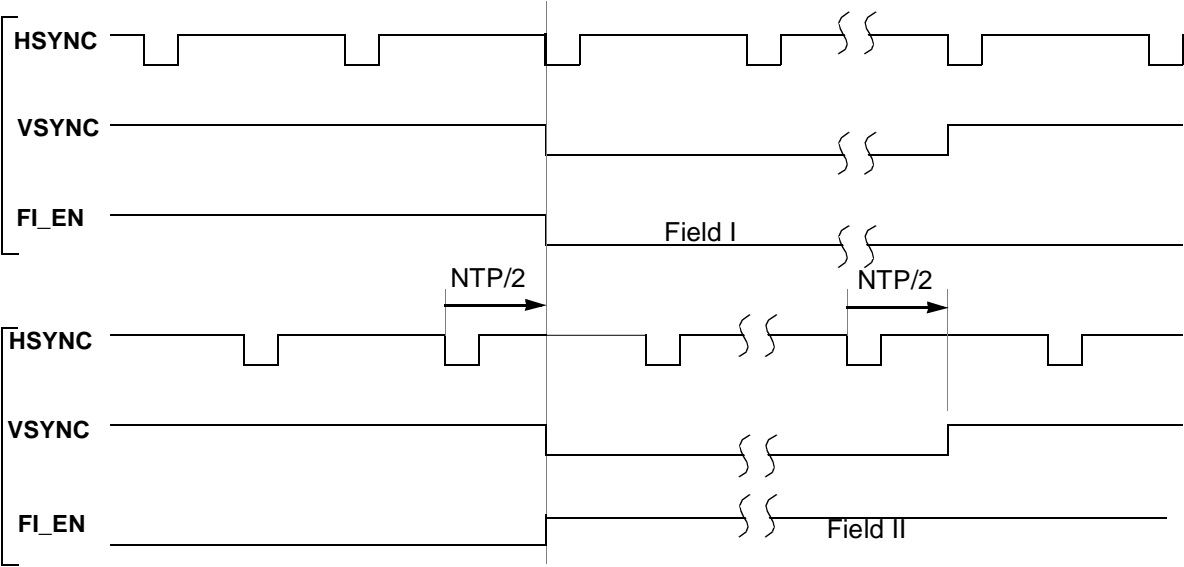
Figure 14. Field Index: (short HSYNC, short VSYNC, width of VSYNC is integer number of lines)
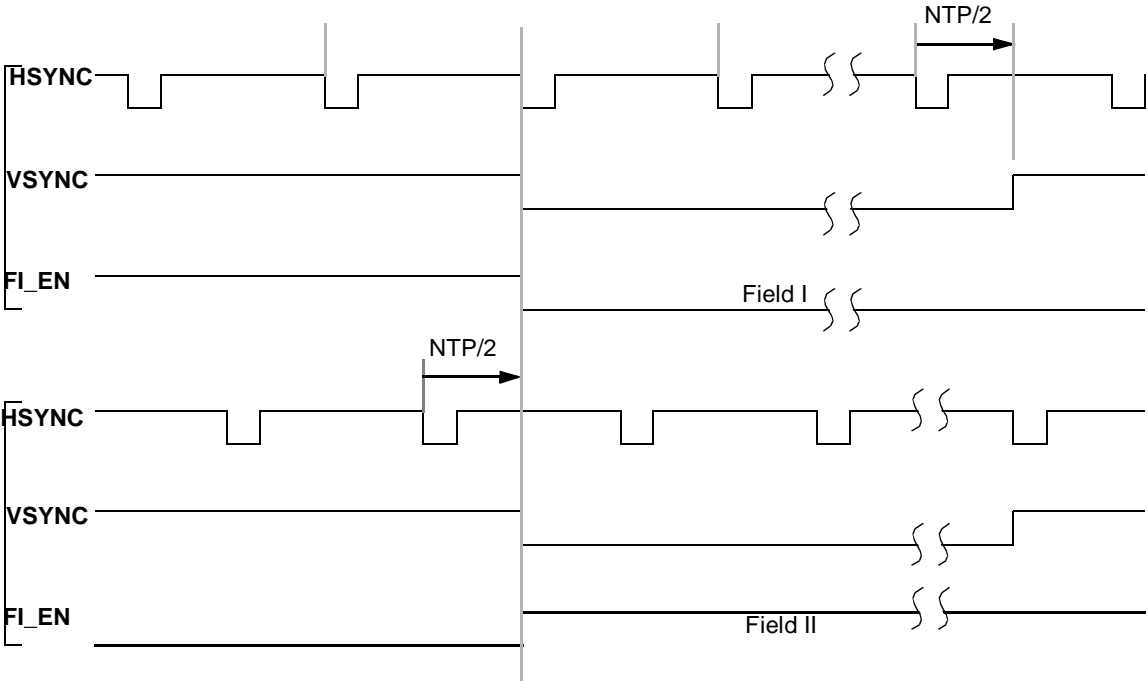

Figure 15. Field Index: (short HYSYNC, short VSYNC, width of VSYNC is non-integer number of lines)
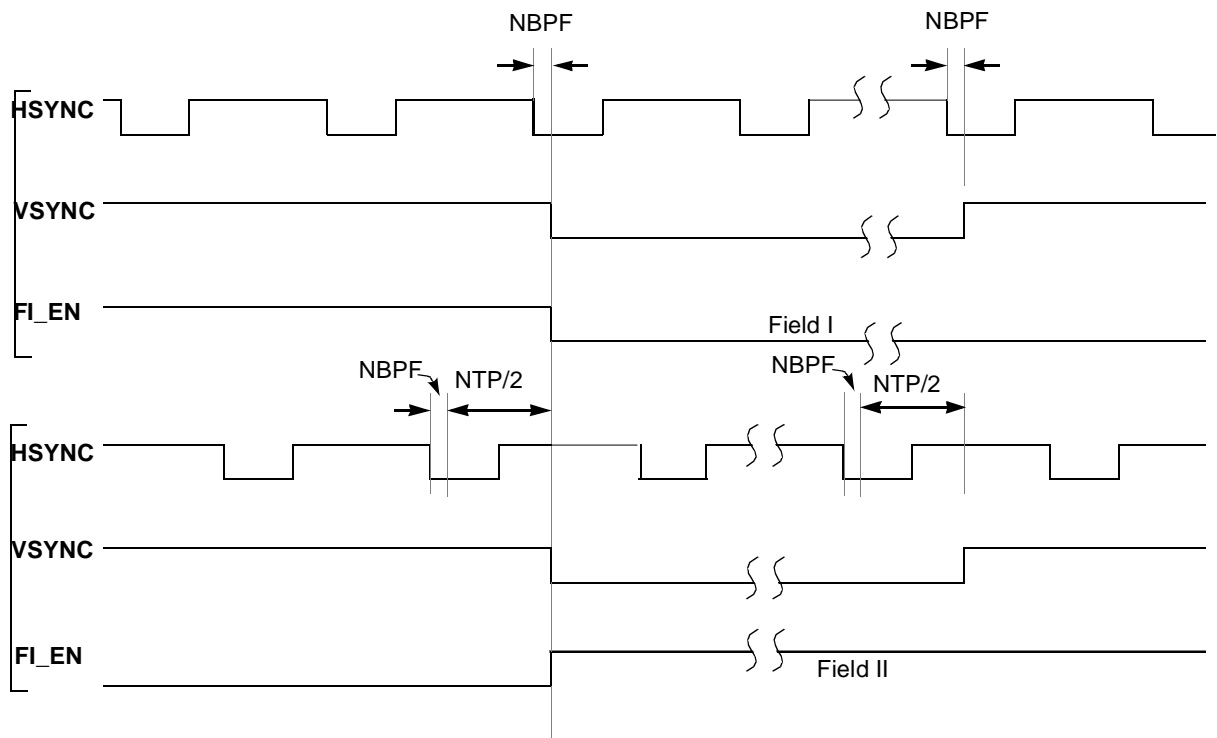
Figure 16. Field Index Signal: (long HSYNC, short VSYNC, width of VSYNC is integer number of lines)
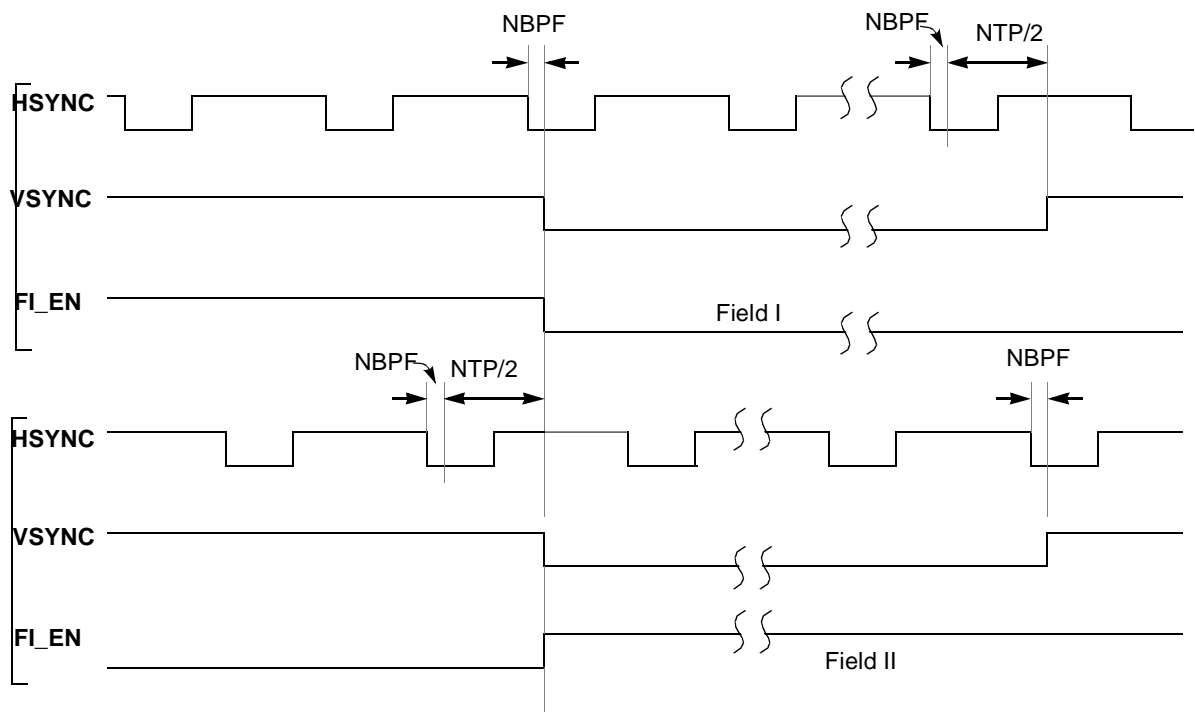

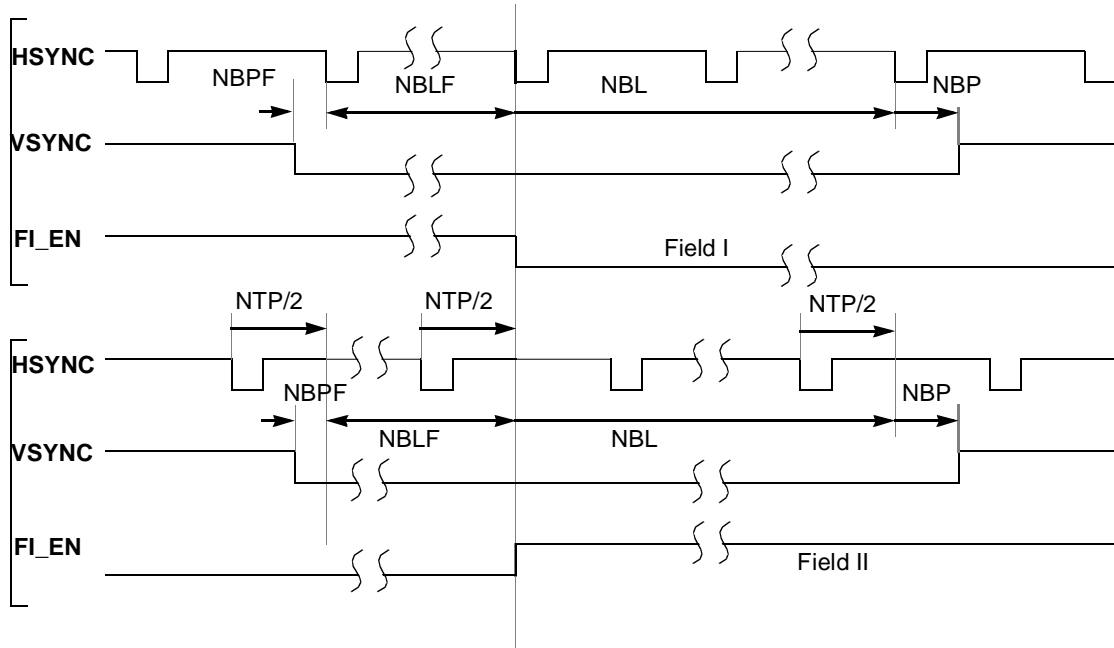**Figure 17. Field Index: (long HSYNC, short VSYNC, width of VSYNC is non-integer number of lines)**

Figure 18. Field Index: (short HSYNC, long VSYNC, NBL is integer number of lines)
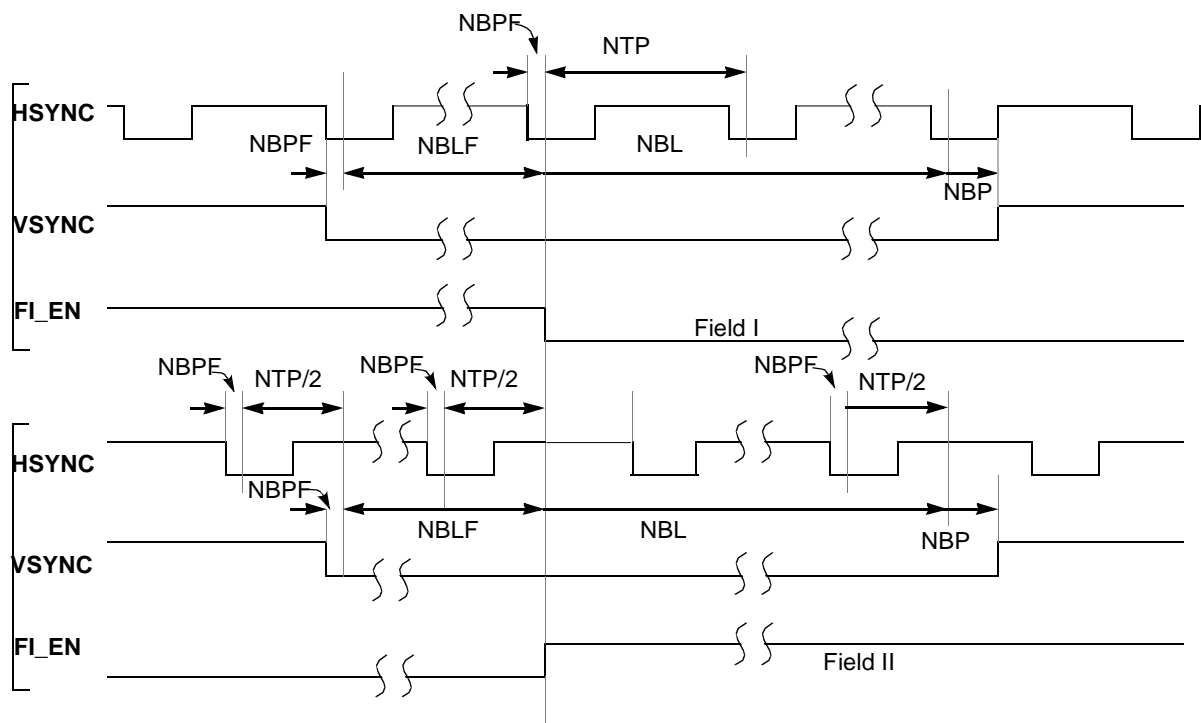Note: Sync. signals are always output for the short HSYNC, long VSYNC case
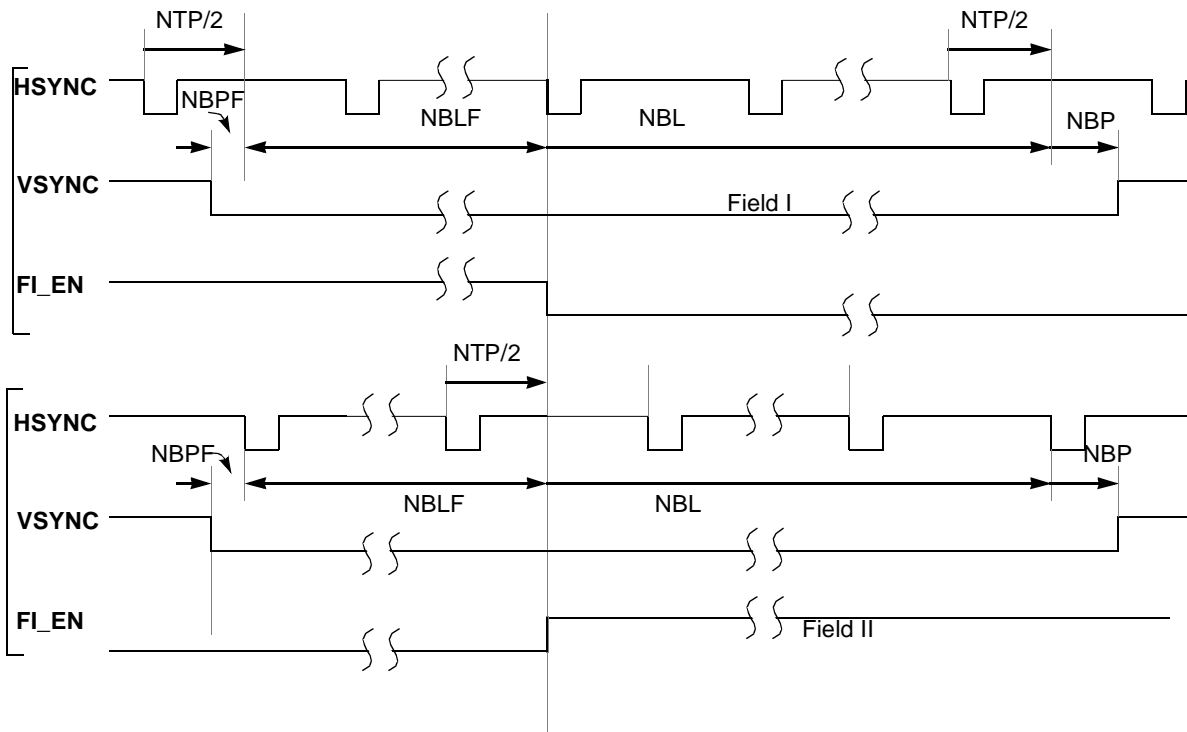
Figure 19.   Field Index: (short HSYNC, long VSYNC, NBL is non-integer number of lines)
Note: Sync. signals are always outputs for the short HSYNC, long VSYNC case.

Figure 20. Field Index: (long HSYNC, long VSYNC, NBL is integer number of lines)
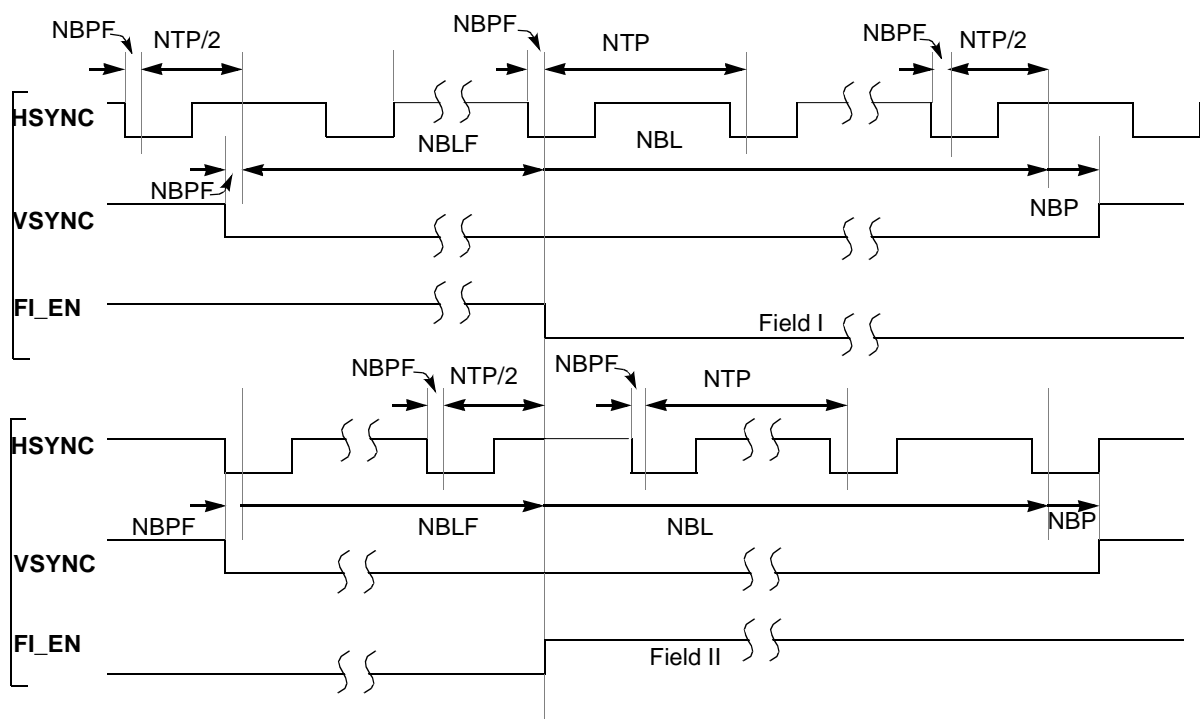

Figure 21. Field Index: (long HSYNC, long VSYNC, NBL is non-integer number of lines)

SERIAL PORTS INTERFACE

The ZR36100 has two serial output ports that operate independently of each other. These serial ports can be used to transfer the audio or private streams embedded in a system bitstream to a decoders for these streams.

   Note: Not all versions of the ZR36100 microcode support two simultaneously active serial ports.

Each serial port has one data line (SP1DAT and SP2DAT), used to transfer the bitstream, one frame synchronization line (SP1FRM and SP2FRM) and one clock line (SP1CLK and SP2CLK). Serial port 1 has an additional data line (SP1CMD), used to transfer commands to the receiver of the bitstream. The transfers of data (and serial port 1 commands) are done in 16-bit groups, which are called frames. The SP1FRM and SP2FRM signals synchronize the transfer of these frames.

Serial Port Modes

The S1AC, S1CD, S1BS, and S1FT fields in the SP1MODE setup parameter, and the S2AC, S2CD, S2BS, and S2FT fields in the SP2MODE setup parameter, specify the mode of operation of serial port 1 and serial port 2 respectively.

The clock signals can be specified as inputs or as outputs. The frame synchronization signals can be specified as pulse type or as transition type; these signal types are described below.

Each serial port can be specified to be active or inactive. When active, a serial port will output the bitstream assigned by the S1BS or S2BS parameters respectively. When defined to be inactive, a serial port does not output data. When decoding a video-only bitstream, both serial ports must be defined to be inactive.

Serial Port Transfer Rate

When its clock signal is defined to be an output, the clock frequency for a serial port is specified to be an integer divisor of the VCLK frequency via the SP1CD or SP2CD setup parameter. The specified serial port clock frequency must be equal to or above the bit rate specification of the stream assigned to the port.

The SP1BR or SP2BR setup parameter must be programmed to be the ratio of bit rate to the clock frequency of the serial port. The ZR36100 uses this value to generate a constant average data transfer rate from the serial port equal to this bit rate.

Note that when the display frame rate is such as would cause the video to be decoded at a picture rate different from the picture rate of the sequence header, the serial port bit rate has to be multiplied by the appropriate ratio (actual-picture-decoding-rate/sequence-header-picture-rate) when calculating the SP1BR or SP2BR setup parameter.

Note also that since the video decoding rate, MPEG bitstream consumption rate, audio bitstream buffer status, and serial port output data rate are closely linked with one another, the audio decoder's output sample rate and the ZR36100's video clock (VCLK) frequency must be locked to ensure glitch-free operation.

Frame Synchronization Signal

The frame synchronization signal indicates the beginning of a serial port frame (16 bits of data and/or a 16 bit command word for serial port 1, or 16 bits of data for serial port 2). The two frame synchronization signals may be independently selected to be either pulse type or transition type. Pulse type frame synchronization signals are active high for one serial port clock period, which precedes the first bit of the frame. The pulse type frame synchronization signal is activated and deactivated with the rising edge of the clock signal of the same port. The transition type frame synchronization signal changes levels at the beginning of each frame. The transition is concurrent with the falling edge of the clock and precedes the first data bit by one clock cycle.

The length of a frame, that is, the interval between two activations (or transitions) of the frame synchronization signal, is at least 16 serial port clock periods, but may be larger depending on the value of SP1BR or SP2BR. When data is being output from the port, the interval typically fluctuates between two intervals that differ by one serial port clock period. For example, if SP2BR is 1.0, all frames are exactly 16 clocks long. If SP2BR is 0.5, all frames are 32 clocks long. If SP2BR is slightly larger than 0.5, say 0.5 + 1/128, the frame length fluctuates between 31 and 32 clocks.

The serial port bitstream is organized into 16-bit words; the first bit to be output in a frame is the most significant bit of a word or the earlier bit of a bitstream.

The SP1FRM signal of port 1 is activated whenever there is a word of bitstream data to be clocked out, or when a serial port command has to be transferred. Bit 3 of the command (bit 0 is the lsb) indicates whether the data transferred with the command on the SP1DAT line is valid or not.

Figure 22 and Figure 23 illustrate the timing relationships at the beginning of a serial port frame, with transition-type frame sync, for two representative cases. In the first case, the length of the previous frame was exactly 16 clocks, and in the second case it was greater than 16 clocks, specifically 18 clocks. Figure 24 and Figure 25 show the same examples for pulse-type frame sync. These figures show the signals of serial port 1, but are equally valid for the corresponding signals of serial port 2.
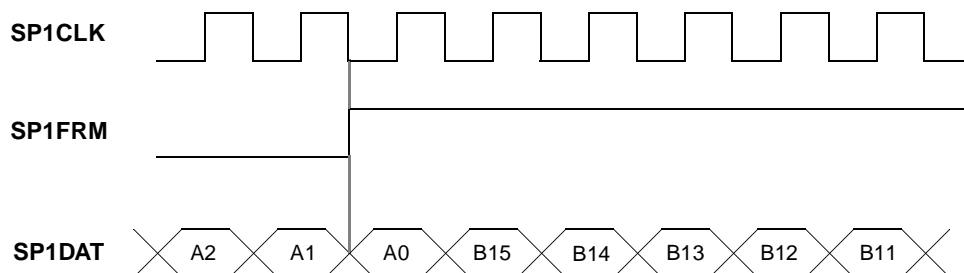
Figure 22. Beginning of serial port frame with transition frame sync signal, length of previous frame is 16 clocks
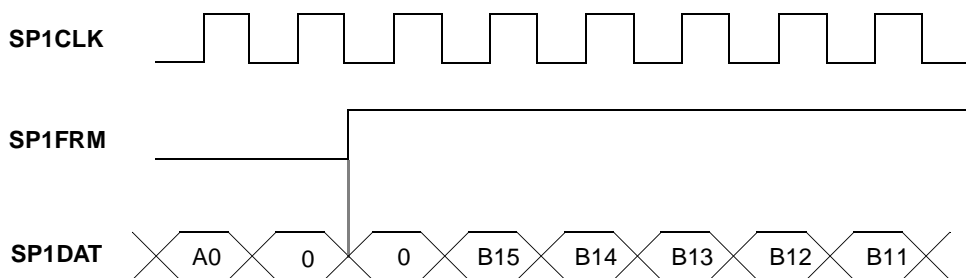
Figure 23. Beginning of serial port frame with transition frame sync signal, length of previous frame is 18 clocks
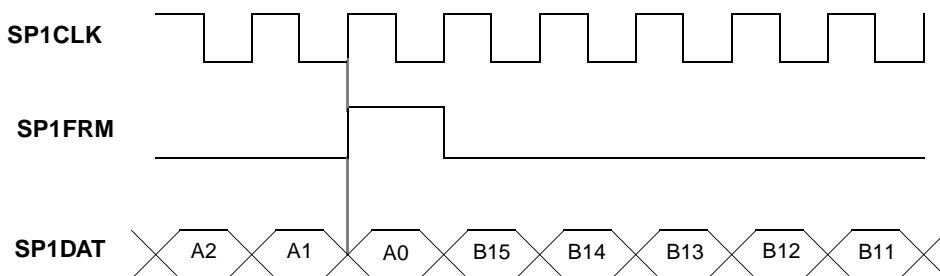
Figure 24. Beginning of serial port frame with pulse frame sync signal, length of previous frame is 16 clocks
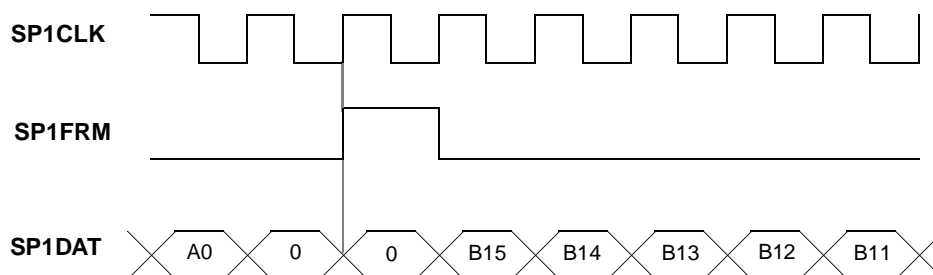
Figure 25.   Beginning of serial port frame with pulse frame sync signal, length of previous frame is 18 clocks

Serial port 1 commands

Serial port 1 uses a second data line (SP1CMD) to relay commands from the ZR36100 to the receiver of the serial port data. The commands are 16-bit words with the 3 lowest bits specifying the command, one bit indicating the validity of the data appearing on the data line in the same frame as the command, and 12 high bits which are zero. The commands are "change state" commands, i.e. they are issued only once. All subsequent words on the SP1CMD line (until the next different command) are all zero. Examples are shown in Figure 26, Figure 27 and Figure 28.

A description of the serial port commands is given in the *On-line Commands* section of this data sheet.
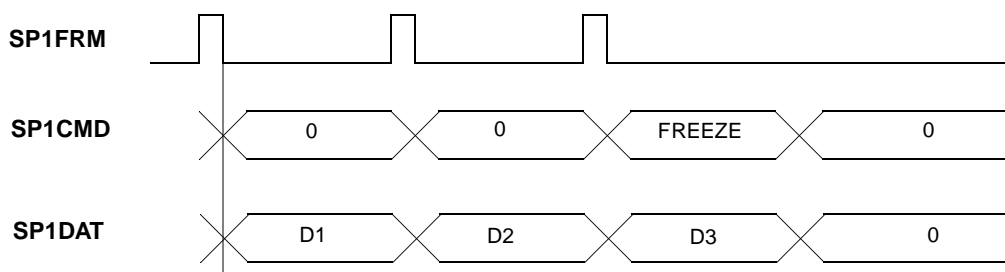

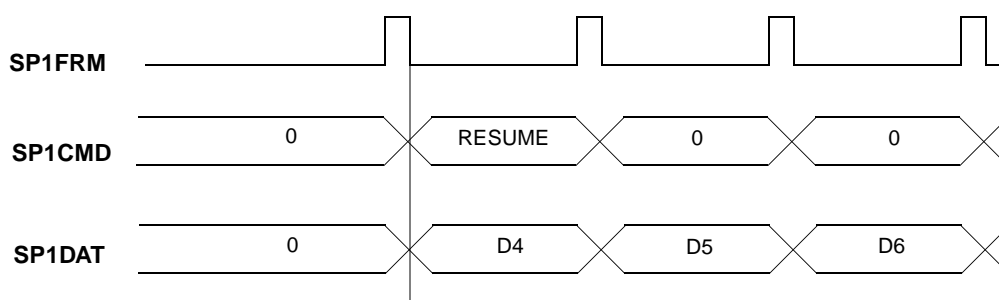**Figure 26.   Example - Freeze serial port command (with valid data)**

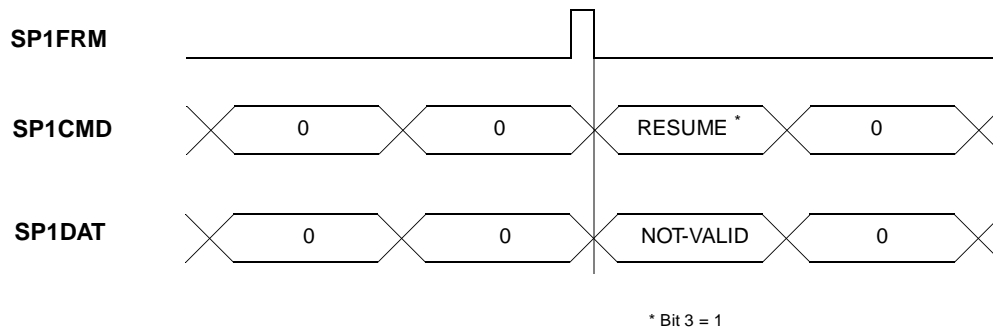**Figure 27.   Example - Resume serial port command (with valid data)**

Figure 28. Example - Resume serial port command (without valid data)

DRAM INTERFACE

The ZR36100 uses external DRAM to buffer the video and serial port data streams and to store decoded pictures. The timing specifications for the DRAM interface support typical devices of 80ns speed or faster. The DRAM interface circuits in the ZR36100 assume that the DRAM structure is symmetric, 512 rows by 512 cells each. Based on this assumption of DRAM structure symmetry, only nine address lines are used. The DRAM must be configured as a 256K x 16 memory and therefore can use either four 256K x 4 devices or one 256K x 16 device.

The DRAM interface consists of a 16-line data bus (RAMDAT), a 9-line address bus (RAMADD) and three control lines ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$).

The write and read operations are in the "fast page" mode. The ZR36100 indicates a write cycle by activating the $\overline{WE}$ signal, otherwise the cycle is a read. The output enable pin of the DRAM must be tied active.

The DRAMs are refreshed at rate not less than 512 rows in 8 milliseconds. The timing for the refreshes is given in the *AC Characteristics* section.

Note that the DRAM can not be accesed by the host, either directly or indiretly, but only by the internal MPEG decoding circuitry of the ZR36100.

CLOCK INPUTS

The ZR36100 requires a general clock, GCLK, that is used as the reference clock for an internal PLL clock multiplier. The output of the clock multiplier (available on the PCLK pin; but note that this signal is provided for monitoring only, and must not be loaded) is used to run the internal processing circuits, and to derive the DRAM interface timing. By means of the $\overline{MB4}$ pin, the PLL can be configured to multiply GCLK by 4 ($\overline{MB4}$ low) or 4.5 ($\overline{MB4}$ high). This allows the attainment of a PCLK frequency in the required range, when GCLK is one of a number of frequencies commonly available in video circuits.

As an alternative to using an external clock generator, an internal crystal oscillator can be used to generate GCLK. For this, a crystal of the appropriate resonant frequency is connected between the GCLK and XT pins, with a 20pF capacitor connected from each terminal to ground.

The other clock that must be provided to the ZR36100 is the video clock VCLK, which is used as the timing reference for the video interface and the video sync generator. VCLK is also the reference from which the time delays required for video and audio synchronization are derived. VCLK can be asynchronous with and independent of GCLK, but it is legitimate for GCLK and VCLK to be connected to the same clock generator if this is convenient.

RESET AND STANDBY

Activation of the $\overline{\text{RESET}}$ pin of the ZR36100 affects the device in one of two ways, depending on the active duration:

- If $\overline{\text{RESET}}$ is active for 160 or more GCLK periods, this is called a "cold reset."
- If $\overline{\text{RESET}}$ is active for between 32 and 128 GCLK periods, this is called a "warm reset."

If $\overline{\text{RESET}}$ is activated for less than 32 or between 129 and 159 GCLK periods, behavior of the device is unpredictable.

Cold Reset

A cold reset causes the PLL to lock on the frequency of GCLK. It also initializes the set-up parameters to their default values. It is *required* after any of the following events that invalidate the PLL lock:

- Power-up
- Deactivation of the $\overline{\text{STDBY}}$ signal
- A significant change in the frequency of GCLK (greater than the drift of a typical crystal oscillator)
- A change in the $\overline{\text{MB4}}$ input signal

A cold reset *must* also precede either of the following initialization changes:

- Any change to one or more of the "fixed" set-up parameters
- Loading a different version of the first microcode program (described in the *Initialization* section)

If $\overline{\text{RESET}}$ is active (low) at power up, it must remain active for at least 2.5 milliseconds after VCC, GCLK, $\overline{\text{MB4}}$ and $\overline{\text{STDBY}}$ have stabilized, in order to ensure that the PLL to locks correctly. If $\overline{\text{RESET}}$ is high at power up, it must remain high for at least 2.5 milliseconds, after VCC, GCLK, $\overline{\text{MB4}}$ and $\overline{\text{STDBY}}$ have stabilized, before a cold reset pulse is applied to trigger the PLL to lock.

The PLL lock procedure starts when $\overline{\text{RESET}}$ goes high, and terminates not more than 5000 GCLK periods thereafter. When the PLL is locked, the READY and IDLE signals and status bits are high, indicating that the device is ready for initialization as described in the *Initialization* section.

Warm Reset

Warm reset is not needed in normal operation of the ZR36100. It is reserved for use in work-arounds for bugs in early versions of the device. A warm reset forces the processor to go idle and display the background color, clears the on-line command queue, flushes the internal buffers and resets the internal controls. Note that a warm reset does not force the set-up parameters to their default values.

Standby Power

The ZR36100 can be switched to Standby power, by activation of $\overline{\text{STDBY}}$, only if it is currently idle and the PLL is stable. While in the Standby state, output signals are forced to float (with suitable pull-ups or pull-downs, as described in Table 22). The external DRAM is not refreshed, so its contents are lost. In this state the ZR36100 consumes a minimum amount of power.

After the de-activation of $\overline{\text{STDBY}}$, a cold reset is required before the ZR36100 can be operated.

If $\overline{\text{RESET}}$ and $\overline{\text{STDBY}}$ are both active, the ZR36100 consumes more than the specified standby power. Note that for the device to recover correctly from this condition, $\overline{\text{RESET}}$ must be activated after $\overline{\text{STDBY}}$ is activated, and must be deactivated before $\overline{\text{STDBY}}$ is deactivated.

Signal States Under Standby and Reset Conditions

Table 22 shows the states of output and bidirectional signal pins under the following conditions:

- Standby, when $\overline{\text{STDBY}}$ is active and $\overline{\text{RESET}}$ is inactive,
- Cold Reset, starting with deactivation of $\overline{\text{RESET}}$ and ending at most 5000 GCLK periods after its deactivation, when the PLL is locked,
- Standby with reset, when $\overline{\text{RESET}}$ and $\overline{\text{STDBY}}$ are both active,
- After a cold reset, when the PLL is locked and READY is active.

.

Table 22. Output and Bidirectional Signal States Under Standby and Reset Conditions [1] [2] [3]

Name	Type O: output B: Bidirectional	Standby	Cold Reset	Standby + Reset	After Cold Reset
IDLE	O	floating+weak pullup	unknown	floating	high
VIDOUT	O	floating+weak pulldown	floating +weak pulldown	floating	floating +weak pulldown
QCLK_V	O	floating+weak pulldown	unknown	floating	VCLK/4
HSYNC	B	floating+weak pullup	unknown	floating	input
VSYNC	B	floating+weak pullup	unknown	floating	input
FI_EN	B	floating+weak pullup	unknown	floating	input
BUSDAT	B	floating +weak pulldown	floating +weak pulldown	floating	input (while $\overline{\text{BUSCS}}$ is high)
DREQ	O	floating+weak pulldown	unknown	floating	low
READY	O	floating+weak pulldown	unknown	floating	high
RAMDAT	B	floating +weak pulldown	floating +weak pulldown	floating	input
RAMADD	O	floating +weak pulldown	floating +weak pulldown	floating	unknown
$\overline{\text{RAS}}$	O	floating+weak pullup	unknown	floating	high
$\overline{\text{CAS}}$	O	floating+weak pullup	unknown	floating	high
$\overline{\text{WE}}$	O	floating+weak pullup	unknown	floating	high
SP1DAT	O	floating +weak pulldown	floating +weak pulldown	floating	low
SP1CMD	O	floating +weak pulldown	floating +weak pulldown	floating	low
SP1CLK	B	input + internal pullup	unknown	floating	input
SP1FRM	O	floating+weak pulldown	floating +weak pulldown	floating	low
SP2DAT	O	floating +weak pulldown	floating +weak pulldown	floating	low
SP2CLK	B	input + internal pullup	unknown	floating	input
SP2FRM	O	floating+weak pulldown	floating +weak pulldown	floating	low

1. A weak pullup is implemented as a weakly conducting P channel transistor. Pullup current is less than 70 microamps.
2. A weak pulldown is implemented as a weakly conducting N channel transistor. Pulldown current is less than 70 microamps.
3. An internal pullup is used only to prevent excessive current consumption when an input pin is disabled. Leakage current from this pullup or pulldown is not measured at the input pin. All input-only pins have internal pullups or pulldowns in Standby.

The reason for the "unknowns" in the Cold Reset column is that the internal processing clock (the output of the PLL) is disabled as soon as the cold reset state begins (160 GCLKs after $\overline{\text{RESET}}$ is activated), so it is uncertain whether these signals are able to attain the states prescribed by the internal cold reset logic. After cold reset (after $\overline{\text{RESET}}$ is deactivated and the PLL is locked), the signals will be in the states shown in the After Cold Reset column. Note, however, that if a bidirectional signal is already defined as an input at the time cold reset begins, it will remain an input.

INITIALIZATION

Before it can start decoding an MPEG bitstream, the ZR36100 must be initialized by loading the microcode and set-up parameters. Microcode is provided in three parts: the first part consists of 3064 bytes, the second of 2048 bytes, and the third of 2048 bytes. The first and third parts each have more than one variant, to support different bitstream types or applications.

A complete initialization is required in the following circumstances:

- After power-up,
- When the first part of the microcode must be changed,
- Whenever a cold reset is performed for any reason.

When only the set-up parameters and/or the third part of the microcode must be changed, a partial re-initialization suffices, as described below.

A complete initialization procedure begins with a cold reset of the ZR36100, and continues in the following sequence:

1. When the cold reset ends and the PLL is locked, the READY signal and the READY status bit go active. The host must wait for this before proceeding with the initialization. Note that the host bus is in its default configuration after cold reset: 8-bit bus width, BSLN=16, programmed-I/O bitstream transfer.

2. When READY is active, the host can load the first part of the microcode. This is done by writing the 3064 bytes to address 10. There is no need to recheck the READY signal at any time during the load, so the microcode can be loaded in a single burst if so desired.

3. Following the loading of the first part of the microcode, the TEST2 status bit can be read. If it is 1, the microcode load was successful and initialization can continue. If it is 0, the load failed, and the initialization procedure must be restarted with a cold reset (the only way to restore the state of the test bit to 1).

4. The host then loads the second part of the microcode by writing the 2048 bytes to address 11. The state of READY is not relevant for this microcode load.

5. Following the loading of the second part of the microcode, the TEST1 status bit can be read. If it is 1, the load was successful. If it is 0, the load failed, and the initialization procedure must be restarted with a cold reset.

6. After loading the second part of the microcode, the host must load the set-up parameters (the complete set of 128 bytes). This is done using writes to address 00. The data must be transferred to the ZR36100 in bursts of at most BSLN writes; prior to each burst, the host must check that the READY status bit or the READY signal line is active. Note that if the set-up parameters define a change of the host bus configuration, this change takes effect only *after* the next Go on-line command; the initialization continues with the prevailing host bus configuration. Other interface signal changes affected by the set-up parameters take effect soon after the parameters are loaded.

7. As the final step in the initialization, the host loads the third part of the microcode by writing the 2048 bytes to address 11. The host must wait until READY is active before starting this microcode load, but after that READY and BSLN are irrelevant and the microcode can be loaded in a single burst. The TEST1 status bit is also an indication of correct loading of the third part of the microcode, exactly as for the second part.

If it is necessary to change only the setup parameters or the third part of the microcode, a cold reset is not required. Only a partial re-initialization, consisting of reloading the second part of the microcode, loading the set-up parameters (all 128 bytes), and loading the third part of the microcode, must be performed. The partial re-initialization uses the prevailing host bus configuration (bus width, byte order and BSLN). Before starting a partial re-initialization, IDLE and READY must be active; subsequently the sequence can proceed according to stages 4 - 7 above.

Note: After the set-up parameters are loaded, the display always reverts to the background color.

PLAYBACK OPERATION

This section describes how the ZR36100 operates after it has been initialized (as described in the *Initialization* section). It covers the behavior of the device in response to each of the on-line commands mentioned in the *On-Line Commands* section.

General principles

Decoding and display of the video, and consumption of the MPEG bitstream, are tightly synchronized to VSYNC, the vertical sync signal, in the following way.

In the simplest case, the picture rate defined in the bitstream is the same as the video output frame rate defined by VSYNC; for example, a 29.97 pictures-per-second bitstream with 29.97 frames per second NTSC display, or a 25 pictures-per-second bitstream with 25 frames per second PAL display. Every video frame, a new decoded picture is read out from the DRAM and displayed. This effectively determines that the picture decoding rate must be the same as the display frame rate, since a new picture must be ready to be displayed at the beginning of every frame. (If the video interface is configured for progressive SIF-size, a frame begins every VSYNC; if it is configured for interlaced CCIR-size, a frame begins every second VSYNC.) This rate of picture decoding in turn ensures that the bitstream will, on the average, be consumed at its nominal bit rate. This is illustrated in Figure 29, where the marks on the time lines indicate the decoding and display start times.

As indicated in the figure, because of the presence of B-pictures requiring prediction from both an earlier and a later reference frame, the order in which the pictures are encoded in the bitstream is not the same as the display order. A typical display order is $I_1B_1B_2P_1B_3B_4P_2$..., and the corresponding decoding order is $I_1P_1B_1B_2P_2B_3B_4$.... (The picture indices here and in the figure have no meaning and are for illustration only.) Thus, I- and P-pictures must be completely buffered in DRAM before they are displayed whereas B-pictures do not need to be. The ZR36100 starts to display a B-picture soon after starting to decode it, I-pictures and P-pictures are displayed at intervals after decoding that depend on the arrangement of encoded pictures.
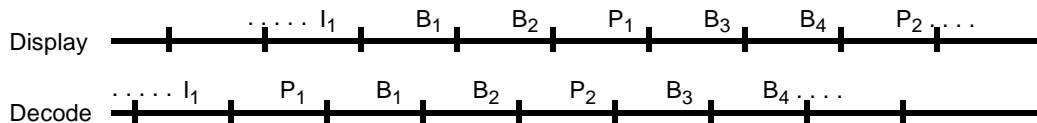
.

Figure 29. Decoding and Display

When playing back a bitstream in which the picture rate is not the same as the display frame rate, the ZR36100 can exactly compensate for the difference, for the common picture rates, with standard NTSC or PAL display frame rates (to do this, it must be configured as described in the *Set-up Parameters* section). Consequently, the correct relationships of display, decoding and bitstream consumption rates are preserved, on the average.

In the interests of clarity, all the illustrations in this section assume that the display frame rate is equal to the bitstream picture rate.

While normal playback is in progress, the on-line command queue is checked at every decoding start time, and if there is a pending command, it is executed immediately. While execution of a command is in progress, the queue is checked only when the command has completed execution, or for certain commands at other times, as indicated below.

Bitstream Buffering

When decoding a system multiplexed bitstream, the ZR36100 demulitiplexes the video and audio or private packet data, and stores these in separate buffers in the DRAM. It requests the bitstream, by activating DREQ (in DMA transfer mode) or READY (in I/O transfer mode), as long as none of these buffers is full. If one of the buffers is full, the ZR36100 stops requesting data until space becomes available in the buffer. It is the responsibility of the host I/O or DMA controller to ensure that the video and audio buffers never underflow, by ensuring that the bitstream is transferred at the required rate; no indication of an underflow condition is provided.

In case the bitstream is provided to the ZR36100 at a constant rate which is exactly equal to the encoded bit rate, the VSYNC frequency should be locked to the bit rate, otherwise the buffers may overflow or underflow.

In the case of a video-only bitstream, no demultiplexing takes place and the entire bitstream is stored in the buffer. Otherwise, the bistream request mechanism, and the requirement to avoid buffer underflow, are similar to the above.

Note that an on-line command, such as Freeze, that causes playback to pause, does not necessarily cause the ZR36100 to stop requesting the bitstream immediately, but only when one of the buffers fills up.

For system multiplexed bitstreams, the audio and private bitstreams are mapped to serial ports 1 and 2 as determined by the S1BS and S2BS bits in the SP1MODE and SP2MODE parameters respectively. The ZR36100 will only buffer, decode and output a stream on a serial port if the Serial Port Active bit (S1AC or S2AC as appropriate) is set for that port. Otherwise, the audio and/or private data packets will be discarded. When decoding a video only bitstream, both serial ports must be disabled by zeroing S1AC and S2AC.

The Go command and playback start-up

The Go on-line command signals the ZR36100 to commence playback of an MPEG bitstream. It is legal only when the device is idle, as indicated by the IDLE pin and status bit being active, and is the only valid command in the idle state. (The ZR36100 is in the idle state after a complete or partial initialization. It goes idle after decoding the end of an MPEG sequence, and after playback was aborted by the End Decoding command.)

Immediately after the Go command, the ZR36100 enters a start-up phase. The start-up procedure depends on the type of bitstream, and whether serial port output is enabled or not, but in all cases it begins with a search for a suitable start-up point; all data from the bitstream entry point (the first byte transferred after the Go command) to the start-up point is discarded. In the case of a system bitstream with video and audio streams, and an active serial port, the procedure includes the synchronization of the video with the audio.

Video-only bitstream

In the case of a video-only bitstream, a valid start-up point is a sequence header. The horizontal and vertical sizes, picture rate and quantizer matrices are extracted from the sequence header and stored for use in the decoding. Decoding and display commence at the first I-picture after the sequence header.

If the entry point is not at the beginning of the bitstream, as in a random access or seek, the valid start-up point is the first I-picture after the entry point. In this case, however, the pictures will be decoded correctly only if the sequence header parameters stored from the previous sequence header, and in particular the quantizer matrices, are still valid. If they are not, a mechanism which makes use of a special start code is provided to allow them to be specified by the host software. To make use of this feature, the following 144 bytes of data must be transferred to the ZR36100, before the first bitstream data byte:

Description	Size of data
000001FA	4 bytes
000001FA	4 bytes
intra_quantizer_matrix	64 bytes
non_intra_quantizer_matrix	64 bytes
horizontal_size	12 bits
vertical_size	12 bits
picture_rate	1 byte
reserved	4 bytes

The reserved bytes must be 0. All data from the entry point until the valid start-up point is discarded by the ZR36100.

System bitstream

In the case of a system bitstream, a suitable start-up point is a pack start code. All data is discarded until a pack start code is encountered, that satisfies the following stipulations:

■ the pack defined by the pack start code contains a video packet with a stream that is designated to be decoded, or an audio packet

with a stream that is designated to be output from a serial port (or a private-1 packet; "audio" in this description should be understood to mean audio or private-1)

- the specified video or audio packet contains a PTS

The streams are designated for decoding or serial output by means of the stream selection set-up parameters, as described in the *Set-up Parameters* section. In the terminology used here, the SCR of the pack header associated with the pack start code is called the "initial SCR." The PTSs of the first video packet containing a PTS, and the first audio packet containing a PTS, are called the "initial video PTS" and "initial audio PTS" respectively. For correct operation, the difference between each of the initial PTSs and the initial SCR must be smaller than 0.72 seconds.

Video decoding and display commence with the first I-picture after the start-up point. If the first picture after the start-up point was not an I-picture (this may occur at a random-access entry point), video display is nevertheless enabled soon after the start-up point is identified, and the last available reference picture (from a previously decoded video sequence) is displayed until the first I-picture is available.

If the stored sequence header parameters are not valid at the entry point, and there is no sequence header between the entry point and the first I-picture, the same mechanism as described for video-only bitstream can be used to provide the correct parameters.

Note: After the Go command, on-line commands should be held off until serial port output has started, unless the serial port output starts while the first picture is being decoded, otherwise the ZR36100 may operate incorrectly.

Once proper synchronization of audio and video has been achieved as described above, video decoding and serial port output proceed in lock-step, provided that the serial port bit rate parameter SP1BR or SP2BR is set to the correct value. Whenever there is a pause in playback as a result of an on-line command being executed, serial port output is paused and restarted in step with the pausing and restarting of the video decoding, and synchronization is maintained.

Audio-only bitstream

In the case of an audio-only bitstream, there is no parsing or decoding of the bitstream by the ZR36100. Whatever data is transferred by the host is buffered in the audio bitstream buffer, and shortly after data is first available in the buffer, serial port output commences.

The End Decoding command and playback termination

In the absence of on-line commands, normal playback continues until the bitstream ends. Video decoding terminates when the last picture has been decoded and the sequence_end_code is decoded, serial port output stops when there is no more data to be output. The ZR36100 stops requesting a system bitstream when the iso_11172_end_code is decoded, and a video-only bitstream when the sequence_end_code is decoded. The IDLE signal and status register bit are activated after the last picture has been decoded and all decoded pictures have been displayed, and all serial data has been output. After IDLE has been activated, the ZR36100 continuously displays the last picture or the background color, as determined by the LPIC bit of the SYSMODE set-up parameter.

Since no termination code is present in an audio-only bitstream, the ZR36100 must be put into the idle state by means of an End Decoding command.

The above behavior in response to the end codes applies equally when they are encountered while the ZR36100 is in the process of executing an on-line command.

The End Decoding command is used when it is desired to pre-emptively terminate playback and put the ZR36100 into the idle state. When executing the End Decoding command, the ZR36100 terminates decoding immediately, and activates IDLE after displaying all the pictures that were decoded up to this point. After IDLE has been activated, it continuously displays the last picture or the back-

ground color, as determined by a field in the command code (described in the *On-Line Commands* section). This is illustrated in Figure 30, where a Freeze command and an End Decoding command are shown being executed at consecutive decoding start times.
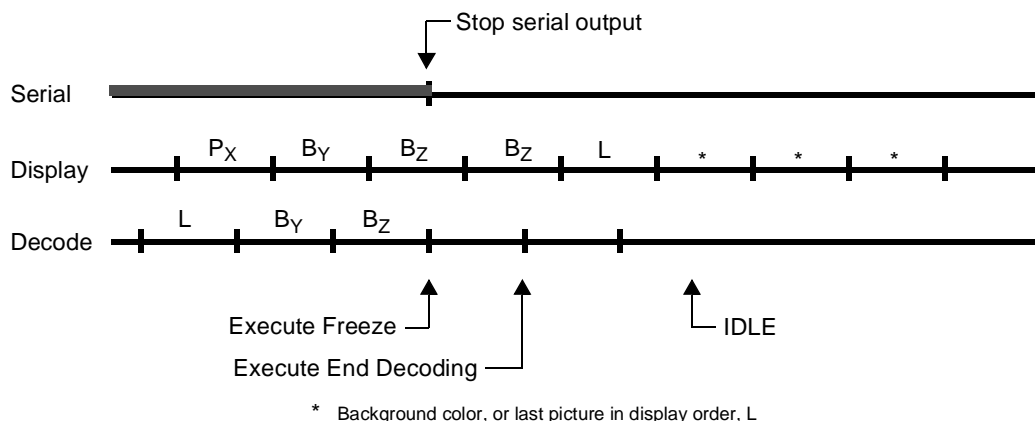

* Background color, or last picture in display order, L

Figure 30. End Decoding

Note: After a sequence_end_code is decoded and decoding is terminated, the only on-line command allowed to be still pending in the command queue is End Decoding. If there is any other command in the queue, the ZR36100 will not start up correctly after the next Go command. If this restriction cannot be formally guaranteed, it is recommended to apply a warm reset before the Go command, to flush the queue.

The Freeze, Single Step and Continue commands

The behavior of the ZR36100 when executing these commands is relatively self-explanatory. Figure 31 is an example, showing a Freeze command, followed by two Single Steps and a Continue. The Freeze command is assumed to be given when the command FIFO is empty, hence it is executed at the next decoding start time. The Single Step and Continue commands are entered in rapid succession, and are executed as shown.
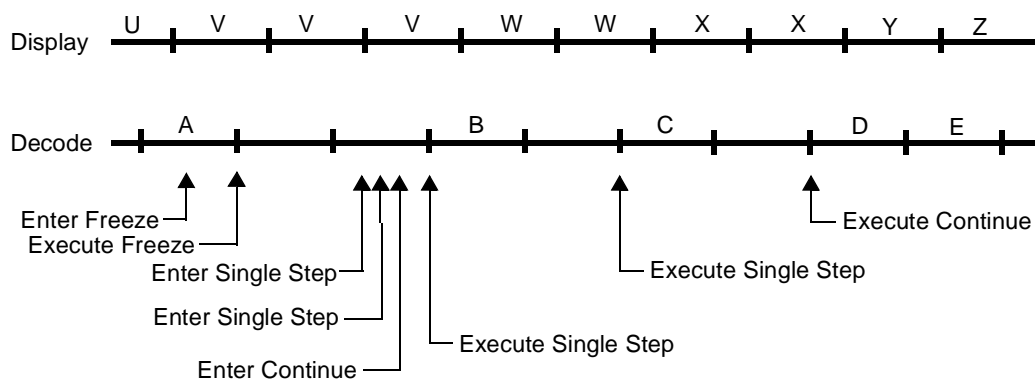

Figure 31. Freeze, Single Step and Continue

The Decode-to-First-I-Picture command

The Decode-to-First-I-Picture command is entered when the ZR36100 is in normal playback mode, as illustrated in Figure 32. The ZR36100 continues decoding and displaying pictures until the next I-picture is displayed, regardless of the type of picture being displayed when the command was executed. It then pauses playback, and is ready to execute another command.
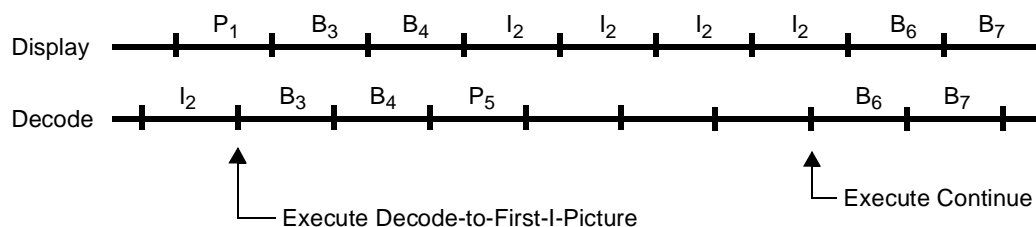

Figure 32. Decode-to-First-I-Picture

The Decode-to-Next-I-Picture command

The Decode-to-Next-I-Picture command performs a step to the next I-picture, while the currently displayed picture (the previous I-picture) remains unchanged. The display changes only when the new I-picture is displayed, as Figure 33 shows. In this example, it is assumed that the Decode-to-Next-I-Picture command was entered in place of the Continue command of the previous example.
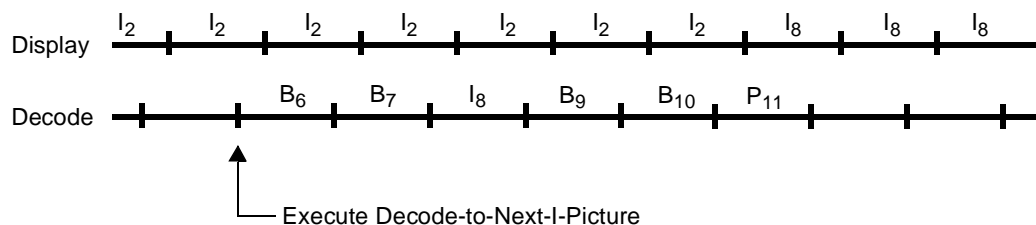
Figure 33. Decode-to-Next-I-Picture

The Slow Motion command

Execution of the Slow Motion command is a repeating sequence, each element of which entails decoding a single picture followed by a pause for the appropriate number of frame times. Slow Motion is anomalous in that it does not have a definite duration of execution like the other on-line commands. Consequently, whenever playback is paused, the command queue is checked at every scheduled decoding time; only if there is no pending command will another iteration of the Slow Motion sequence be executed. An example of Slow Motion with slowdown factor of 3 is shown in Figure 34.
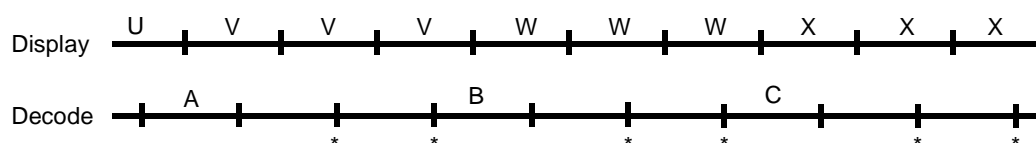
* Times at which the on-line command queue is checked for pending commands

Figure 34. Slow Motion , with slowdown factor of 3

Note: When the video interface is configured for the interlaced CCIR-size mode, and the relationship of frame rate to picture rate is such that 3/2 pulldown is performed by the ZR36100, only odd slow motion factors should be used, otherwise errors may result. This applies whenever the parameter VIDS in Table 2 has the value 0.

HIGH RESOLUTION STILL IMAGES

For decoding of high-resolution still image sequences, the ZR36100 must be configured as follows:

■ Bit VSTL of the SYSMODE parameter is 1
■ The video interface is configured for the interlaced CCIR-size mode, that is, the VSIZ bit of the VIDMODE parameter is 0
■ Frame rate conversion can not be used (the set-up parameters must not be programmed for frame rate conversion)

A suitable bitstream is a video-only sequence of pictures, in which each pair of pictures can be interlaced to double the effective vertical resolution.

After the Go command, the first pair of pictures are decoded and displayed, and playback is paused. The vbv_delay must be long enough to ensure that all the code of the two pictures is in the video buffer before decoding starts. A Single Step command advances to the next pair of pictures, and an End Decoding command can be used to terminate the sequence. None of the other on-line commands are supported.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ....-65°C to +150°C
Supply Voltage .... -0.5V to +7.0V
DC Voltage Applied to outputs in high impedance output state ....-0.5V to VCC + 0.5V
DC Input Voltage ....-0.5V to VCC + 0.5V
DC Output Current, into outputs ....20mA/output, max 200mA
DC Input Current... -30mA to +5.0mA

Stresses above the values listed may cause permanent device failure.

OPERATING RANGE

Ambient Temperature..0°C < Ta < 70°C

Supply Voltage   4.75V < VCC< 5.25V

DC CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage				
	GCLK and VCLK	2.2	Vcc + 0.5	V	
	All other inputs	2.0	Vcc + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA
I_{CC}	Power Supply Current		440	mA	@13.5 MHz, 5V, $\overline{MB4}$=0
I_{SC}	Standby Current		50	mA	
I_{LI}	Input Leakage Current		±10	uA	0 < V_{IN} < Vcc
I_{LP}	Pull down Leakage Current		50	uA	0 < V_{IN} < Vcc
I_{LO}	Output Leakage Current		±10	uA	0 < V_{OUT} < Vcc
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O and Output Capacitance		10	pF	

AC CHARACTERISTICS

AC Characteristics over operating range

No.	Symbol	Parameter	Min.	Max.	Units	Test Conditions
General signals						
1	T_{GCP1}	GCLK Period ($\overline{MB4}$ low)	1000 / 14.75	1000 / 13.50	nsec	
1	T_{GCP2}	GCLK Period ($\overline{MB4}$ high)	1000 / 13.11	1000 / 12.00	nsec	
2	T_{GCH}	GCLK High	40	60	%	@2.0V
3	T_{GCL}	GCLK Low	40	60	%	@0.8V
4	T_{GCR}	GCLK Rise		3	nsec	0.8V to 2.0V
5	T_{GCF}	GCLK Fall		3	nsec	2.0V to 0.8V
6	T_{WRW}	"Warm" Reset Width	$32 * T_{GCP}$	$128 * T_{GCP}$	nsec	
7	T_{CRW}	"Cold" Reset Width	$160 * T_{GCP}$		nsec	
Video interface signals						
13	T_{VCP}	VCLK Period	1000 / 14.75	2000	nsec	
14	T_{VCH}	VCLK High	25		nsec	@2.0V
15	T_{VCL}	VCLK Low	25		nsec	@0.8V
16	T_{VCR}	VCLK Rise		3	nsec	0.8V to 2.0V
17	T_{VCF}	VCLK Fall		3	nsec	2.0V to 0.8V
18	T_{ISV}	Input setup	15		nsec	
19	T_{IHV}	Input Hold	0		nsec	
20	T_{ODV}	Output Delay	6	20	nsec	C_L = 50PF
Serial Port interface signals						
21	T_{SCP}	SPiCLK Period	280	2,000,000	nsec	
22	T_{SCH}	SPiCLK High	100		nsec	@2.0V
23	T_{SCL}	SPiCLK Low	100		nsec	@0.8V
24	T_{SCR}	SPiCLK Rise		5	nsec	0.8V to 2.0V
25	T_{SCF}	SPiCLK Fall		5	nsec	2.0V to 0.8V
28	T_{ODS}	Output Delay	8	50	nsec	C_L = 50PF
DRAM interface signals						
29	T_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay	(3*PCLK)-2 see note 2		nsec	
30	T_{CAS}	$\overline{CAS}$ pulse width	2*PCLK	10000	nsec	
31	T_{CP}	$\overline{CAS}$ precharge time	PCLK-4		nsec	
32	T_{RP}	$\overline{RAS}$ precharge time	(4*PCLK)-7		nsec	
33	T_{ASC}	Column address setup time	PCLK-2		nsec	

No.	Symbol	Parameter	Min.	Max.	Units	Test Conditions
34	T_{CAH}	Column address hold time	PCLK		nsec	
35	T_{ASR}	Row address setup time	PCLK-2		nsec	
36	T_{RAH}	Row address hold time	PCLK		nsec	
37	T_{DS}	Data out setup time	PCLK		nsec	
38	T_{DH}	Data out hold time	PCLK		nsec	
39	T_{RAC}	Access from $\overline{RAS}$		80	nsec	
40	T_{AA}	Access from column address		40	nsec	
41	T_{RASP}	$\overline{RAS}$ pulse width	5*PCLK	10000	nsec	
42	T_{CSH}	$\overline{CAS}$ hold time	5*PCLK		nsec	
43	T_{PC}	$\overline{CAS}$ cycle time	3*PCLK		nsec	
44	T_{RSH}	$\overline{RAS}$ hold time	2*PCLK		nsec	
45	T_{AR}	Column address hold to $\overline{RAS}$	4*PCLK		nsec	
46	T_{RHCP}	$\overline{RAS}$ hold time from $\overline{CAS}$	3*PCLK		nsec	
47	T_{OFF}	Data input hold	0		nsec	
48	T_{RAD}	$\overline{RAS}$ to column add delay time	PCLK	25	nsec	
49	T_{RAL}	Column add to $\overline{RAS}$ lead time	3*PCLK		nsec	

Host bus interface signals

No.	Symbol	Parameter	Min.	Max.	Units	Test Conditions
50	T_{ISB}	Input set-up	10		nsec	
51	T_{IHB}	Input Hold	10		nsec	
52	T_{RWL}	Read/Write Low time	70		nsec	
53	T_{RWH}	Read/Write High time	PCLK+2 or 100 see note 1		nsec	
54	T_{DSB}	Data Input set-up	10		nsec	
55	T_{DHB}	Data Input Hold	5		nsec	
56	T_{DBD}	Data Bus Driven	1		nsec	$C_L = 50PF$
57	T_{DBV}	Data Bus Valid		25	nsec	$C_L = 50PF$
58	T_{DBY}	Data Bus Float Delay		5	nsec	$C_L = 50PF$
59	T_{WER}	Write to End of DREQ		50	nsec	

Video output in Enabled mode

No.	Symbol	Parameter	Min.	Max.	Units	Test Conditions
60	T_{ENS}	FI_EN setup to VCLK	20		nsec	
61	T_{VOD}	VIDOUT delay	6	20	nsec	
62	T_{VOF}	VIDOUT float	6	20	nsec	

1. The minimum value of T_{RWH} is PCLK+2ns from read to read, from write to write, or from read to write. From write to read, the minimum value of T_{RWH} is 100ns.
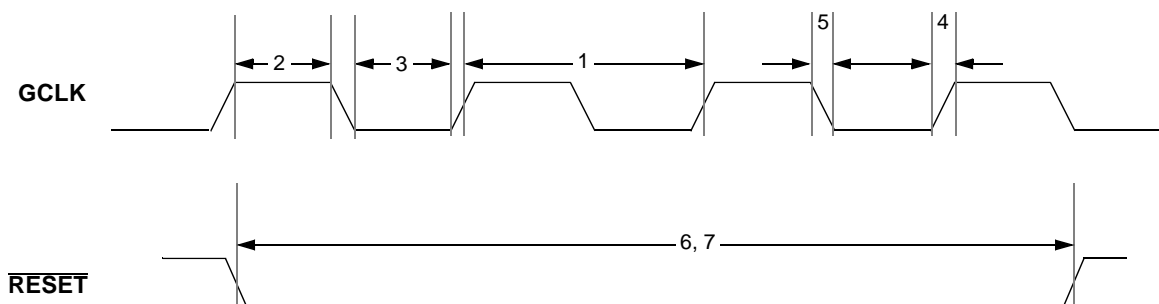2. PCLK here represents the period of the PCLK signal.

General Signals

Figure 33. GCLK and $\overline{\text{RESET}}$ timing
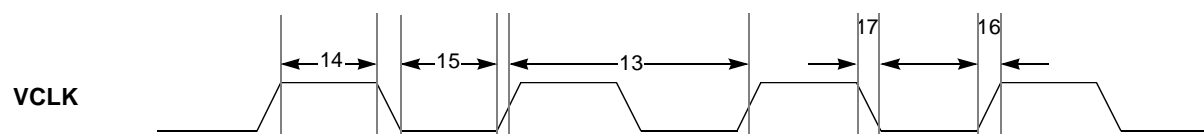
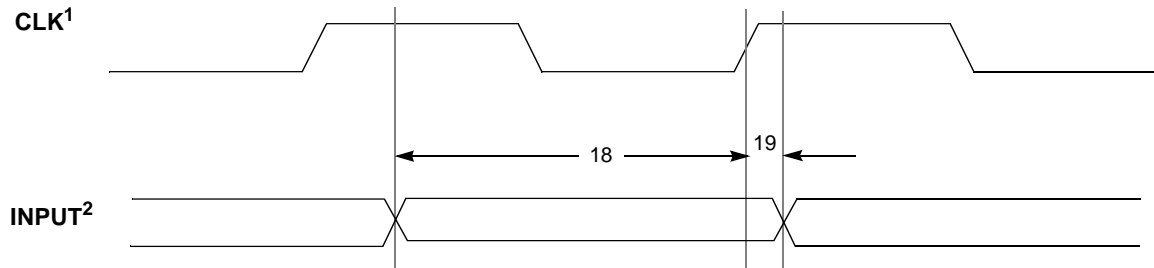**Video Signals**

Figure 34. VCLK timing

Figure 35. INPUT setup and hold timing

Note 1: VCLK (or QCLK_V if VCRS setup parameter is set)
Note 2: HSYNC, VSYNC and FI_EN; when these signals are inputs (the SDIR set-up
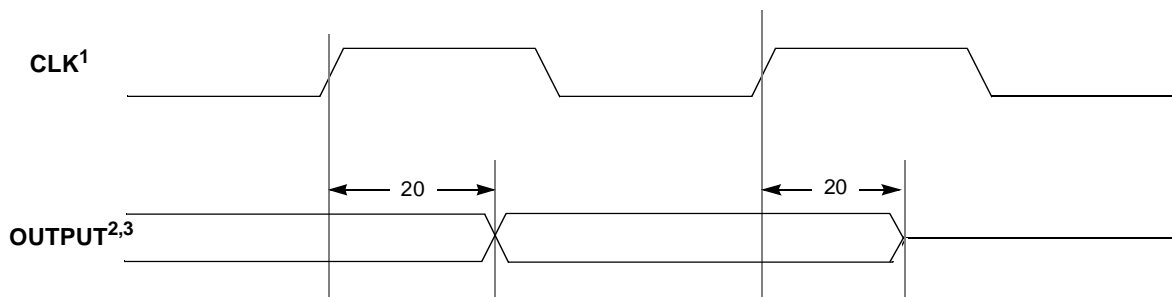parameter = 0)

Figure 36. OUTPUT delay timing

Note 1: VCLK (or QCLK if VCRS setup parameter is set)
Note 2: HSYNC, VSYNC and FI-EN; when these signals are outputs (the SDIR set-up parameter = 1)
Note 3: VIDOUT

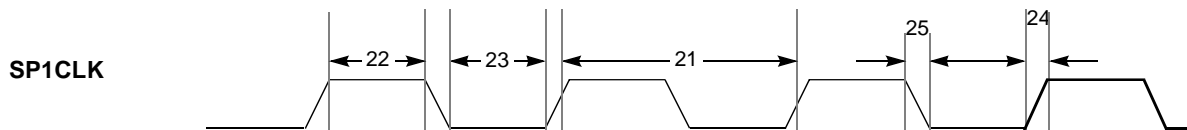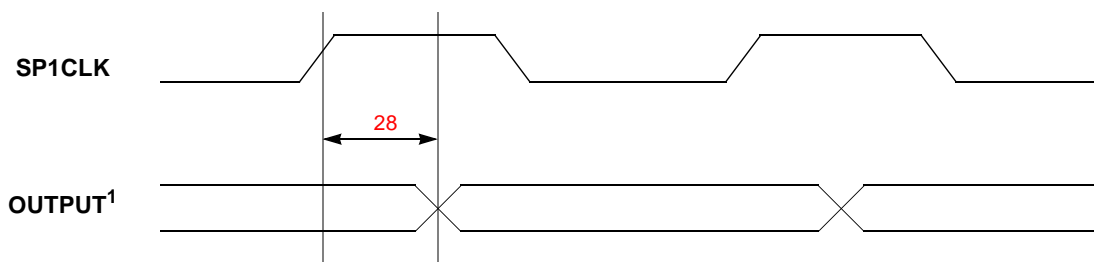## Serial Port Interface Signals

Figure 37. SP1CLK and SP2CLK timing
(SP2CLK has identical timing)

Note: Timing requirements are the same for either input or output SP1CLK

**Figure 38. Serial Port 1 timing (SP1FRM pulse mode)
(timing is identical for serial port two)**

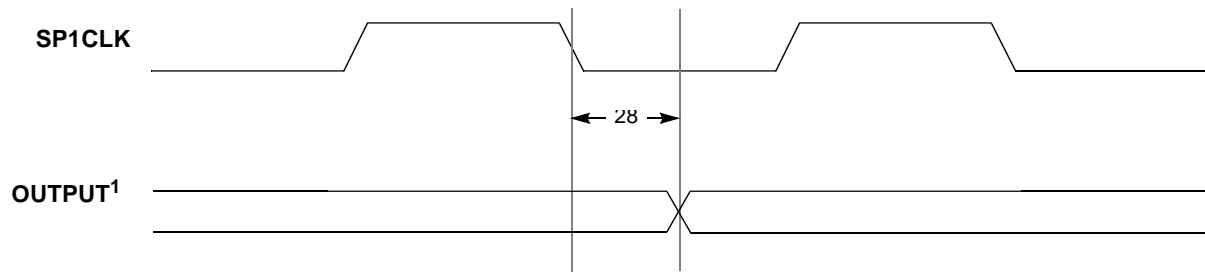Note 1: SP1FRM (pulse mode), SP1CMD,
SP1DAT

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Figure 39. Serial Port 1 timing (SP1FRM transition mode)
(Timing is identical for serial port 2)

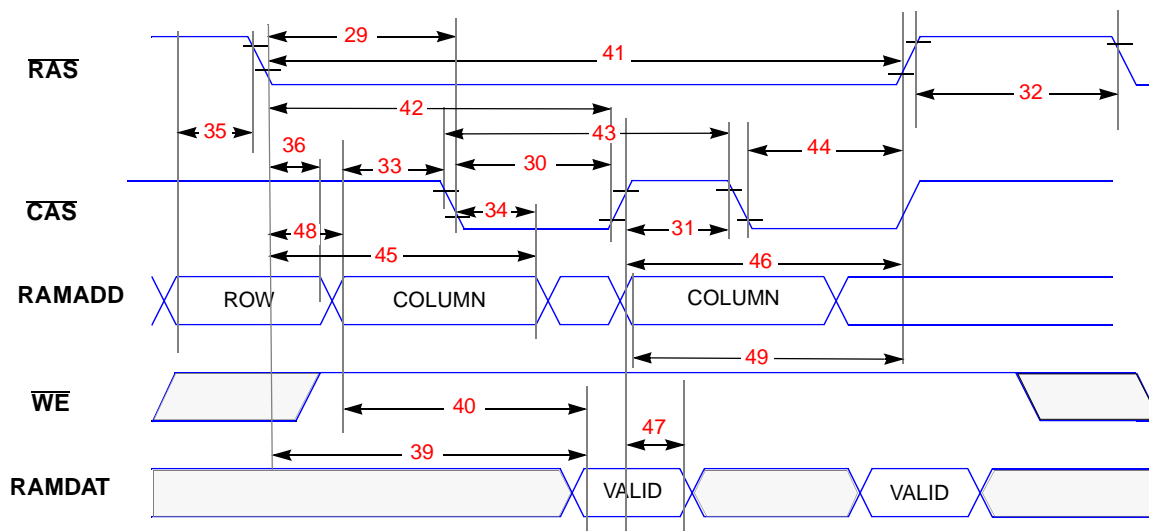Note 1: SP1FRM (pulse mode), SP1CMD, SP1DAT

DRAM Interface Signals

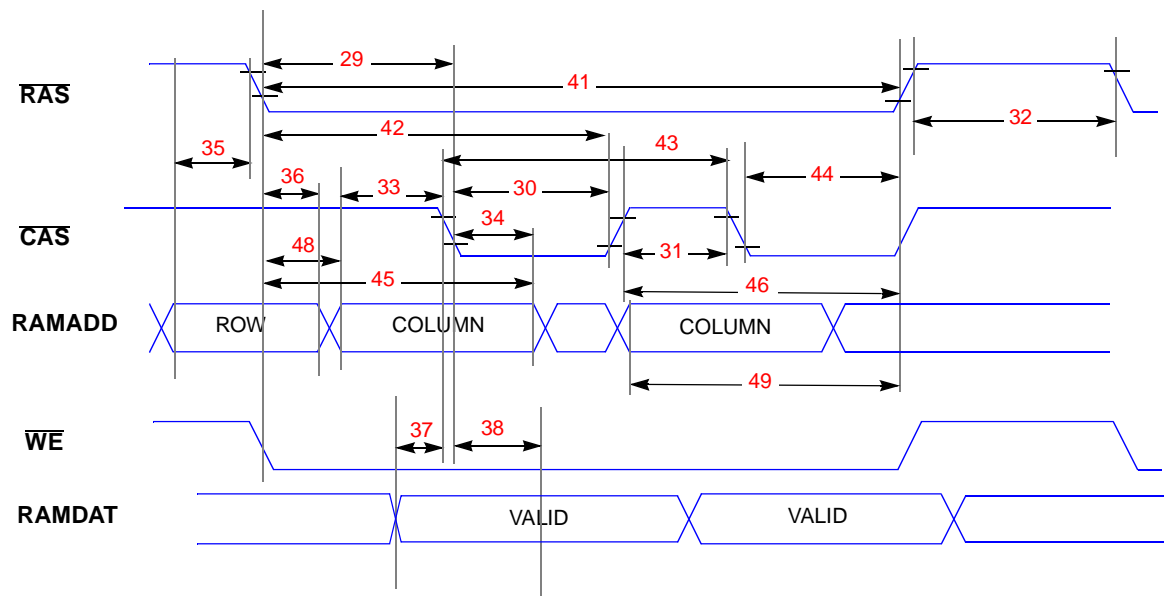**Figure 40. DRAM Fast Page Mode Read timing**

Figure 41. DRAM Fast Page Mode Write timing
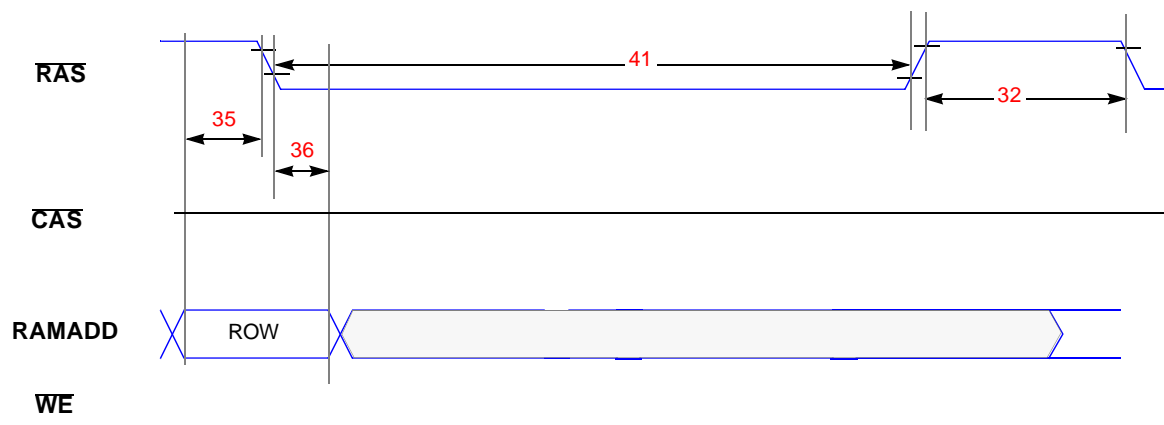
Figure 42. DRAM refresh cycle timing (RAS-only)
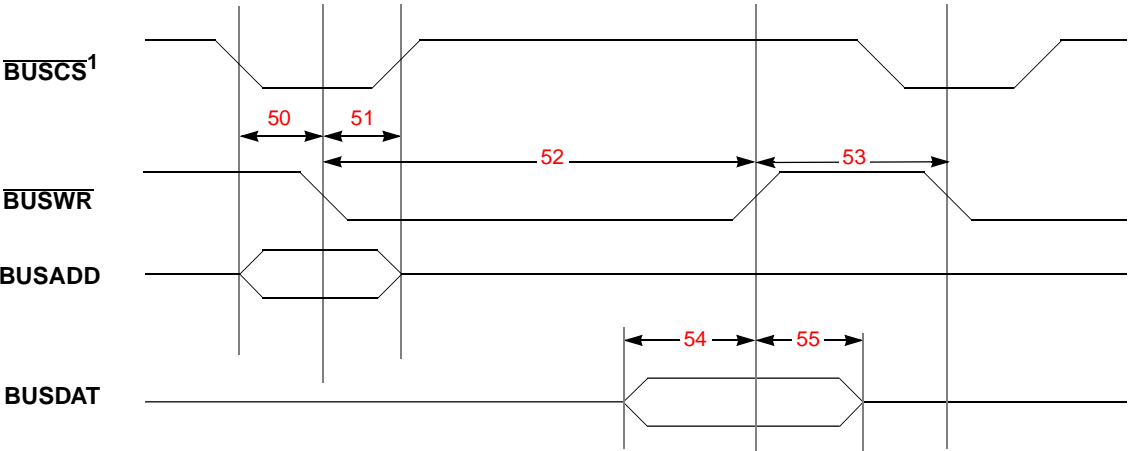
Host Bus Interface

Figure 43. I/O Write timing

Note 1: $\overline{\text{BUSCS}}$ can remain active for multiple I/O write cycles
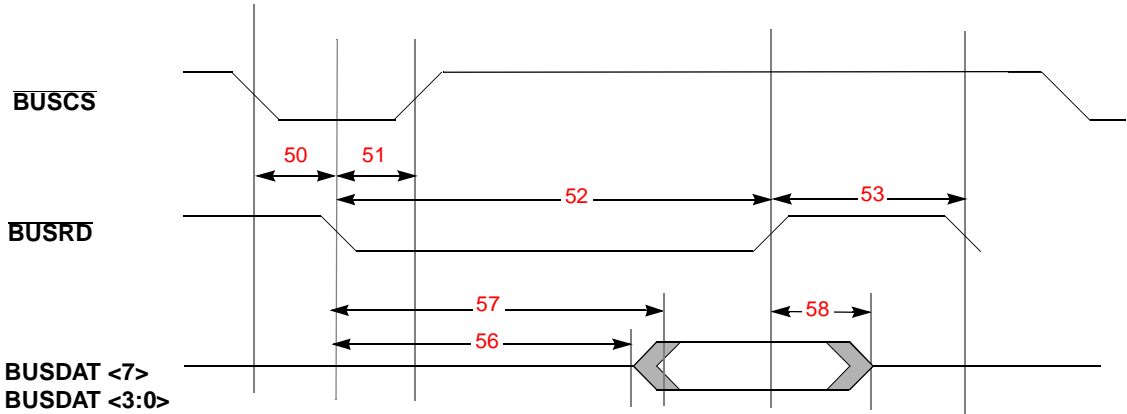

Figure 44. I/O Read timing

BUSDAT <15:8>, <6:4> remain at high Impedance
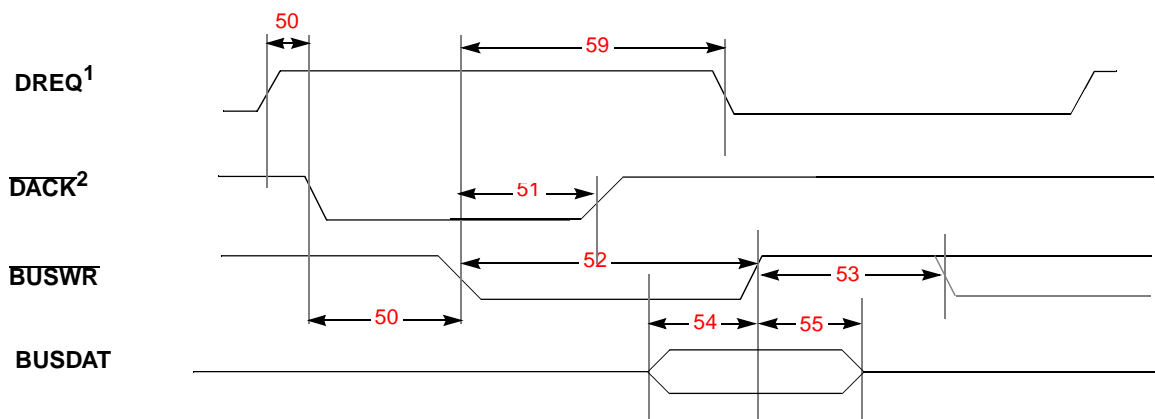
Figure 45. DMA timing (for BSLN=1)

Note 1: DREQ will remain active for BSLN transfer cycles

Note 2: DACK can remain active for BSLN transfer cycles, or can be pulsed for each transfer cycle

Video Output in Enabled Mode
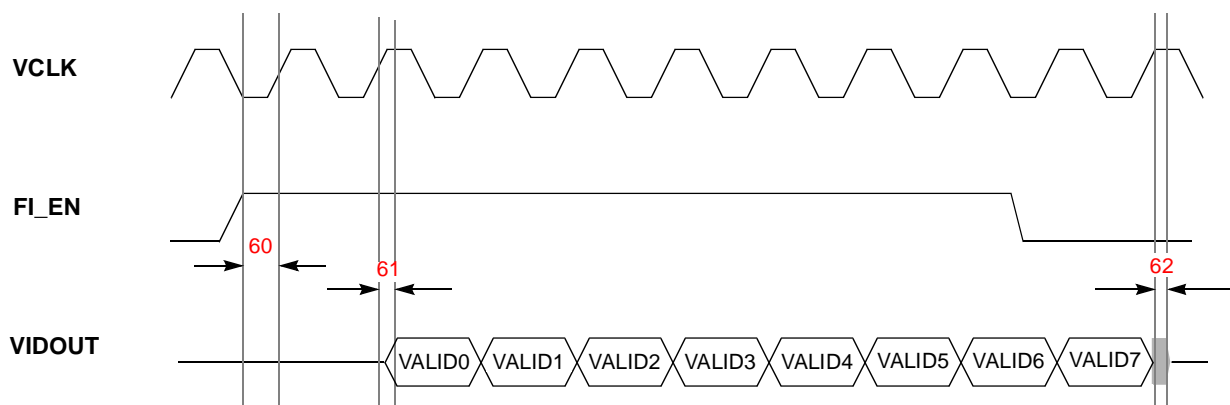
Figure 46. Video output in Enabled Mode

AC TEST CONDITIONS

During AC testing, inputs are driven at 0.4V and 2.4V levels. Input to output switching times are measured from the 1.5V level of the input to the 1.5V level at the output. Pulse widths and clock periods are measured between the 1.5V level of one output and 1.5V level of the other output.

Normal test load during AC testing is 50 pF.

Figure 47. AC Test Reference Levels

Figure 48. Normal AC Test Load

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PINOUT INFORMATION

Table 23. 128-Pin MQFP pin assignment

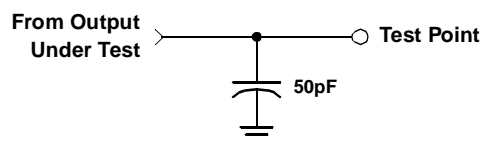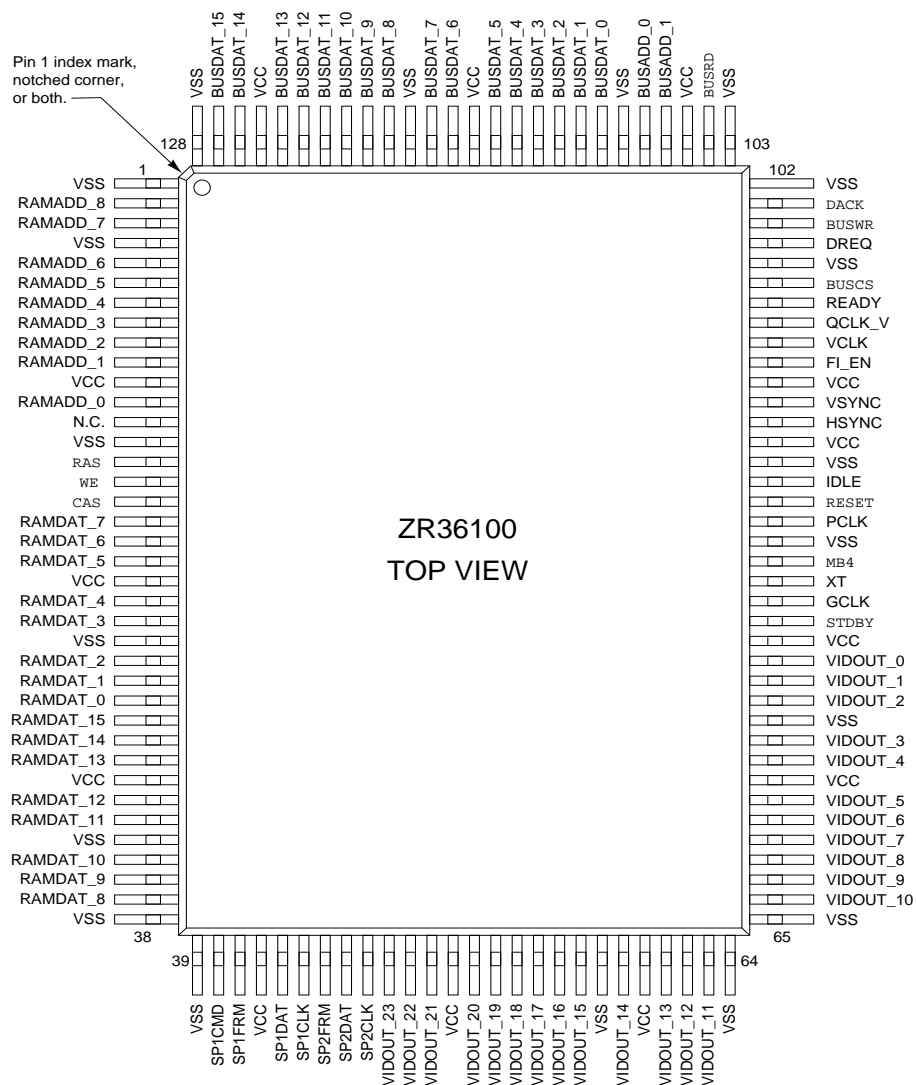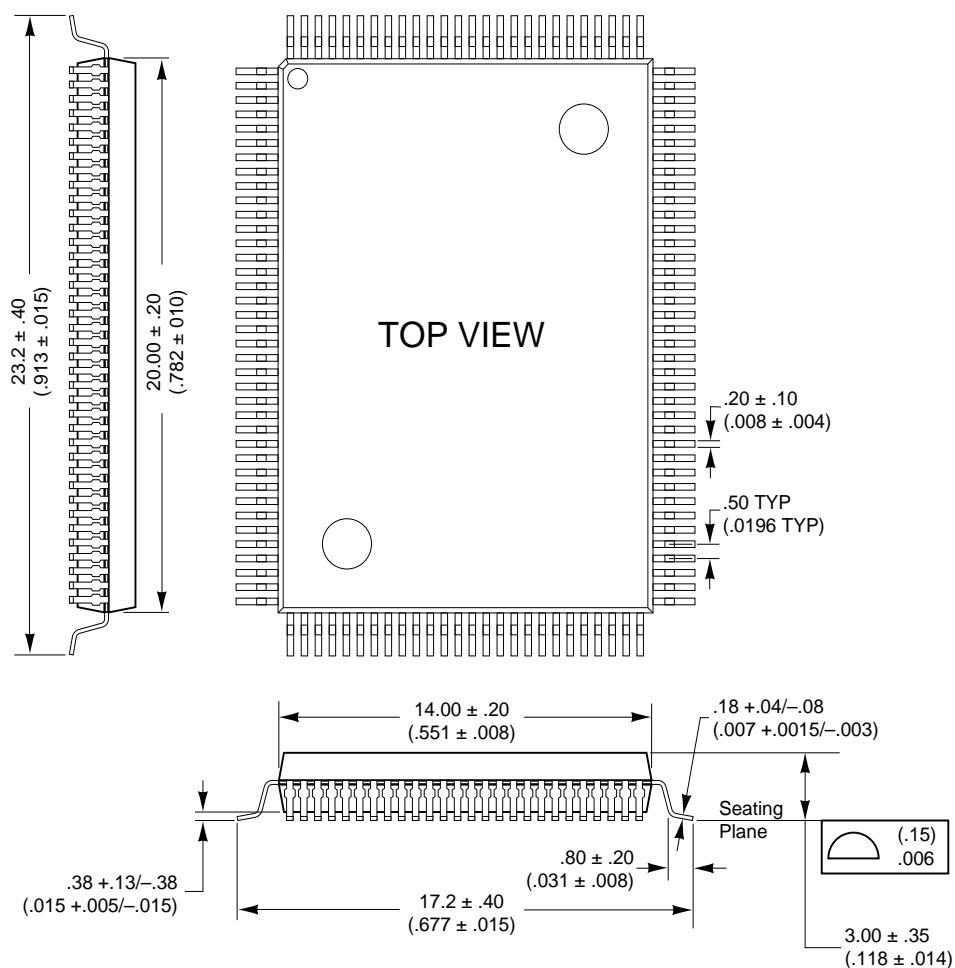| Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type
1	VSS	S	27	RAMDAT_0	B	53	VIDOUT_19	O	79	VCC	S	105	VCC	S
2	RAMADD_8	O	28	RAMDAT_15	B	54	VIDOUT_18	O	80	$\overline{\text{STDBY}}$	I	106	BUSADD_1	I
3	RAMADD_7	O	29	RAMDAT_14	B	55	VIDOUT_17	O	81	GCLK	I	107	BUSADD_0	I
4	VSS	S	30	RAMDAT_13	B	56	VIDOUT_16	O	82	XT	O	108	VSS	S
5	RAMADD_6	O	31	VCC	S	57	VIDOUT_15	O	83	$\overline{\text{MB4}}$	I	109	BUSDAT_0	I/B
6	RAMADD_5	O	32	RAMDAT_12	B	58	VSS	S	84	VSS	I	110	BUSDAT_1	I/B
7	RAMADD_4	O	33	RAMDAT_11	B	59	VIDOUT_14	O	85	PCLK	O	111	BUSDAT_2	I/B
8	RAMADD_3	O	34	VSS	S	60	VCC	S	86	$\overline{\text{RESET}}$	I	112	BUSDAT_3	I/B
9	RAMADD_2	O	35	RAMDAT_10	B	61	VIDOUT_13	O	87	IDLE	O	113	BUSDAT_4	I/B
10	RAMADD_1	O	36	RAMDAT_9	B	62	VIDOUT_12	O	88	VSS	S	114	BUSDAT_5	I/B
11	VCC	S	37	RAMDAT_8	B	63	VIDOUT_11	O	89	VCC	S	115	VCC	S
12	RAMADD_0	O	38	VSS	S	64	VSS	S	90	HSYNC	B	116	BUSDAT_6	I/B
13	N.C.	-	39	VSS	S	65	VSS	S	91	VSYNC	B	117	BUSDAT_7	I/B
14	VSS	S	40	SP1CMD	O	66	VIDOUT_10	O	92	VCC	S	118	VSS	S
15	$\overline{\text{RAS}}$	O	41	SP1FRM	O	67	VIDOUT_9	O	93	FI_EN	B	119	BUSDAT_8	I/B
16	$\overline{\text{WE}}$	O	42	VCC	S	68	VIDOUT_8	O	94	VCLK	I	120	BUSDAT_9	I/B
17	$\overline{\text{CAS}}$	O	43	SP1DAT	O	69	VIDOUT_7	O	95	QCLK_V	O	121	BUSDAT_10	I/B
18	RAMDAT_7	B	44	SP1CLK	B	70	VIDOUT_6	O	96	READY	O	122	BUSDAT_11	I/B
19	RAMDAT_6	B	45	SP2FRM	O	71	VIDOUT_5	O	97	$\overline{\text{BUSCS}}$	I	123	BUSDAT_12	I/B
20	RAMDAT_5	B	46	SP2DAT	O	72	VCC	S	98	VSS	S	124	BUSDAT_13	I/B
21	VCC	S	47	SP2CLK	B	73	VIDOUT_4	O	99	DREQ	O	125	VCC	S
22	RAMDAT_4	B	48	VIDOUT_23	O	74	VIDOUT_3	O	100	$\overline{\text{BUSWR}}$	I	126	BUSDAT_14	I/B
23	RAMDAT_3	B	49	VIDOUT_22	O	75	VSS	S	101	$\overline{\text{DACK}}$	I	127	BUSDAT_15	I/B
24	VSS	S	50	VIDOUT_21	O	76	VIDOUT_2	O	102	VSS	S	128	VSS	S
25	RAMDAT_2	B	51	VCC	S	77	VIDOUT_1	O	103	VSS	S			
26	RAMDAT_1	B	52	VIDOUT_20	O	78	VIDOUT_0	O	104	$\overline{\text{BUSRD}}$	I			

Note: I = Input, O = Output, S = Supply, B = Bidirectional

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NOTE: Pins identified as 'N.C.' must
remain completely unconnected.

PACKAGE DIMENSIONS

TOP VIEW

23.2 ± .40
(.913 ± .015)

20.00 ± .20
(.782 ± .010)

.20 ± .10
(.008 ± .004)

.50 TYP
(.0196 TYP)

14.00 ± .20
(.551 ± .008)

.18 +.04/−.08
(.007 +.0015/−.003)

Seating
Plane

.80 ± .20
(.031 ± .008)

(.15)
.006

.38 +.13/−.38
(.015 +.005/−.015)

17.2 ± .40
(.677 ± .015)

3.00 ± .35
(.118 ± .014)

NOTE: Principal dimensions in millimeters, dimensions in brackets in inches.

ZR36100

ORDERING INFORMATION

```
ZR   36100   PQ   C
```

SCREENING KEY

PACKAGE

PART NUMBER

PREFIX

PACKAGE
PQ - Plastic Quad Flat Pack

SCREENING KEY
C - 0°C to +70°C   (V_{CC} = 4.75V to 5.25V)

SALES OFFICES

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FAX: 408-986-1240

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P.O. Box 2495
Haifa, 31024 Israel
Telephone: 972-4-551-551
FAX: 972-4-551-550

APPENDIX

Some ZR36100 devices that were shipped prior to the date of this data sheet were fabricated using a mask version that caused some discrepancies from the specifications contained in the data sheet. These devices can be identified by the date codes marked on the packages. The date code is the last 5 characters of a 9 character identification code marked on the package.

The affected data codes are the following:

9429B	9430A	9431A	9433A	9437A	9438C	9440A	9442A	9443C	9448A
	9430B	9431B	9433B	9437B		9440B		9443D	9448B
	9430J		9433C	9437C		9440C		9443E	9448C
	9430K		9433D	9437D				9443F	9448D
				9437E					
				9437F					
				9437G					
				9437H					
				9437J					
				9437K					

Note that the device versions must be distinguished by their complete date codes, which have the form <year><week><serial letter>. Devices with the same year and week but different serial letter may have been fabricated from different mask versions.

The following are the discrepancies exhibited by the above devices.

Status Register

The status register does not include the OLC_RDY bit.

On-Line Commands

On-line commands can not be entered at intervals of 150 microseconds They must be entered at minimum intervals of 50 milliseconds if the output frame rate is 29.97 frames per second, or 60 milliseconds if the output frame rate is 25 frames per second. In either case, this minimum interval is equivalent to 3 VSYNC periods, with interlaced CCIR-size video interface mode.

Reset before GO or parameter change

The device must be reset before every GO command and before every change of the set-up parameters.

The cold reset which is part of a complete initialization satisfies this requirement. If no initialization or a partial initialization is performed, a warm reset is required.

Decode-To-Next-I

The Decode-to-Next-I-Picture on-line command is not supported.

Pull-up and pull-down transistors

The pull-up and pull-down resistors (implemented as weakly conducting transistors) draw a current of approximately 250 microamps, instead of 70 microamps.

Power Supply Current

The maximum power supply current is 480 mA.