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ZipWireMulti™
Octal G.shdsl Transceiver with Embedded Microprocessor

CX28985

Complete G.shdsl/HDSL2/SDSL/ HDSL/IDSL Multimode DSL Solution

The ZipWireMulti eight-port multimode DSL solution implements Mindspeed Technologies'™ LoopWizard™ technology to diagnose line problems without expensive test equipment or truck rolls (see LoopWizard xDSL Loop Diagnostic Software literature). The ZipWireMulti DSL solution goes beyond simple compliance with the ITU G.shdsl standard by supporting the optional enhanced performance asymmetrical PSD (EPAP) modes of operation.In addition, it complies with the ANSI HDSL2 standard (ANSI T1.418) and provides interoperability with Mindspeed's market-leading ZipWire™ transceivers by operating in 2B1Q multi-rate mode. The 2B1Q mode supports AutoBaud™ for SDSL interoperability, rate optimization, fast connect times and standards-based HDSL operation. The ZipWireMulti also runs in IDSL mode for interoperability with basic-rate ISDN repeaters. The solution supports Mindspeed's proprietary modes, such as 32-PAM,64 Kbps and 3.088 Mbps operation, which provide enhanced spectral compatibility, extended subscriber-line reach and high-speed operation. One hardware circuit (i.e.,one transformer, crystal and hybrid) supports all these modes, which can be configured in real time via software control.

Embedded Microprocessor

The ZipWireMulti chipset includes an embedded ARM microprocessor and a full suite of software that facilitates speedy, simplified development of systems that comply with all applicable ITU, ANSI and ETSI standards.

KEY FEATURES

- Eight-port CO solution implementing LoopWizard technology
- Multimode operation
- Low power consumption
- Highly integrated solution
- Embedded microprocessor
- Simultaneous operation ofUTOPIA Level 2 and PCM interfaces
- Interoperable with ZipWire 2B1Q transceivers including AutoBaud

The embedded microprocessor and software handle the EOC processing and many other functions often delegated to an external host controller in competing solutions. This greatly reduces software-porting effort and eliminates real-time processing requirements for an external host controller. The host controls the ZipWireMulti through a simple and well-defined software API structure while the internal ARM processor handes all real-time processing.

UTOPIA and PCM Interfaces Operate Simultaneously

The ZipWireMulti's integrated framers include full-featured UTOPIA Level 2 and PCM interfaces. The UTOPIAinterface includes ATM TC-layer processing. The DSL payload can be mapped to either interface, or split between them to enable simultaneous connections to ATM- and TDM-based systems. This feature is programmable on a per-port basis, and supports a mix of channels transporting data, data plus time slot voice, or only time slot voice.

The framer automatically extracts and inserts DSL overhead (i.e., EOC, indicator and Z-bits, CRC, sync word, etc.) and passes it to the embedded microprocessor for processing.

In addition, the framer supports all G.shdsl, HDSL2, HDSL and IDSL frame formats; EOC messaging protocols; and other non-standard SDSL frame formats. For non-framed protocols, the ZipWireMulti supports a framer bypass mode.

Integrated Line Driver and Frequency Synthesizer

The ZipWireMulti includes an integrated line driver and frequency synthesizer for a full DSL solution. The integrated line driver can drive the high line-power EPAPs for payload rates of 768; 1,544; 2,048; and 2,304 Kbps, in compliance with the G.shdsl standard. The frequency synthesizer, along with the rest of the ZipWireMulti, supports data rates from 64 Kbps to 3.088 Mbps, and requires only one external crystal. This highly integrated DSL solution enables OEMs to design and manufacture the most feature-rich, lowest-power, and highest-density DSL equipment in the industry.
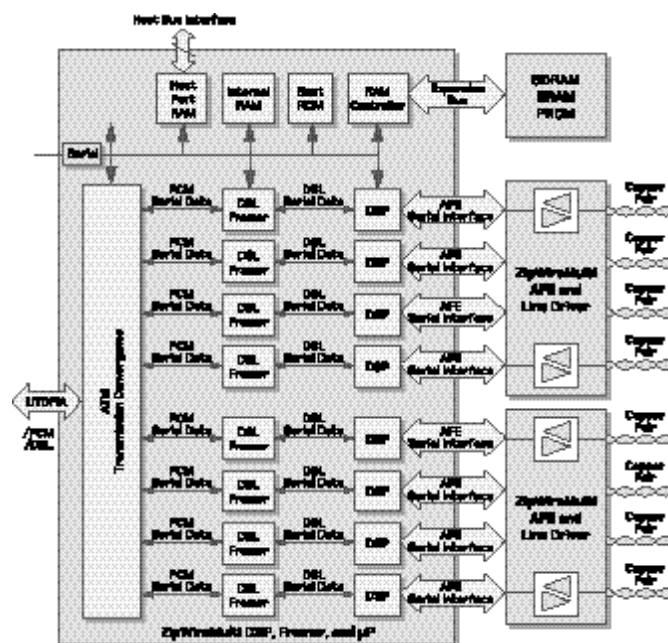
CX28985 Block Diagram

Product Highlights

- Multimode operation including ITU G.shdsl, with EPAP modes (ITU G.991.2)
- ITU G.handshake (ITU G.994.1)
- HDSL2 (ANSI T1.418)
- SDSL/2B1Q (AutoBaud)
- HDSL (ITU G.991.1, ETS 101 135 and ANSI TR-28)
- IDSL (ANSI T1.601)
- Proprietary/extended reach (ANSI spectrum management for loop transmission systems)
- Proprietary/high-speed (ANSI spectrum management for loop transmission systems)

- Low power consumption of < 1 W at 2.32 Gbps, which includes the AFE and line-driver dissipation
- Highly integrated solution includes framer, microprocessor, ROM/RAM, frequency synthesizer, DSP, AFE and line driver
- Embedded microprocessor for autonomous operation and EOC processing
- Data rates from 64 Kbps to 3.088 Mbps in 8 Kbps increments
- Interoperability with ZipWire 2B1Q transceivers, including AutoBaud
- Simultaneous operation of UTOPIA Level 2 and PCM interfaces on a per-channel basis

- Central office (COT) and remote (RT) operation
- Individual clock-recovery circuits per channel
- Fast warm startup
- Glueless interface to popular microprocessors
- Single hardware circuit supports all speeds and modes of operation
- +1.8 V, +3.3 V and +12 V power supplies
- JTAG boundary scan
- Package: 27 x 27 mm PBGA, 7 x 7 mm LGA
- Operating temperature: -40°C to +85°C

Applications

- Digital subscriber line access muxes (DSLAMs)
- DSL-enabled digital loop carriers (DLCs)
- Nx64K data transport
- Remote LAN access
- T1 and E1 HDSL-enabled transport systems
- Cellular base-station data links
- Campus modems
- Data, voice and video transport systems

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