ZEN2011P

PROGRAMMABLE UNIVERSAL COUNTER

Description

ZENIC INC. ZEN2011P is a 24 bit programmable universal counter LSI.
THE ZEN2011P counts phase-shifted signals and up/down pulse signals, generated from rotary encoders or linear scales.

Since the counter response speed is as high as 8MHz(MAX),the ZEN2011P is used in a variety of high speed services including digital servo control and precision measurement.

THE ZEN2011P is provided with a function which monitors input signals and detects any abnormal input accompanied with noise or other disturbances, so that the reliability of counted values are secured.

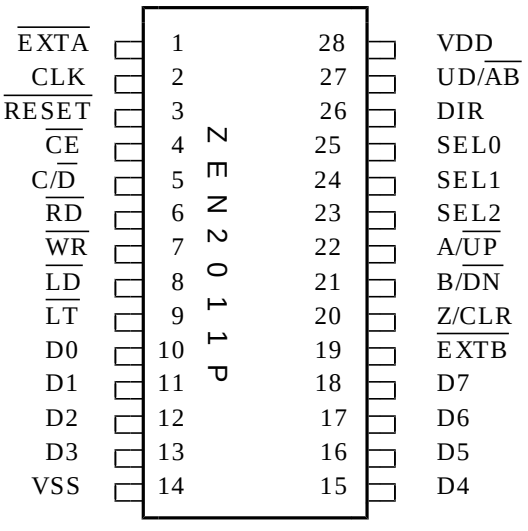
1, Features

- 24bit binary up/down counter.
- Counter response speed:
  8MHz.(MAX) (CLK f_0 = 8MHz at 50% duty)
- Input frequency of count pulse.
- Two phase-shifted pulses signal input:
  A/B phase input DC ~ 2MHz.
  (less than f_0 ÷ 1/4)
- Up/down pulse signal input:
  Up/down input DC ~ 4MHz
  (less than f_0 ÷ 1/2)
- CLK frequency DC ~ 8MHz.
  (MAX.: duty ratio 50%)
- Direction recognition for up/down count
- Abnormal input detection circuit.
- Preload register for the up/down counter.
- Latch register for the up/down counter.
- Reference value - count value coincidence detection function.
- On-chip status register.
- Counter operation mode.
  Quad/double/single edge evaluation.
  (for phase-shifted signal and single pulse)
  Count direction selection.
  Counter clear control:synchronous/asynchronous clear.
- Command mode
  Mode 0:
  1 ch. reference value - count value coincidence detection function.
  Mode 1:
  Mode 0 instruction set compatible.
  2 ch. reference value - count value coincidence detection function.
  Logical OR output of each coincidence detections available.
  Interrupt output under some conditions available.
- 8 bit data bus.
- Low power CMOS technology.
- TTL compatible.
- Single 5V power supply.
- 28 pin DIP.

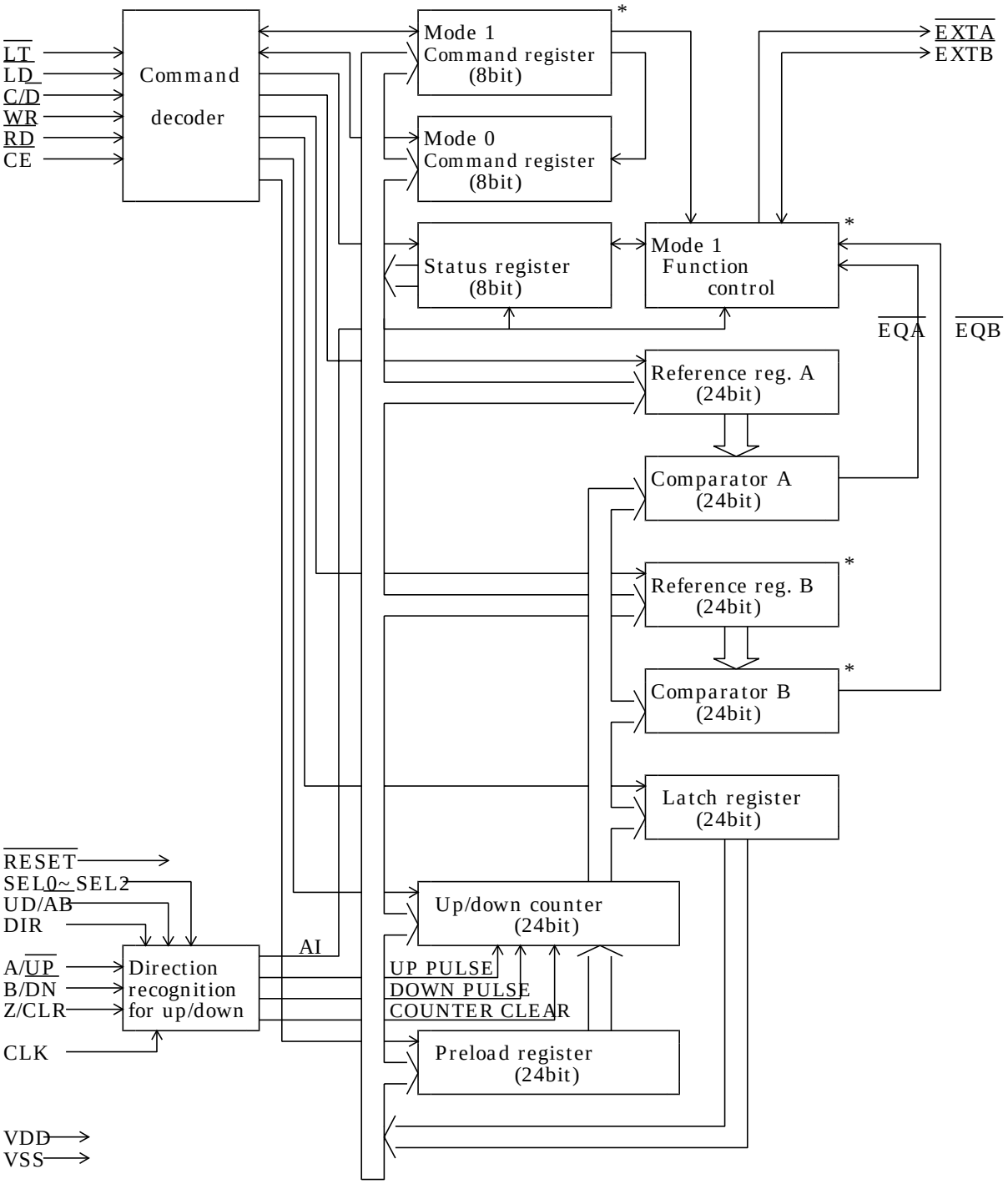
Typical Applications

- NC machine tools
- Precision positioners
- Robot arm controllers
- Speed controllers for rotating machines
- Electronic gauges
- Frequency counters

Pin configuration
(Top View)



2, Block diagram



3, Pin Description

(1)
EXTA External A(Output)
This output depends on the command mode.
In mode 0, EXTA outputs the equal signal (EQA).
In Mode 1, either of data (EQA), (EQA+EQB) or (INTEQA) is selected by the command and it is output.
Refer to "5-3 Mode 1 command format".

(2)
CLK Clock(Input:single phase clock)
The CLK serves as a clock input solely to synchronize the internal circuit operation of the ZEN2011P.

(3)
RESET Reset(Input)
The RESET initializes the up/down counter, phase discrimination circuit, command register,and status register.

(4)
CE Chip enable(Input)
A "Low" level at this input enables the ZEN2011P to accept a command or a data input from the CPU during a write cycle, or to transmit a data to the CPU during a read cycle.

(5)
C/D Command/data select(Input)
The C/D defines the type of information transfer performed between the CPU and the ZEN2011P.

(6)
RD Read strobing(Input)
The RD is a strobing signal for reading data from an internal register.

(7)
WR Write strobing(Input)
The WR is a strobing signal for writing data into an internal register.

(8)
LD Data loading to the counter*(Input)
The LD collectively transmits the data stored in the preload register to the up/down counter.

(9)
LT Count data latch*(Input)
The LT collectively stores the data of the up/down counter into the reading register.

(10~13,15~18)
D0~ Data bus(Bidirectional 3-state)
D7

(19)
EXTB External B (I/O)
The data set depending on the command is input or output.
In mode 0, EXTB is set as univarsal input terminal U and it is monitored by the status register.
In Mode 1, EXTB is set as an output terminal, either of data (EQB), (INTAI) or (INTEQB) is selected by the command and it is output.
Refer to "5-3. Mode 1 command format".

(20)
Z/CLR Counter clear*(Input)
The Z/CLR accepts reset signal which clears the up/down counter data.

(21)
B/DN Count pulse input B or DN*(Input)

(22)
A/UP Count pulse input A or UP*(Input)
The B/DN and A/UP accepts count pulse signals for the 24 bit counter.

(23~25)
SEL0~SEL2
Counter mode select(Input)
The conditions of these pins define the counter operation mode to single phase or to dual phase.
This definition is effective when UD/AB ="Low".

(26)
DIR Counter direction select(Input)
The DIR selects the count direction of the up/down counter.

(27)
UD/AB Up/down or dual phase pulse mode select (Input)
Please refer to the paragraph of "4-3. Selection of counter operation mode".

(14)
VSS Ground(0v)

(28)
VDD Supply voltage(+5v)

Note: Signals with(*)mark are sampled by CLK.
Sampled at the rising edge of CLK:
Z/CLR,B/DN,A/UP
Sampled at the failing edge of CLK:
LD,LT.

4, Operation

The operation of ZEN2011P is controlled with the system software. To use this counter, it is necessary to specify "command words", "counter reference value",and "counted value" in advance.
Since the timing is synchronized which transfer data between the up/down counter and other registers, the data read/write, command write, and status read can be carried out evenwhen the counter is operating.

4-1.Command mode

In ZEN2011P, two kinds of system mode described in the following can be selected.
First of all, it is necessary to select eitherof system mode by the command in initialization. Next, it is necessary to specify a command word, a counter value, and avalue of each register necessary for initializing the count operation beforehand.

(1) Mode 0 (After command:90H is executed or system reset)
$\overline{\text{EXTB}}$ (pin No.19) is set as universal input terminal U.
The reference register-A and the comparator-A become effective.

(2) Mode 1 (After command:91H is executed)
In this mode it is available as for all instruction sets of mode 0.
$\overline{\text{EXTB}}$ (pin No.19) is set in the output terminal. Moreover, $\overline{\text{EXTA}}$ (pin No.1) and $\overline{\text{EXTB}}$ (pin No.19) can control the output data by the instruction set of Mode 1.
Moreover, the reference register-B and the comparator-B become effective.

4-2.Read/write logic

The read or write operation of the ZEN2011P is selected using four signals, $\overline{\text{CE}}$, C/$\overline{\text{D}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$. Detail of the selection is shown in Tab.1.

Tab.1 The read/write operation

$\overline{\text{CE}}$	C/$\overline{\text{D}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	Operation
H	X	X	X	Disable(data bus is at high impedance condition)
L	L	L	H	Data read(latch register)
L	L	H	L	Data write(preload,reference register, up/down counter)
L	H	L	H	Status read(status register)
L	H	H	L	Command write(command register)

4-3.Selection of counter operation mode

The ZEN2011P samples the count inputs using the CLK.
Using four signals of UD/$\overline{\text{AB}}$ and SEL0~ SEL2, the type of counter pulse input and the type of counter clear can be selected. Refer to Tab.2 for detail.
The counting operations are carried out by sampling the conditions of A,B,and Z at the rising edge of CLK.

Tab.2 Counting mode selection

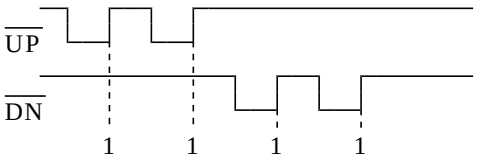
UD/$\overline{AB}$	SEL2	SEL1	SEL0	Pulse input (Edge eval.)	Clear mode
H	X	X	X	Up/Down pulse	Asynch-ronous clear
L	L	L	L	Phase-shifted (Single)	Synchro-nous clear mode
	L	L	H	Phase-shifted (Double)	
	L	H	L	Phase-shifted (Quad)	
	H	L	L	Phase-shifted (Single)	Asynch-ronous clear mode
	H	L	H	Phase-shifted (Double)	
	H	H	L	Phase-shifted (Quad)	
	L	H	H	Single pulse (Single)	
	H	H	H	Single pulse (Double)	

4-4.Count operation with pulse input

Pulse	Count operation
Up/down pulse	At the rising $\overline{UP}$,$\overline{DN}$ pulse.
Phase-shifted	At the phase change of A,B pulse Single:Change of phase A (only when phase B is "L") Double:Change of phase A Quad :Change of phase A,B
Single pulse	Count up with pulse A, as count enable signal with B. Single:Change of phase A (only at the rising pulse) Double:Change of phase A

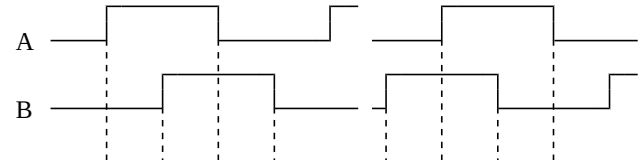
Edge evaluation (1:count 0:not count)

Up/down pulse input



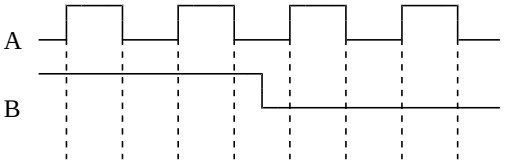
Note: Both up/down pulse should not be simultaneously set to a "Low" level.

Phase-shifted pulse input



Single	1	0	0	0	0	0	0	1
Double	1	0	1	0	0	1	0	1
Quad	1	1	1	1	1	1	1	1

Single pulse input



Single	1	0	1	0	0	0	0	0
Double	1	1	1	1	0	0	0	0

Note: B is used for a count enable signal.

4-5.Detection of abnormal input

The ZEN2011P has a function to check whether the phase-shifted input pulse input show a correct transition state (shown in Fig.1 with ⟷ marks) or not.
When an abnormal transition state (shown in Fig.1 with <----> marks) occurs,D7 of the status register to "H" which means the abnormal input flag(AI). Some of abnormal transition state are as follows:

(1)The frequencies of phase-shifted pulse inputs exceed the one fourth of the system clock frequency, so CLK can not sample the transition state correctly.
(2)The line-noises are sampled, so that ZEN2011P detects an abnormal transition.

Phase-shifted pulse input

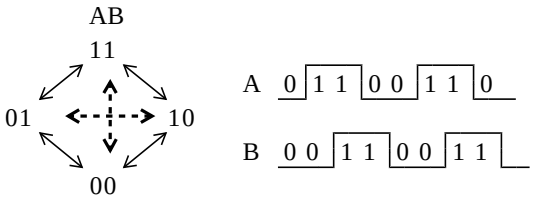


Fig.1 Example of transition state

4-6.Internal register conditions

After the system reset, the default values of the internal registers and the system mode are defined Tab.3.
The system reset is done, by applying a "Low" level pulse to $\overline{\text{RESET}}$.

Tab.3 Internal register condition

Register, mode	System reset
Counter	000000H
Preload register	the value just before the resetting
Reference reg.	"
Preload register	"
Latch register	"
Command register	
D7 (LD)	0 (NOP)
D6 (ZE1)	0) ZNE mode
D5 (ZE0)	1)
D4 (LT)	0 (NOP)
D3 (RS1)	0) Low byte of the up/down
D2 (RS0)	0) counter and
D1 (BS1)	0) the reading register
D0 (BS0)	0) are selected.
Status register	
D7 (AI)	0
D6 (Z)	Determined by input (Z)
D5 (A)	" (A)
D4 (B)	" (B)
D3 (DTR)	0
D2 ($\overline{\text{U}}$/D)	Determined by input (A,B)
D1 (EQA)	1
D0 (U)	Determined by input (U)
System mode	mode 0

5,Command register

This is a register which stores the "command words" to control the ZEN2011P.
The command words are entered through a data bus and are stored into the command register.

The command words have two kinds of the instruction set of Mode 0 and Mode 1.
The instruction set of Mode 1 cannot be executed at Mode 0 operations. However, all instruction sets are executable at Mode 1 operations.

5-1. System mode set command

It is the command word to select system mode.
It is necessary to select either of mode.

Format of the command register(system mode)

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Operation
1	0	0	1	0	0	0	0	90	Mode 0 select
1	0	0	1	0	0	0	1	91	Mode 1 select

(1) Mode 0 (default)

As for $\overline{\text{EXTA}}$ (pin No.1), comparator output $\overline{\text{EQA}}$ is output. Moreover, $\overline{\text{EXTB}}$ (pin No.19) becomes an input mode and is set in universal input U.

(2) Mode 1

$\overline{\text{EXTB}}$ (pin No.19) becomes an output mode and can set output data with $\overline{\text{EXTA}}$ (pin No.1) depending on the command of Mode 1.

5-2. Mode 0 : Functions and formats of the command register

BS0,BS1(Byte select)
Since the three registers(preload,reference, and latch) and up/down counter have 24 bit length, The BS0 and BS1 divide the 24 bit into high byte, middle byte, and low byte, each of which has 8 bit, and specify the byte to be accessed.

RS0,RS1(Register select)
The RS0 and RS1 specify a register to be accessed among the three registers(preload, reference and latch) and up/down counter.

This specification does not need to be entered for every byte, because the specified position automatically moves.

LT(Latch)
This command is used to store the counted data of the up/down counter into the reading register.

ZE0,ZE1(Z phase control)
The Z phase input signals are used as a clear signal for the up/down counter. ZE0 and ZE1 set the effective number of clear pulses.

LD(Load)
This command is used to transmit the data which are stored in the preload register to the up/down counter.

Note 1) In the Load and Latch operations, do not execute LD and LT simultaneously either by software commands or by external pins.

Note 2) To execute a LT command or a LD command , it is necessary to fix the external pins, $\overline{\text{LT}}$ and $\overline{\text{LD}}$, at a "H" level.

field format of command register(mode 0)

D7	D6	D5	D4	D3	D2	D1	D0
LD	ZE1	ZE0	LT	RS1	RS0	BS1	BS0

Format of the command register(mode 0)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
x	x	x	x	0	0	x	x	Selecting the up/down counter (default)
x	x	x	x	0	1	x	x	Selecting the reference register-A
x	x	x	x	1	x	x	x	Selecting the preload register (mode 0)
x	x	x	x	1	0	x	x	" (mode 1)
x	x	x	x	1	1	x	x	Selecting the reference register-B (mode 1)
x	x	x	x	x	x	0	0	Selecting low byte of the register(default)
x	x	x	x	x	x	0	1	Selecting middle byte of the register
x	x	x	x	x	x	1	x	Selecting high byte of the register
x	0	0	x	x	x	x	x	No operation
x	0	1	x	x	x	x	x	Z phase input is not effective (default)
x	1	0	x	x	x	x	x	Only next Z phase input is effective
x	1	1	x	x	x	x	x	Every Z phase input is effective
0	x	x	0	x	x	x	x	No operation
0	x	x	1	x	x	x	x	LT(Latching the count value)
1	x	x	0	x	x	x	x	LD(Loading the preload value)
1	0	0	1	x	x	x	x	Command ID.
1	x	x	1	x	x	x	x	Inhibit

5-3. Mode 1 : Functions and formats of the command register

The command group of Mode 1 becomes effective by setting system mode in Mode 1. Therefore, even if the command group of Mode 1 is input at Mode 0, it is not executed. Moreover, the reference register B can be accessed in Mode 1. The D0 of the status register is monitor the comparator B output $\overline{EQB}$.

$\overline{EXTA}$ can be programmed to output one of three signals ($\overline{EQA}$, $\overline{EQA+EQB}$, $\overline{INTEQA}$).

$\overline{EXTB}$ can be programmed to output one of three signals ($\overline{EQB}$, $\overline{INTEQB}$, $\overline{INTAI}$).

$\overline{EQA}$ It is Low only when the counted value is equal to the reference register A value.

$\overline{EQB}$ It is Low only when the counted value is equal to the reference register B value.

$\overline{EQA+EQB}$ It is Low when either $\overline{EQA}$ or $\overline{EQB}$ is Low.

$\overline{INTEQA}$ After $\overline{EQA}$ is Low, $\overline{INTEQA}$ is holding Low.
It can be used for interrupt request.

$\overline{INTEQB}$ After $\overline{EQB}$ is Low, $\overline{INTEQB}$ is holding Low.
It can be used for interrupt request.

$\overline{INTAI}$ After abnormal transition state is detected, $\overline{INTAI}$ is holding Low.
It can be used for interrupt request.
The commands of Enable interrupt(EI), Disable interrupt(DI) and reset, are available.
AI reset command resets this output, initializes the phase discrimination circuit.
AI reset command is effective only when $\overline{INTAI}$ is selected (after 9AH, 9BH command executed).

Format of the command register(mode 1)

D7	D6	D5	D4	D3	D2	D1	D0	Hx	Operation
1	0	0	1	0	0	1	0	92	Inhibit
1	0	0	1	0	0	1	1	93	Inhibit
1	0	0	1	0	1	0	0	94	$\overline{EQA}$+ $\overline{EQB}$ P $\overline{EXTA}$
1	0	0	1	0	1	0	1	95	$\overline{EQA}$ P $\overline{EXTA}$ *)
1	0	0	1	0	1	1	0	96	Inhibit
1	0	0	1	0	1	1	1	97	$\overline{EQB}$ P $\overline{EXTB}$ *)
1	0	0	1	1	0	0	0	98	$\overline{INTEQA}$ **)
1	0	0	1	1	0	0	1	99	$\overline{INTEQB}$,$\overline{INTAI}$ **)
1	0	0	1	1	0	1	0	9A	$\overline{INTAI}$ P $\overline{EXTB}$ & DI
1	0	0	1	1	0	1	1	9B	$\overline{INTAI}$ P $\overline{EXTB}$ & EI
1	0	0	1	1	1	0	0	9C	$\overline{INTEQA}$ P $\overline{EXTA}$ & DI
1	0	0	1	1	1	0	1	9D	$\overline{INTEQA}$ P $\overline{EXTA}$ & EI
1	0	0	1	1	1	1	0	9E	$\overline{INTEQB}$ P $\overline{EXTB}$ & DI
1	0	0	1	1	1	1	1	9F	$\overline{INTEQB}$ P $\overline{EXTB}$ & EI

*) default **) command reset
Hx:Hexa code

Note: Both $\overline{EXTA}$ and $\overline{EXTB}$ cannot be connected to other IC output, because they cannot be high- impedance in mode 1.

6. Status register

The status register is used to monitor theinternal condition. Please refer to the paragraph of "4-1.CPU interface" for the method of readout this register.

Bit description

D7 AI Abnormal input detection flag (only phase-shifted pulse input)
It is shown that an abnormal transition state of phase-shifted input is detected. This flag is cleared by the status readout.

D6 Z Z/CLR input monitor
It indicates the value of Z/CLR that is sampled at the rising edge of CLK.

D5 A A/$\overline{UP}$ input signal monitor
It indicates the value of A/$\overline{UP}$ that is sampled at the rising edge of CLK.

D4 B B/$\overline{DN}$ input signal monitor
It indicates the value of B/$\overline{DN}$ that is sampled at the rising edge of CLK.

D3 DTR Data ready flag of the reading register
It is shown that the counter data has been transfered to the reading register by latch execution. This flag is cleared by reading the data from the reading register.

D2 U/D Counting direction status of internal counter.
A present direction where an internal counter is counted is indicated.
(up count: "L" and down count: "H")

D1 $\overline{EQA}$ Comparator A coincident flag
It is shown that the count data is corresponding to the data of reference register A.

D0 U Universal input U monitor (mode 0)
It is possible to do though signal (U) input to $\overline{EXTB}$ (No.19 pin) is directly monitored.

$\overline{EQB}$ Comparator B coincident flag (Mode 1)
It is shown that the count data is corresponding to the data of reference register B.

7.Electrical specification

(1) Absolute maximum rating

Rating	Symbol	Values	Unit
Supply voltage	VDD	-0.3 ~ 7.0	V
Input voltage	Vi	-0.3 ~ VDD+0.3	V
Output voltage	Vo	-0.3 ~ VDD+0.3	V
Operation temperature	Topr	-10 ~ +70	C
Storage temperature	Tstg	-55 ~ +150	C

(2) Recommended operating conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	VDD	4.75	5.0	5.25	V
Operation temperature	Topr	-10	-	+70	C

(3) DC characteristics(at the recommended operating conditions)

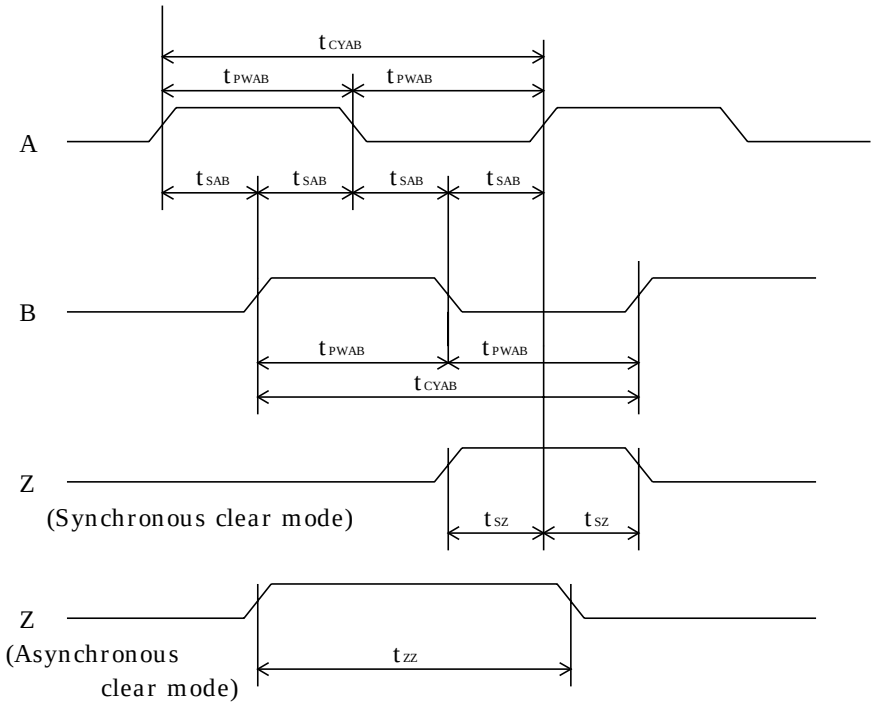
Parameter	Symbol	Measuring conditions	Limit values			Unit
			MIN	TYP	MAX	
Input "Low" voltage	V_{IL}		-	-	0.8	V
Inout "High" voltage	V_{IH}		2.0	-	-	V
Output "Low" voltage	V_{OL}	I_{OL}= 4mA	-	-	0.4	V
Output "High" voltage	V_{OH}	I_{OH}= -2mA	2.4	-	-	V
Input leakage current	I_{OL}	Vi= 0V~ VDD	-10	-	10	μA
Output leakage current	I_{OZ}	Under a high impedance	-10	-	10	μA
Standby current	I_{DDS}	Vi= 0V or VDD	-	-	20	μA
Operation current	I_{DDO}	f=8MHz Outputs open	-	-	40	mA

8.AC characteristics (Ta=-10~ 70 C, Vcc=5V }5%)

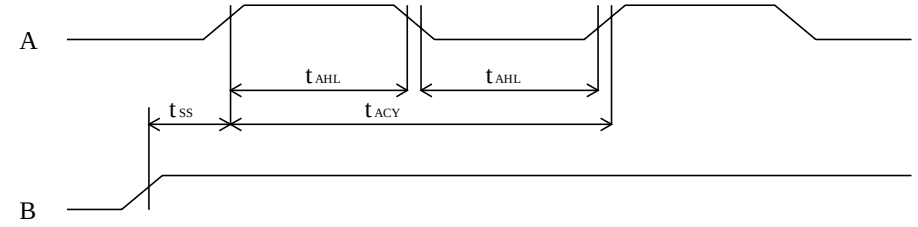
Parameter	Symbol	Condition	Values(Unit:nS)	
			MIN	MAX
C/$\overline{D}$,$\overline{CE}$setup time (to D_7~ D_0)	t_{AW}		0	-
C/$\overline{D}$,$\overline{CE}$ hold time (to D_7~ D_0)	t_{WA}		0	-
Data setup time (to $\overline{WR}$-)	t_{DW}		80	-
Data hold time (to $\overline{WR}$-)	t_{WD}		40	-
$\overline{WR}$ pulse width	t_{WW}		80	-
C/$\overline{D}$,$\overline{CE}$setup time (to $\overline{RD}$-)	t_{AR}		50	-
C/$\overline{D}$,$\overline{CE}$ hold time (to $\overline{RD}$-)	t_{RA}		30	-
$\overline{RD}$ pulse width	t_{RR}		80	-
Data access time (from $\overline{RD}$)	t_{RD}		-	50
Data float delay (from $\overline{RD}$-)	t_{DF}		20	-
Clock high/low pulse width	ϕ_0		60	-
Clock cycle time	ϕ_{cy}		125	-
Reset pulse width	t_{RST}		80	-
$\overline{LD}$ setup time (to CLK)	t_{LDS}		30	-
$\overline{LD}$ pulse width	t_{LDW}		50	-
UDC data definite delay time	t_{LDD}		-	30
$\overline{LT}$ setup time (to CLK)	t_{LTS}		30	-
$\overline{LT}$ pulse width	t_{LTW}		50	-
RDR data definite delay time	t_{LTD}		-	30
$\overline{EXTB}$ set time (from $\overline{WR}$-)	t_{SEB}		-	50
$\overline{EXTB}$ float time (from $\overline{WR}$-)	t_{FEB}		-	50
$\overline{EXTA}$,$\overline{EXTB}$ fix time(to CLK)	t_{EXF}		20	-
A,B cycle time	t_{CYAB}		ϕ_{cy} /4+200	-
A,B high/low level time	t_{PWAB}		ϕ_{cy} /2+100	-
A,B phase difference time	t_{SAB}		ϕ_{cy}+ 50	-
Z high level width	t_{SZ}	Synchronous clear mode	ϕ_{cy}+ 50	-
Z pulse width	t_{ZZ}	Asynchronous clear mode	ϕ_{cy}+ 50	-
A- setup time (to B-)	t_{SS}	Single phase mode	ϕ_{cy}+ 50	-
A high/low level width	t_{AHL}	Single phase mode	ϕ_{cy}+ 50	-
A cycle time	t_{ACY}	Single phase mode	ϕ_{cy} /2+100	-
$\overline{UP}$,$\overline{DN}$ cycle time	t_{UDCY}	Up/down mode	ϕ_{cy} /2+100	-
$\overline{UP}$,$\overline{DN}$ high/low level width	t_U	Up/down mode	ϕ_{cy}+ 50	-

9, Timing of ZEN2011P

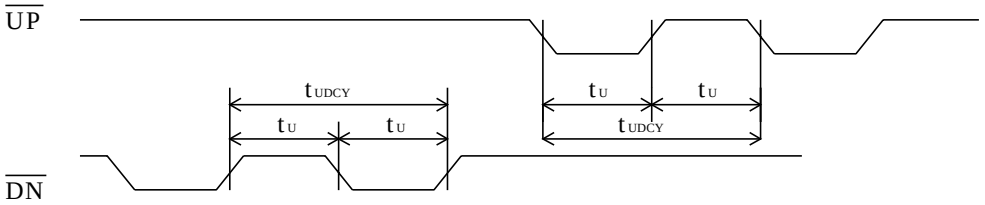
Input timing of phase-shifted pulse signal



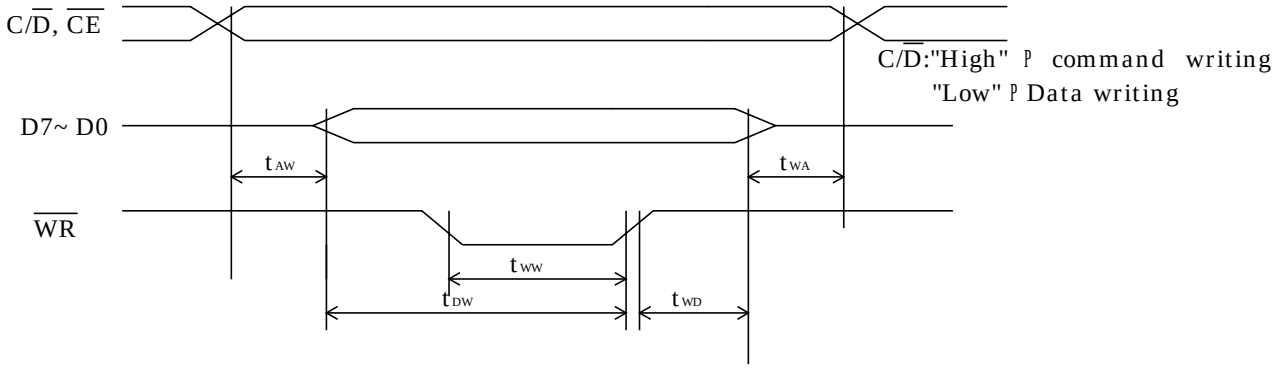
Input timing of single phase signal



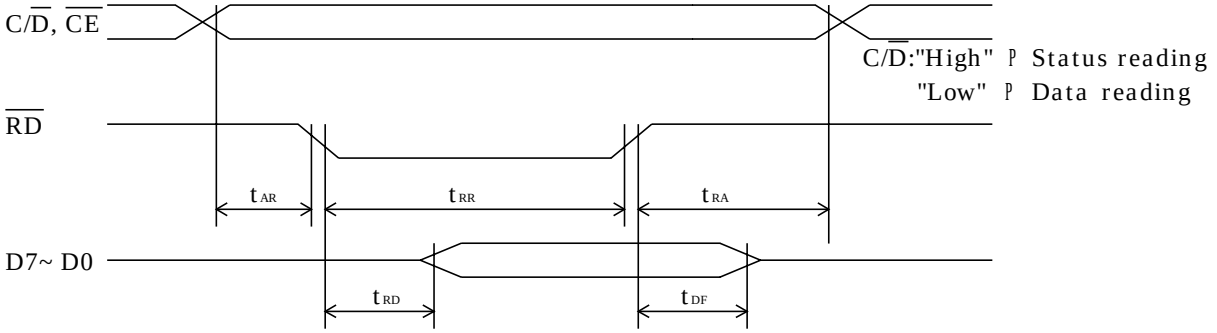
Input timing of up/down pulse signal



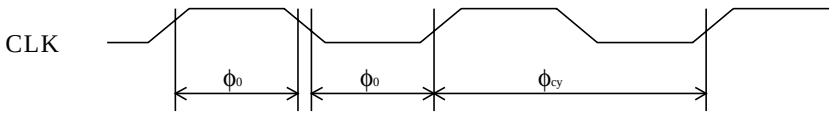
Write cycle



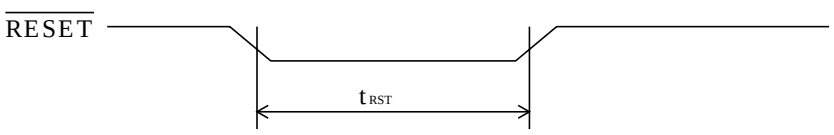
Read cycle



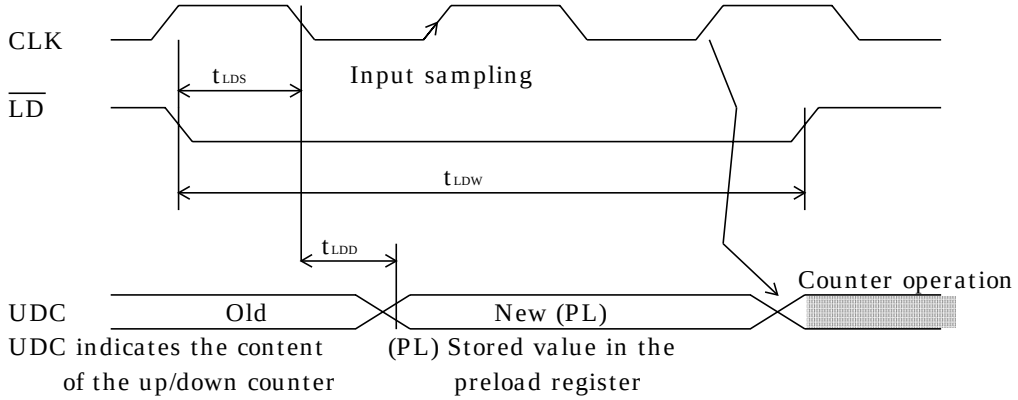
Clock waveform



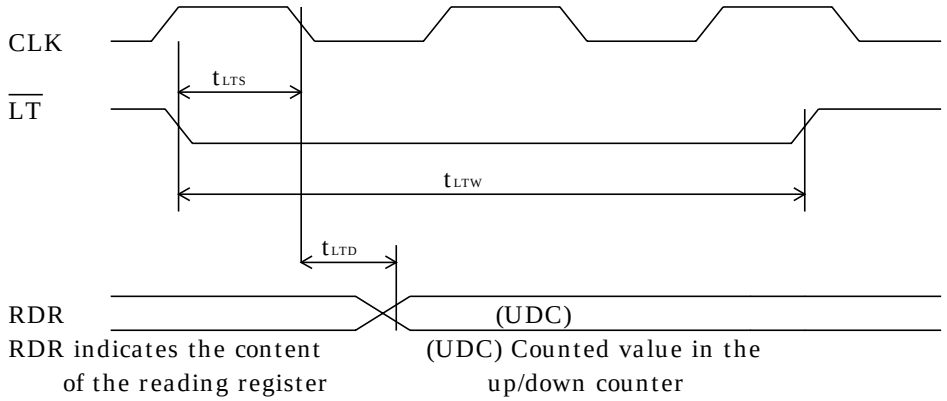
Reset waveform



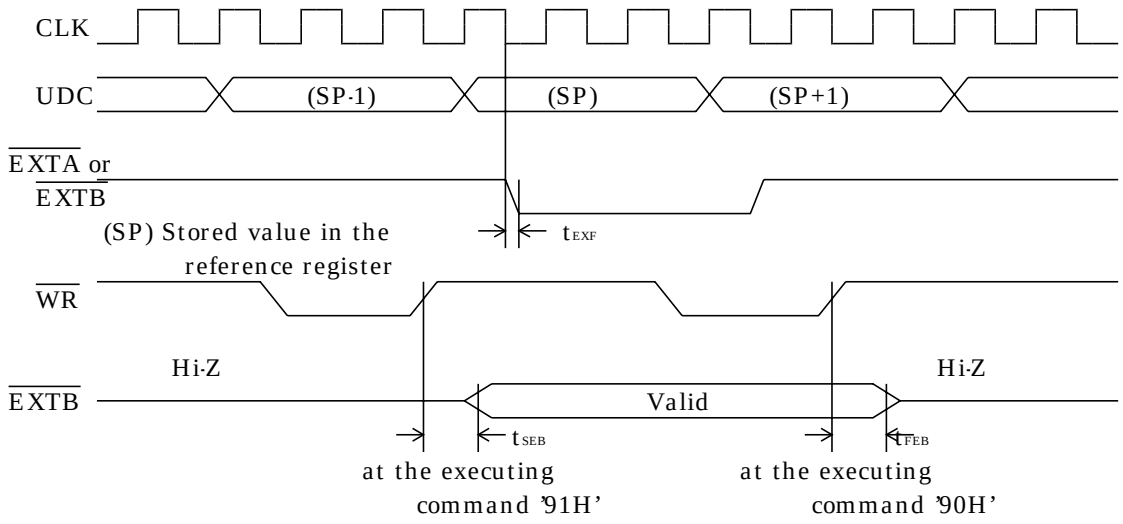
Load cycle



Latch cycle



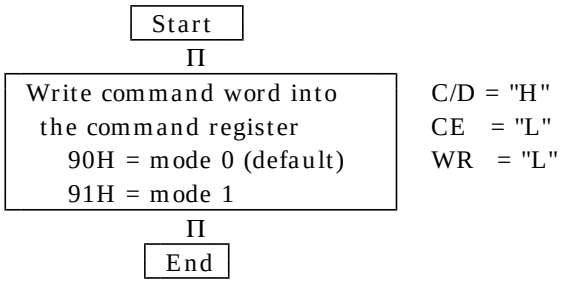
Output timing of EXTA or EXTB signal



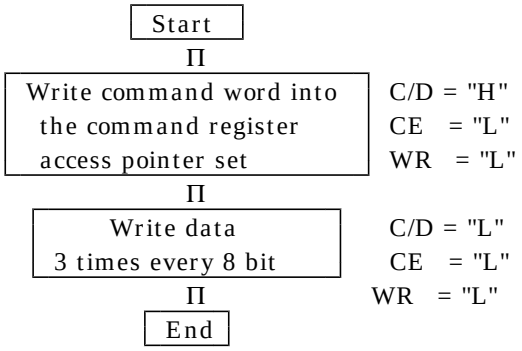
10. Outline of software design

The ZEN2011P is controlled by software.
Following is the outline of designing software,
in a form of flow chart, for the basic operations.

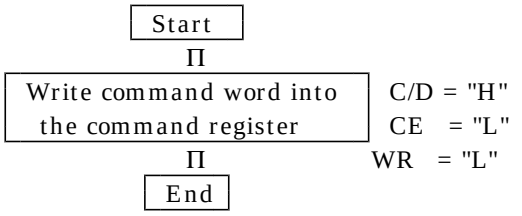
(1) System mode set



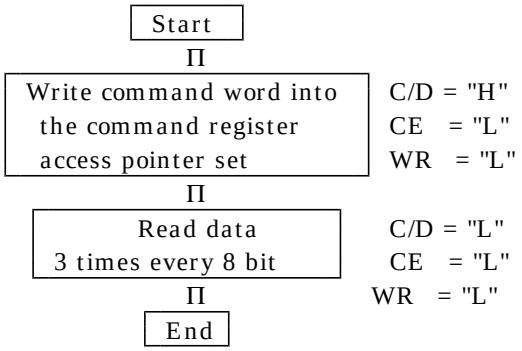
(2) Initial value set to the each register



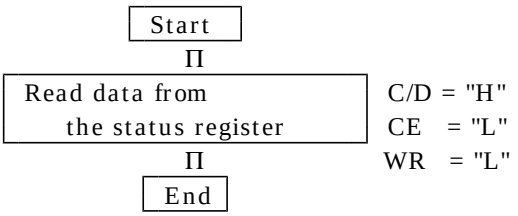
(3) Command writes



(4) Count data read

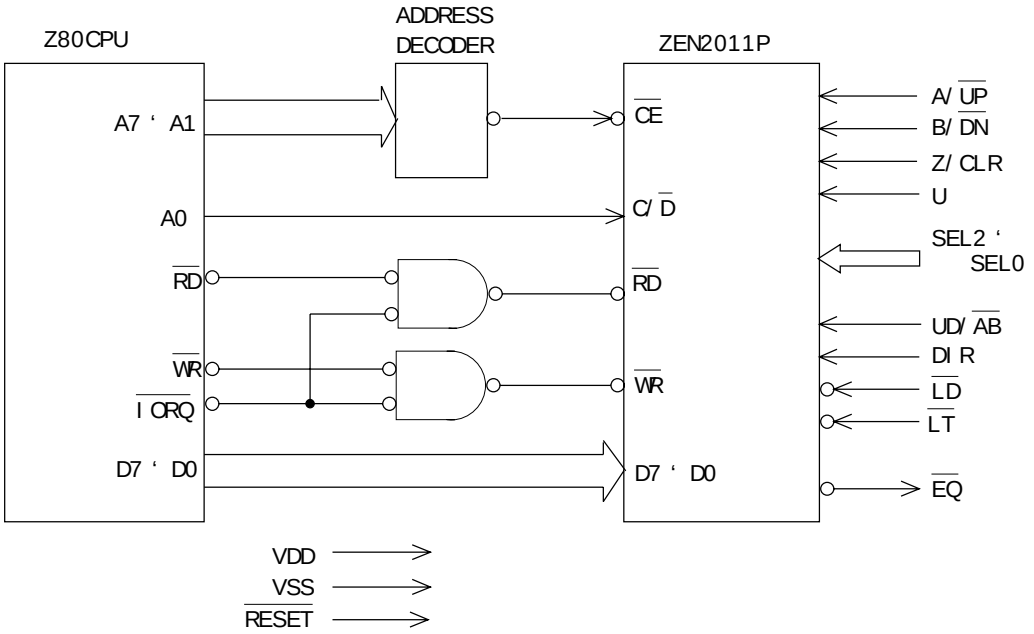


(5) Status read

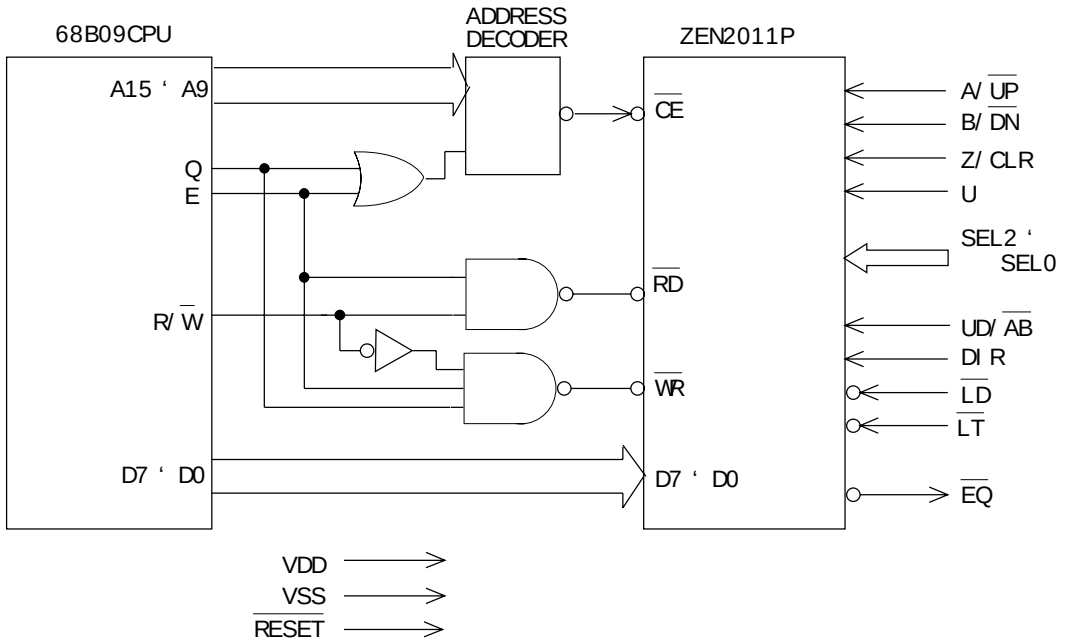


11. Interface example

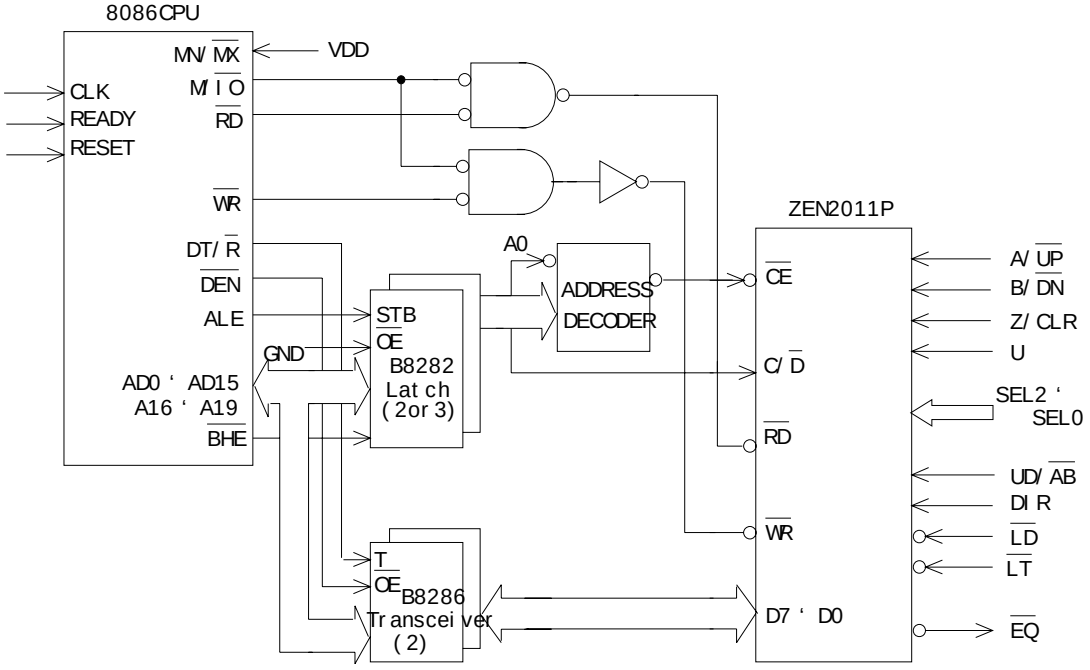
Z80



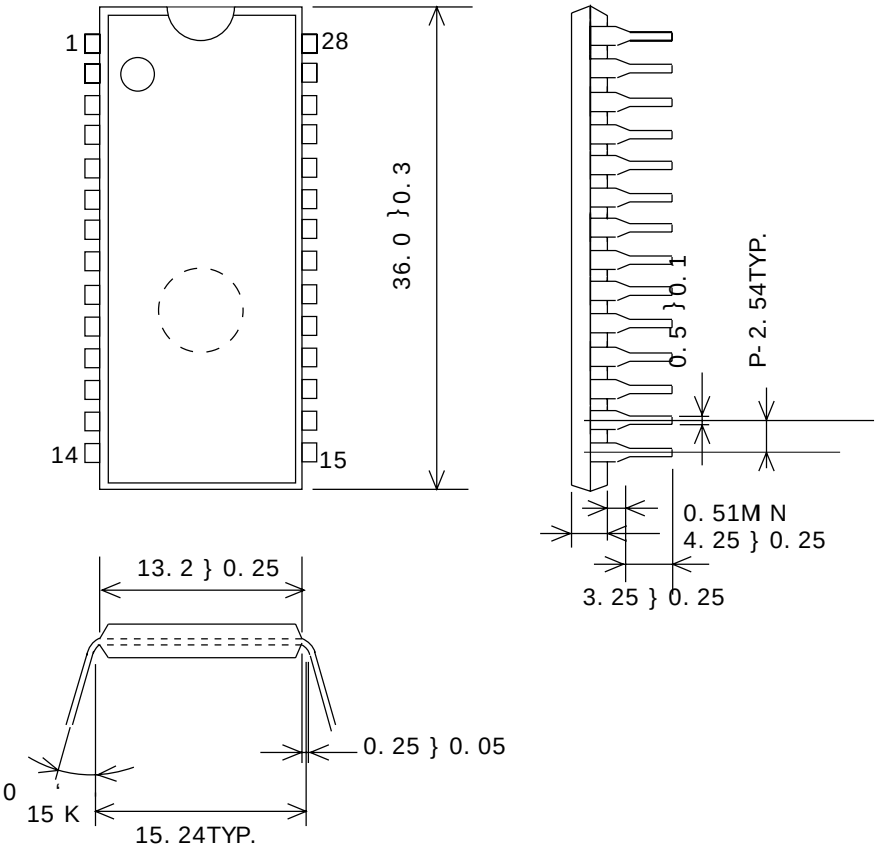
6809



8086(Minimum mode)



12. Package Outlines (Dimensions in mm)



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