Z9102

Variable Delay Motherboard Clock Buffer

Approved Product

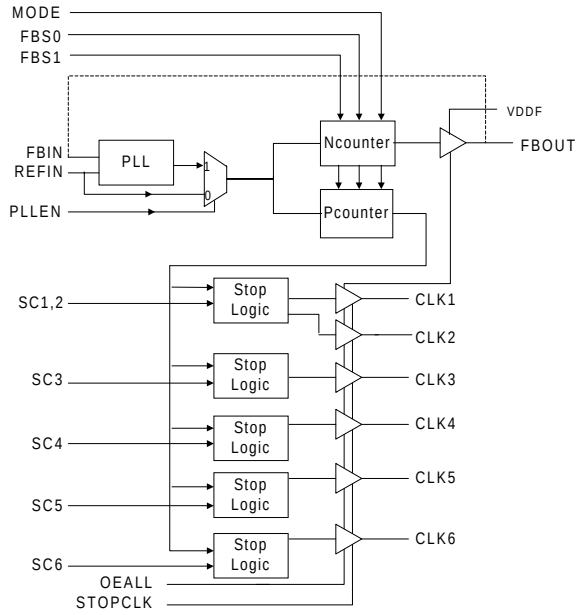
Product Features

- Output phase relationship is precisely controllable with respect to input clock via a dedicated external feedback path.
- 6 Low Skew Clocks Generated
- Outputs are individually enabled.
- Output frequencies from 30 to 100 MHz.
- 3.3 Volt Vdd operation
- Synchronous output enable and disable control
- 45 - 55% output duty cycle
- +/- 100 pSec Cycle to Cycle Jitter
- 32-Lead TQFP (in LQFP Profile) package

Feedback Scale Select Codes

Mode	FBS1	FBS0	Pcounter	Ncounter
0	0	0	÷ 4	÷ 8
0	0	1	÷ 4	÷ 10
0	1	0	÷ 4	÷ 12
0	1	1	÷ 8	÷ 12
1	0	0	÷ 4	÷ 4
1	0	1	÷ 4	÷ 5
1	1	0	÷ 4	÷ 6
1	1	1	÷ 8	÷ 8

Block Diagram



Pin Configuration