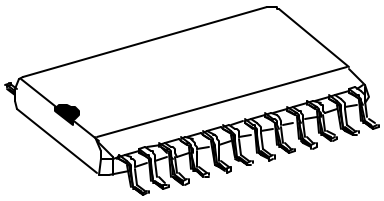
USBvision™ II Data Decoder

ZR36505

VBI Data and Remote Control Interface for ZR6504

Data Sheet



Revision 1.00 November 1999.

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ZR36505 - VBI (Teletext) pipe and Remote Control interface for USB TV applications

The ZR36505 is a complimentary chip for the ZR36504 in USB TV applications. Combined with certain video decoders, it adds a VBI (Vertical Blank Interval) data pipe to the system, which utilizes the general purpose Bulk channel of the NT1004. The VBI is used by TV broadcast providers to send digital data hidden in the analog video signal. One or more video lines, taken from lines 1-21 of each video field are used for carrying this information - each line providing about 9,600 bits/sec data rate.

The ZR36505 provides the application S/W with access to data such as Teletext, Close-Caption, Intercast, IR receiver samples, etc. It uses a 1KByte SRAM buffer to grabe the processed data from the video decoder during the Blank Interval time slot, and sends this data to the USB through the ZR36504 Bulk pipe during the time left prior to beginning of next Blak Interval. For the remote Control interface, the input pin IO_1 is sampled at 4Ksamp/sec rate, and the sampled bits are moved to host computer via the (NT1004) for S/W process.

Features

- Enables Teletext and Close-Caption
- Supports WST625, WST525, CC625, CC525, US NABTS, MOJI (Japanese), and JFS formats
- Provides Remote Control interface with IR receiver (sampled at 4K samp./sec.)
- Low Cost, Low Power, 3.3v operated
- 24-pin SOIC package

Product Description

Refer to Fig.1 for an internal Block Diagram of the ZR36505.

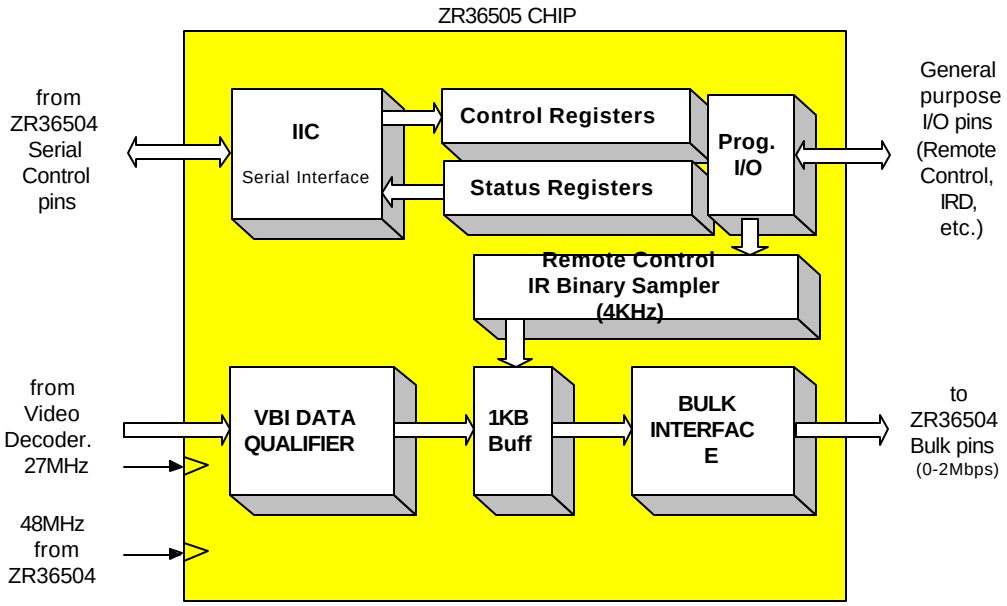


Fig.1 ZR36505 Block Diagram

The IIC block uses the LRNACK mode of the ZR36504 serial control bus to provide access to its internal registers. The address range for output registers and input registers is 0x00-0x07 each.

The internal Input and Output Registers are used by the Host (PC S/W via ZR36504) to control the parameters of the ZR36505 blocks and to read their status. There are two general I/O pins to be used by S/W for specific designs.

The VBI DATA QUALIFIER block can be programmed to restrict VBI data capture to any specified range of lines within the video field. Also, a specific data type can be defined, to filter out all other types of VBI data.

The 1KByte Buffer is used for capturing all VBI data from every coming video field (after qualification), and sending it via the Bulk Interface. This is done for one field at a time, and Write/Read cannot be done simultaneously.

The BULK INTERFACE block is designed to match the ZR36504 specification. It can coexist with an audio Codec source to share the same clock and data pins of the NT1004.

Finally, The ZR36505 uses 2 clock sources: 27MHz for VBI data, and 48MHz (from NT1004) for the other blocks. The ZR36505 does not require a crystal of its own.

Pin Assignments (Top View)

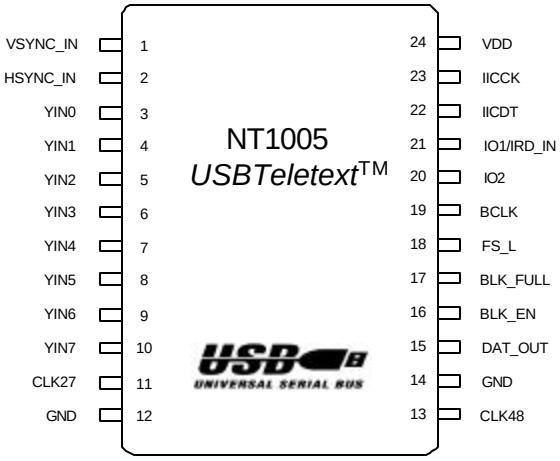


Table 1 - PIN DESCRIPTIONS

PIN NUMBER	SIGNAL	I/O	DESCRIPTION
24	VDD		Digital 3.3V power supply
12, 14	GND		Digital ground connection
1	VSYNC_IN	I	Video Vertical-Sync input signal from Video Decoder
2	HSYNC_IN	I	Video Vertical-Sync input signal from Video Decoder
3-10	YIN0-YIN7	I	VBI data-bus from Video Decoder. Usually used also for delivering the digital video samples.
11	CLK27	I	VBI clock from Video Decoder. Used to sample the VBI data in its positive edge. This clock is used for capturing and storing the VBI data.
13	CLK48	I	This is the ZR36505 Global clock, which comes from the NT1004.
15	DAT_OUT	O	VBI Data Output pin, goes to DAT_IN pin of the ZR36504(which is used for both Audio CODEC T x chan and Bulk Data in This pin is Open Drain, and is set to high-z upon Power-On or Soft Reset. It requires an external pull-up resistor.
16	BLK_EN	O	Bulk Data Enable output. When set to '1', Bulk output data at DAT_OUT pin is sampled into the ZR36504by falling edge of BCLK . This pin is set to Hi-Z upon Power-On or Soft Reset.
17	BLK_FULL	I	"Bulk-Fifo full" indication signal from NT1004. This signal is normally '0', and is set to '1' when the ZR36504Bulk-Fifo is full.
18	FS_L	I	Audio Codec Frame-Sync pulse for Left channel., which comes from the NT1004. The ZR36505 uses this signal to trigger the beginning of its VBI Bulk data output immediately after the 16th

			bit of audio Left.
19	BCLK	I	Bulk-data clock (ZR36504uses this clock for both Audio CODEC and Bulk Data). This clock must be set to 2.024MHz for proper operation with ZR36505.

Table 1- PIN DESCRIPTIONS (continued)

PIN NUMBER	SIGNAL	I/O	DESCRIPTION
20-21	IO-1/IRD_IN IO-2	I/O	General Programmable I/O pins. Each of these 2 pins has a 5-volt Tolerant Open Drain output, and it is supposed to be connected to an external pull-up resistor. The host uses these pins as programmable output ports by writing '0' or '1'. By writing '1' and read back, the host can use these pins as input ports - as this allows any external source to force the pull-up resistor. These outputs are set to high-z upon Power-On or Soft Reset. The pin IO-1 is also used as the input for IRD data. This pin is internally sampled at 4KHz sampling rate.
22	IICDT	I/O	This pin is used for sending and receiving serial control data between the ZR36505 (slave) and ZR36504(master). It operates in the LRNACK mode of operation (refer to the ZR36504data sheet). This pin is Open Drain, and is set to high-z upon Power-On or Soft Reset.
23	IICCK	I	This pin is used as the sampling clock for sending and receiving serial control data between the ZR36505 (slave) and ZR36504(master). It operates in the LRNACK mode of operation (refer to the ZR36504data sheet).

Table 2- ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{dd} - GND	-0.5 to 4.6	V
Voltage, any pin to GND	V	-0.5 to V_{dd}+0.5	V
DC Current Drain per Pin (Excluding V_{dd}, GND)	I	±10	mA
Operating Temperature Range	T_A	0 to +70	^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC

Table 3- ELECTRICAL CHARACTERISTICS (V_{dd}=3.3V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Supply Voltage (V_{dd} to GND)	V_{dd}	3.0	3.3	3.6	V
DC Supply Current (@ V_{dd}=3.3V)	I_{CC}	-	12	18	mA
High Level Input Voltage (other than XIN, CAPTRN, and RESIN)	V_{IH}	2.0	-	V_{dd}+0.3*	V
Low Level Input Voltage (other than XIN, CAPTRN, and RESIN)	V_{IL}	-0.3	-	0.8	V
Input Current $V_I = V_{dd}$+0.3 or GND	I_{in}	-10	+1	+10	µA
Input Capacitance	C_{in}	-	2.5	7.0	pF

3-State Output Leakage Current $V_O = V_{dd}+0.3$ or GND	I_{OZ}	-10	+1	+10	µA
Output Capacitance	C_{out}	-	2.0	7.0	pF
High Level Output Voltage (@ Iout = -4mA)	V_{OH}	2.4	-	V_{dd}	V
Low Level Output Voltage (@ Iout = 4mA)	V_{OL}	0	-	0.4	V

1. SERIAL CONTROL

The ZR36505 uses a Serial Control Interface to access its internal registers.

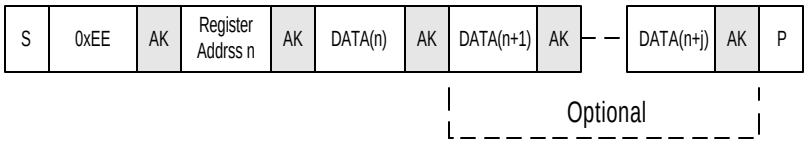
Table 4 - ZR36505 Registers List:

Reg. Address	Reg. Name	Function	Default Value
0	LINE_LEN_L	d7-d0: LINE_LEN[7..0]	00H
1	LINE_LEN_H	d2-d0: LINE_LEN[10..8] d7-d3: reserved	00H
2	LINE_WIN_L	d7-d0: WIN_OFFSET[7..0]	00H
3	LINE_WIN_H	d7-d3: WIN_LEN[4..0] d2-d1: reserved d0: WIN_OFFSET[8]	00H
4	VBI_REG	d7: EN_TYPE_QUALIFIER '1': enable '0': disable d6: EN_WIN_QUALIFIER '1': enable '0': disable d5: EN_RAW_SAMPLES '1': enable '0': disable d4: EN_VBI_QUALIFIER '1': enable '0': disable d3-d0: DATA_TYPE_QUALIFIER[3..0]	00H
5	BLK_OPER_ MODE	d3: BCLK_RATE '1': 2048KHz '0': 1544KHz d2: AUDIO_DAT '1': exists '0': does not exist d1: AUDIO_RATE '1': 16KS/s '0': 8KS/s d0: AUDIO_STEREO '1': stereo '0': mono d7: BLK_IO_EN '1': En bulk output pins. '0': Disable. d6-d4: reserved	00H
6	IO_REG	d0: IO_1 Read/Write level of ZR36505 pin IO-1 d1: IO_2 Read/Write level of ZR36505 pin IO-2 d7-d2: reserved	00H
7	SOFT_RESET	d0: SOFT_RESET '1' : Perform RESET This reg is always read 0x00 (even after writing 0x01). Writing 0x01 to this register will result in a general reset operation to the ZR36505, leaving all registers in their default values.	00H

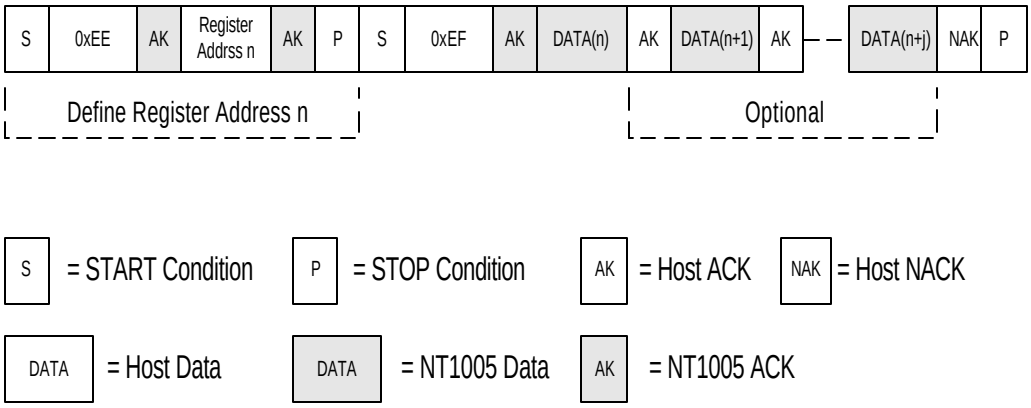
The serial bus consists of a clock signal and a data signal, which relate to the ZR36505 as a bus slave (where the ZR36504 is used as the bus master).
The ZR36505 device address is 0xEE for a Write operation, and 0xEF for a Read operation.

The diagram in the following page specifies general Read and Write transactions. In both transactions the register address is auto-incremented, which requires from the host computer to define the address of the first register only. The data bytes are then sent or received one after the other from the first register to the last one (any number of registers is possible). A Read transaction requires a Write sequence of 0 data bytes, in order to define the first address register to be read.

Write transaction

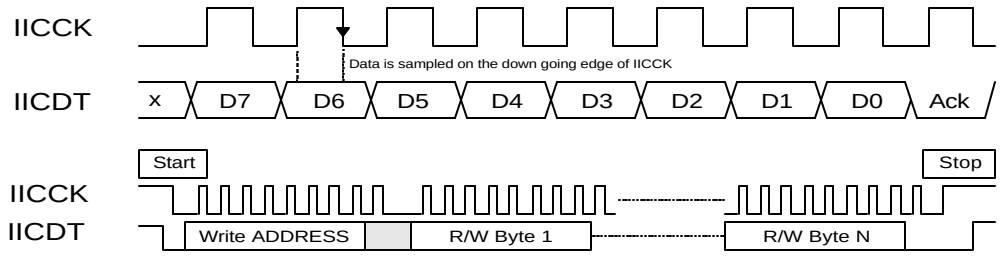


Read transaction

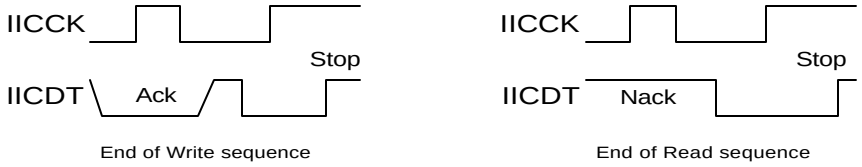


It is recommended to set the ZR36504(master) chip to its IIC LRNACK mode of operation to communicate with the ZR36505.

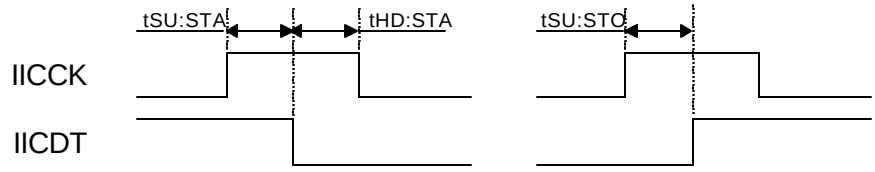
The following waveforms and timing diagrams specify the IIC serial interface bus in the signal level:



NOTE: Start is defined when the IICDT turns from '1' to '0' while the IICCK is '1'. Stop is defined when the IICDT turns from '0' to '1' while the IICCK is '1'. The Address byte is written like any other byte.



Start/Stop Timings



Data Timings

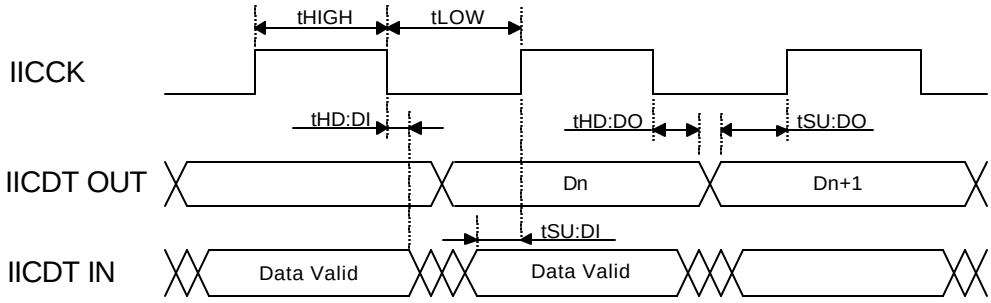


Table 5 - SERIAL CONTROL TIMINGS

Symbol	Parameter	Min	Max	Unit
$t_{SU:STA}$	START condition setup time	5300	-	ns
$t_{HD:STA}$	START condition hold time	5300	-	ns
$t_{SU:STO}$	STOP condition setup time	5300	-	ns
t_{HIGH}	Clock high time	5300	-	ns
t_{LOW}	Clock low time	5300	-	ns
$t_{SU:DO}$	Data output setup time	2500	2670	ns
$t_{HD:DO}$	Data output hold time	2500	2670	ns
$t_{SU:DI}$	Data input setup time	20	-	ns
$t_{HD:DI}$	Data input hold time	0	-	ns
Fiicck	Frequency of IICCK clock signal	0	100	KHz

2. VBI DATA QUALIFIER

2.1 VBI Input Interface

The ZR36505 is designed to connect to the 8-bit VBI output bus of the Video Decoder (Philips SAA7113 in its CCIR-656 mode of operation). This bus is sampled by the rising edge of CLK27 (27MHz clock, which is also provided by the Video Decoder chip), and provides the processed data bytes in the Blank lines. The same bus contains the Y/U/V video data on the valid video lines, which go directly to the NT1004.

The VBI input interface consists of the following signals:

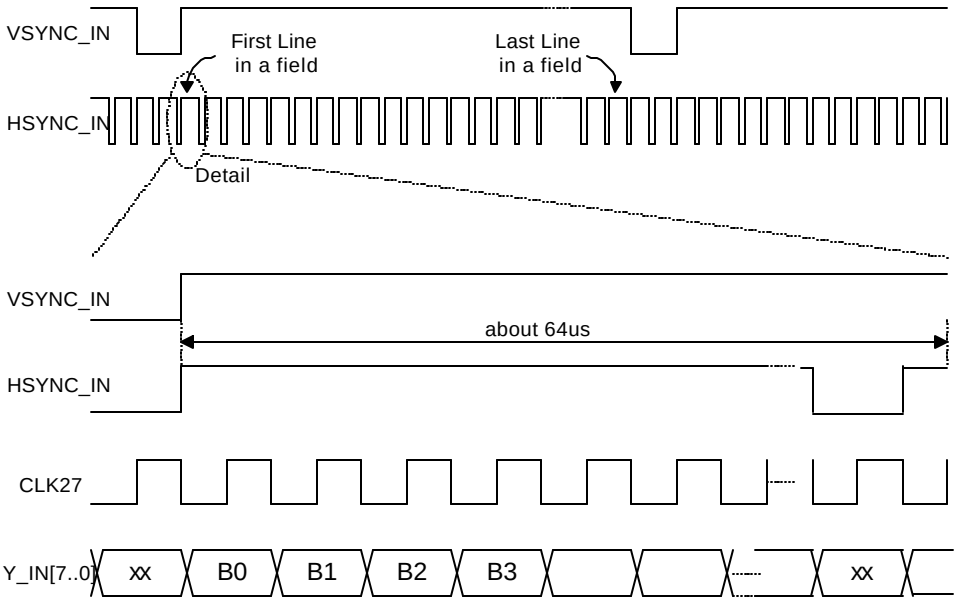
Y_IN[7..0] (Inputs)
This is the 8-bit VBI bus (contains also the Y/U/V samples in non-blank lines).

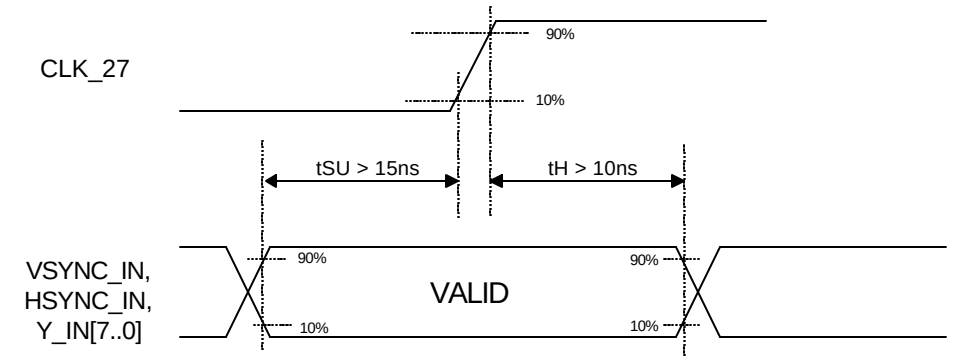
VSYNC_IN (Input)
This is the negative Vertical Synchronization pulse, which indicates the start of a new video field (Interlace mode).

HSYNC_IN (Input)
This is the negative Horizontal Synchronization pulse, which indicates the start of a new video line.

CLK27 (Input)
This signal is the video pixel clock. It is used by the ZR36505 to sample all the other inputs in the digital video interface. It is also used by all state machines and logic to capture the VBI data into the 1Kbyte on-chip memory.

The timing of the VBI input bus, as expected by the ZR36505 is specified in the following timing diagram:





2.2 VBI Lines Qualifier

The VBI lines are defined in the range 2-21 of the 1st and 2nd fields, but in most TV stations not all the VBI lines are used for digital data.

The ZR36505 provides a way of restricting the search range, and filtering out the undesired data. This allows the ZR36505 to produce smaller buffers of data to be delivered via the USB Bulk channel, which do not interfere with the isochroneous video and audio channels. To do this, the ZR36505 uses the following qualifiers:

Line Window Qualifier (Regs. 0-3):

LINE_LEN_L (Reg. 0)

D7	D6	D5	D4	D3	D2	D1	D0
LINE_LEN[7..0]							

LINE_LEN_H (Reg. 1)

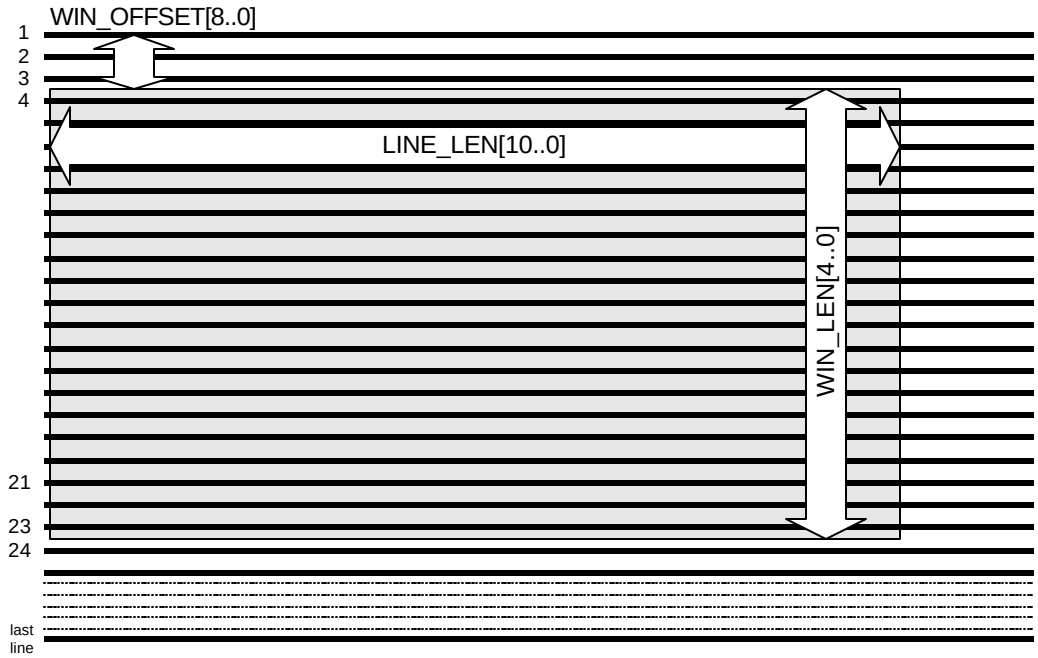
D7	D6	D5	D4	D3	D2	D1	D0
resrved	resrved	resrved	resrved	resrved	LINE_LEN[10..8]		

LINE_WIN_L (Reg. 2)

D7	D6	D5	D4	D3	D2	D1	D0
WIN_OFFSET[7..0]							

LINE_WIN_H (Reg. 3)

D7	D6	D5	D4	D3	D2	D1	D0
WIN_LEN[4..0]					resrved	resrved	WIN_OFFSET[8]



The dark window represents the Line Window Qualifier. LINE_LEN[10..0] is counted from the up-going edge of the HSYNC_IN pulse and relates to CLK27 cycles, and WIN_OFFSET[8..0] is counted from the up-going edge of the VSYNC_IN pulse and relates to HSYNC_IN pulses. Note that bit d6 of VBI_REG (reg.4) should be enabled:

VBI_REG (Reg. 4)

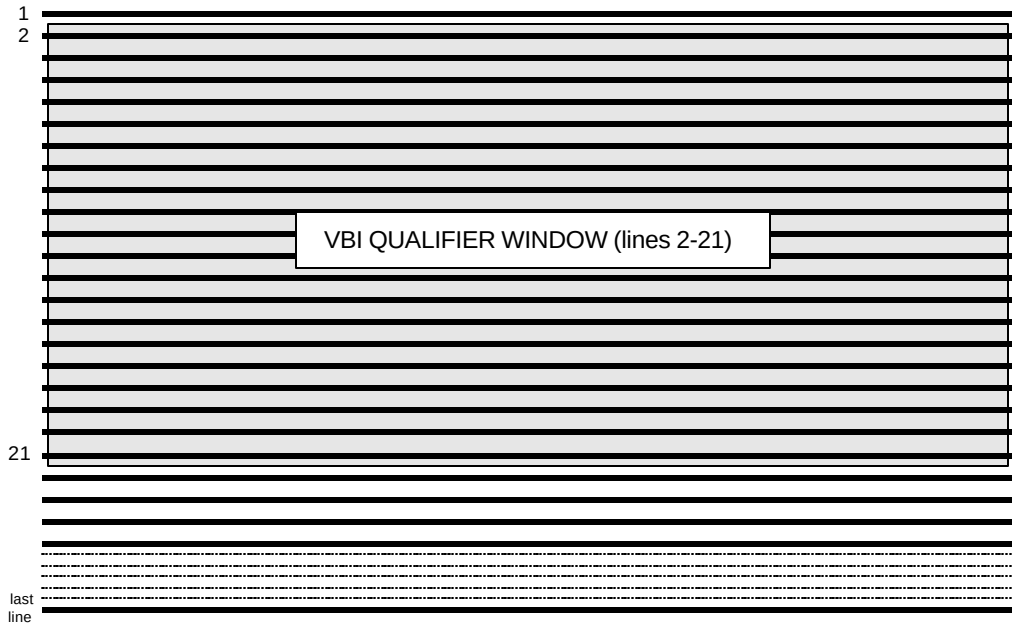
D7	D6	D5	D4	D3	D2	D1	D0
	EN_WIN_QUALIFIER						

VBI Window Qualifier:

To enable VBI Window Qualifier, bit d4 of VBI_REG (reg.4) should be set to '1'. This will restrict data capture to those lines that are reported "VBI lines" by the video decoder. Normally, the VBI lines are expected to be lines 2-21.

VBI_REG (Reg. 4)

D7	D6	D5	D4	D3	D2	D1	D0
			EN_VBI_QUALIFIER				



Note that if both bits d4 and d6 of VBI_REG (reg.4) are enabled, the data capture window will consist of all lines that are common to the VBI wondow and the given Line Window.

VBI Type Qualifier:

To enable VBI Type Qualifier, bit d7 of VBI_REG (reg.4) should be set to '1', and the desired VBI Type code should be defined in the DATA_TYPE_QUALIFIER[3..0] field (bits d3-d0 of VBI_REG).

VBI_REG (Reg. 4)

D7	D6-D4	D3	D2	D1	D0
EN_TYPE_QUALIFIER		DATA_TYPE_QUALIFIER[3..0]			

Refer to Table 6 for available VBI Data Type codes for this qualifier. Note that the same code should be defined to the video decoder for specific lines in order to get any data that will match this qualifier.

Raw Samples:

To enable Raw Samples, bit d5 of VBI_REG (reg.4) should be set to '1':

VBI_REG (Reg. 4)

D7	D6	D5	D4	D3	D2	D1	D0
		EN_RAW_SAMPLES					

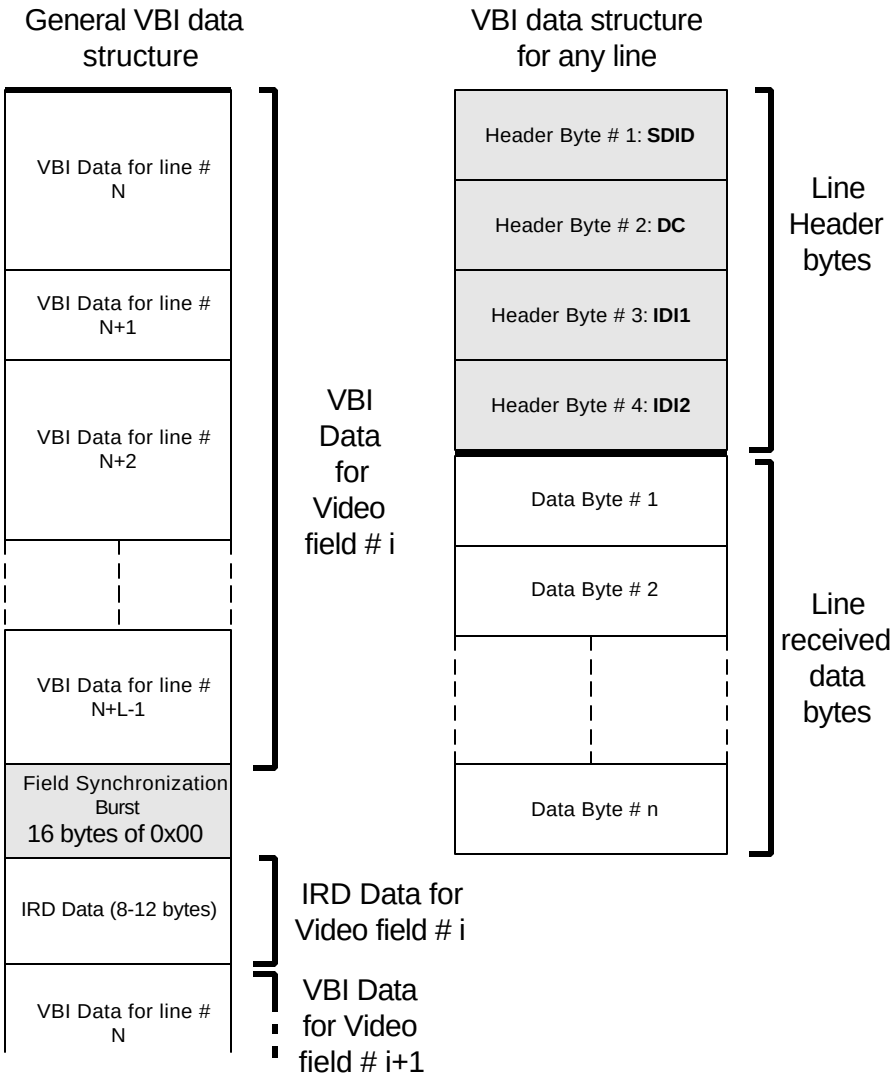
When Raw Samples are enabled, up to 720 raw samples of a VBI line (or any other video line) can be provided for S/W processing.

If the EN_RAW_SAMPLES bit is not set, raw samples are filtered out by default.

2.3 VBI and IRD (Remote Control) Data Format

During the Vertical Blank Time Interval, The VBI Data Qualifier stores the incoming VBI data into the internal 1KByte SRAM. Soon after that, all binary samples from the IRD input (IO_1) are added (about 8-12 bytes per video field). It is assumed that the total VBI data and IRD data in a single video field never exceeds the 1KB boundary, and that all accumulated data can be transfered via the Bulk port until the beginning of next Blank Interval.

The data that is transfered to the host computer via the Bulk interface contains an additional Field Synchronization Burst (which is produced after the VBI data and before the IRD data), and is specified in the following diagrams:


General VBI data structure
VBI data structure for any line
VBI Data for line # N
VBI Data for line # N+1
VBI Data for line # N+2
VBI Data for line # N+L-1
Field Synchronization Burst
16 bytes of 0x00
IRD Data (8-12 bytes)
VBI Data for line # N
VBI Data for Video field # i
IRD Data for Video field # i
VBI Data for Video field # i+1
Header Byte # 1: SDID
Header Byte # 2: DC
Header Byte # 3: IDI1
Header Byte # 4: IDI2
Line Header bytes
Data Byte # 1
Data Byte # 2
Data Byte # n
Line received data bytes

The following tables specifies the Line Header bytes:

SDID

D7	D6	D5	D4	D3	D2	D1	D0
'1'	'0'	'0'	'0'	'0'	'1'	'0'	'1'

DC

D7	D6	D5	D4	D3	D2	D1	D0
'1'	'0'	DC5	DC4	DC3	DC2	DC1	DC0

DC[5:0] is the number of data bytes that were actually received in this line. Note that this number may be different than the expected number of data bytes, due to noise or corruption in the received analog signal.
DC[5:0]='000000' means that no data bytes follow the Line Header.

IDI1

D7	D6	D5	D4	D3	D2	D1	D0
OP	FID	L8	L7	L6	L5	L4	L3

L[8:3] : MSbits of Line Number (look for LSbits 2:0 in IDI2 byte).

FID : Field Identifier. '0' means FIRST field, '1' means SECOND field.

OP is Odd Parity bit. Examp.: D6:D0='0000101' ==> OP='1', IDI1=0x85.

IDI2

D7	D6	D5	D4	D3	D2	D1	D0
OP	L2	L1	L0	DT3	DT2	DT1	DT0

OP is Odd Parity bit. Examp.: D6:D0='1110000' ==> OP='0', IDI1=0x70.

L[2:0] : LSbits of Line Number (look for MSbits 8:3 in IDI1 byte).

DT[3:0] defines the VBI Data Type for the given line. The host computer should define the Data Type per every VBI line (lines between 2-21). The video decoder needs this information in order to look for the given data type per line (there is no auto detect). Regardless of decoding success, the same data type code that was programmed by the host controller will be returned in the DT[3:0] nibble.

The following table specifies the Data Type codes (DT[3:0]):

Table 6 - VBI DATA TYPE CODES

DT[3:0]	VBI Data Type	Standard	Expected number of Data bytes
0000	Teletext EuroWST, CCST	WST625	42
0001	European Closed Caption	CC625	2
0010	Video Programming Service	VPS	26
0011	Wide screen signalling bits	WSS	14
0100	US Teletext (WST)	WST525	34
0101	US Closed Caption (line 21)	CC525	2
0110	Video Component signal	S/W mode	718
0111*	Oversampled CVBS data (do not use)	** intercast **	
1000	Teletext	General Text	42
1001	VITC/EBU time codes (Europe)	VITC625	11
1010	VITC/EBU time codes (USA)	VITC625	11
1011*	reserved (do not use)		
1100	US NABTS	NABTS	34
1101	MOJI (Japanese)	Japtext	35
1110	Japanese format switch (L20/22)	JFS	26
1111*	Active Video Region (do not use)		718

The IRD (Remote Control) data Header byte contains two fields as specified bellow. It is followed by 7 to 11 bytes (depends one broadcast system PAL/NTSC, and sampling phase):

IR_HEADER

D7	D6	D5	D4	D3	D2	D1	D0
'0'	'1'	'1'	'1'	IRD_LENGTH			

IRD_LENGTH contains the number of bytes for IRD data samples that follow the header.

3. Bulk Interface

The Bulk Interface in the ZR36505 is capable of transferring serial data from the 1KB buffer to the ZR36504 at a bit rate of up to 2Mbit/sec.

The Bulk channel takes advantage of the existing interface for the audio codec. In order to work simultaneously with the audio channel, the ZR36505 stops the data transfer from time to time - as specified in the Bulk waveform diagram.

The ZR36505 pins for the Bulk interface are BCLK, DAT_OUT, BLK_EN, BLK_FULL, and FS_L. The signal FS_L is monitored by the ZR36505 in order to coexist with the audio channel (if exists).

The following parameters in the BLK_OPER_MODE register (reg. 5) must be properly defined to match the ZR36504 setup:

BLK_OPER_REG (Reg. 5)

D7	D6-D4	D3	D2	D1	D0
BLK_IO_EN	resrved	BCLK_RATE	AUDIO_DAT	AUDIO_RATE	AUDIO_STEREO

BLK_IO_EN - This bit enables the ZR36505 Bulk control output signals. When this bit is '0', the DAT_OUT and BLK_EN pins are constant Hi-Z.

BCLK_RATE - This bit defines the BCLK frequency, and must match the appropriate parameter that is programmed in the AUDO_CONT register of the ZR36504(Reg.50, d7-d6). BCLK_RATE='1' defines 2048KHz (= '11' in NT1004), and BCLK_RATE='0' defines 1544KHz (= '10' in NT1004).

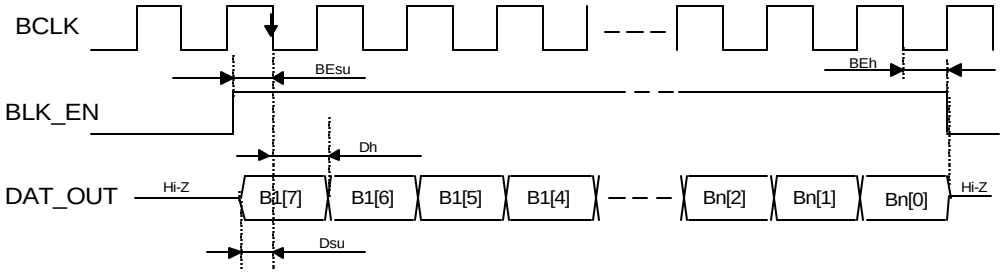
AUDIO_DAT - This bit defines whether or not the audio channel is active, and must match the appropriate parameter that is programmed in the AUDO_CONT register of the ZR36504(Reg.50, d0). AUDIO_DAT='1' defines audio active (= '1' in NT1004), and AUDIO_DAT='0' defines that there is no audio data sharing the bus (= '0' in NT1004).

AUDIO_RATE - This bit defines the audio sampling rate, and must match the appropriate parameter that is programmed in the AUDO_CONT register of the ZR36504(Reg.50, d5). AUDIO_RATE='1' defines 16Ks/sec (= '1' in NT1004), and AUDIO_RATE='0' defines 8Ks/sec (= '0' in NT1004).

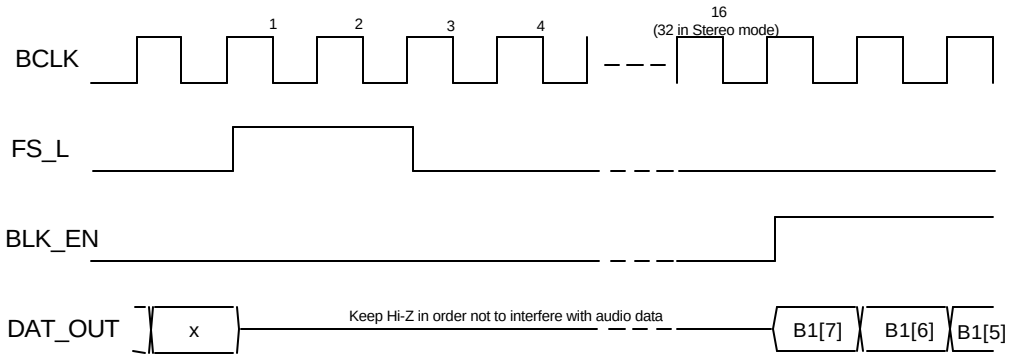
AUDIO_STEREO - This bit defines the audio stereo/mono mode, and must match the appropriate parameter that is programmed in the AUDO_CONT register of the

ZR36504(Reg.50, d4). AUDIO_STEREO='1' defines Stereo mode (= '1' in NT1004), and AUDIO_STEREO ='0' defines Mono mode (= '0' in NT1004).

The following waveform diagrams specify the procedure and timings for the ZR36505 Bulk interface. Note that the output data is supposed to be sampled on the falling edge of the BCLK clock signal. The BLK_EN output is set to '1' to indicate the beginning of a byte sequence; it always turns to '1' before the most significant bit of the first byte, and returns to '0' after the least significant bit of the last byte in sequence. When the BLK_FULL input signal turns '1', the ZR36505 waits (by switching BLK_EN to '0') until the BLK_FULL indication returns to '0'.



If the audio channel is enabled (bit d2 of Reg.5 is '1'), the ZR36505 waits at least 16 clock cycles after the FS_L pulse before beginning to send its own data (if bit d0 of Reg.5 is '1', it waits for 32 clock cycles). During this time it keeps the DAT_OUT signal in the Hi-Z state, in order not to interfere with the audio data.



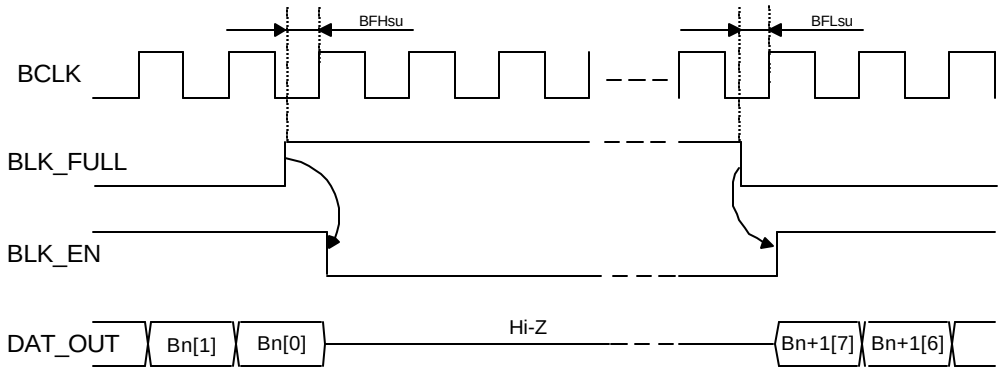


Table 7 - BULK INTERFACE TIMINGS

Parameter	Symbol	Min	Max	Unit
Setup Time from BLK_EN High to BCLK Low	BEsu	100	-	ns
Hold Time from BCLK Low to BLK_EN Low	BEh	100	-	ns
Setup Time from DAT_IN valid to BCLK Low	Dsu	100	-	ns
Hold Time from BCLK Low to DAT_IN valid	Dh	100	-	ns
Setup Time from BLK_FULL High to BCLK High	BFHsu	80	-	ns
Hold Time from BLK_FULL Low to BCLK High	BFLsu	0	-	ns
BCLK frequency	Freq.BCLK	1544	2048	KHz

4. Programmable I/O Pins

The ZR36505 has two programmable I/O pins for general purpose usage. These are IO-1 and IO-2 pins, which are Open-Drain.

Each of these pins - if used - must be connected to an external pull-up resistor to 3.3v (if not used, it can be tied to GND). The external pull-up resistor should be in the range 1-10KΩ.

To use these pins as inputs, the host computer should write '1' to the appropriate bit in the IO_REG register (reg. 6); these are IO_1 and IO_2 bits respectively. In this condition, the voltage level presented on the IO-1 or IO-2 pin can be read by the host computer via the appropriate bit ('0' represents <0.8v, '1' represents >2.0v).

To use these pins as outputs, the host computer should write the output value to the appropriate bit in the IO_REG register; In this condition, and assuming that no external device forces the voltage level presented on the IO-1 or IO-2 pin, the written value will be reflected out ('0' will generate 0v, '1' will generate 3.3-5.0v).

IO_REG (Reg. 6)

D7	D6	D5	D4	D3	D2	D1	D0
resrved	resrved	resrved	resrved	resrved	resrved	IO_2	IO_1

Upon a Soft Reset operation, the IO-1 and IO-2 pins are cleared to '0'.

5. Soft Reset operation

It is strongly recommended that the S/W application will perform a Soft Reset to the ZR36505 prior to any other operation. All registers will contain their default values after this operation (refer to table 4 for default values).

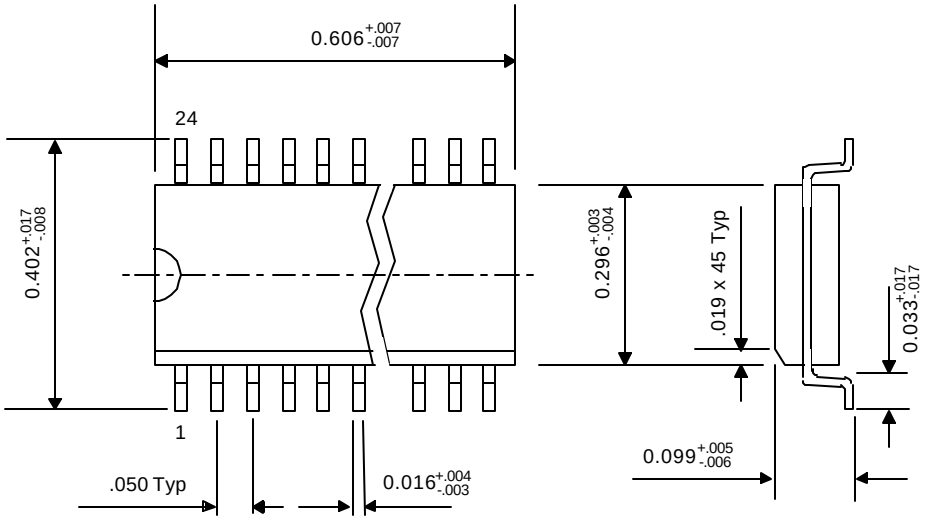
To perform a Soft Reset, the value 0x01 must be written in the SOFT_RESET register (reg. 7). There is no need to write 0x00 after writing 0x01, because this register is automatically cleared.

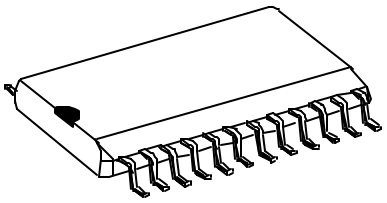
SOFT_RESET (Reg. 7)

D7-D1	D0
resrved	SOFT_RESET

6. Mechanical Specification

Dimensions in inches.





24-pin 300-Mil SOIC GULL WING

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