Features

- **A/D conversion with 6-bit resolution**
- **Time base programmable from 50ns to 3.27 ms (at a clock frequency of 20 MHz)**
- **Trigger Modes: Auto, Internal + /-, External + /-**
- **5 discrete trigger levels**
- **Internal SRAM for 128 values**
- **SRAM bypass mode**
- **Shift of base line by adjustable offset**
- **Supply voltage 5 Volts**
- **Bidirectional µC interface**
- **Power-down for analog part**
- **PLCC44 package**

Application

The Graphic Signal Monitor IC was developed for visualization of the time behavior of electrical signals. Interaction with an external µC makes it possible to achieve the functionality of a one-channel digital storage oscilloscope with additional digital voltmeter function.

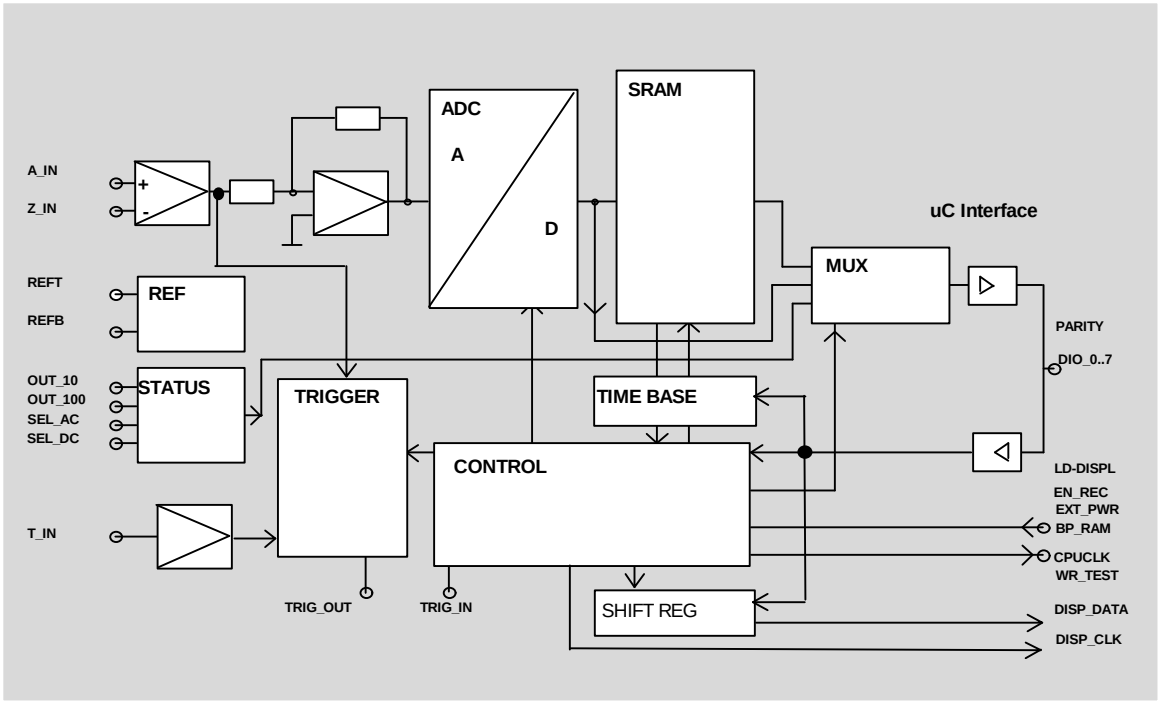
The small dimensions as well as a minimum of external wiring facilitate both the application in miniaturized measuring devices for service and test area, and placement near the front panels in control panels and switch cabinets.

Description

After the parameters of time basis, trigger level and trigger mode have been loaded into the control register, the recording starts as soon as the trigger condition occurs. This procedure ends when 128 times 6 bit data have been written from the flash A/D converter into the internal SRAM.

Afterwards, an externally connected microcontroller can read the data and formate it for an LC display or for transmission via an interface.

Block Diagram



Functional Description

The **input amplifier** serves for impedance matching and amplifies the input signal.

In order to allow also bipolar input signals to be processed even if there is only one supply voltage, a level shift takes place in the input amplifier. Using an external potentiometer, such shift can be varied into a **base line shift.**

The measuring range can be extended by connection of an external voltage divider. An AC input can be implemented by means of an additional external capacitor. Two special inputs of the integrated circuit can be connected with the external voltage divider; they supply a low current during the measurement pauses. The resulting voltage at the pins indicates the selected measurement range. Two more pins have been provided for detection of the selected signal coupling type. The external AC/DC switch is to tie the pins to ground. The status information about measurement range and coupling type, multiplexed with the measured data, is provided for interpretation at the **bidirectional interface**.

The measured signal is digitized in an **analog-to-digital converter** operating according to the flash principle. When the measurement is activated, it converts the input signal into a 6-bit digital word at a fixed conversion rate of 20 MHz.

The 63 comparators of the flash ADC consist of a differential stage with subsequent latch.

For storaging the measured data, the integrated circuit contains an **SRAM** which is 6 bits wide and 128 values deep**.**

The SRAM Write signal is generated by the **Time Base** unit by means of a programmable shift register.

The time base is freely selectable within the range from 2^0 to 2^{16} times the clock period.

Connection with a 20-MHz quartz will result in a range from 50ns to 3,27ms.

The RAM bypass mode creates more possibilities of application; the values are output directly to the bidirectional interface, not into the RAM.

The measurement can be initiated by an external signal or, controlled by the **trigger logic**, depending on the level of the input signal, in an automatic or edge- and level triggered mode.

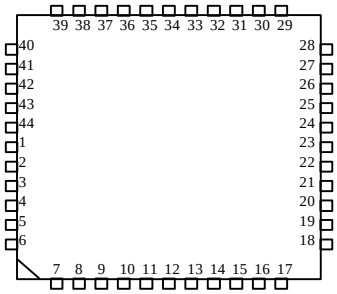
For this purpose, there is a comparator, the reference level of which can be selected in five discrete stages. The comparator has been provided with a hysteresis for noise suppression.

The **Control** unit coordinates the circuit functions, such as the data exchange via the interface. Measured data and status information are output in parallel. The loading of the time base, trigger level, trigger mode parameters into registers, which is uncritical with regard to time, is done serially via 2 pins of the bidirectional interface.

The analog part of the circuit is activated only during the short data recording time, which significantly reduces the total power consumption.

For special applications, e. g. for control of an LCD module, a **shift register** has been implemented. Loading of information into the shift register is parallel, while the output is serial via two pins.

Pin Configuration



Pin Description

Pin	Name	IN/OUT	Description	Pin	Name	IN/OUT	Description
Power Supply Connections				**Digital Outputs**			
29	VDD		Pos. supply voltage, digital	8	PD	O (ub)	Analog power-down
38	VDDA		Pos. supply voltage, analog	31	CPUCLK	O	5 MHz clock (for processor)
17	VSS		Neg. supply voltage, digital	30	WR_TEST	O	RAM Write mode active
3	VSSA		Neg. supply voltage, analog	36	TRIG_OUT	O	Trigger output
44	AGND		Signal ground	32	DISP_CLK	O	1.25 MHz clock (Display data clock)
Analog Inputs				33	DISP_DATA	O	Display data serial
43	A_IN	I	Analog signal input	**Data I/Os**			
42	T_IN	I	Trigger signal input	20	PARITY	bid	Bid. data pin (parity)
41	Z_IN	I	Zero-level input	28...21	DIO_0...7	bid	Bidirectional data interface
Digital Inputs				**Analog Outputs**			
1	OUT_10	I (puc)	Status 1 (10V area switch)	6	REFT	O	Reference voltage (top)
2	OUT_100	I (puc)	Status 2 (100V area switch)	5	REFB	O	Reference voltage (bottom)
10	SEL_AC	I (pu)	Status 3 (AC operation)	4	VED	O	Internal base potential
9	SEL_DC	I (pu)	Status 4 (DC operation)	**External Components**			
34	N_MODE	I (pu)	Control 1 (operating mode)	12	XOUT		Crystal output
35	TRIG_IN	I	Trigger input	13	XIN		Qrystal input
19	EN_REC	I	Enable Record	40	CF		Follower stage, Connection to trim-C
18	LD_DISPL	I	Load Display	39	CZ		Amplifier , Connection to trim-C
16	EXT_PWR	I	Control 2 (external power)	7	CW		A/D converter power bypass capacitor
15	BP_RAM	I	Bypass Ram Mode	**Test Pins**			
				11	TRESULT	O	Test mode output
				14	TEST	I (pd)	Test mode input

pu = Internal Pull-Up puc = Internal Pull-Up Controlled pd= Internal Pull-Down
ub = Unbuffered output

Characteristics (Selection)

Maximum Ratings	Symbol	Min	Typ	Max	Unit
General					
Supply voltage (VDDA= VDD)	V_{DD}	4.75	5.0	5.25	V
Oscillator frequency	f_q			20	MHz
Operating temperature	T	0		70	^oC
Current drain	I_S		60	100	mA
Digital					
Input H-level	V_{IH}	V_{DD}-0.8			V
Input L-level	V_{IL}			0.8	V
Output H-level (2mA, pin32: 8mA))	V_{OH}	2.4			V
Output L-level (-2mA, pin32 -8mA)	V_{OL}			0.4	V
Analog Part					
Input voltage	V_{is},V_{it}	-0.5		+ 0.5	V
Input resistance	R_{is},R_{id}	100			MΩ
Input capacitance	C_{is},C_{it}			5	pF
A/D Converter					
Resolution	radc		6		Bit
Differential non-linearity	DNL			0.8	LSB
Integral non-linearity	INL			1	LSB

Notes for Application

Before starting the measurement, the parameters of time base, trigger level and trigger mode are to be serially loaded to DIO(0) (clock) and DIO(1) (data) by the microcontroller.

The recording of measured values is prepared by activation of EN_REC.

Then, the IC outputs the status of the 4 pins for measurement range and AC/DC coupling to DIO(2 to 5) (parallel), until a High pulse is applied to the LD_DISPL pin.

The integrated circuit is now ready to record measured values, which happens as soon as the trigger condition occurs.

Subsequently, the microcontroller, by clocking of LD_DISPL, reads out the contents of the SRAM in bit-parallel and byte-serial form at DIO(0 to 5).

The measured data and status information taken over are prepared in the external microcontroller in a way that allows to indicate them on an external LC display or to transfer them to a computer, for instance, formatted according to the RS232-Protocol.

For digital voltmeter functions, the microprocessor can calculate the average value of all 128 recorded measured values, and, by multiplying them by 0.7, it can determine the approximate effective value. This value can be shown on the display as well.

A shift register is available in the integrated circuit for special applications. In the application shown below, it controls an LCD module of 16 x 32 pixels. The microcontroller loads the data available in parallel at DIO (0 to 7) as well as the parity information into the register.

The process of loading is controlled by means of the signals EN_REC and LD_DISPL. A start and stop bit are added, then the output takes place at DISP_CLK (data) and DISP_DATA (data).

When using the ZM407, it is absolutely necessary to ensure synchronous operation of the system. Therefore, a 5-MHz system clock for an external microcontroller is provided at the CPUCLK pin.

Multi-channel recording is possible by cascading of several SCOPE ICs. In this case, one TRIG_OUT output will control several TRIG_IN inputs.

Application Circuit