P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVP0540A

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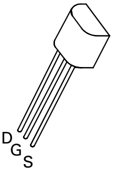
FEATURES

- 400 Volt V_{DS}
- $R_{DS(on)}$=150Ω



E-Line
TO92 Compatible

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	-400	V
Continuous Drain Current at T_{amb}=25°C	I_D	-45	mA
Pulsed Drain Current	I_{DM}	-400	mA
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at T_{amb}=25°C	P_{tot}	700	mW
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	-400		V	I_D=-1mA, V_{GS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-4.5	V	ID=-1mA, V_{DS}= V_{GS}
Gate-Body Leakage	I_{GSS}		20	nA	V_{GS}=± 20V, V_{DS}=0V
Zero Gate Voltage Drain Current	I_{DSS}		-20 -2	µA mA	V_{DS}=-400 V, V_{GS}=0 V_{DS}=-320 V, V_{GS}=0V, T=125°C(2)
On-State Drain Current(1)	$I_{D(on)}$	-100		mA	V_{DS}=-25 V, V_{GS}=-10V
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		150	Ω	V_{GS}=-10V,I_D=-50mA
Forward Transconductance(1)(2)	g_{fs}	40		mS	V_{DS}=-25V,I_D=-50mA
Input Capacitance (2)	C_{iss}		120	pF	V_{DS}=-25 V, V_{GS}=0V, f=1MHz
Common Source Output Capacitance (2)	C_{oss}		20	pF	
Reverse Transfer Capacitance (2)	C_{rss}		5	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		10	ns	V_{DD}≈-25V, I_D=-50mA
Rise Time (2)(3)	t_r		15	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		15	ns	
Fall Time (2)(3)	t_f		20	ns	

(1) Measured under pulsed conditions. Width=300µs. Duty cycle ≤2%

(2)