

SOT23 P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVP3310F

ISSUE 3 – OCTOBER 1995

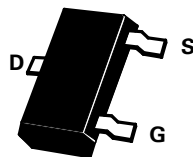


FEATURES

- * 100 Volt V_{DS}
- * $R_{DS(on)}=20\Omega$

COMPLEMENTARY TYPE - ZVN3310F

PARTMARKING DETAIL - MR



ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	-100	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	I_D	75	mA
Pulsed Drain Current	I_{DM}	-1.2	A
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}C$	P_{tot}	330	mW
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}C$

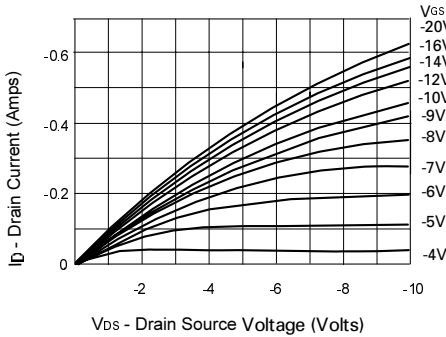
ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	-100		V	$I_D=-1mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	$I_D=-1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		-20	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	I_{DSS}		-1 -50	μA μA	$V_{DS}=-100V, V_{GS}=0$ $V_{DS}=-80V, V_{GS}=0V, T=125^{\circ}C(2)$
On-State Drain Current(1)	$I_{D(on)}$	-300		mA	$V_{DS}=-25V, V_{GS}=-10V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		20	Ω	$V_{GS}=-10V, I_D=-150mA$
Forward Transconductance (1)(2)	g_{fs}	50		mS	$V_{DS}=-25V, I_D=-150mA$
Input Capacitance (2)	C_{iss}		50	pF	$V_{DS}=-25V, V_{GS}=0V, f=1MHz$
Common Source Output Capacitance (2)	C_{oss}		15	pF	
Reverse Transfer Capacitance (2)	C_{rss}		5	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		8	ns	$V_{DD}\approx -25V, I_D=-150mA$
Rise Time (2)(3)	t_r		8	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		8	ns	
Fall Time (2)(3)	t_f		8	ns	

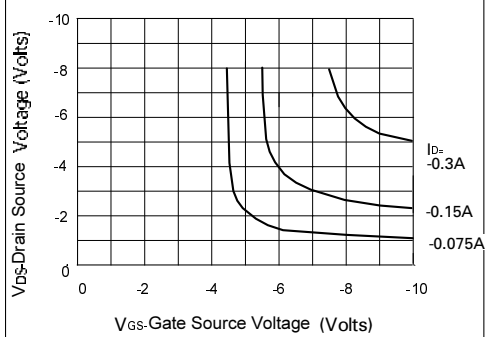
(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$ (2) Sample test.

(3) Switching times measured with 50 Ω source impedance and <5ns rise time on a pulse generator

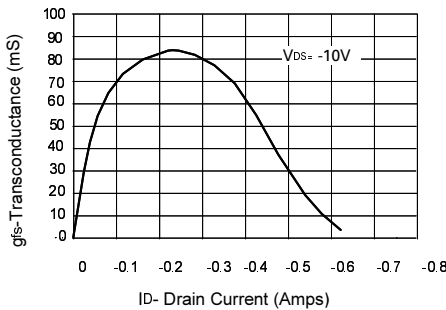
TYPICAL CHARACTERISTICS



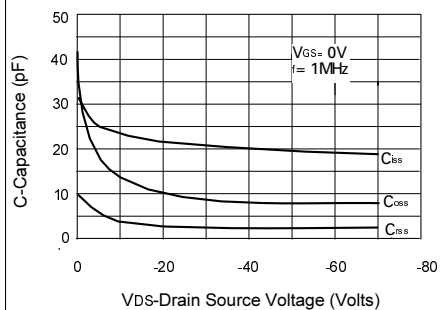
Saturation Characteristics



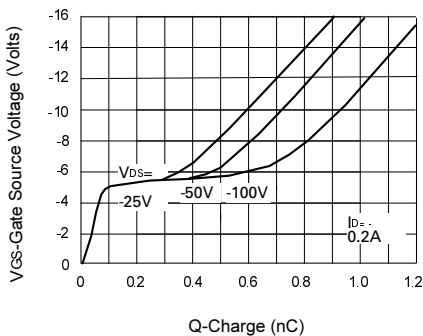
Voltage Saturation Characteristics



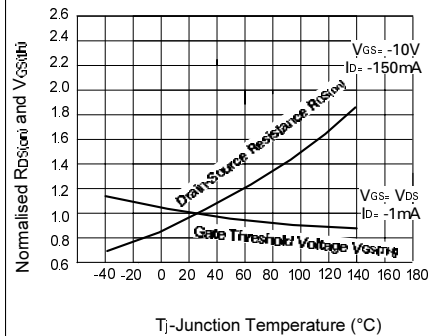
Transconductance v drain current



Capacitance v drain-source voltage



Gate charge v gate-source voltage



Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v Temperature