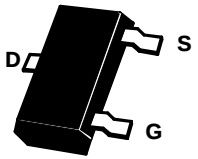
# SOT23 N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

**ISSUE 2 – DECEMBER 1995**

# ZVN4106F

PARMARKING DETAIL - MZ




## ABSOLUTE MAXIMUM RATINGS.

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 60 | V |
| Continuous Drain Current at $T_{amb}$=25°C | $I_D$ | 0.2 | A |
| Pulsed Drain Current | $I_{DM}$ | 3 | A |
| Gate-Source Voltage | $V_{GS}$ | ± 20 | V |
| Max Power Dissipation at $T_{amb}$=25°C | $P_{tot}$ | 330 | mW |
| Operating and Storage Temperature Range | $T_j$:$T_{stg}$ | -55 to +150 | °C |

## ELECTRICAL CHARACTERISTICS (at $T_{amb}$ = 25°C unless otherwise stated).

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT | CONDITIONS. |
|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 60 | | V | $I_D$=1mA, $V_{GS}$=0V |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | 1.3 | 3 | V | $I_D$=1mA, $V_{DS}$= $V_{GS}$ |
| Gate-Body Leakage | $I_{GSS}$ | | 100 | nA | $V_{GS}$=± 20V, $V_{DS}$=0V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | | 10<br>50 | µA<br>µA | $V_{DS}$=60V, $V_{GS}$=0<br>$V_{DS}$=48V, $V_{GS}$=0V, T=125°C(2) |
| On-State Drain Current(1) | $I_{D(on)}$ | 1 | | A | $V_{DS}$=25V, $V_{GS}$=10V |
| Static Drain-Source On-State Resistance (1) | $R_{DS(on)}$ | | 2.5<br>5 | Ω<br>Ω | $V_{GS}$=10V, $I_D$=500mA<br>$V_{GS}$=5V, $I_D$=200mA |
| Forward Transconductance(1)(2) | $g_{fs}$ | 150 | | mS | $V_{DS}$=25V, $I_D$=250mA |
| Input Capacitance (2) | $C_{iss}$ | | 35 | pF | $V_{DS}$=25V, $V_{GS}$=0V, f=1MHz |
| Common Source Output Capacitance (2) | $C_{oss}$ | | 25 | pF | |
| Reverse Transfer Capacitance (2) | $C_{rss}$ | | 8 | pF | |
| Turn-On Delay Time (2)(3) | $T_{d(on)}$ | | 5 | ns | $V_{DD}$≈25V, $I_D$=150mA |
| Rise Time (2)(3) | $T_r$ | | 7 | ns | |
| Turn-Off Delay Time (2)(3) | $T_{d(off)}$ | | 6 | ns | |
| Fall Time (2)(3) | $T_f$ | | 8 | ns | |

(1) Measured under pulsed conditions. Width=300µs. Duty cycle ≤2% (2) Sample test.
(3) Switching times measured with 500Ω source impedance and <5ns rise time on a pulse generator
Spice parameter data is available upon request for this device

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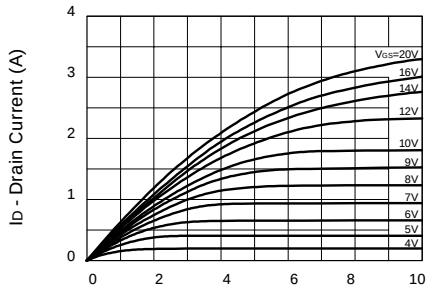
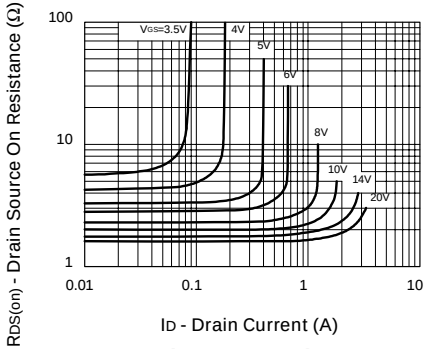
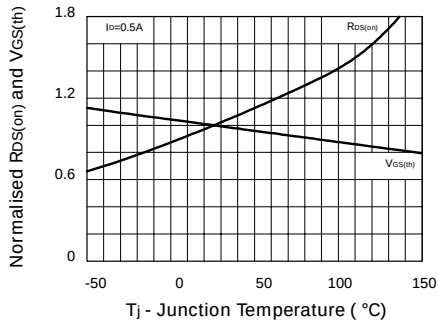


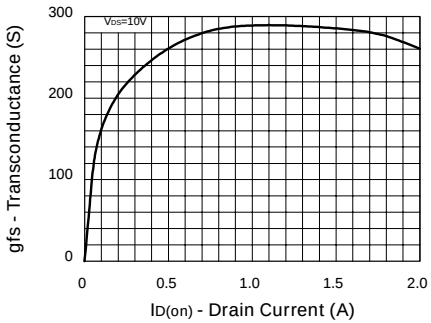

**Saturation Characteristics**



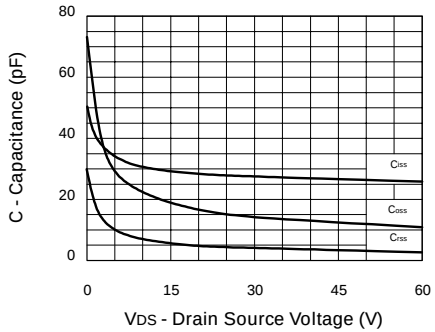

**On-Resistance v Drain Current**



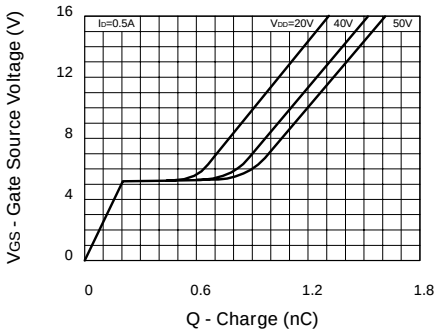

**Normalised $R_{DS(on)}$ & $V_{GS(th)}$ v Temperature**




**Transconductance v Drain Current**




**Capacitance v Drain Source Voltage**




**Gate Source Voltage v Gate Charge**