

MOS INTEGRATED CIRCUIT

Z78F9418A

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The Z78F9418A is a product in the Z789417A Subseries (for driving LCD) of the 78K/0S Series.

The Z78F9418A has flash memory in place of the internal ROM of the Z789415A, Z789416A, and Z789417A.

Because flash memory allows the program to be written and erased electrically with the device mounted on the board, this product is ideal for the evaluation stages of system development, small-scale production, and rapid development of new products.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

Z789407A, Z789417A Subseries User's Manual: U13952E

78K/0S Series User's Manual Instructions: U11047E

FEATURES

- Pin compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 32 KB
- Internal data memory
 - High-speed RAM: 512 bytes
 - LCD display RAM: 28 bytes
- Minimum instruction execution time can be changed from high-speed (0.4 μ s:@ 5.0 MHz operation with main system clock) to ultra-low-speed (122 μ s:@ 32.768 kHz operation with subsystem clock)
- I/O port: 43 pins
- Serial interface: 1 channel
3-wire serial I/O mode/UART mode selectable
- 10-bit resolution A/D converter: 7 channels
- Timer: 6 channels
 - 16-bit timer: 1 channel
 - 8-bit timer/event counter: 2 channels
 - 8-bit timer: 1 channel
 - Watch timer: 1 channel
 - Watchdog timer: 1 channel
- LCD controller/driver
 - Segment signal: 28 pins MAX.
 - Common signal: 4 pins MAX.
 - 1/2- or 1/3-bias selectable
- Supply voltage : V_{DD} = 1.8 to 5.5 V

APPLICATIONS

APS compact cameras, blood pressure gauges, rice cookers, etc.

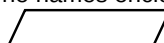
ORDERING INFORMATION

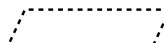
Part Number	Package
Z78F9418AGC-8BT	80-pin plastic QFP (14 × 14 mm)
Z78F9418AGK-9EU	80-pin plastic TQFP (fine pitch) (12 × 12 mm)

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.

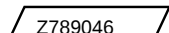
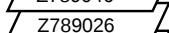
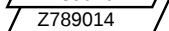
 Products in mass production

 Products under development

Y subseries is products with SMB support.

For small-scale general-purpose applications

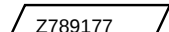
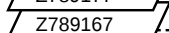
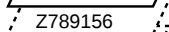
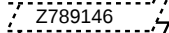
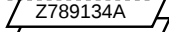
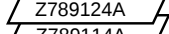
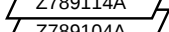
44-pin
42/44-pin
28-pin

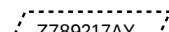
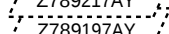
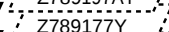
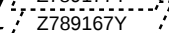
 Z789046
 Z789026
 Z789014

Z789026 with internal subsystem clock
Z789014 with enhanced timer and expanded ROM and RAM
On-chip UART and capable of low-voltage (1.8 V) operation

For small-scale general-purpose applications and A/D function

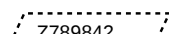
44/48-pin
44/48-pin
44-pin
44-pin
30-pin
30-pin
30-pin
30-pin
30-pin
30-pin

 Z789177
 Z789167
 Z789156
 Z789146
 Z789134A
 Z789124A
 Z789114A
 Z789104A

 Z789217AY RC oscillation version of the Z789197AY
 Z789197AY Z789177 with internal EEPROM™
 Z789177Y Z789167 with enhanced A/D converter
 Z789167Y Z789104A with enhanced timer
Z789146 with enhanced A/D converter
Z789104A with EEPROM
Z789124A with enhanced A/D converter
RC oscillation version of the Z789104A
Z789104A with enhanced A/D converter
Z789026 with A/D converter and multiplier

For inverter control

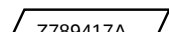
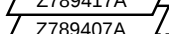
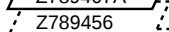
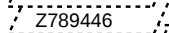
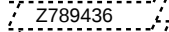
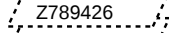
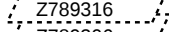
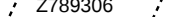
44-pin

 Z789842

On-chip inverter control circuit and UART

For LCD driving

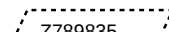
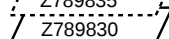
80-pin
80-pin
64-pin
64-pin
64-pin
64-pin
64-pin
64-pin

 Z789417A
 Z789407A
 Z789456
 Z789446
 Z789436
 Z789426
 Z789316
 Z789306

Z789407A with enhanced A/D converter
Z789456 with enhanced I/O
Z789446 with enhanced A/D converter
Z789426 with enhanced display output
Z789426 with enhanced A/D converter
Z789306 with A/D converter
RC oscillation version of the Z789306
Basic subseries for LCD driving

For Dot LCD driving

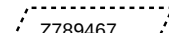
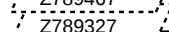
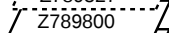
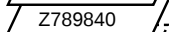
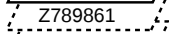
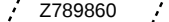
144-pin
88-pin

 Z789835
 Z789830

Segment/common output: 96
Segment: 40, common 16

For ASSP

64-pin
64-pin
44-pin
44-pin
20-pin
20-pin

 Z789467
 Z789327
 Z789800
 Z789840
 Z789861
 Z789860

Z789327 with A/D converter
For remote control, on-chip LCD controller/driver
For PC keyboard, on-chip USB function
For keypad, on-chip POC
RC oscillation version of the Z789860
For keyless entry, on-chip POC and key return circuit

78K/0S
Series

The major functional differences among the subseries are listed below.

Function Subseries Name		ROM Capacity	8-Bit	16-Bit	Watch	WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V _{DD} MIN. Value	Remark
Small-scale general-purpose applications	Z789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	Z789026	4 K to 16 K			–							
	Z789014	2 K to 4 K	2 ch	–						22		
Small-scale general-purpose applications and A/D function	Z789177	16 K to 24 K	3 ch	1 ch	1 ch		–	8 ch	1 ch (UART: 1 ch)	31		–
	Z789167						8 ch	–				
	Z789156	8 K to 16 K	1 ch		–		–	4 ch		20		On-chip EEPROM
	Z789146						4 ch	–				
	Z789134A	2 K to 8 K					–	4 ch				RC oscillation version
	Z789124A						4 ch	–				
	Z789114A						–	4 ch				–
	Z789104A						4 ch	–				
Inverter control	Z789842	8 K to 16 K	3 ch	Note	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
LCD driving	Z789417A	12 K to 24 K	3 ch	1 ch	1 ch	1 ch	–	7 ch	1 ch (UART: 1 ch)	43	1.8 V	–
	Z789407A						7 ch	–				
	Z789456	12 K to 16 K	2 ch				–	6 ch		30		
	Z789446						6 ch	–				
	Z789436						–	6 ch		40		
	Z789426						6 ch	–				
	Z789316	8 K to 16 K					–		2 ch (UART: 1 ch)	23		RC oscillation version
	Z789306											–
Dot LCD driving	Z789835	24 K to 60 K	6 ch	–	1 ch	1 ch	2 ch	–	1 ch	27	1.8 V	–
	Z789830	24 K	1 ch	1 ch			–		1 ch (UART: 1 ch)	30	2.7 V	
ASSP	Z789467	4 K to 24 K	2 ch	–	1 ch	1 ch	1 ch	–	–	18	1.8 V	On-chip LCD
	Z789327		3 ch				–		1 ch			
	Z789800	8 K	2 ch	1 ch	–	1 ch	–		2 ch (USB: 1 ch)	31	4.0 V	–
	Z789840						4 ch		1 ch	29	2.8 V	
	Z789861	4 K		–			–		–	14	1.8 V	RC oscillation version, on-chip EEPROM
	Z789860											On-chip EEPROM

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Item		Function
Internal memory	Flash memory	32 KB
	High-speed RAM	512 bytes
	LCD display RAM	28 bytes
Minimum instruction execution time		0.4 μ s/1.6 μ s (@5.0 MHz operation with main system clock) 122 μ s (@32.768 kHz operation with subsystem clock)
General-purpose register		8 bits $\times$ 8 registers
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test), etc.
I/O port		Total: 43 pins • CMOS input: 7 pins • CMOS I/O: 32 pins • N-ch open drain (12 V): 4 pins
A/D converter		10-bit resolution $\times$ 7 channels
Comparator		Timer output controllable
Serial interface		3-wire serial I/O mode/UART mode selectable: 1 channel
LCD controller/driver		• Segment signal output: 28 pins MAX. • Common signal output: 4 pins MAX. • 1/2 or 1/3 bias selectable
Timer		• 16-bit timer: 1 channel • 8-bit timer: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer output		2 pins
Vectored interrupt source	Maskable	Internal: 12, external: 4
	Non-maskable	Internal: 1
Supply voltage		$V_{DD} = 1.8$ to 5.5 V
Operating ambient temperature		$T_A = -40$ to $+85^\circ\text{C}$
Package		• 80-pin plastic QFP (14 $\times$ 14 mm) • 80-pin plastic TQFP (fine pitch) (12 $\times$ 12 mm)

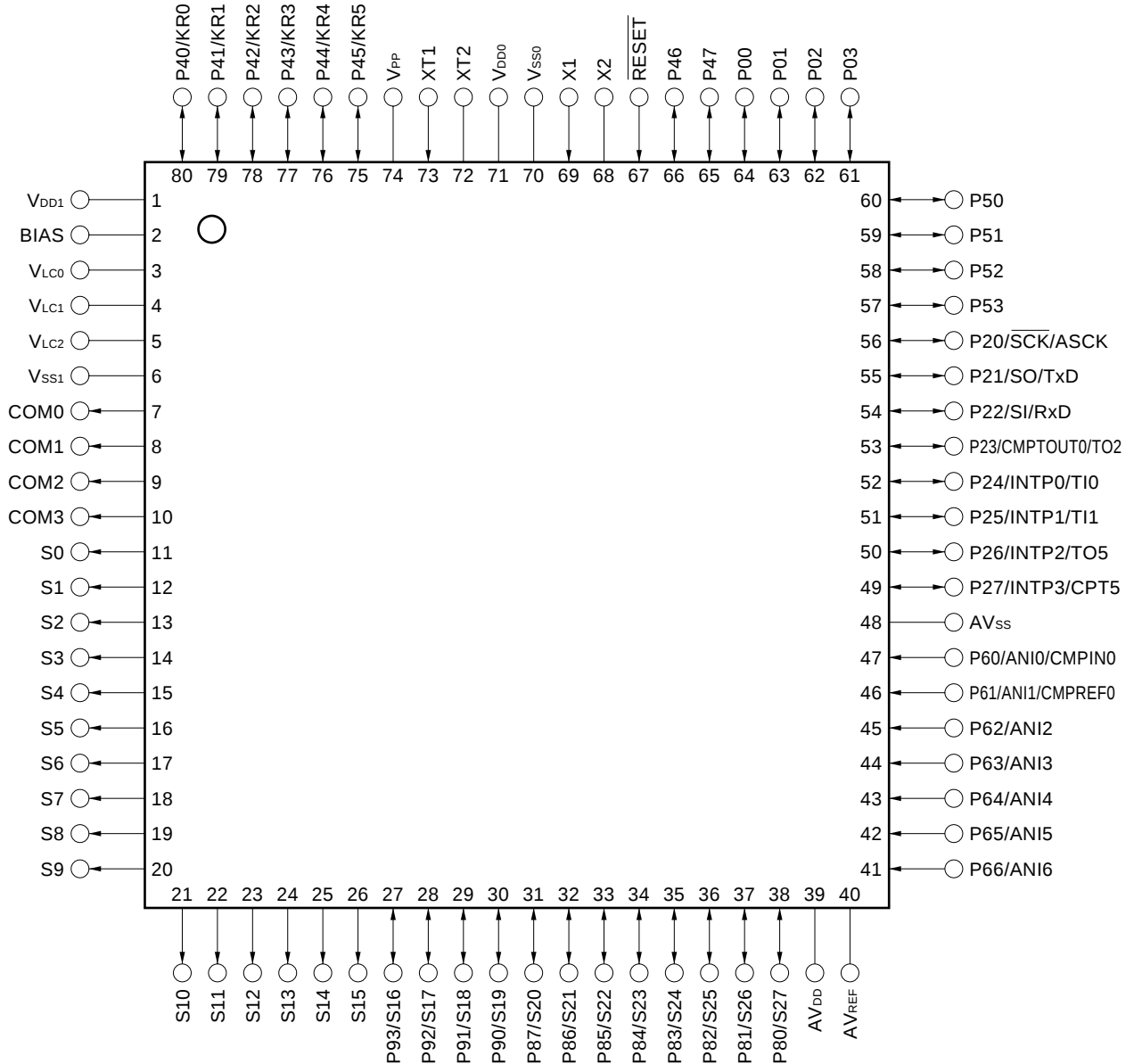
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1. PIN CONFIGURATION (Top View)

• 80-pin plastic QFP (14 x 14 mm)
Z78F9418AGC-8BT

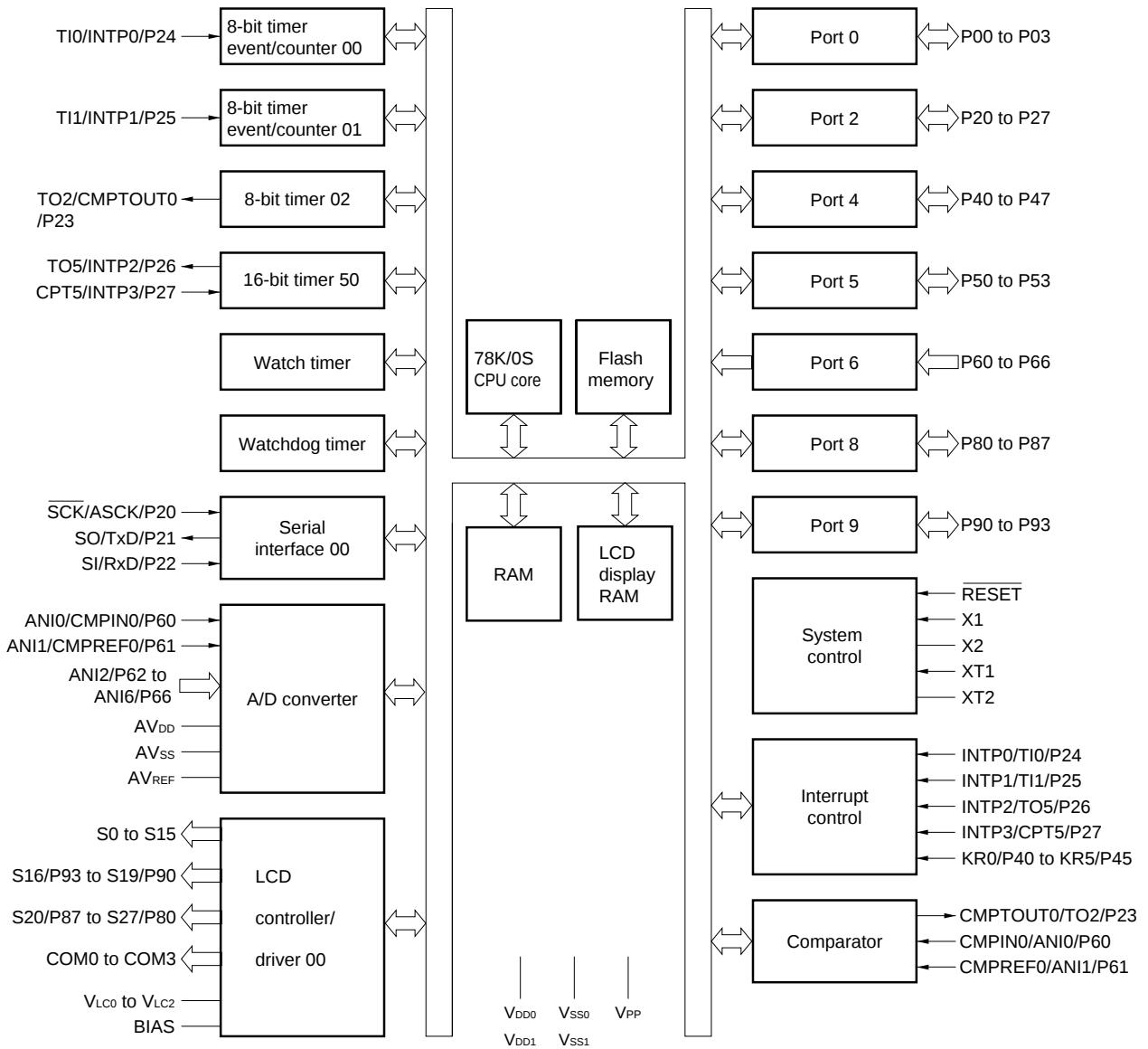
• 80-pin plastic TQFP (fine pitch) (12 x 12 mm)
Z78F9418AGK-9EU



Caution Connect the V_{PP} pin directly to the V_{SS0} or V_{SS1} pin in normal operation mode.

ANI0 to ANI6:	Analog Input	P60 to P66:	Port 6
ASCK:	Asynchronous Serial Input	P80 to P87:	Port 8
AV _{DD} :	Analog Power Supply	P90 to P93:	Port 9
AV _{REF} :	Analog Reference Voltage	RESET:	Reset
AV _{SS} :	Analog Ground	RxD:	Receive Data
BIAS:	LCD Power Supply Bias Control	S0 to S27:	Segment Output
CMPIN0:	Comparator Input	SCK:	Serial Clock
CMREF0:	Comparator Reference	SI:	Serial Input
CMPTOUT0:	Comparator Output	SO:	Serial Output
COM0 to COM3:	Common Output	TI0, TI1:	Timer Input
CPT5:	Capture Trigger Input	TO2, TO5:	Timer Output
INTP0 to INTP3:	Interrupt from Peripherals	TxD:	Transmit Data
KR0 to KR5:	Key Return	V _{DD0} , V _{DD1} :	Power Supply
P00 to P03:	Port 0	V _{LC0} to V _{LC2} :	LCD Power Supply
P20 to P27:	Port 2	V _{PP} :	Programming Power Supply
P40 to P47:	Port 4	V _{SS0} , V _{SS1} :	Ground
P50 to P53:	Port 5	X1, X2:	Crystal (Main System Clock)
		XT1, XT2:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	–
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	$\overline{\text{SCK}}/\text{ASCK}$
P21				SO/TxD
P22				SI/RxD
P23				CMPTOUT0/TO2
P24				INTP0/TI0
P25				INTP1/TI1
P26				INTP2/TO5
P27				INTP3/CPT5
P40 to P45	I/O	Port 4. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	KR0 to KR5
P46, P47				–
P50 to P53	I/O	Port 5. 4-bit N-ch open-drain I/O port. Input/output can be specified in 1-bit units.	Input	–
P60	Input	Port 6. 7-bit input only port.	Input	ANI0/CMPIN0
P61				ANI1/CMPREF0
P62 to P66				ANI2 to ANI6
P80 to P87	I/O	Port 8. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	S27 to S20
P90 to P93	I/O	Port 9. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	S19 to S16

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising, falling, or both rising and falling edges) can be specified	Input	P24/TI0
INTP1				P25/TI1
INTP2				P26/TO5
INTP3				P27/CPT5
KR0 to KR5	Input	Key return signal detection	Input	P40 to P45
SI	Input	Serial interface serial data input	Input	P22/RxD
SO	Output	Serial interface serial data output	Input	P21/TxD
SCK	I/O	Serial interface serial clock input/output	Input	P20/ASCK
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P20/SCK
RxD	Input	Serial data input for asynchronous serial interface	Input	P22/SI
TxD	Output	Serial data output for asynchronous serial interface	Input	P21/SO
TI0	Input	External count clock input to 8-bit timer (TM00)	Input	P24/INTP0
TI1	Input	External count clock input to 8-bit timer (TM01)	Input	P25/INTP1
TO2	Output	8-bit timer (TM02) output	Input	P23/CMPTOUT0
TO5	Output	16-bit timer (TM50) output	Input	P26/INTP2
CPT5	Input	Capture edge input	Input	P27/INTP3
CMPTOUT0	Output	Comparator output	Input	P23/TO2
CMPIN0	Input	Comparator input	Input	P60/ANI0
CMPREF0	Input	Comparator reference voltage input	Input	P61/ANI1
ANI0	Input	Analog input for A/D converter	Input	P60/CMPIN0
ANI1				P61/CMPREF0
ANI2 to ANI6				P62 to P66
AV _{REF}	–	Reference voltage for A/D converter	–	–
AV _{SS}	–	Ground potential for A/D converter	–	–
AV _{DD}	–	Analog power supply for A/D converter	–	–
S0 to S15	Output	Segment signal output of LCD controller/driver	Output	–
S16 to S19			Input	P93 to P90
S20 to S27				P87 to P80
COM0 to COM3	Output	Common signal output of LCD controller/driver	Output	–
V _{LC0} to V _{LC2}	–	LCD driving voltage	–	–
BIAS	–	Supply voltage for LCD driving	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
RESET	Input	System reset input	Input	–

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
V _{DD0}	–	Positive power supply for ports	–	–
V _{DD1}	–	Positive power supply (except ports)	–	–
V _{SS0}	–	Ground potential for ports	–	–
V _{SS1}	–	Ground potential (except ports)	–	–
V _{PP}	–	Flash memory programming mode setting. High-voltage application for program write/verify. In normal operation mode, connect directly to V _{SS0} or V _{SS1} .	–	–

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the I/O circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P03	5-H	I/O	Input: Independently connect to V _{DD0} , V _{DD1} , V _{SS0} , or V _{SS1} via a resistor. Output: Leave open.
P20/SCK/ASCK	8-C		
P21/SO/TxD			
P22/SI/RxD			
P23/CMPTOUT0/TO2	10-B		
P24/INTP0/TI0	8-C		
P25/INTP1/TI1			
P26/INTP2/TO5			
P27/INTP3/CPT5			
P40/KR0 to P45/KR5			
P46, P47	5-H		
P50 to P53	13-T	Input: Independently connect to V _{DD0} or V _{DD1} via a resistor. Output: Leave open.	
P60/ANI0/CMPIN0	9-D	Input	Connect directly to V _{DD0} , V _{DD1} , V _{SS0} , or V _{SS1} .
P61/ANI1/CMPREF0			
P62/ANI2 to P66/ANI6	9-C		
P80/S27 to P87/S20	17-F	I/O	Input: Independently connect to V _{DD0} , V _{DD1} , V _{SS0} , or V _{SS1} via a resistor. Output: Leave open.
P90/S19 to P93/S16			
S0 to S15	17-B	Output	Leave open.
COM0 to COM3	18-A		
V _{LC0} to V _{LC2}	–	–	Leave open (If all V _{LC0} through V _{LC2} are unused, however, independently connect them to V _{SS0} or V _{SS1} via a resistor).
BIAS			
XT1		Input	Connect to V _{SS0} or V _{SS1} .
XT2		–	Leave open.
RESET	2	Input	–
V _{PP}	–	–	Connect directly to V _{SS0} or V _{SS1} .

Figure 3-1. Pin I/O Circuits (1/2)

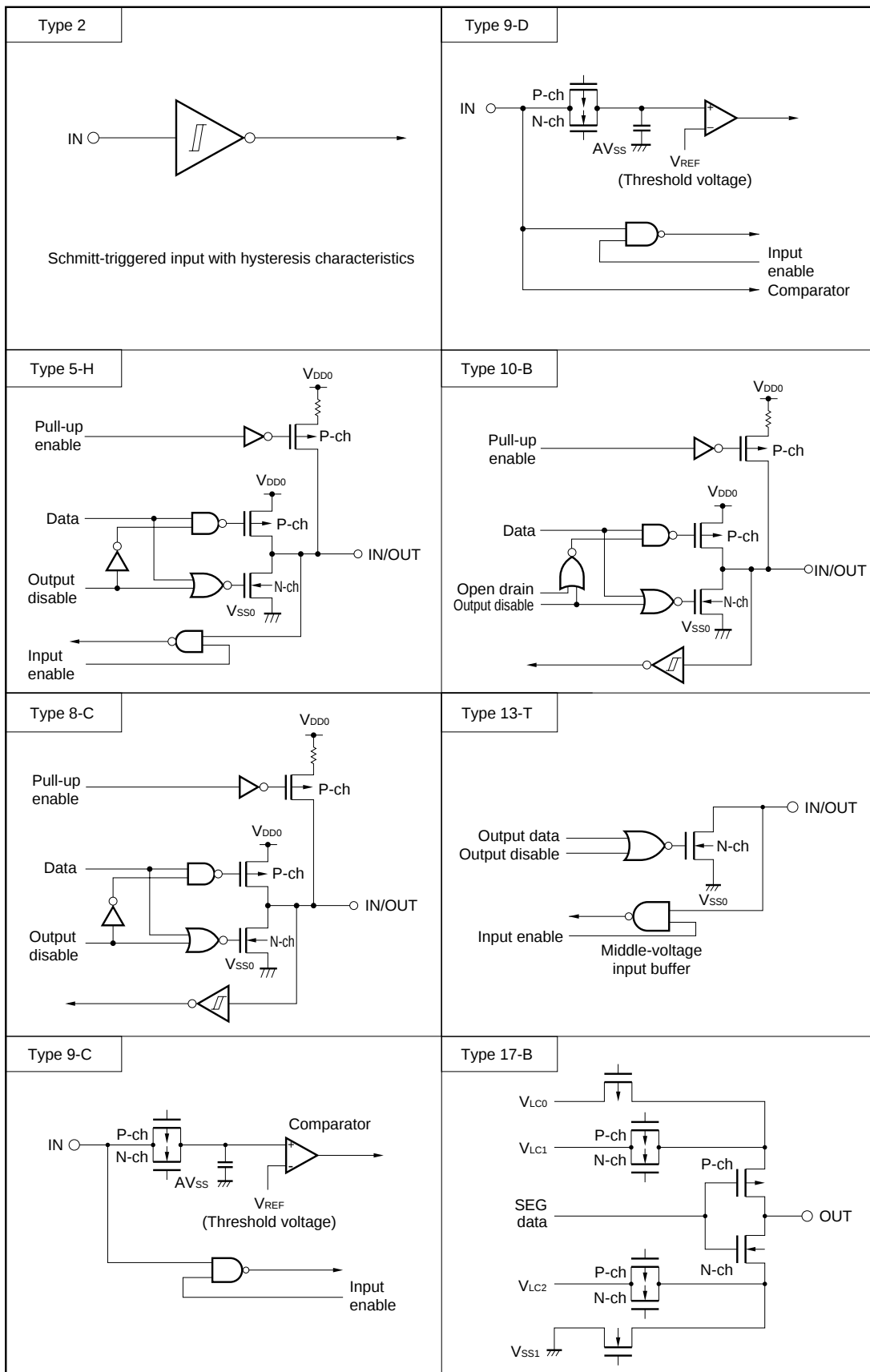
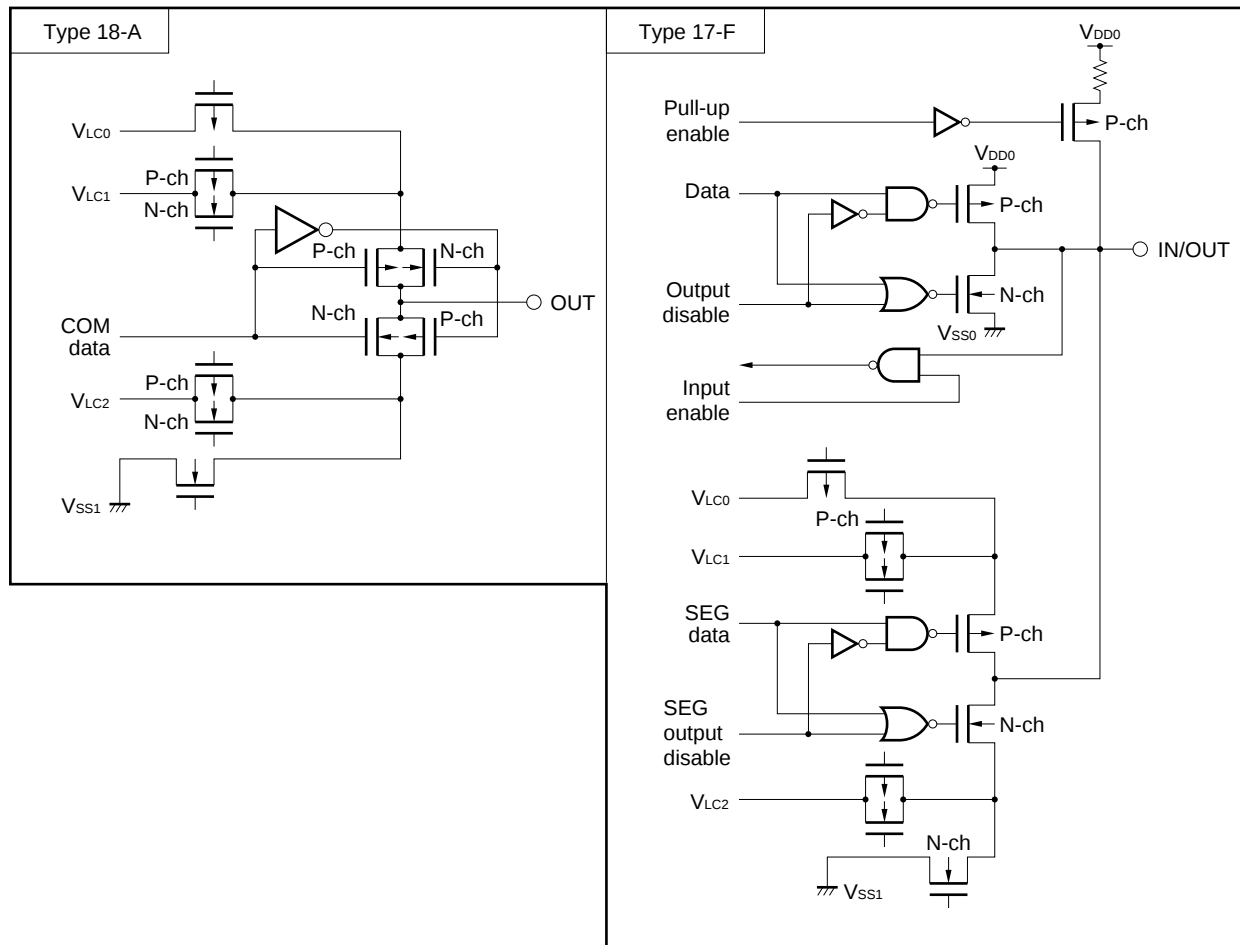


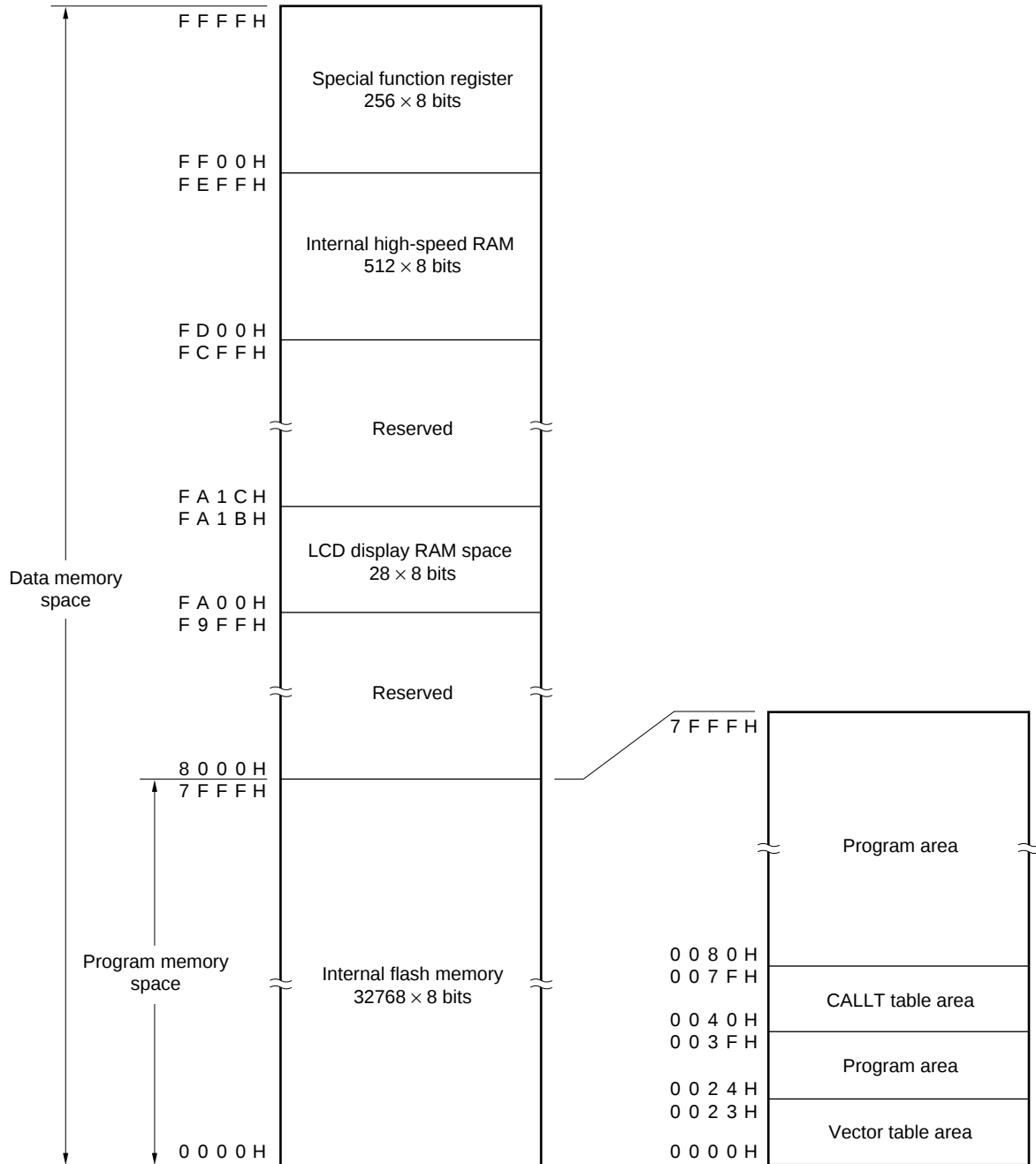
Figure 3-1. Pin I/O Circuits (2/2)



4. MEMORY SPACE

The Z78F9418A can access 64 KB of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



5. FLASH MEMORY PROGRAMMING

The program memory that is incorporated in the Z78F9418A is flash memory.

With flash memory, it is possible to write programs on-board. Writing is performed by connecting a dedicated flash programmer (Flashpro III (Part No. FL-PR3, PG-FP3)) to the host machine and the target system.

Remark FL-PR3 is a product of Naito Densai Machida Mfg. Co., Ltd.

5.1 Selecting Communication Mode

Writing to flash memory is performed using the Flashpro III in a serial communication mode. Select one of the communication modes in Table 5-1. The selection of the communication mode is made by using the format shown in Figure 5-1. Each communication mode is selected using the number of V_{PP} pulses shown in Table 5-1.

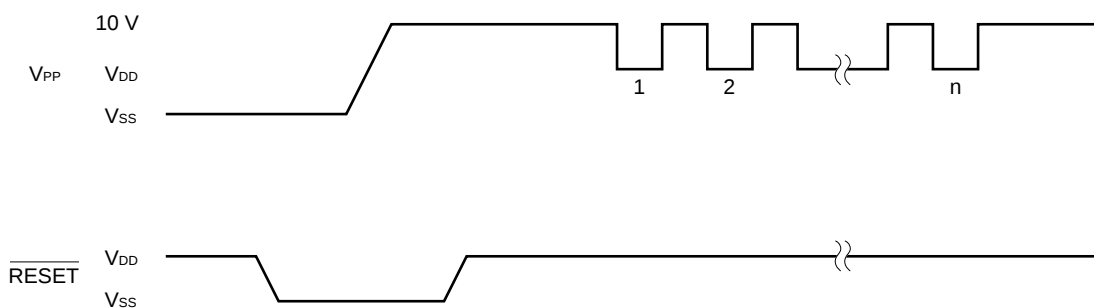
Table 5-1. List of Communication Mode

Communication Mode	Pins	V_{PP} Pulses
3-wire serial I/O	SCK/ASCK/P20 SO/TxD/P21 SI/RxD/P22	0
UART	TxD/SO/P21 RxD/SI/P22	8
Pseudo 3-wire ^{Note}	P00 (Serial clock input) P01 (Serial data output) P02 (Serial data input)	12
	P40/KR0 (Serial clock input) P41/KR1 (Serial data output) P42/KR2 (Serial data input)	13

Note Serial transfer is carried out by controlling ports with software.

Caution Be sure to select a communication mode using the number of V_{PP} pulses shown in Table 5-1.

Figure 5-1. Format of Communication Mode Selection



5.2 Function of Flash Memory Programming

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. Table 5-2 shows the major functions of flash memory programming.

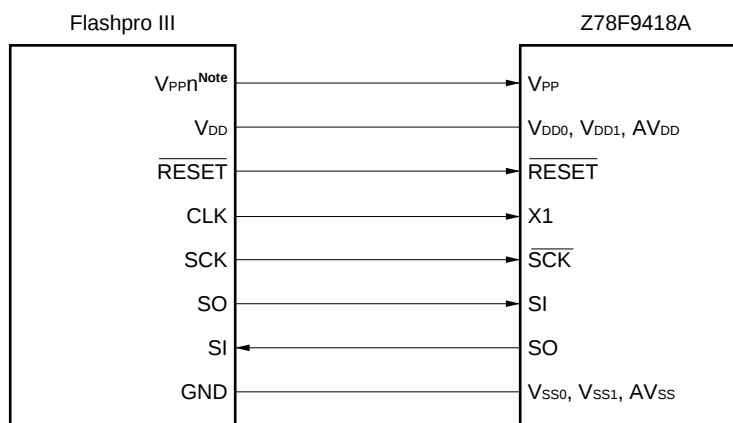
Table 5-2. Major Function of Flash Memory Programming

Function	Description
Batch erase	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
Data write	Performs a write operation to the flash memory based on the write start address and the number of data to be written (number of bytes).
Batch verify	Compares the entire memory contents with the input data.

5.3 Connecting Flashpro III

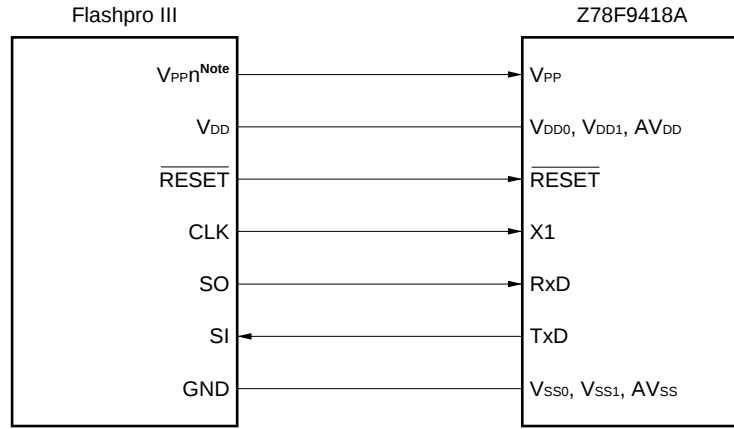
The connection of the Flashpro III and the Z78F9418A differs according to the communication mode (3-wire serial I/O, UART, and pseudo 3-wire). The connections for each communication mode are shown in Figures 5-2, 5-3, and 5-4, respectively.

Figure 5-2. Connection Example of Flashpro III When Using 3-Wire Serial I/O Mode



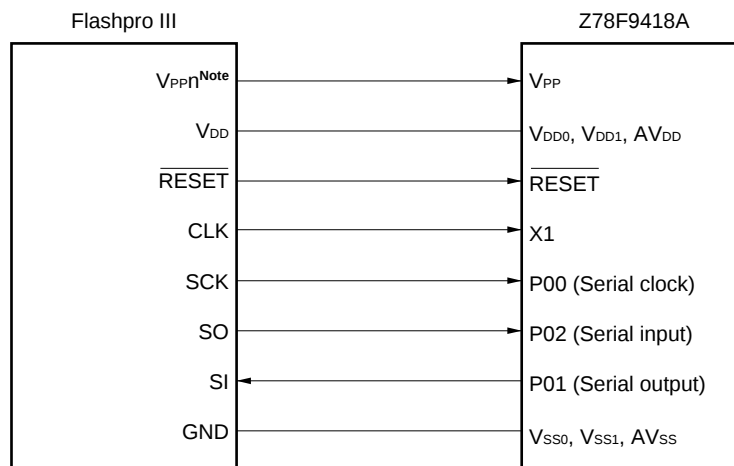
Note n = 1, 2

Figure 5-3. Connection Example of Flashpro III When Using UART Mode



Note n = 1, 2

Figure 5-4. Connection Example of Flashpro III When Using Pseudo 3-Wire (When P0 Is Used)



Note n = 1, 2

5.4 Example of Settings for Flashpro III (PG-FP3)

When writing to flash memory using Flashpro III (PG-FP3), make the following settings.

- <1> Load a parameter file.
- <2> Select the mode of serial communication and serial clock with a type command.
- <3> Make the settings according to the example of settings for PG-FP3 shown below.

Table 5-3. Example of Settings for PG-FP3

Communication Mode	Example of Settings for PG-FP3		V _{PP} Pulse Number ^{Note 1}
3-wire serial I/O	COMM PORT	SIO-ch0	0
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
UART	SIO CLK	1.0 MHz	8
	COMM PORT	UART-ch0	
	CPU CLK	On Target Board	
	On Target Board	4.1943 MHz	
Pseudo 3-wire	UART BPS	9600 bps ^{Note 2}	12/13
	COMM PORT	Port A/B	
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 kHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 kHz	

Notes 1. This is the number of V_{PP} pulses that are supplied by the Flashpro III at serial communication initialization. The pins that will be used for communication are determined according to this number.

2. Select one of 9600 bps, 19200 bps, 38400 bps, or 76800 bps.

Remark COMM PORT: Serial port selection
 SIO CLK: Serial clock frequency selection
 CPU CLK: Input CPU clock source selection

6. OUTLINE OF INSTRUCTION SET

This section shows a list of the instructions of the Z78F9418A.

6.1 Conventions

6.1.1 Operand formats and syntax

One or more operands are written in the operand field of each instruction in accordance with the operand format and syntax of that instruction (for details, refer to the assembler specifications). If two or more operands are shown, select one of them. The uppercase characters, and the symbols #, !, \$, [, and] are keywords and must be written as shown. The meanings of these symbols are as follows:

- #: Specifies immediate data.
- \$: Specifies a relative address.
- !: Specifies an absolute address.
- []: Specifies an indirect address.

To specify immediate data, write an appropriate value or label. When using a label, be sure to use the symbols #, !, \$, [, and].

The register syntax operands r and rp can be specified as either a function name (such as X, A, and C) or an absolute name (such as R0, R1, and R2 as shown in the parentheses in the table below).

Table 6-1. Operand Formats and Syntax

Format	Syntax
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol
saddr	FE20H to FF1FH Immediate data or label
saddrp	FE20H to FF1FH Immediate data or label (even address only)
addr16	0000H to FFFFH Immediate data or label (even address only when 16-bit data transfer instruction is used)
addr5	0040H to 007FH Immediate data or label (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

6.1.2 Explanation of symbols in operation field

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
NMIS:	Non-maskable interrupt processing flag
():	Contents of memory addressed by address or register contents in ()
X _H , X _L :	Higher 8 bits and lower 8 bits of 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
⊕:	Exclusive logical sum (exclusive OR)
— :	Inverted data
addr16:	16-bit immediate data or label
jdsp8:	Signed 8-bit data (displacement value)

6.1.3 Explanation of symbols in flag operation field

(Blank):	Not affected
0:	Cleared to 0
1:	Set to 1
×	Set or cleared depending on result
R:	Previously saved value is stored

6.2 Operation List

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	$r \leftarrow \text{byte}$			
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow \text{byte}$			
	sfr, #byte	3	6	$\text{sfr} \leftarrow \text{byte}$			
	A, r Note 1	2	4	$A \leftarrow r$			
	r, A Note 1	2	4	$r \leftarrow A$			
	A, saddr	2	4	$A \leftarrow (\text{saddr})$			
	saddr, A	2	4	$(\text{saddr}) \leftarrow A$			
	A, sfr	2	4	$A \leftarrow \text{sfr}$			
	sfr, A	2	4	$\text{sfr} \leftarrow A$			
	A, !addr16	3	8	$A \leftarrow (\text{addr16})$			
	!addr16, A	3	8	$(\text{addr16}) \leftarrow A$			
	PSW, #byte	3	6	$\text{PSW} \leftarrow \text{byte}$	×	×	×
	A, PSW	2	4	$A \leftarrow \text{PSW}$			
	PSW, A	2	4	$\text{PSW} \leftarrow A$	×	×	×
	A, [DE]	1	6	$A \leftarrow (\text{DE})$			
	[DE], A	1	6	$(\text{DE}) \leftarrow A$			
	A, [HL]	1	6	$A \leftarrow (\text{HL})$			
	[HL], A	1	6	$(\text{HL}) \leftarrow A$			
	A, [HL+byte]	2	6	$A \leftarrow (\text{HL} + \text{byte})$			
	[HL+byte], A	2	6	$(\text{HL} + \text{byte}) \leftarrow A$			
XCH	A, X	1	4	$A \leftrightarrow X$			
	A, r Note 2	2	6	$A \leftrightarrow r$			
	A, saddr	2	6	$A \leftrightarrow (\text{saddr})$			
	A, sfr	2	6	$A \leftrightarrow (\text{sfr})$			
	A, [DE]	1	8	$A \leftrightarrow (\text{DE})$			
	A, [HL]	1	8	$A \leftrightarrow (\text{HL})$			
	A, [HL+byte]	2	8	$A \leftrightarrow (\text{HL} + \text{byte})$			
MOVW	rp, #word	3	6	$\text{rp} \leftarrow \text{word}$			
	AX, saddrp	2	6	$\text{AX} \leftarrow (\text{saddrp})$			
	saddrp, AX	2	8	$(\text{saddrp}) \leftarrow \text{AX}$			
	AX, rp Note 3	1	4	$\text{AX} \leftarrow \text{rp}$			
	rp, AX Note 3	1	4	$\text{rp} \leftarrow \text{AX}$			
XCHW	AX, rp Note 3	1	8	$\text{AX} \leftrightarrow \text{rp}$			

- Notes**
1. Except $r = A$
 2. Except $r = A, X$
 3. $\text{rp} = \text{BC}, \text{DE}, \text{or HL}$ only

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
ADD	A, #byte	2	4	$A, CY \leftarrow A + \text{byte}$	x	x	x
	saddr, #byte	3	6	$(saddr), CY \leftarrow (saddr) + \text{byte}$	x	x	x
	A, r	2	4	$A, CY \leftarrow A + r$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A + (saddr)$	x	x	x
	A, !addr16	3	8	$A, CY \leftarrow A + (addr16)$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A + (HL)$	x	x	x
	A, [HL+byte]	2	6	$A, CY \leftarrow A + (HL + \text{byte})$	x	x	x
ADDC	A, #byte	2	4	$A, CY \leftarrow A + \text{byte} + CY$	x	x	x
	saddr, #byte	3	6	$(saddr), CY \leftarrow (saddr) + \text{byte} + CY$	x	x	x
	A, r	2	4	$A, CY \leftarrow A + r + CY$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A + (saddr) + CY$	x	x	x
	A, !addr16	3	8	$A, CY \leftarrow A + (addr16) + CY$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A + (HL) + CY$	x	x	x
	A, [HL+byte]	2	6	$A, CY \leftarrow A + (HL + \text{byte}) + CY$	x	x	x
SUB	A, #byte	2	4	$A, CY \leftarrow A - \text{byte}$	x	x	x
	saddr, #byte	3	6	$(saddr), CY \leftarrow (saddr) - \text{byte}$	x	x	x
	A, r	2	4	$A, C \leftarrow A - r$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A - (saddr)$	x	x	x
	A, !addr16	3	8	$A, CY \leftarrow A - (addr16)$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A - (HL)$	x	x	x
	A, [HL+byte]	2	6	$A, CY \leftarrow A - (HL + \text{byte})$	x	x	x
SUBC	A, #byte	2	4	$A, CY \leftarrow A - \text{byte} - CY$	x	x	x
	saddr, #byte	3	6	$(saddr), CY \leftarrow (saddr) - \text{byte} - CY$	x	x	x
	A, r	2	4	$A, CY \leftarrow A - r - CY$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A - (saddr) - CY$	x	x	x
	A, !addr16	3	8	$A, CY \leftarrow A - (addr16) - CY$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A - (HL) - CY$	x	x	x
	A, [HL+byte]	2	6	$A, CY \leftarrow A - (HL + \text{byte}) - CY$	x	x	x
AND	A, #byte	2	4	$A \leftarrow A \wedge \text{byte}$	x		
	saddr, #byte	3	6	$(saddr) \leftarrow (saddr) \wedge \text{byte}$	x		
	A, r	2	4	$A \leftarrow A \wedge r$	x		
	A, saddr	2	4	$A \leftarrow A \wedge (saddr)$	x		
	A, !addr16	3	8	$A \leftarrow A \wedge (addr16)$	x		
	A, [HL]	1	6	$A \leftarrow A \wedge (HL)$	x		
	A, [HL+byte]	2	6	$A \leftarrow A \wedge (HL + \text{byte})$	x		

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	$A \leftarrow A \vee \text{byte}$	x		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \vee \text{byte}$	x		
	A, r	2	4	$A \leftarrow A \vee r$	x		
	A, saddr	2	4	$A \leftarrow A \vee (\text{saddr})$	x		
	A, !addr16	3	8	$A \leftarrow A \vee (\text{addr16})$	x		
	A, [HL]	1	6	$A \leftarrow A \vee (\text{HL})$	x		
	A, [HL+byte]	2	6	$A \leftarrow A \vee (\text{HL} + \text{byte})$	x		
XOR	A, #byte	2	4	$A \leftarrow A \oplus \text{byte}$	x		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \oplus \text{byte}$	x		
	A, r	2	4	$A \leftarrow A \oplus r$	x		
	A, saddr	2	4	$A \leftarrow A \oplus (\text{saddr})$	x		
	A, !addr16	3	8	$A \leftarrow A \oplus (\text{addr16})$	x		
	A, [HL]	1	6	$A \leftarrow A \oplus (\text{HL})$	x		
	A, [HL+byte]	2	6	$A \leftarrow A \oplus (\text{HL} + \text{byte})$	x		
CMP	A, #byte	2	4	$A - \text{byte}$	x	x	x
	saddr, #byte	3	6	$(\text{saddr}) - \text{byte}$	x	x	x
	A, r	2	4	$A - r$	x	x	x
	A, saddr	2	4	$A - (\text{saddr})$	x	x	x
	A, !addr16	3	8	$A - (\text{addr16})$	x	x	x
	A, [HL]	1	6	$A - (\text{HL})$	x	x	x
	A, [HL+byte]	2	6	$A - (\text{HL} + \text{byte})$	x	x	x
ADDW	AX, #word	3	6	$\text{AX}, \text{CY} \leftarrow \text{AX} + \text{word}$	x	x	x
SUBW	AX, #word	3	6	$\text{AX}, \text{CY} \leftarrow \text{AX} - \text{word}$	x	x	x
CMPW	AX, #word	3	6	$\text{AX} - \text{word}$	x	x	x
INC	r	2	4	$r \leftarrow r + 1$	x	x	
	saddr	2	4	$(\text{saddr}) \leftarrow (\text{saddr}) + 1$	x	x	
DEC	r	2	4	$r \leftarrow r - 1$	x	x	
	saddr	2	4	$(\text{saddr}) \leftarrow (\text{saddr}) - 1$	x	x	
INCW	rp	1	4	$\text{rp} \leftarrow \text{rp} + 1$			
DECW	rp	1	4	$\text{rp} \leftarrow \text{rp} - 1$			
ROR	A, 1	1	2	$(\text{CY}, \text{A}_7 \leftarrow \text{A}_0, \text{A}_{m-1} \leftarrow \text{A}_m) \times 1$			x
ROL	A, 1	1	2	$(\text{CY}, \text{A}_0 \leftarrow \text{A}_7, \text{A}_{m+1} \leftarrow \text{A}_m) \times 1$			x
RORC	A, 1	1	2	$(\text{CY} \leftarrow \text{A}_0, \text{A}_7 \leftarrow \text{CY}, \text{A}_{m-1} \leftarrow \text{A}_m) \times 1$			x
ROLC	A, 1	1	2	$(\text{CY} \leftarrow \text{A}_7, \text{A}_0 \leftarrow \text{CY}, \text{A}_{m+1} \leftarrow \text{A}_m) \times 1$			x

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) $\leftarrow$ 1			
	sfr. bit	3	6	sfr. bit $\leftarrow$ 1			
	A. bit	2	4	A. bit $\leftarrow$ 1			
	PSW. bit	3	6	PSW. bit $\leftarrow$ 1	×	×	×
	[HL]. bit	2	10	(HL). bit $\leftarrow$ 1			
CLR1	saddr. bit	3	6	(saddr. bit) $\leftarrow$ 0			
	sfr. bit	3	6	sfr. bit $\leftarrow$ 0			
	A. bit	2	4	A. bit $\leftarrow$ 0			
	PSW. bit	3	6	PSW. bit $\leftarrow$ 0	×	×	×
	[HL]. bit	2	10	(HL). bit $\leftarrow$ 0			
SET1	CY	1	2	CY $\leftarrow$ 1			1
CLR1	CY	1	2	CY $\leftarrow$ 0			0
NOT1	CY	1	2	CY $\leftarrow$ $\overline{\text{CY}}$			×
CALL	!addr16	3	6	(SP-1) $\leftarrow$ (PC+3) _H , (SP-2) $\leftarrow$ (PC+3) _L , PC $\leftarrow$ addr16, SP $\leftarrow$ SP-2			
CALLT	[addr5]	1	8	(SP-1) $\leftarrow$ (PC+1) _H , (SP-2) $\leftarrow$ (PC+1) _L , PC _H $\leftarrow$ (00000000, addr5+1), PC _L $\leftarrow$ (00000000, addr5), SP $\leftarrow$ SP-2			
RET		1	6	PC _H $\leftarrow$ (SP+1), PC _L $\leftarrow$ (SP), SP $\leftarrow$ SP+2			
RETI		1	8	PC _H $\leftarrow$ (SP+1), PC _L $\leftarrow$ (SP), PSW $\leftarrow$ (SP+2), SP $\leftarrow$ SP+3, NMIS $\leftarrow$ 0	R	R	R
PUSH	PSW	1	2	(SP-1) $\leftarrow$ PSW, SP $\leftarrow$ SP-1			
	rp	1	4	(SP-1) $\leftarrow$ rp _H , (SP-2) $\leftarrow$ rp _L , SP $\leftarrow$ SP-2			
POP	PSW	1	4	PSW $\leftarrow$ (SP), SP $\leftarrow$ SP+1	R	R	R
	rp	1	6	rp _H $\leftarrow$ (SP+1), rp _L $\leftarrow$ (SP), SP $\leftarrow$ SP+2			
MOVW	SP, AX	2	8	SP $\leftarrow$ AX			
	AX, SP	2	6	AX $\leftarrow$ SP			
BR	!addr16	3	6	PC $\leftarrow$ addr16			
	\$addr16	2	6	PC $\leftarrow$ PC+2+jdisp8			
	AX	1	6	PC _H $\leftarrow$ A, PC _L $\leftarrow$ X			

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
BC	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if $CY = 1$			
BNC	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if $CY = 0$			
BZ	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if $Z = 1$			
BNZ	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if $Z = 0$			
BT	saddr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if (saddr. bit) = 1			
	sfr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if sfr. bit = 1			
	A. bit, \$addr16	3	8	$PC \leftarrow PC + 3 + jdisp8$ if A. bit = 1			
	PSW. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if PSW. bit = 1			
BF	saddr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if (saddr. bit) = 0			
	sfr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if sfr. bit = 0			
	A. bit, \$addr16	3	8	$PC \leftarrow PC + 3 + jdisp8$ if A. bit = 0			
	PSW. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if PSW. bit = 0			
DBNZ	B, \$addr16	2	6	$B \leftarrow B - 1$, then $PC \leftarrow PC + 2 + jdisp8$ if $B \neq 0$			
	C, \$addr16	2	6	$C \leftarrow C - 1$, then $PC \leftarrow PC + 2 + jdisp8$ if $C \neq 0$			
	saddr, \$addr16	3	8	(saddr) $\leftarrow$ (saddr) - 1, then $PC \leftarrow PC + 3 + jdisp8$ if (saddr) $\neq 0$			
NOP		1	2	No Operation			
EI		3	6	$IE \leftarrow 1$ (Enable Interrupt)			
DI		3	6	$IE \leftarrow 0$ (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

7. ELECTRICAL SPECIFICATIONS

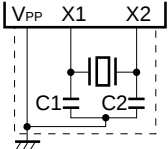
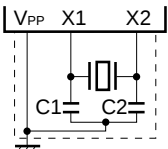
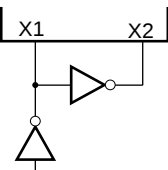
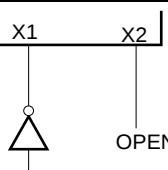
Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V _{DD}	AV _{DD} − 0.3 V ≤ V _{DD} ≤ AV _{DD} + 0.3 V		−0.3 to +6.5	V
	AV _{DD}				
	AV _{REF}				
Input voltage	V _{I1}	Pins other than P50 to P53		−0.3 to V _{DD} + 0.3	V
	V _{I2}	P50 to P53	N-ch open drain	−0.3 to +13	V
Output voltage	V _O			−0.3 to V _{DD} + 0.3	V
Output current, high	I _{OH}	1 pin		−10	mA
		Total for all pins		−30	mA
Output current, low	I _{OL}	1 pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T _A	In normal operation mode		−40 to +85	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T _{stg}			−40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_x) ^{Note 1}	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	After V_{DD} has reached MIN. of oscillation start voltage			4	ms
Crystal resonator		Oscillation frequency (f_x) ^{Note 1}		1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	$V_{DD} = 4.5$ to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f_x) ^{Note 1}		1.0		5.0	MHz
		X1 input high-/low-level widths (t_{xH} , t_{xL})		85		500	ns
		X1 input frequency (f_x) ^{Note 1}	$V_{DD} = 2.7$ to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level widths (t_{xH} , t_{xL})	$V_{DD} = 2.7$ to 5.5 V	85		500	ns

- Notes**
1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.
 2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator whose oscillation is stabilized within the oscillation wait time.

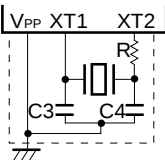
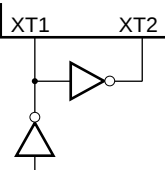
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS0} .
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) ^{Note 1}		32	32.768	35	kHz
		Oscillation stabilization time ^{Note 2}	$V_{DD} = 4.5$ to 5.5 V		1.2	2	s
						10	s
External clock		XT1 input frequency (f_{XT}) ^{Note 1}		32		35	kHz
		XT1 input high-/low-level widths (t_{XTH} , t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator whose oscillation is stabilized within the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS0} .
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I _{OH}	Per pin				–1	mA
		Total for all pins				–15	mA
Output current, low	I _{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V _{IH1}	P00 to P03, P46, P47, P60 to P66, P80 to P87, P90 to P93	V _{DD} = 2.7 to 5.5 V	0.7V _{DD}		V _{DD}	V
				0.9V _{DD}		V _{DD}	V
	V _{IH2}	P50 to P53 N-ch open drain	V _{DD} = 2.7 to 5.5 V	0.7V _{DD}		12	V
				0.9V _{DD}		12	V
	V _{IH3}	RESET, P20 to P27, P40 to P45	V _{DD} = 2.7 to 5.5 V	0.8V _{DD}		V _{DD}	V
				0.9V _{DD}		V _{DD}	V
	V _{IH4}	X1, X2, XT1, XT2		V _{DD} –0.1		V _{DD}	V
Input voltage, low	V _{IL1}	P00 to P03, P46, P47, P60 to P66, P80 to P87, P90 to P93	V _{DD} = 2.7 to 5.5 V	0		0.3V _{DD}	V
				0		0.1V _{DD}	V
	V _{IL2}	P50 to P53	V _{DD} = 2.7 to 5.5 V	0		0.3V _{DD}	V
				0		0.1V _{DD}	V
	V _{IL3}	RESET, P20 to P27, P40 to P45	V _{DD} = 2.7 to 5.5 V	0		0.2V _{DD}	V
				0		0.1V _{DD}	V
	V _{IL4}	X1, X2, XT1, XT2		0		0.1	V
Output voltage, high	V _{OH}	V _{DD} = 4.5 to 5.5 V, I _{OH} = –1 mA		V _{DD} –1.0			V
		V _{DD} = 1.8 to 5.5 V, I _{OH} = –100 μA		V _{DD} –0.5			V
Output voltage, low	V _{OL1}	Pins other than P50 to P53	V _{DD} = 4.5 to 5.5 V I _{OL} = 10 mA			1.0	V
			V _{DD} = 1.8 to 5.5 V I _{OL} = 400 μA			0.5	V
	V _{OL2}	P50 to P53	V _{DD} = 4.5 to 5.5 V I _{OL} = 10 mA			1.0	V
			V _{DD} = 1.8 to 5.5 V I _{OL} = 1.6 mA			0.4	V
Input leakage current, high	I _{LIH1}	V _I = V _{DD}	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			3	μA
	I _{LIH2}					20	μA
	I _{LIH3}	V _I = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I _{LIL1}	V _I = 0 V	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			–3	μA
	I _{LIL2}		X1, X2, XT1, XT2			–20	μA
	I _{LIL3}		P50 to P53 (N-ch open drain)			–3 ^{Note}	μA

Note When P50 to P53 are set in the input mode, a low-level input leakage current of –30 μA (MAX.) flows only for the duration of one cycle time if an instruction to read P50 to P53 is executed. Otherwise, the leakage current of –3 μA (MAX.) flows.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	$V_O = 0$ V				-3	μA
Software pull-up resistor	R_1	$V_I = 0$ V, pins other than P50 to P53		50	100	200	$\text{k}\Omega$
Supply current	I_{DD1} ^{Note 1}	5.0 MHz crystal oscillation operating mode ($C1 = C2 = 22$ pF)	$V_{DD} = 5.0$ V $\pm 10\%$ ^{Note 4}		5.0	14.0	mA
			$V_{DD} = 3.0$ V $\pm 10\%$ ^{Note 5}		2.0	5.0	mA
			$V_{DD} = 2.0$ V $\pm 10\%$ ^{Note 5}		1.5	3.0	mA
	I_{DD2} ^{Note 1}	5.0 MHz crystal oscillation HALT mode ($C1 = C2 = 22$ pF)	$V_{DD} = 5.0$ V $\pm 10\%$ ^{Note 4}		2.0	6.0	mA
			$V_{DD} = 3.0$ V $\pm 10\%$ ^{Note 5}		1.0	3.0	mA
			$V_{DD} = 2.0$ V $\pm 10\%$ ^{Note 5}		0.7	2.0	mA
	I_{DD3} ^{Note 1}	32.768 kHz crystal oscillation operating mode ^{Note 3} ($C3 = C4 = 22$ pF, $R1 = 220$ $\text{k}\Omega$)	$V_{DD} = 5.0$ V $\pm 10\%$		200	600	μA
			$V_{DD} = 3.0$ V $\pm 10\%$		150	450	μA
			$V_{DD} = 2.0$ V $\pm 10\%$		100	300	μA
	I_{DD4} ^{Note 1}	32.768 kHz crystal oscillation HALT mode ^{Note 3} ($C3 = C4 = 22$ pF, $R1 = 220$ $\text{k}\Omega$)	$V_{DD} = 5.0$ V $\pm 10\%$		50	150	μA
			$V_{DD} = 3.0$ V $\pm 10\%$		30	90	μA
			$V_{DD} = 2.0$ V $\pm 10\%$		20	60	μA
	I_{DD5} ^{Note 1}	32.768 kHz crystal oscillation STOP mode	$V_{DD} = 5.0$ V $\pm 10\%$		0.1	10	μA
			$V_{DD} = 3.0$ V $\pm 10\%$		0.05	5.0	μA
			$T_A = 25^\circ\text{C}$		0.05	3.0	μA
	I_{DD6} ^{Notes 1, 2}	5.0 MHz crystal oscillation A/D operation mode ($C1 = C2 = 22$ pF)	$V_{DD} = 5.0$ V $\pm 10\%$ ^{Note 4}		6.0	16.0	mA
			$V_{DD} = 3.0$ V $\pm 10\%$ ^{Note 5}		3.0	7.0	mA
			$V_{DD} = 2.0$ V $\pm 10\%$ ^{Note 5}		2.5	5.0	mA

- Notes**
1. The current flowing to the AV_{REFON} (ADCS0 (bit 7 of A/D converter mode register 0 (ADM0)) = 1) current, AV_{DD} current, and port current (including the current flowing through the on-chip pull-up resistors) is not included.
 2. For the current flowing into AV_{REF} , refer to **10-Bit A/D Converter Characteristics**.
 3. When main system clock is stopped
 4. High-speed mode operation (when processor clock control register (PCC) is set to 00H)
 5. Low-speed mode operation (when PCC is set to 02H)

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

LCD Characteristics (T_A = -40 to +85°C, V_{DD} = 2.2 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{LCD}	VAON20 = 1	2.2		V _{DD}	V
		VAON20 = 0 ^{Note 1}	At 1/3 bias		V _{DD}	V
			At 1/2 bias		V _{DD}	V
LCD output voltage deviation ^{Note 2} (common)	V _{ODC}	I _O = ±5 μA	0		±0.2	V
LCD output voltage deviation ^{Note 2} (segment)	V _{ODS}	I _O = ±1 μA	0		±0.2	V

Notes 1. T_A = -10 to +85°C in the normal mode (VAON20 = 0)

2. Voltage deviation is the voltage difference between the ideal value of a segment or the common output (V_{LCDn}: n = 0 to 2) and output voltage.

Flash Memory Write/Erase Characteristics

(T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V, in 5.0 MHz crystal oscillation operating mode)

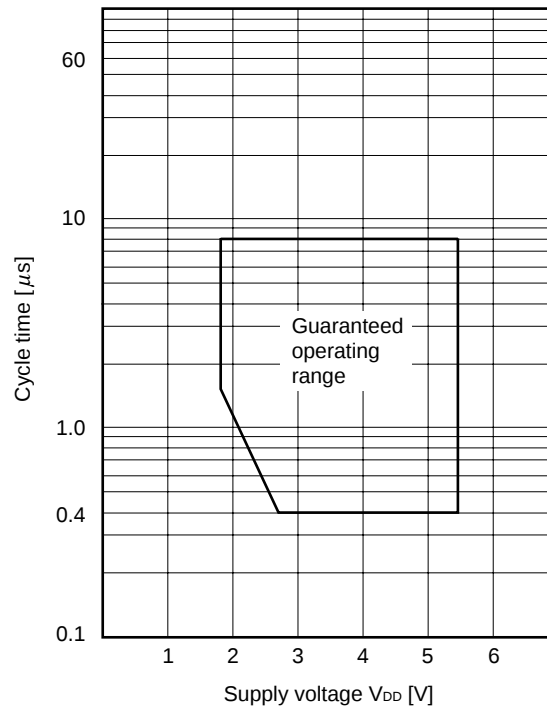
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current ^{Note} (V _{DD} pin)	I _{DDW}	When V _{PP} supply voltage = V _{PP1}			18	mA
Write current ^{Note} (V _{PP} pin)	I _{PPW}	When V _{PP} supply voltage = V _{PP1}			22.5	mA
Erase current ^{Note} (V _{DD} pin)	I _{DDE}	When V _{PP} supply voltage = V _{PP1}			18	mA
Erase current ^{Note} (V _{PP} pin)	I _{PPE}	When V _{PP} supply voltage = V _{PP1}			115	mA
Unit erase time	t _{er}		0.5	1	1	s
Total erase time	t _{era}				20	s
Write count		Erase/write are regarded as 1 cycle			20	Times
V _{PP} supply voltage	V _{PP0}	In normal operation	0		0.2V _{DD}	V
	V _{PP1}	During flash memory programming	9.7	10.0	10.3	V

Note The current flowing to the ports (including the current flowing through the on-chip pull-up resistors) is not included.

AC Characteristics

(1) Basic operation ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating with main system clock	$V_{DD} = 2.7$ to 5.5 V	0.4	8	μs
				1.6	8	μs
		Operating with subsystem clock		114	122	μs
TI0, TI1 input frequency	f_{TI}	$V_{DD} = 2.7$ to 5.5 V	0		4	MHz
			0		275	kHz
TI0, TI1 input high-/low-level widths	t_{TIH}, t_{TIL}	$V_{DD} = 2.7$ to 5.5 V	0.1			μs
			1.8			μs
Interrupt input high-/low-level widths	t_{INTH}, t_{INTL}	INTP0 to INTP3	10			μs
RESET input low-level width	t_{RSL}		10			μs

 T_{CY} vs V_{DD} (Main system clock)

(2) Serial interface ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)(a) 3-wire serial I/O mode ($\overline{\text{SCK}}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY1}	$V_{DD} = 2.7$ to 5.5 V	800			ns
			3200			ns
$\overline{\text{SCK}}$ high-/low-level widths	$t_{\text{KH1}}, t_{\text{KL1}}$	$V_{DD} = 2.7$ to 5.5 V	$t_{\text{KCY1}}/2-50$			ns
			$t_{\text{KCY1}}/2-150$			ns
SI setup time (to $\overline{\text{SCK}}\uparrow$)	t_{SIK1}	$V_{DD} = 2.7$ to 5.5 V	150			ns
			500			ns
SI hold time (from $\overline{\text{SCK}}\uparrow$)	t_{KSI1}	$V_{DD} = 2.7$ to 5.5 V	400			ns
			600			ns
SO output delay time from $\overline{\text{SCK}}\downarrow$	t_{KS01}	$R = 1\text{ k}\Omega$, $C = 100\text{ pF}$ ^{Note}	$V_{DD} = 2.7$ to 5.5 V	0	250	ns
				0	1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(b) 3-wire serial I/O mode ($\overline{\text{SCK}}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY2}	$V_{DD} = 2.7$ to 5.5 V	900			ns
			3500			ns
$\overline{\text{SCK}}$ high-/low-level widths	$t_{\text{KH2}}, t_{\text{KL2}}$	$V_{DD} = 2.7$ to 5.5 V	400			ns
			1600			ns
SI setup time (to $\overline{\text{SCK}}\uparrow$)	t_{SIK2}	$V_{DD} = 2.7$ to 5.5 V	100			ns
			150			ns
SI hold time (from $\overline{\text{SCK}}\uparrow$)	t_{KSI2}	$V_{DD} = 2.7$ to 5.5 V	400			ns
			600			ns
SO output delay time from $\overline{\text{SCK}}\downarrow$	t_{KS02}	$R = 1\text{ k}\Omega$, $C = 100\text{ pF}$ ^{Note}	$V_{DD} = 2.7$ to 5.5 V	0	300	ns
				0	1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

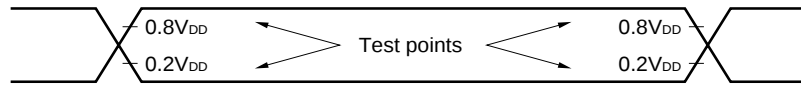
(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$V_{DD} = 2.7$ to 5.5 V			78125	bps
					19531	bps

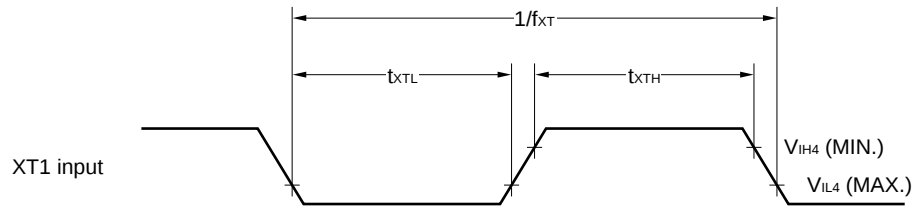
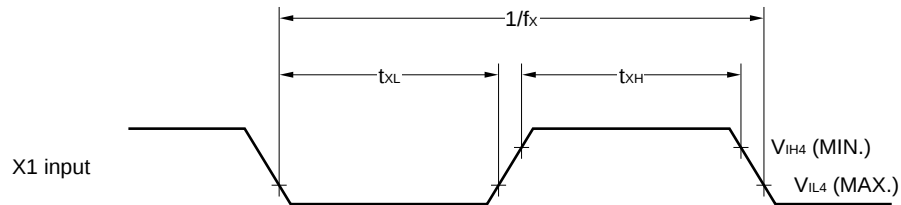
(d) UART mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$	900			ns
			3500			ns
ASCK high-/low-level widths	t_{KH3}, t_{KL3}	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$	400			ns
			1600			ns
Transfer rate		$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$			39063	bps
					9766	bps
ASCK rise/fall times	t_R, t_F				1	μs

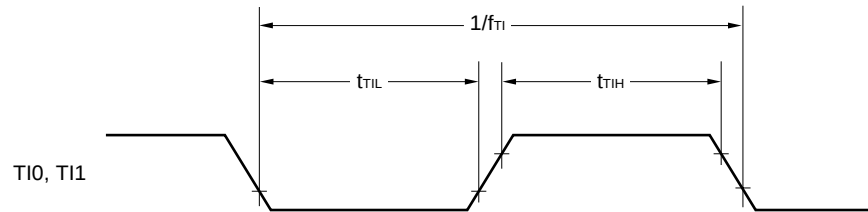
AC Timing Test Points (excluding X1 and XT1 inputs)



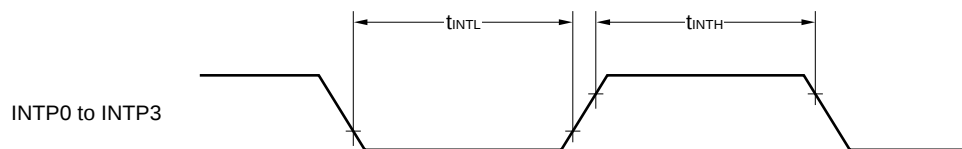
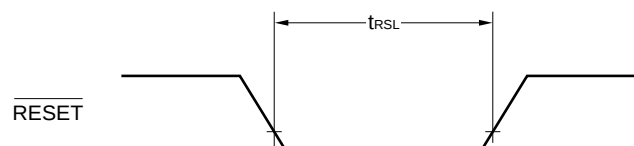
Clock Timing



TI Timing

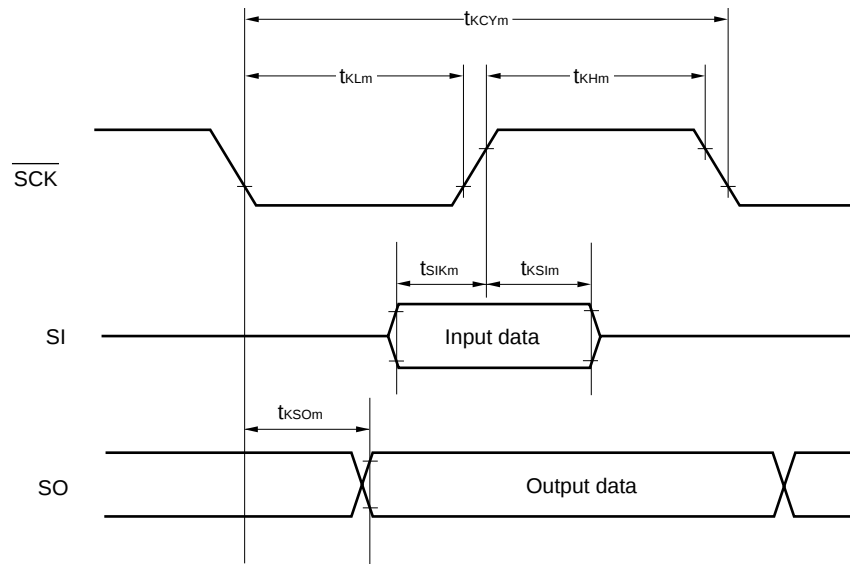


Interrupt Input Timing

 $\overline{\text{RESET}}$ Input Timing

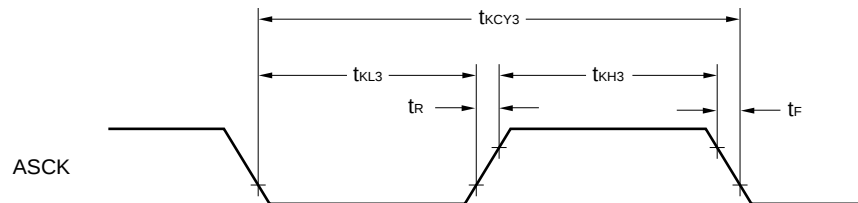
Serial Transfer Timing

3-wire serial I/O mode:



Remark $m = 1$ or 2

UART mode (external clock input):



10-Bit A/D Converter Characteristics(T_A = –40 to +85°C, 1.8 V ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error ^{Note}		4.5 V AV _{REF} AV _{DD} 5.5 V		0.2	0.4	%FSR
		2.7 V AV _{REF} AV _{DD} 5.5 V		0.4	0.6	%FSR
		1.8 V AV _{REF} AV _{DD} 5.5 V		0.8	1.2	%FSR
Conversion time	t _{CONV}	4.5 V AV _{REF} AV _{DD} 5.5 V	14		100	μs
		2.7 V AV _{REF} AV _{DD} 5.5 V	14		100	μs
		1.8 V AV _{REF} AV _{DD} 5.5 V	28		100	μs
Zero-scale error ^{Note}	AINL	4.5 V AV _{REF} AV _{DD} 5.5 V			0.4	%FSR
		2.7 V AV _{REF} AV _{DD} 5.5 V			0.6	%FSR
		1.8 V AV _{REF} AV _{DD} 5.5 V			1.2	%FSR
Full-scale error ^{Note}	AINL	4.5 V AV _{REF} AV _{DD} 5.5 V			0.4	%FSR
		2.7 V AV _{REF} AV _{DD} 5.5 V			0.6	%FSR
		1.8 V AV _{REF} AV _{DD} 5.5 V			1.2	%FSR
Non-integral linearity ^{Note}	INL	4.5 V AV _{REF} AV _{DD} 5.5 V			2.5	LSB
		2.7 V AV _{REF} AV _{DD} 5.5 V			4.5	LSB
		1.8 V AV _{REF} AV _{DD} 5.5 V			8.5	LSB
Non-differential linearity ^{Note}	DNL	4.5 V AV _{REF} AV _{DD} 5.5 V			1.5	LSB
		2.7 V AV _{REF} AV _{DD} 5.5 V			2.0	LSB
		1.8 V AV _{REF} AV _{DD} 5.5 V			3.5	LSB
Analog input voltage	V _{IAN}		0		AV _{REF}	V
Reference voltage	AV _{REF}		1.8		AV _{DD}	V
Resistance between AV _{REF} and AV _{SS}	R _{ADREF}		20	40		k

Note Excludes quantization error (±0.05%).**Comparator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Analog input range	V _{CIN}		0		V _{DD}	V
Reference voltage input range	V _{CREF}	V _{DD} = 2.7 to 5.5 V	1.35	1.6	1.85	V
			1.35	1.4	1.45	V
Accuracy					100	mV

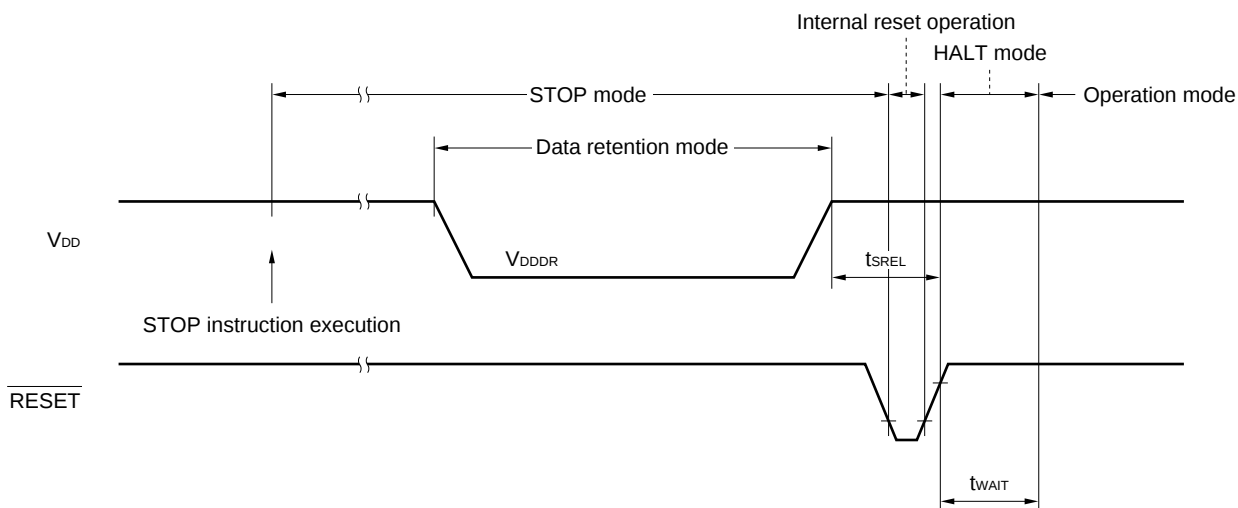
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics ($T_A = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time ^{Note 1}	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Release by interrupt request		Note 2		ms

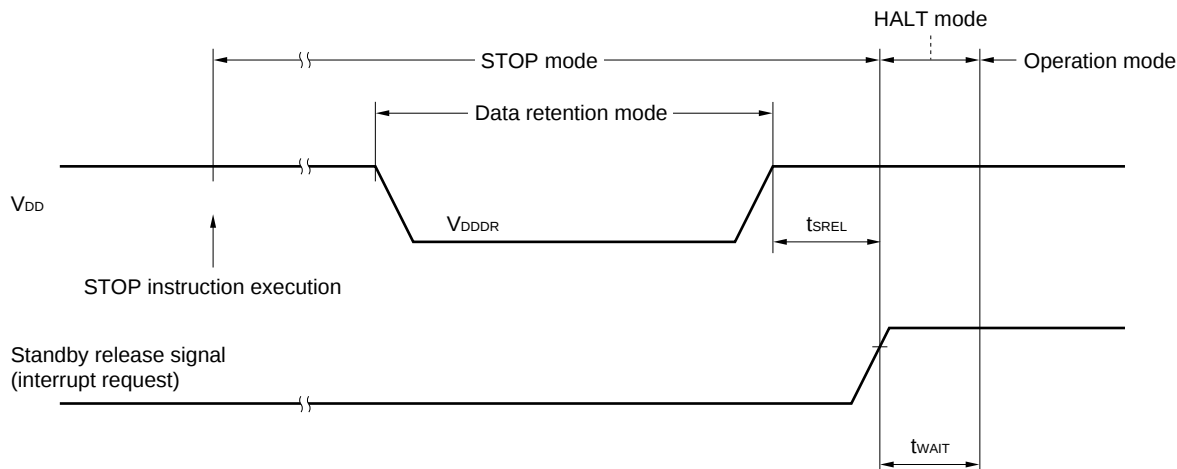
Notes 1. The oscillation stabilization wait time is the time after oscillation has started during which the CPU is stopped to prevent unstable operation.

2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

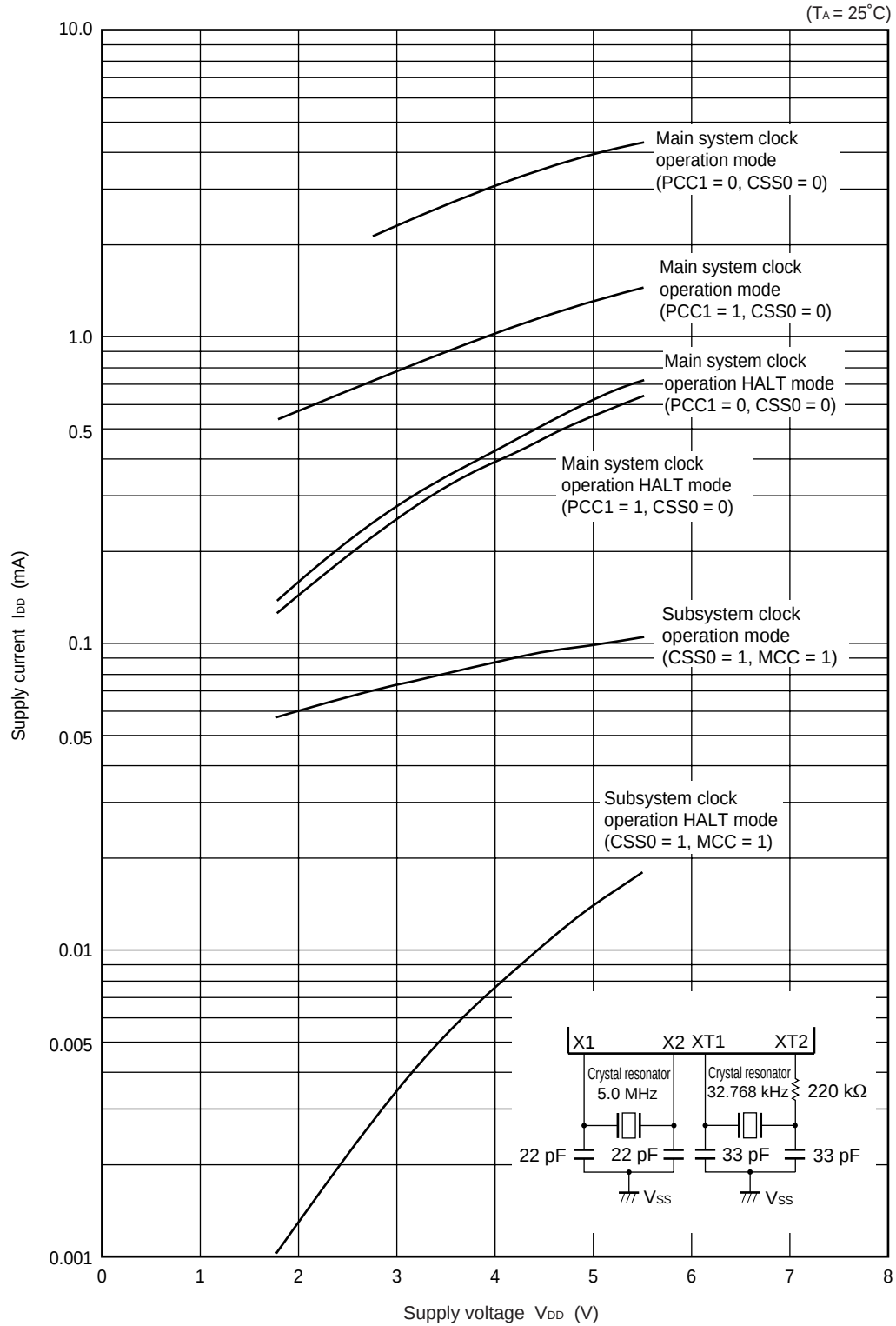
Remark f_X : Main system clock oscillation frequency

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)

Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)

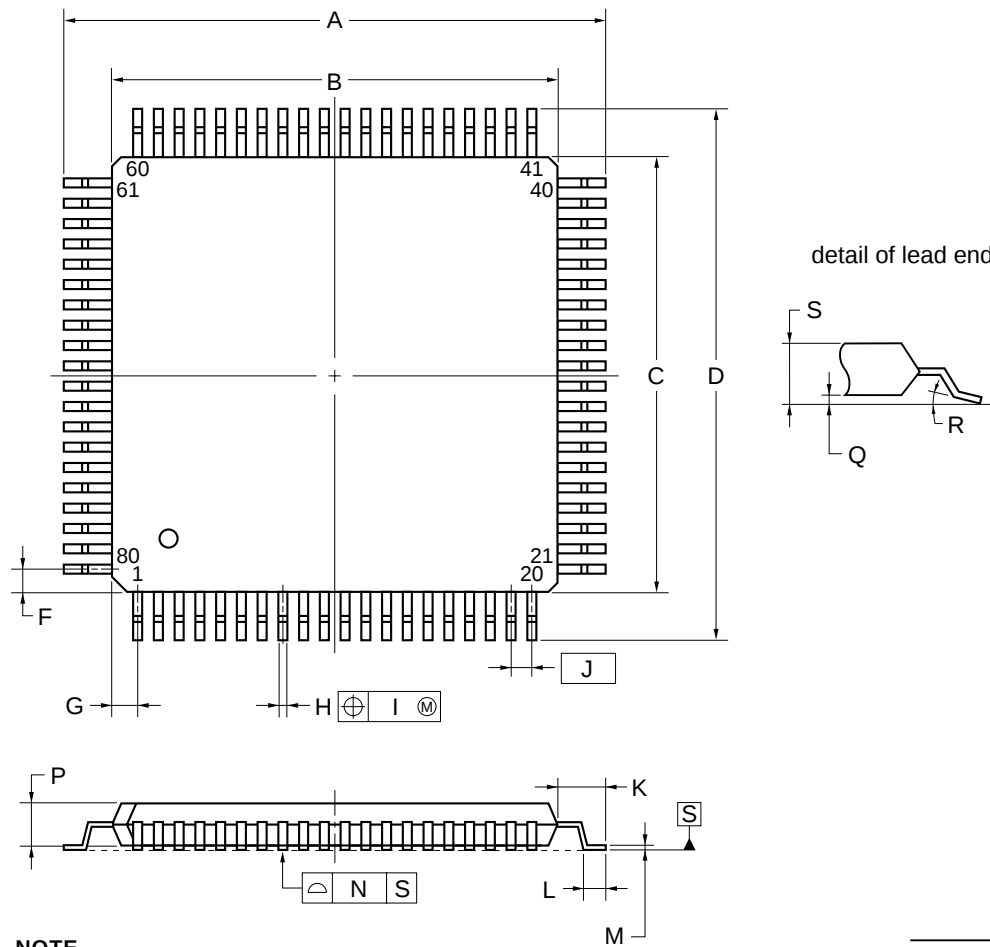


8. CHARACTERISTIC CURVE



9. PACKAGE DRAWINGS

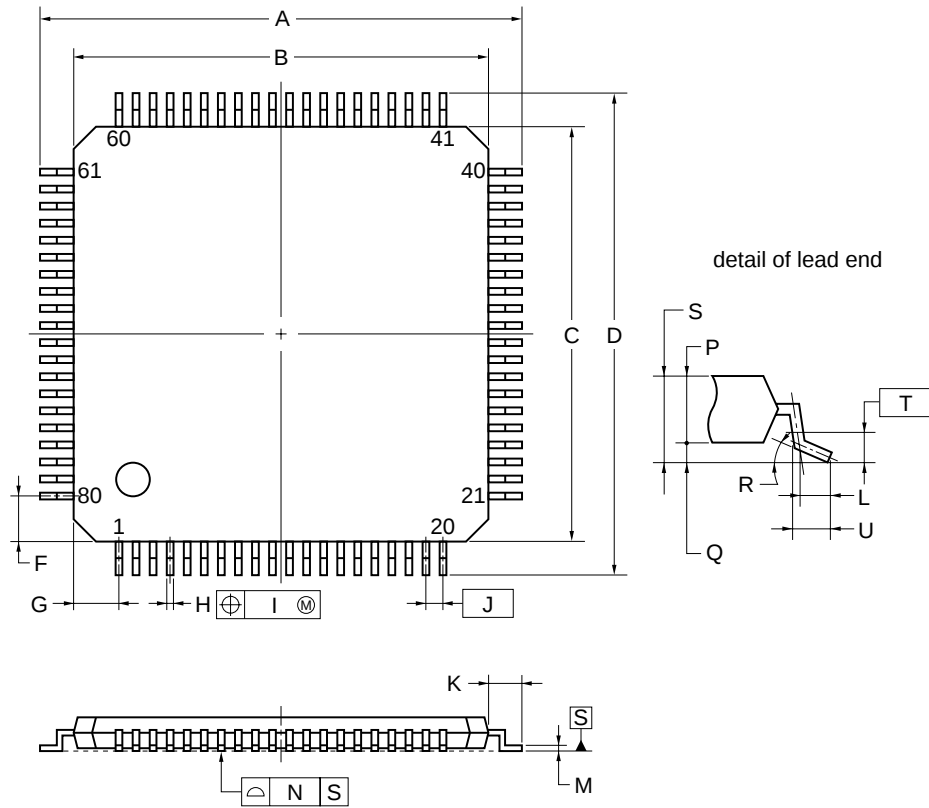
80-PIN PLASTIC QFP (14x14)



ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	0.17 ^{+0.03} _{-0.07}
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	3° ^{+7°} _{-3°}
S	1.70 MAX.

P80GC-65-8BT-1

80-PIN PLASTIC TQFP (FINE PITCH) (12x12)

**NOTE**

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.145±0.05
N	0.08
P	1.0
Q	0.1±0.05
R	3°+4° -3°
S	1.1±0.1
T	0.25
U	0.6±0.15

P80GK-50-9EU-1

10. RECOMMENDED SOLDERING CONDITIONS

The Z78F9418A should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 10-1. Surface Mounting Type Soldering Conditions (1/2)

Z78F9418AGC-8BT: 80-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 C, Time: 30 sec. MAX. (at 210 C or higher), Count: two times or less	IR35-00-2
VPS	Package peak temperature: 215 C, Time: 40 sec. MAX. (at 200 C or higher), Count: two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260 C MAX., Time: 10 sec. MAX., Count: once, Preheating temperature: 120 C MAX. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 C MAX., Time: 3 sec. MAX. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

Table 10-1. Surface Mounting Type Soldering Conditions (2/2)

Z78F9418AGK-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 C, Time: 30 sec. MAX. (at 210 C or higher), Count: two times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125 C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215 C, Time: 40 sec. MAX. (at 200 C or higher), Count: two times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125 C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300 C MAX., Time: 3 sec. MAX. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DIFFERENCES BETWEEN Z78F9418A AND MASK ROM VERSIONS

The Z78F9418A has flash memory in place of the internal ROM of the mask ROM versions (Z789415A, Z789416A, and Z789417A). Differences between the Z78F9418A and mask ROM versions are shown in Table A-1.

Table A-1. Differences Between Z78F9418A and Mask ROM Versions

Parameter		Flash Memory Version	Mask ROM Versions		
		Z78F9418A	Z789415A	Z789416A	Z789417A
Internal memory	ROM structure	Flash memory	Mask ROM		
	ROM capacity	32 KB	12 KB	16 KB	24 KB
	High-speed RAM capacity	512 bytes			
	LCD display RAM	28 bytes			
Pull-up resistor		32 (software control only)	36 (software control: 32, mask option control: 4)		
Divider resistor for LCD driving		Not available	Can be specified on-chip by mask option		
V _{PP} pin		Available	Not available		
IC pin		Not available	Available		
Electrical specifications		See the relevant data sheet			

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the Z78F9418A.

Language processing software

RA78K0S ^{Notes 1, 2, 3}	Assembler package common to 78K/0S Series
CC78K0S ^{Notes 1, 2, 3}	C compiler package common to 78K/0S Series
DF789418 ^{Notes 1, 2, 3}	Device file for Z789407A and Z789417A Subseries

Flash memory writing tools

Flashpro III (Part No. FL-PR3 ^{Note 4} , PG-FP3)	Flash programmer for microcontrollers with flash memory
FA-80GC ^{Note 4}	Flash memory writing adapter for 80-pin plastic QFP (GC-8BT type)
FA-80GK-9EU ^{Note 4}	Flash memory writing adapter for 80-pin plastic TQFP (fine pitch) (GK-9EU type)

Debugging tools

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging the hardware and software of the application system using the 78K/0S Series. Supports the integrated debugger (ID78K0S-NS). Used with an AC adapter, emulation probe, and interface adapter that connects the host machine.
IE-70000-MC-PS-B AC adapter	Adapter that distributes power from an AC 100 to 240 V outlet.
IE-70000-98-IF-C Interface adapter	Adapter necessary when using a PC-9800 series (except notebook type) as the host machine of the IE-78K0S-NS (supports C bus).
IE-70000-CD-IF-A PC card interface	PC card and interface cable necessary when a notebook type personal computer is used as the host machine of the IE-78K0S-NS (supports PCMCIA socket).
IE-70000-PC-IF-C Interface adapter	Adapter necessary when an IBM PC/AT™ or compatible machine is used as the host machine of the IE-78K0S-NS (supports ISA bus).
IE-70000-PCI-IF Interface adapter	Adapter necessary when using a personal computer with PCI bus is used as the host machine of the IE-78K0S-NS.
IE-789418-NS-EM1 Emulation board	Board for emulating device-specific peripheral hardware. Used with an in-circuit emulator.
NP-80GC ^{Note 4}	Board for connecting an in-circuit emulator and target system. For 80-pin plastic QFP (GC-8BT type).
NP-80GK ^{Note 4}	Board for connecting an in-circuit emulator and target system. For 80-pin plastic TQFP (fine pitch) (GK-9EU type).
SM78K0S ^{Notes 1, 2}	System simulator common to 78K/0S Series
ID78K0S-NS ^{Notes 1, 2}	Integrated debugger common to 78K/0S Series
DF789418 ^{Notes 1, 2}	Device file for Z789407A and Z789417A Subseries

Real-time OS

MX78K0S ^{Notes 1, 2}	OS for 78K/0S Series
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- Notes**
1. PC-9800 series (Japanese Windows™) based
 2. IBM PC/AT or compatible machine (Japanese/English Windows) based
 3. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based, NEWS™ (NEWS-OS™) based
 4. This is a product of Naito Densetsu Machida Mfg. Co., Ltd. (Tel: +81-44-822-3813).

Remark The RA78K0S, CC78K0S, and SM78K0S are used in combination with the DF789418.

APPENDIX C. RELATED DOCUMENTS

Device-Related Documents

Document Name	Document No.	
	Japanese	English
Z789405A, Z789406A, Z789407A, Z789415A, Z789416A, Z789417A Product Specification	U14024J	U14024E
Z78F9418A Product Specification	U14595J	U14595E
Z789407A, Z789417A Subseries User's Manual	U13952J	U13952E
78K/0S Series User's Manual Instructions	U11047J	U11047E
78K/0, 78K/0S Series Application Note Flash Memory Write	U14548J	U14548E

Documents on Development Tools (User's Manual)

Document Name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly Language	U11599J	U11599E
	Structured Assembly Language	U11623J	U11623E
CC78K0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator, Windows-Based	Reference	U11489J	U11489E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K0S-NS Integrated Debugger, Windows-Based	Reference	U12901J	U12901E
IE-78K0S-NS In-Circuit Emulator		U13549J	U13549E
IE-789418-NS-EM1 Emulation Board		U14364J	To be prepared

Documents on Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0S Series OS MX78K0S	Fundamental	U12938J	U12938E

Other Documents

Document Name	Document No.	
	Japanese	English
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Microcomputer-Related Products by Third Party	U11416J	-

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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