Z86L33/L43

CONSUMER CONTROLLER PROCESSOR

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86L33	4	237	24	2.0V - 4.5V
Z86L43	4	236	32	2.0V - 4.5V

Note: *General-Purpose

- 40-Pin DIP, 44-Pin PLCC and QFP Packages (L43) 28-Pin DIP, 28-Pin SOIC (L33)
- Low-Power Consumption
- 0°C to +70°C Operating Range
- Expanded Register File (ERF)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86L33/L43 Consumer Controller Processor (CCP™) is a member of Zilog's Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. This low-power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86L33/L43 features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, External Data Memory (L43), and ERF. The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The ERF consists of three control registers (Banks 0,D, and F)

For applications demanding powerful I/O capabilities, the Z86L33 provides 24 pins, and the Z86L43 provides 32 pins dedicated to input and output. These lines are configurable under software control to provide timing,status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z86L33/L43 offers two on-chip counter/timers with a large number of user-selectable modes.

With ROM/ROMless selectivity, the Z86L43 provides both external memory and pre-programmed ROM, which enables this Z8 microcontroller to be used in high-volume applications, or where code flexibility is required.

GENERAL DESCRIPTION (Continued)

Notes: All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

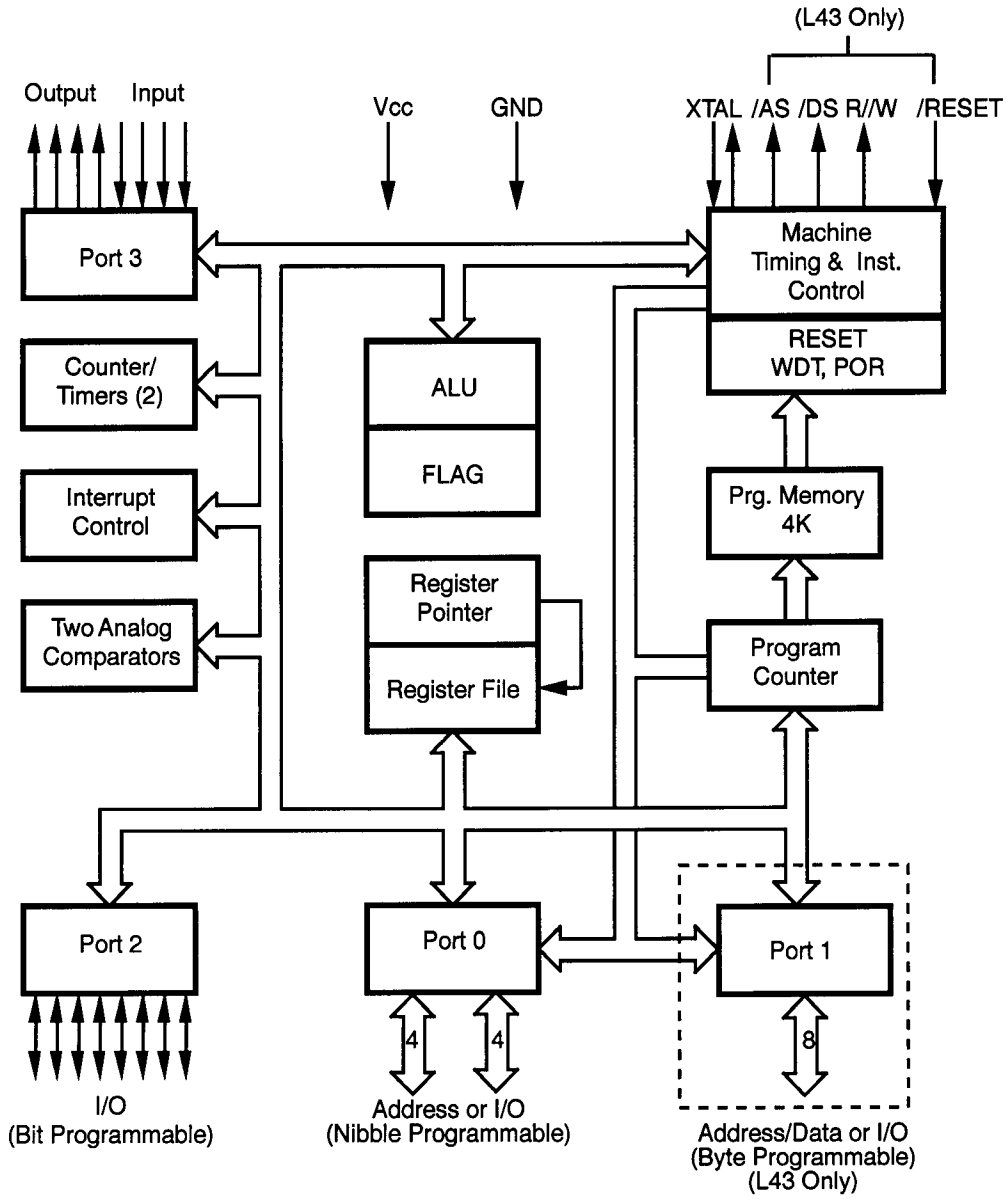

Figure 1. Functional Block Diagram

PIN DESCRIPTION

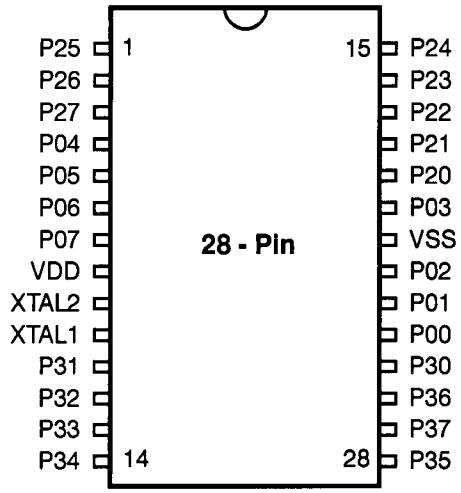

Figure 2. 28-Pin DIP/SOIC Pin Configuration

Table 1. 28-Pin DIP/SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-3	P25-27	Port 2, Pins 5,6,7	In/Output
4-7	P04-07	Port 0, Pins 4,5,6,7	In/Output
8	V_{DD}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-33	Port 3, Pins 1,2,3	Fixed Input
14-15	P34-35	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P00-02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P20-24	Port 2, Pins 0,1,2,3,4	In/Output

PIN DESCRIPTION (Continued)

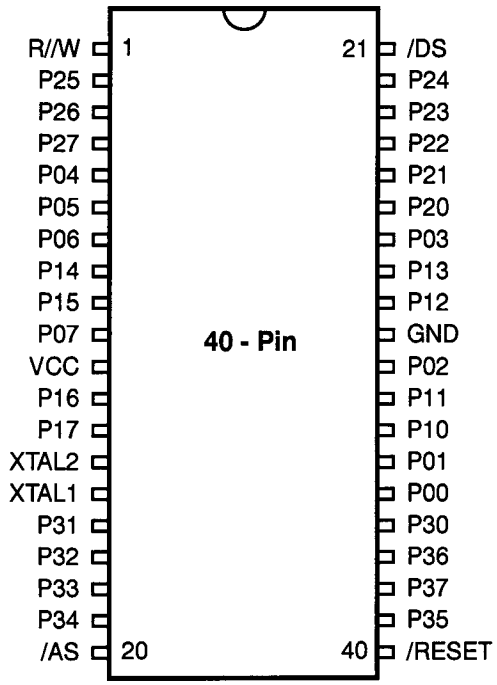

Figure 3. 40-Pin DIP Pin Configuration

Table 2. 40-Pin DIP Package Pin Identification

Pin #	Symbol	Function	Direction
1	R//W	Read/Write	Output
2-4	P25-27	Port 2, Pins 5,6,7	In/Output
5-7	P04-06	Port 0, Pins 4,5,6	In/Output
8-9	P14-15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal, Oscillator Clock	Output
15	XTAL1	Crystal, Oscillator Clock	Input
16-18	P31-33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output

Table 2. 40-Pin DIP Package Pin Identification

Pin #	Symbol	Function	Direction
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-01	Port 0, Pin 0,1	In/Output
28-29	P10-11	Port 1, Pin 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-13	Port 1, Pin 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-24	Port 2, Pin 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

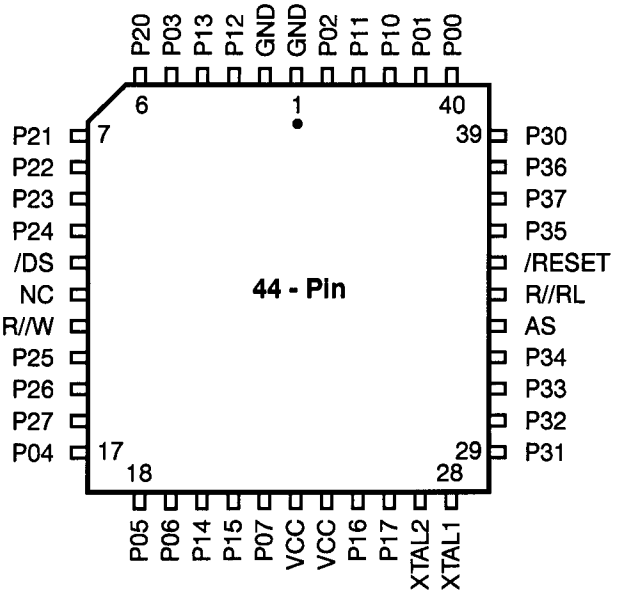

Figure 4. 44-Pin PLCC Pin Configuration

Table 3. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	NC	Not Connected	
13	R//W	Read/Write	Output
14-16	P25-27	Port 2, Pins 5,6,7	In/Output
17-19	P04-06	Port 0, Pins 4,5,6	In/Output
20-21	P14-15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23,24	V_{CC}	Power Supply	
25-26	P16-17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal, Oscillator Clock	Output

Table 3. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
28	XTAL1	Crystal, Oscillator Clock	Input
29-31	P31-33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless Control	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-01	Port 0, Pins 0,1	In/Output
42-43	P10-11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN DESCRIPTION (Continued)

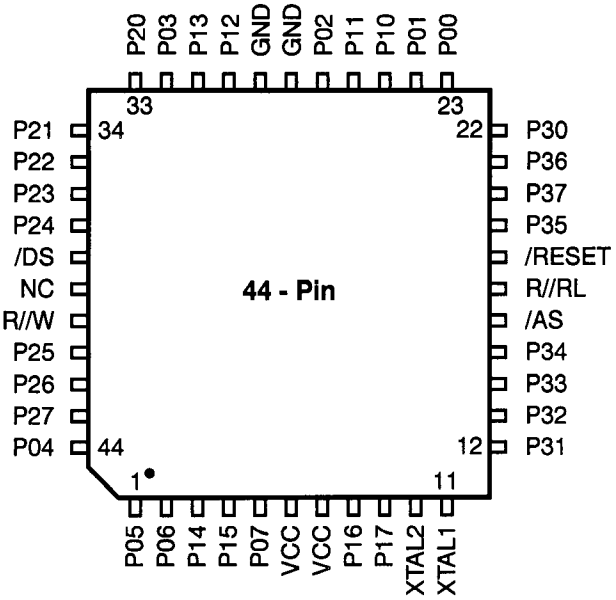

Figure 5. 44-Pin QFP Pin Configuration

Table 4. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
1-2	P05-06	Port 0, Pins 5,6	In/Output
3-4	P14-15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6-7	V_{CC}	Power Supply	
8-9	P16-17	Port 1 Pins 6,7	In/Output
10	XTAL2	Crystal, Oscillator Clock	Output
11	XTAL1	Crystal, Oscillator Clock	Input
12-14	P31-33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	/AS	Address Strobe	Output
17	R//RL	ROM/ROMless Control	Input
18	/RESET	Reset	Input
19	P35	Port 3, Pin 5	Output

Table 4. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-01	Port 0, Pins 0,1	In/Output
25-26	P10-11	Port 1, Pins 0,1	In/Output
27	P02	Port 0, Pin 2	In/Output
28-29	GND	Ground	
30-31	P12-13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
38	/DS	Data Strobe	Output
39	NC	Not Connected	
40	R//W	Read/Write	Output
41-43	P25-27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp Power Dissipation		2.2	W

Notes:
* Voltage on all pins with respect to GND.
See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Test Load Diagram).

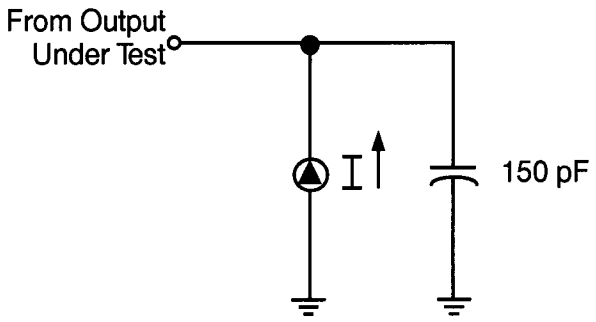

Figure 6. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, Unmeasured pins to GND

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	TA = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	2.0V		7		V	$I_{IN} < 250\ \mu A$	
		4.5V		7		V	$I_{IN} < 250\ \mu A$	
V_{CH}	Clock Input High Voltage	2.0V	0.7 V_{CC}	V_{CC}+0.3		V	Driven by External Clock Generator	
		4.5V	0.7 V_{CC}	V_{CC}+0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	GND-0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
		4.5V	GND-0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	0.7 V_{CC}	V_{CC}+0.3		V		
		4.5V	0.7 V_{CC}	V_{CC}+0.3		V		
V_{IL}	Input Low Voltage	2.0V	GND-0.3	0.2 V_{CC}		V		
		4.5V	GND-0.3	0.2 V_{CC}		V		
V_{OH1}	Output High Voltage	2.0V	V_{CC}-0.4			V	I_{OH} = -1.0 mA	8
		4.5V	V_{CC}-0.4			V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	2.0V		0.6		V	I_{OL} = +4.0 mA	8
		4.5V		0.4		V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	2.0V		1.2		V	I_{OL} = +6 mA	8
		4.5V		1.2		V	I_{OL} = +12 mA	8
V_{RH}	Reset Input High Voltage	2.0V	.8 V_{CC}	V_{CC}		V		
		4.5V	.8 V_{CC}	V_{CC}		V		
V_{RI}	Reset Input Low Voltage	2.0V	GND-0.3	0.2 V_{CC}		V		
		4.5V	GND-0.3	0.2 V_{CC}		V		
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		10
		4.5V		25	10	mV		10
I_{IL}	Input Leakage	2.0V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	2.0V	-1	1	<1	µA	V_{IN} = 0V, V_{CC}	
		4.5V	-1	1	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	2.0V		-130	-25	µA		
		4.5V		-180	-40	µA		
I_{CC}	Supply Current	2.0V		10		mA	@ 8 MHz	4
		4.5V		17		mA	@ 8 MHz	4
I_{CC1}	Standby Current	2.0V		4.0		mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	4
		4.5V		6.0		mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	4
		2.0V		3.0		mA	Clock Divide-by-16 @ 8 MHz	4
		4.5V		5.0		mA	Clock Divide-by-16 @ 8 MHz	4

Sym	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC2}	Standby Current	2.0V		8		µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	6,11
		4.5V		10		µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	6,11,14
		2.0V		500		µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	6,11,14
		4.5V		1000		µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	6,11,14
V_{ICR}	Input Common Mode Voltage Range	2.0V	0	V_{CC}-1.0V		V		10
		4.5	0	V_{CC}-1.0V		V		10
I_{ALL}	Auto Latch Low Current	2.0V	0.7	8	2.4	µA	$0V < V_{IN} < V_{CC}$	9
		4.5V	1.4	25		µA	$0V < V_{IN} < V_{CC}$	9
I_{ALH}	Auto Latch High Current	2.0V	-0.6	-5	-1.8	µA	$0V < V_{IN} < V_{CC}$	9
		4.5V	-1.0	-14		µA	$0V < V_{IN} < V_{CC}$	9
V_{LV}	V_{CC} Low Voltage Protection Voltage			2.15		V	2 MHz max Int. CLK Freq.	7
V_{OH}	Output High Voltage (Low EMI Mode)	2.0V	V_{CC}-0.4			V	I_{OH} = -0.25 mA	
		4.5V	V_{CC} -0.4			V	I_{OH} = -0.5 mA	
V_{OL}	Output Low Voltage (Low EMI Mode)	2.0V		0.6	0.2	V	I_{OL} = 1.0 mA	
		4.5V		0.4	0.1	V	I_{OL} = 1.0 mA	

Notes:

1.

I_{CC1}	Typ	Max	Unit	Freq
Clock-Driven	0.3 mA	5	mA	8 MHz

2. GND = 0V.
3. V_{CC} = 2.0V to 4.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 10 pF.
6. Same as note [4] except inputs at V_{CC}.
7. The V_{LV} voltage increases as the temperature decreases and will overlap lower VCC operating region.
8.]Standard Mode (not Low EMI).
9. Auto Latch (Mask Option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Typicals are at V_{CC} = 3.0V.
14. Internal RC selected.

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Diagram (L43 Only)

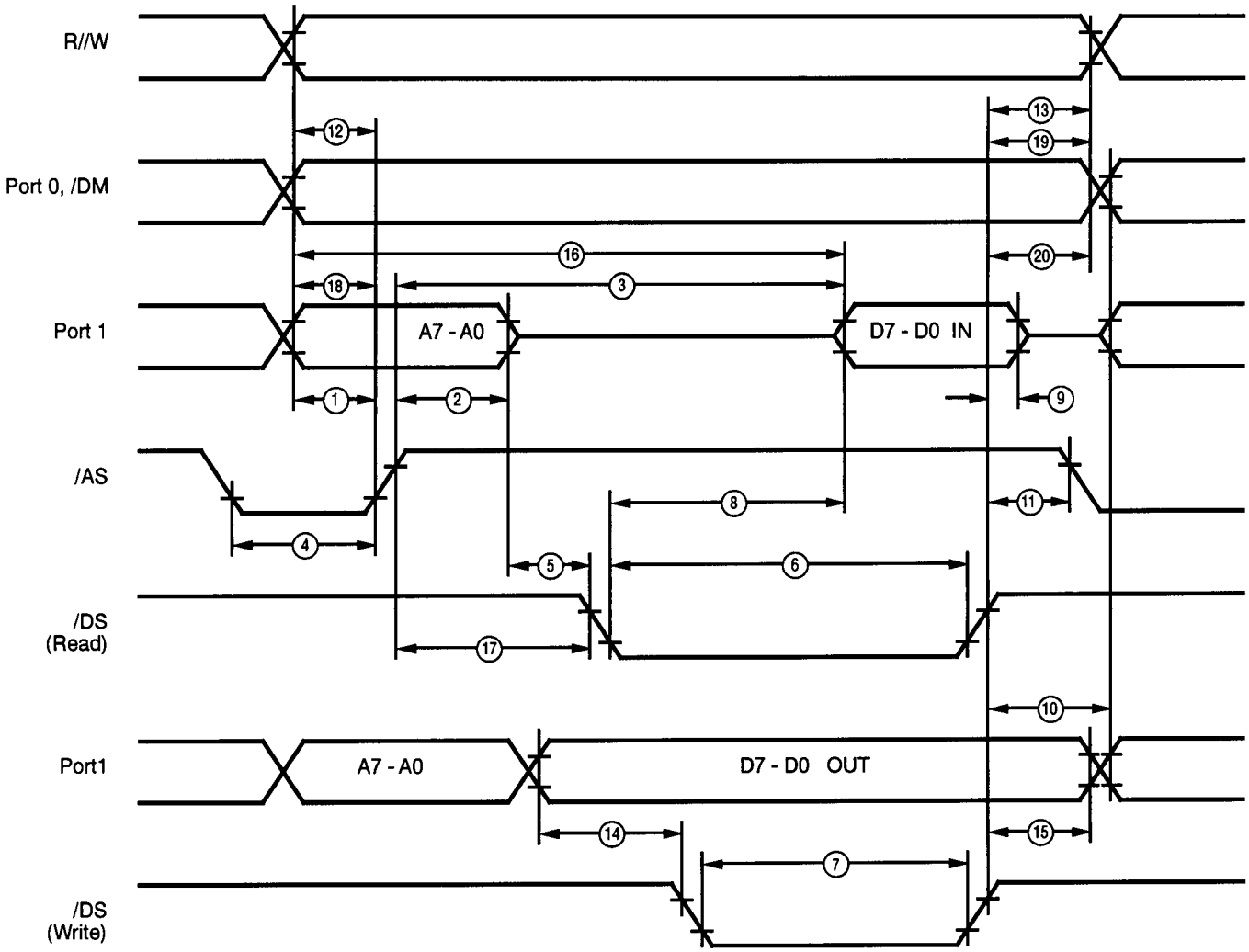

Figure 7. External I/O or Memory Read/Write Timing (Z86L43 Only)

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table (L43 Only)
(SCLK/TCLK = XTAL/2)

			T_A = 0°C to +70°C				
			Note 3	8 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	2.0V	35		ns	2
			4.5V	35		ns	
2	TdAS(A)	/AS Rise to Address Float Delay	2.0V	45		ns	2
			4.5V	45		ns	
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	2.0V		250	ns	1,2
			4.5V		250	ns	
4	TwAS	/AS Low Width	2.0V	55		ns	2
			4.5V	55		ns	
5	TdAS(DS)	Address Float to /DS Fall	2.0V	0		ns	
			4.5V	0		ns	
6	TwDSR	/DS (Read) Low Width	2.0V	200		ns	1,2
			4.5V	200		ns	
7	TwDSW	/DS (Write) Low Width	2.0V	110		ns	1,2
			4.5V	110		ns	
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	2.0V		150	ns	1,2
			4.5V		150	ns	
9	ThDR(DS)	Read Data to /DS Rise Hold Time	2.0V	0		ns	2
			4.5V	0		ns	
10	TdDS(A)	/DS Rise to Address Active Delay	2.0V	45		ns	2
			4.5V	55		ns	
11	TdDS(AS)	/DS Rise to /AS Fall Delay	2.0V	30		ns	2
			4.5V	45		ns	
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	2.0V	45		ns	2
			4.5V	45		ns	
13	TdDS(R/W)	/DS Rise to R//W Not Valid	2.0V	45		ns	2
			4.5V	45		ns	
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	2.0V	45		ns	2
			4.5V	55		ns	
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	2.0V	45		ns	2
			4.5V	45		ns	
16	TdA(DR)	Address Valid to Read Data Req'd Valid	2.0V		310	ns	1,2
			4.5V		310	ns	
17	TdAS(DS)	/AS Rise to /DS Fall Delay	2.0V	65		ns	2
			4.5V	65		ns	
18	TdDM(AS)	/DM Valid to /AS Rise Delay	2.0V	35		ns	2
			4.5V	35		ns	
19	TdDS(DM)	/DS Rise to DM Valid Delay	2.9V	45		ns	
			4.5V	45		ns	
20	ThDS(AS)	/DS Valid to Address Valid Hold Time	2.0V	45		ns	
			4.5V	45		ns	

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. V_{CC} = 2.0V to 4.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

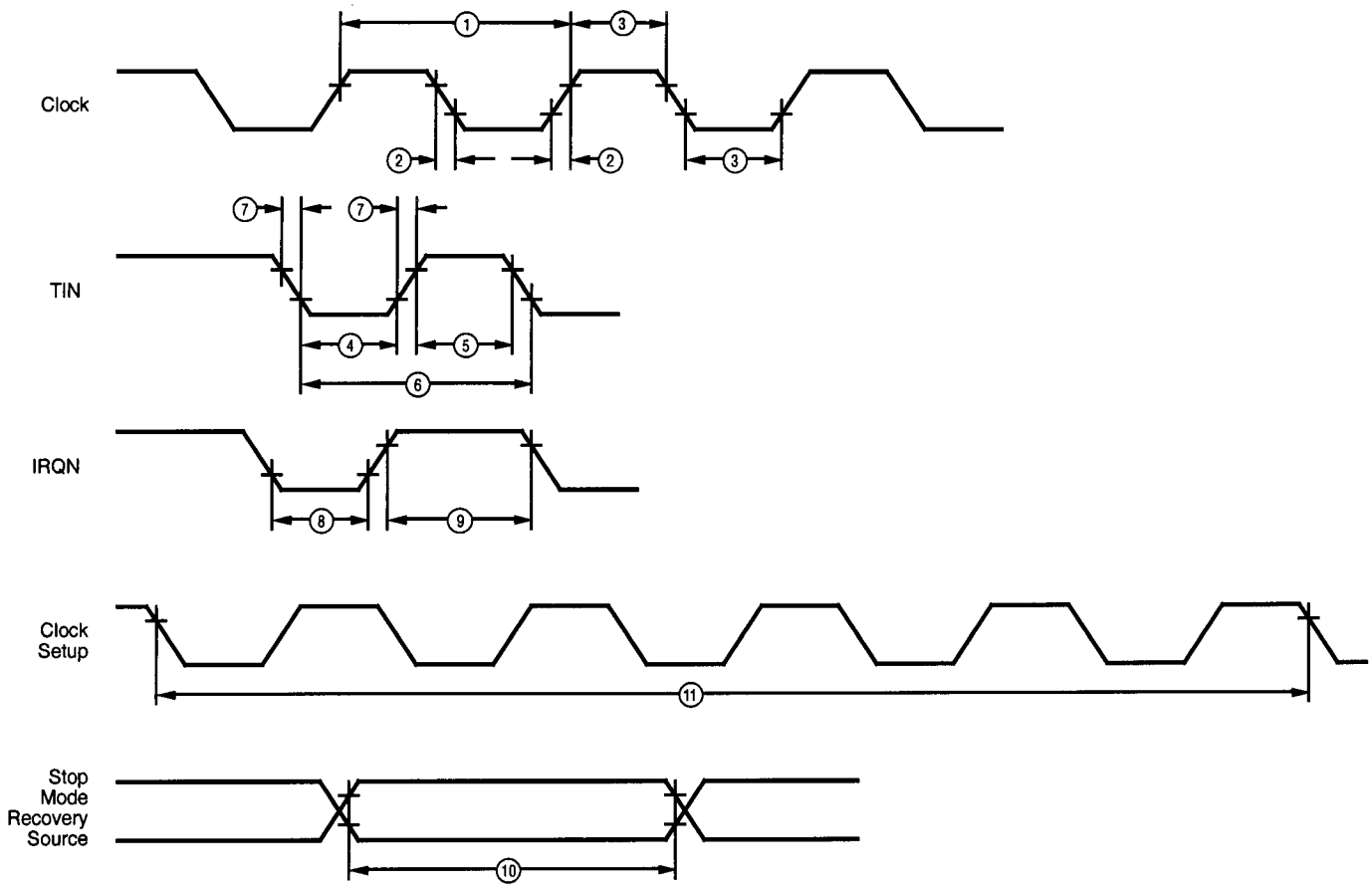

Figure 8. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (SCLK/TCLK=XTAL/2)

				T_A = 0°C to +70°C			
			Note [3]	8 MHz			
No	Sym	Parameter	V_{CC}	Min	Max	Units	Notes
1	TpC	Input Clock Period	2.0V	83	DC	ns	1
			4.5V	83	DC	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times	2.0V		15	ns	1
			4.5V		15	ns	1
3	TwC	Input Clock Width	2.0V	41		ns	1
			4.5V	41		ns	1
4	TwTinL	Timer Input Low Width	2.0V	100		ns	1
			4.5V	70		ns	1
5	TwTinH	Timer Input High Width	2.0V	5TpC			1
			4.5V	5TpC			1
6	TpTin	Timer Input Period	2.0V	8TpC			1
			4.5V	8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	2.0V		100	ns	1
			4.5V		100	ns	1
8A	TwIL	Int. Request Low Time	2.0V	100		ns	1,2
			4.5V	70		ns	1,2
8B	TwIL	Int. Request Low Time	2.0V	5TpC			1,3
			4.5V	5TpC			1,3
9	TwIH	Int. Request Input High Time	2.0V	5TpC			1,2
			4.5V	5TpC			1,2
10	Twsm	STOP Mode Recovery Width Spec	2.0V	12		ns	
			4.5V	12		ns	
11	Tost	Oscillator Startup Time	2.0V		5TpC		4
			4.5V		5TpC		D1, D0,4
12	Twdt	Watch-Dog Timer Delay Time (Before Refresh is Necessary)	2.0V	7		ms	0, 0 [5]
			4.5V	2		ms	0, 0 [5]
			2.0V	14		ms	0, 1 [5]
			4.5V	4		ms	0, 1 [5]
			2.0V	28		ms	1, 0 [5]
			4.5V	7		ms	1, 0 [5]
			2.0V	112		ms	1, 1 [5]
			4.5V	28		ms	1, 1 [5]
13	T_{POR}	Power-On Reset Delay	2.0V		45	ms	
			4.5V		25	ms	

Notes:

1. Timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30)
4. SMR-D5=0.
5. Reg. WDTMR.
6. V_{CC} = 2.0V to 4.5V.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = XTAL)

				T_A = 0°C to +70°C			
			Note [6]	4 MHz			
No	Sym	Parameter	V_{CC}	Min	Max	Units	Notes
1	TpC	Input Clock Period	2.0V	250	DC	ns	1,7,8
			4.5V	250	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	2.0V		25	ns	1,7,8
			4.5V		25	ns	1,7,8
3	TwC	Input Clock Width	2.0V	125		ns	1,7,8
			4.5V	125		ns	1,7,8
4	TwTinL	Timer Input Low Width	2.0V	100		ns	1,7,8
			4.5V	70		ns	1,7,8
5	TwTinH	Timer Input High Width	2.0V	3TpC			1,7,8
			4.5V	3TpC			1,7,8
6	TpTin	Timer Input Period	2.0V	4TpC			1,7,8
			4.5V	4TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	2.0V		100	ns	1,7,8
			4.5V		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	2.0V	100		ns	1,2,7,8
			4.5V	70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	2.0V	3TpC			1,3,7,8
			4.5V	3TpC			1,3,7,8
9	TwIH	Int. Request Input High Time	2.0V	3TpC			1,2,7,8
			4.5V	3TpC			1,2,7,8
10	Twsm	STOP Mode Recovery Width Spec	2.0V	12		ns	4,8
			4.5V	12		ns	4,8
11	Tost	Oscillator Startup Time	2.0V		5TpC		4,8,9
			4.5V		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P33-P31)
3. Interrupt request via Port 3 (P30).
4. SMR-D5=1, POR STOP Mode delay is on.
5. Reg. WDTMR.
6. V_{CC} = 2.0V to 4.5V.
7. SMR D1=0.
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Diagrams

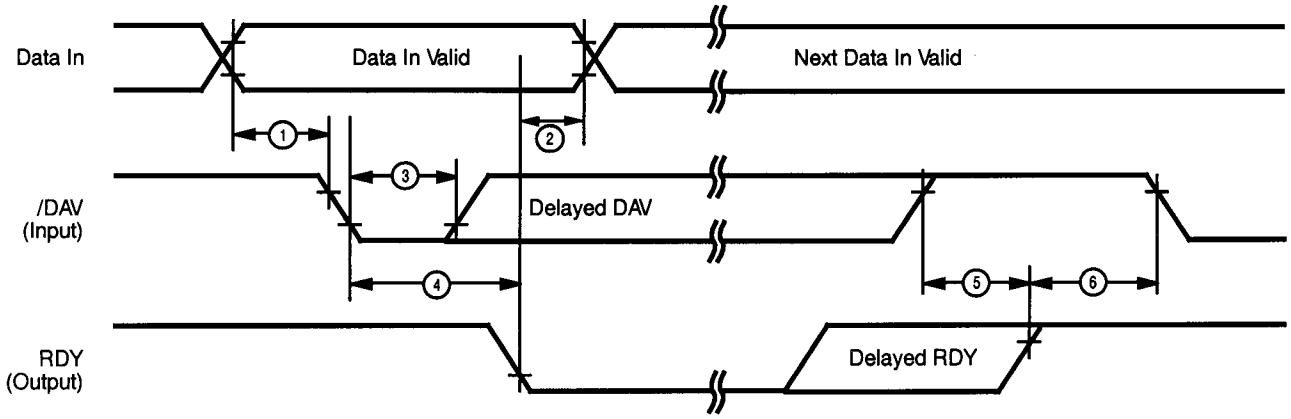

Figure 9. Input Handshake Timing

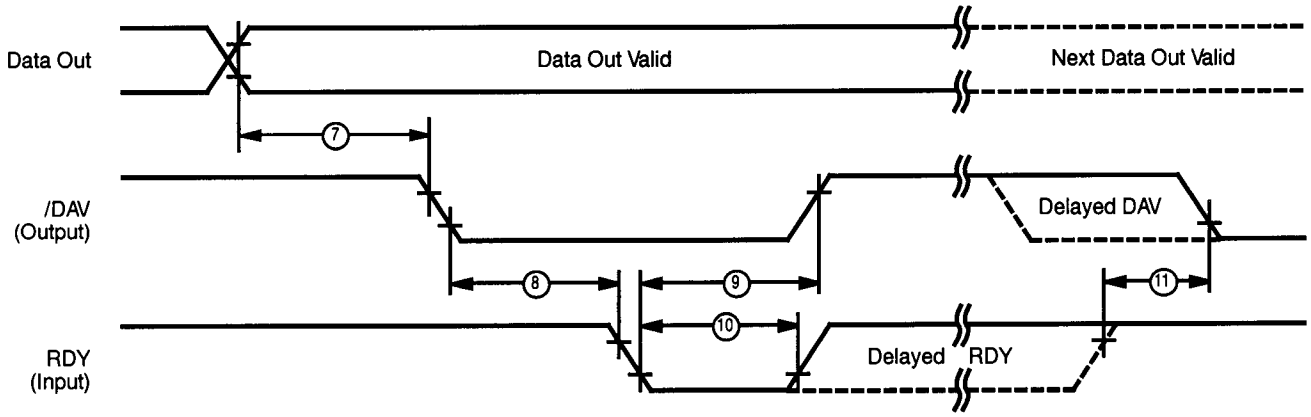

Figure 10. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

			T_A= 0°C to +70°C				
			V_{CC}	8 MHz			Direction
No	Symbol	Parameter	Note [1]	Min	Max	Units	Data
1	TsDI(DAV)	Data In Setup Time	2.0V	0		ms	IN
			4.5V	0		ms	IN
2	ThDI(RDY)	Data In Hold Time	2.0V	0		ms	IN
			4.5V	0		ms	IN
3	TwDAV	Data Available Width	2.0V	155		ms	IN
			4.5V	110		ms	IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	2.0V		0	ms	IN
			4.5V		0	ms	IN
5	TdDAVId(RDY)	DAV Out to DAV Fall Delay	2.0V		120	ms	IN
			4.5V		80	ms	IN
6	RDY0d(DAV)	RDY Rise to DAV Fall Delay	2.0V	0		ms	IN
			4.5V	0		ms	IN
7	TdD0(DAV)	Data Out to DAV Fall Delay	2.0V	42		ms	OUT
			4.5V	42		ms	OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	2.0V	0		ms	OUT
			4.5V	0		ms	OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	2.0V		160	ms	OUT
			4.5V		115	ms	OUT
10	TwRDY	RDY Width	2.0V	110		ms	OUT
			4.5V	80		ms	OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	2.0V		110	ms	OUT
			4.5V		80	ms	OUT

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. V_{CC} = 2.0V to 4.5V..

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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