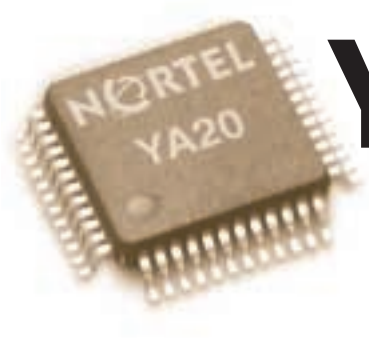

YA20 2.5 Gb/s 1:16 Demultiplexer

Data Sheet

Features

Data and clock inputs accept differential CML signals at up to 2.5 Gb/s

Internally generated divide-by-16 clock and deserialized data delivered via PECL 100 k outputs

Fully differential internal logic for improved noise performance

Typical power dissipation 960 mW

Single 3.3 V supply for simplified system integration

Industry standard LQFP package

Tightly controlled output propagation delays across the 16 outputs

Applications

SONET/SDH-based transmission systems, test equipment and modules

OC-48 fibre optic modules and line termination

WDM for 2.5 Gb/s SONET applications

ATM over SONET/SDH

Section repeaters, muxes, terminators, broadband cross-connects

The Nortel Networks YA20 1:16 Demultiplexer assembles a 2.5 Gb/s input datastream into 16-bit wide 155 Mb/s parallel data. For maximum flexibility it is configured to interface with an external clock and data recovery device such as the Nortel Networks YA18. The CML inputs of the YA20 are configured to interface directly with the YA18 Clock and Data Recovery device.

The Microelectronics Group of Nortel Networks offers a portfolio of optical networking ICs for use in high-performance optical transmitter and receiver functions. The YA20 provides for power and chip-count savings that translate into better utilization of board real-estate and ultimately cost savings to the designer of fibre-based datacom or telecom solutions.

The device is fabricated using Nortel Networks' NT25 high yield, silicon bipolar process. Each product is available in an industry-standard package.

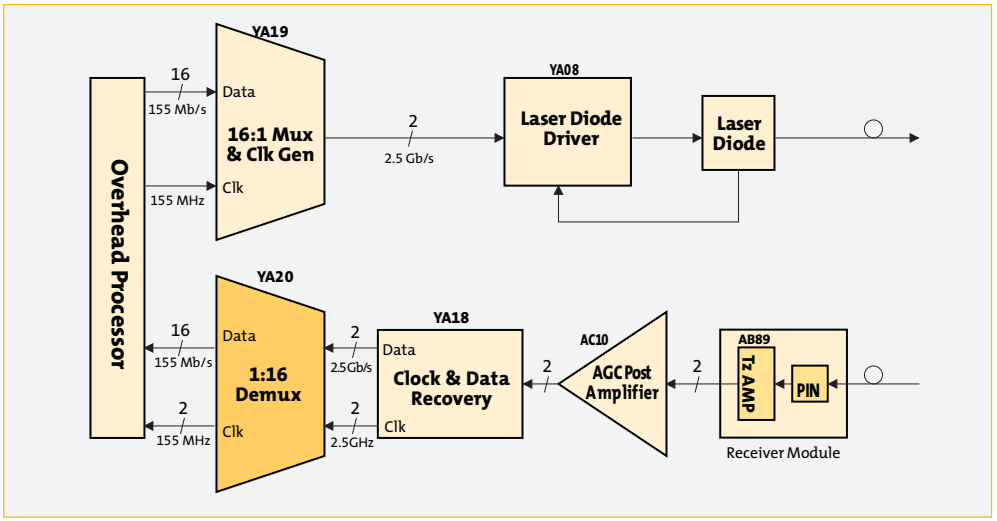

Figure 1: System Block Diagram

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Functional Description

The YA20 demultiplexes a single serial input stream, at up to 2.5 Gb/s, to parallel data on a 16-bit output bus at up to 155 Mb/s. The device is designed to be used with an external clock and data recovery function. The input is captured on the rising edge of the 2.5 GHz clock at the front end of a demultiplexer tree, from where it is progressively converted to 16 bit parallel data at 155 Mb/s. Output changes occur following the falling edge of a 155 MHz clock which is obtained by division from the 2.5 GHz input clock. This 155 MHz clock is also delivered differentially to output pins.

Apart from standard decoupling capacitors, the only external components required are the PECL output termination resistors.

The device operates from a single +3.3 V (±5%) power supply.

System Inputs

The clock and multiplexed data inputs CK2G5_INP/N and RXD_INP/N, which accept signals from a clock and data recovery device, are differential CML. They are terminated on-chip with 50 Ω (nominal) resistors. Data output from the Nortel Networks YA18 Clock and Data Recovery Circuit will be changing on the falling edge of the 2.5 GHz clock and are read into the demultiplexer on the rising edge of CK2G5_INP.

System Outputs

The 16-bit demultiplexed data is output to pins RXD_OUT0 to RXD_OUT15, which are single ended, unterminated, 100 k PECL outputs. The associated 155MHz clock on pins CK155_OUTP/N is of differential PECL type, again unterminated. Data transfer to the output bus is timed from the falling edge of CK155_OUTP as shown in the timing diagram, Figure 3. All PECL outputs are designed to be terminated externally with 50 Ω resistors connected to a V_{CC}-2 Volt supply.

The serial data stream is mapped on to the output bus in conventional order, i.e.bit0 precedes bit1, etc. Since framing information is not extracted at this stage, the actual data bytes might be split across consecutive output words from the demultiplexer. The actual split is indeterminate, but will not change until loss-of-signal or loss-of-lock occurs in the receive path. The device is designed for frame coding to be recovered and utilized in a processor that follows the demultiplexing function.

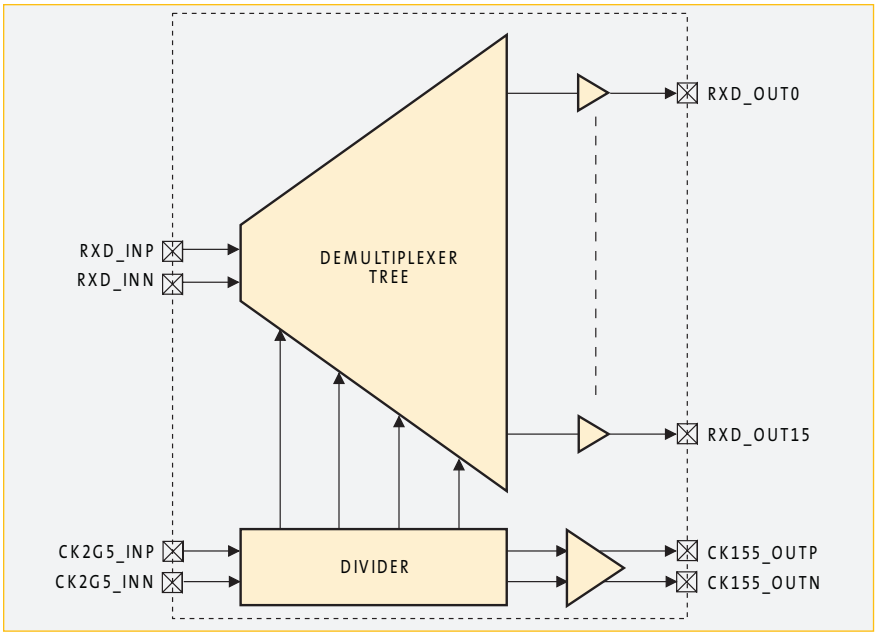

Figure 2: Functional Block Diagram

Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of, the device. Avoid operating the device outside the recommended operating conditions defined below.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage – any V_{CC} pin	-0.7	6.0	V
V_{Icml}	CML input voltage – single ended wrt GND	0	V_{CC}+0.5	V
I_{OPECL}	Output current – PECL outputs		-50	mA
Tstg	Storage temperature	-65	135	˚C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage – any V_{CC} pin	3.13	3.3	3.47	V
V_{IDcml}	CML differential input voltage (peak)	60	350	750	mV
V_{Icml}	CML input voltage, recommended overall range	2.15		V_{CC}	V
Tamb	Operating ambient temperature	-40		85	˚C

DC Electrical Characteristics

Over recommended operating conditions. Outputs terminated in 50 Ω to (VCC-2) Volts

Symbol	Parameter	Min	Typ	Max	Unit
VOHpecl	LVPECL output HIGH voltage	VCC-1.085		VCC-0.88	V
VOLpecl	LVPECL output LOW voltage	VCC-1.83		VCC-1.555	V
RINdiff	Differential input resistance	85	100	115	Ω
RINeff	Effective signal input resistance	42	50	58	Ω
Icc	Supply current		291	390	mA
Pd	Device power dissipation		0.96	1.35	W

AC Characteristics

Over recommended operating conditions. Outputs terminated in 50 Ω to (VCC-2) Volts

Symbol	Parameter	Min	Typ	Max	Unit
TSUdi	Data input SETUP time wrt CK2G5_INP rising edge			100	ps
THdi	Data input HOLD time wrt CK2G5_INP rising edge			100	ps
TRpecl	PECL output rise time	0.5		1.5	ns
TFpecl	PECL output fall time	0.5		1.5	ns
CKmsr	CK155_OUTP/N mark to space ratio	45		55	%
Tpd	Propagation delay from falling edge of CK155_OUT to RXD_OUTn	0.8		1.6	ns

Design Procedure and Applications Information

Timing Information

Data inputs as delivered from the YA18 Clock and Data Recovery Circuit will be changing on the falling edge of the 2.5 GHz clock, hence they are read into the demultiplexer on the rising edge of CK2G5_INP, as shown in Figure 3 below.

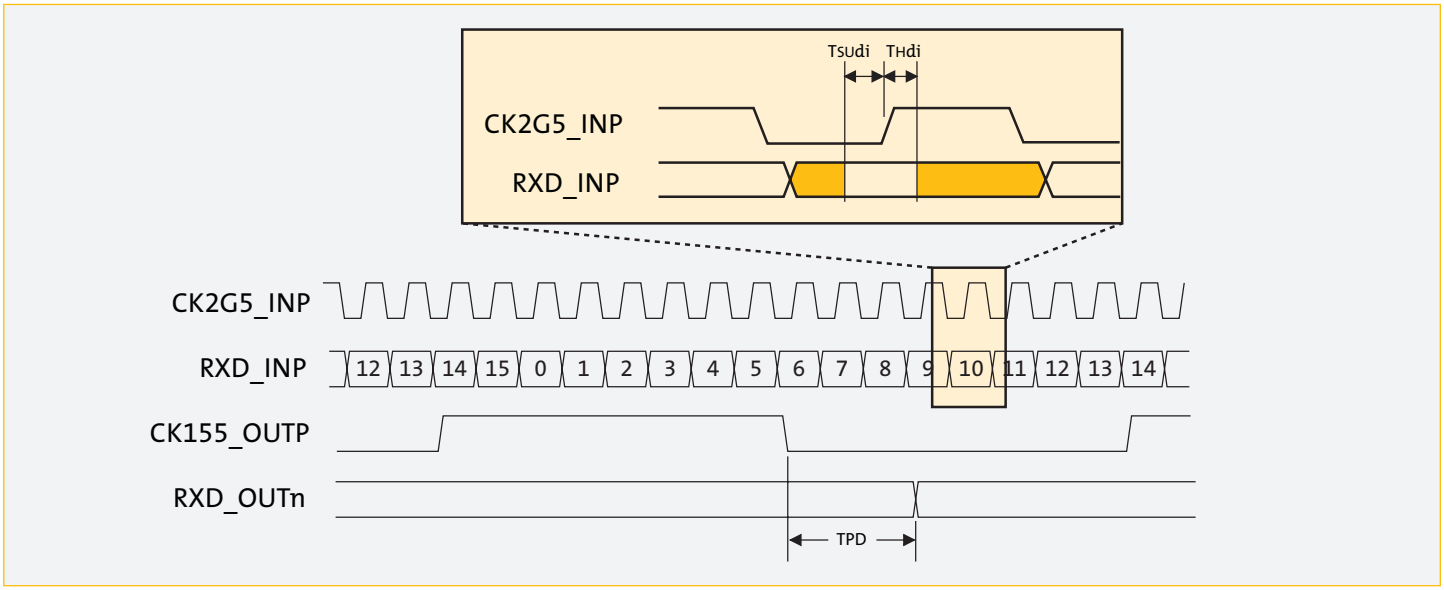

Figure 3: Signal Timing Diagram

Input Interfacing

As with other members of the OC-48/STM-16 2.5 Gb/s optical networking ICs family, the high speed (2.5 Gbps/2.5 GHz) inputs of the YA20 are configured as fully differential CML signal pairs as shown in Figure 4. The inputs are internally terminated with a 100 Ω resistor between the differential inputs and require a typical differential peak voltage of 350 mV. However, the inputs to the YA20 will continue to operate correctly with a peak differential input voltage as low as 60 mV, see Figure 5. Although the YA20 is specifically designed to interface with the Nortel Networks YA18 Clock and Data Recovery device, it is possible to drive the inputs from a range of alternative differential signal sources with voltage levels of between 60 mV and 750 mV peak differential.

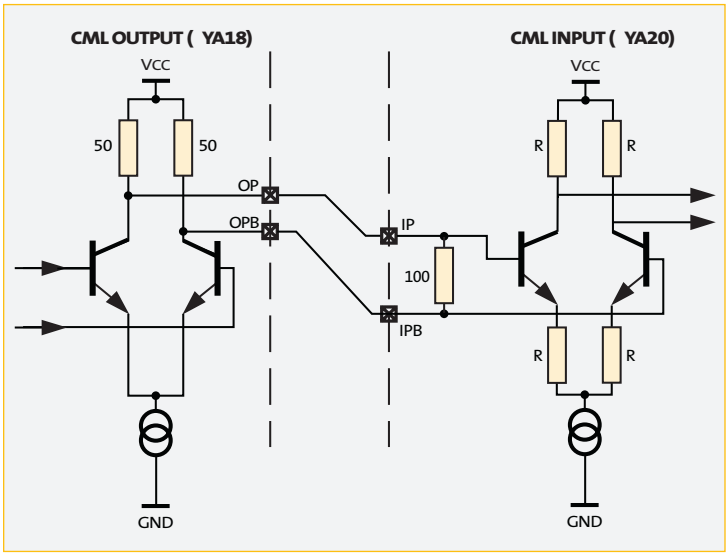

Figure 4: CML Input and Output Configurations

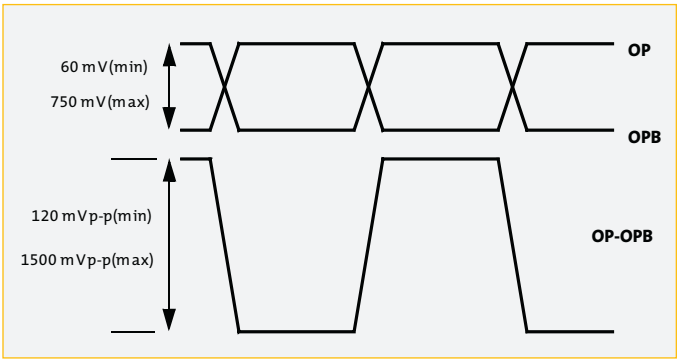

Figure 5: CML Output Differential Voltage Levels

Pin Assignments

Pin No	Symbol	Type	Description	Function
1, 8,25, 45	VCC_CORE	P		Positive supply pins for digital core
2,12,36	GND_CORE	P		Supply ground for digital core
3, 6, 9, 10, 14, 16	VCC_OUT1	P		Positive supply pins for PECL outputs (CK155_OUTP/N and RXD_OUT0,1,2,3)
4	CK155_OUTN	O	PECL 100 K	155 MHz Clock differential negative output
5	CK155_OUTP	O	PECL 100 K	155 MHz Clock differential positive output
7	RXD_OUT0	O	PECL 100 K	Parallel data output, bit 0 (MSB)
11	RXD_OUT1	O	PECL 100 K	Parallel data output, bit1
13	RXD_OUT2	O	PECL 100 K	Parallel data output, bit2
15	RXD_OUT3	O	PECL 100 K	Parallel data output, bit3
17	RXD_OUT4	O	PECL 100 K	Parallel data output, bit4
18, 20, 22, 23, 27, 29	VCC_OUT2	P		Positive supply pins for PECL outputs (RXD_OUT4,5,6,7,8,9)
19	RXD_OUT5	O	PECL 100 K	Parallel data output, bit5
21	RXD_OUT6	O	PECL 100 K	Parallel data output, bit6
24	RXD_OUT7	O	PECL 100 K	Parallel data output, bit7

Pin Assignments (continued)

Pin No	Symbol	Type	Description	Function
26	RXD_OUT8	O	PECL 100 K	Parallel data output, bit8
28	RXD_OUT9	O	PECL 100 K	Parallel data output, bit9
30	RXD_OUT10	O	PECL 100 K	Parallel data output, bit10
31, 33, 35, 38, 40, 42	VCC_OUT3	P		Positive supply pins for PECL outputs (RXD_OUT10,11,12,13,14,15)
32	RXD_OUT11	O	PECL 100 K	Parallel data output, bit11
34	RXD_OUT12	O	PECL 100 K	Parallel data output, bit12
37	RXD_OUT13	O	PECL 100 K	Parallel data output, bit13
39	RXD_OUT14	O	PECL 100 K	Parallel data output, bit14
41	RXD_OUT15	O	PECL 100 K	Parallel data output, bit15 (LSB)
43	RXD_INN	I	CML	Serial data negative differential input
44	RXD_INP	I	CML	Serial data positive differential input
46	CK2G5_INN	I	CML	2.5 GHz clock negative differential input
47	CK2G5_INP	I	CML	2.5 GHz clock positive differential input

Package Pin Configuration

The device is packaged in a 48-lead plastic low-profile quad flat pack (LQFP). To achieve the required thermal resistance, the package contains a heat slug which must be soldered directly to the circuit board.

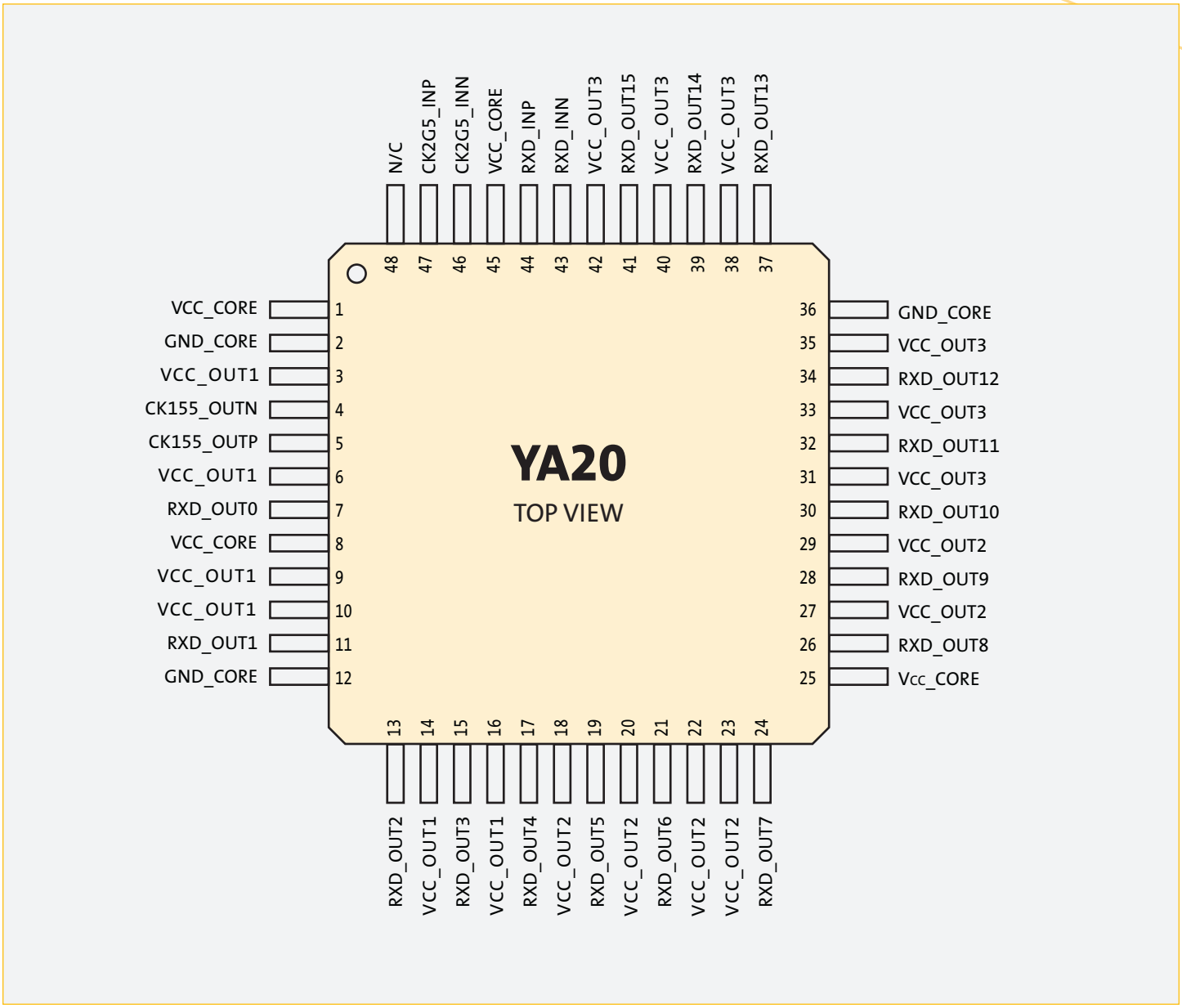

Figure 6: 48-lead LQFP

Package Outline Drawing and Dimensions

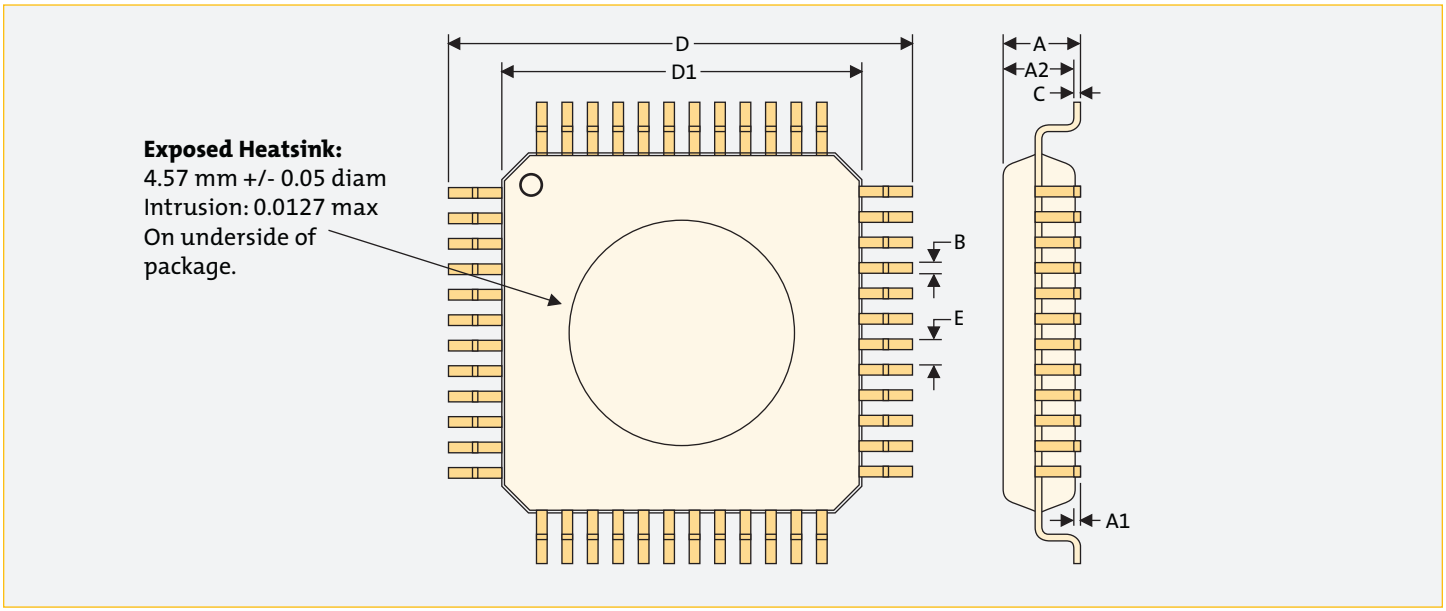

Figure 7: Package Outline

Dimension	Min (mm)	Nom (mm)	Max (mm)
Lead pitch (E)		0.50	
Body size (D1)	6.90	7.00	7.10
Component tip-to-tip (D)	8.80	9.00	9.20
Component height (A)			1.60
Component standoff (A1)	0.05		0.15
Body thickness (A2)	1.35	1.40	1.45
Lead width, plated (B)	0.17	0.22	0.27
Lead thickness, plated (C)	0.09		0.20

Notes:

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