YAMAHA LSI

YM3433B

(ALCDF)

2 channel 8 times oversampling Digital Filter

Operatable at system clock independent from input serial clock.

■ OUTLINE

The digital filter's own system clock rate must be considerably faster than the input bit clock rate and at the same time synchronism is required in the system as a whole. Thus what is normally required is a high-speed clock which is synchronous with the signal handling pre-processor. Then the major application problem is how to interface these different clock rates.

This LSI is a high quality 2 channel 8 times oversampling digital filter which has been developed to solve such problems. It can be used easily as an interface in a wide range of digital audio systems. It is pin-compatible with the YM3434 (16-pin DIP).

Since the system clock of this LSI can be different from the serial input signal and it operates normally at any clock rate above 400 clocks for each input sampling frequency (Fs), it is not necessary to change the clock rate even if the sampling frequency is changed.

For example, by connecting a 20MHz crystal oscillator, there is no need to change the clock rate even when the sampling frequency is changed to 32KHz, 44.1KHz or 48KHz.

■ FEATURES

- Operate at system clock independent from the serial input clock
- Input signals can be handled at any of the following input bit clock rates without adding any circuit: 32Fs, 48Fs, 64Fs, 80Fs, 96Fs, 112Fs, 128Fs, 144Fs, 160Fs, 176Fs and 192Fs.
- Capable to cope with sampling frequencies 32KHz, 44.1KHz and 48KHz.
- Linear phase FIR type filters connected in three vertical stages
  - 1st filter : 161st order FIR filter
  - 2nd filter : 33rd order FIR filter
  - 3rd filter : 17th order FIR filter
- Built-in overflow limiter
- Filter characteristics (at 8 times)
  - Pass band ripple : Within ± 0.002dB at 0 to $0.4535 \times Fs$
  - Stop band attenuation : At least 70dB at $0.5465 \times Fs$ to $7.4535 \times Fs$
- Output data switchable between 16 bit and 18 bit
- Switchable between 1 DAC (4 times) and 2 DAC (8 times).
- C-MOS process, +5V power supply, 16-pin DIP or 24-pin SOP package.

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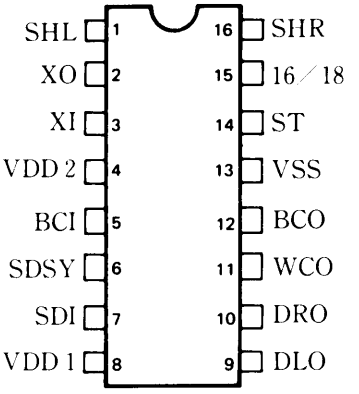
YM3433B CATALOG
CATALOG No.: LSI-2134334
1992. 9

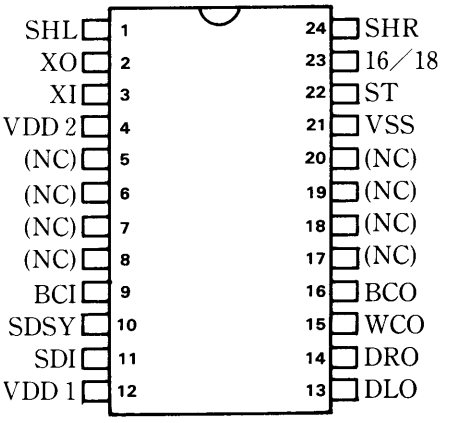
■ PIN CONFIGURATION

YM3433B-D



TOP VIEW

YM3433B-F

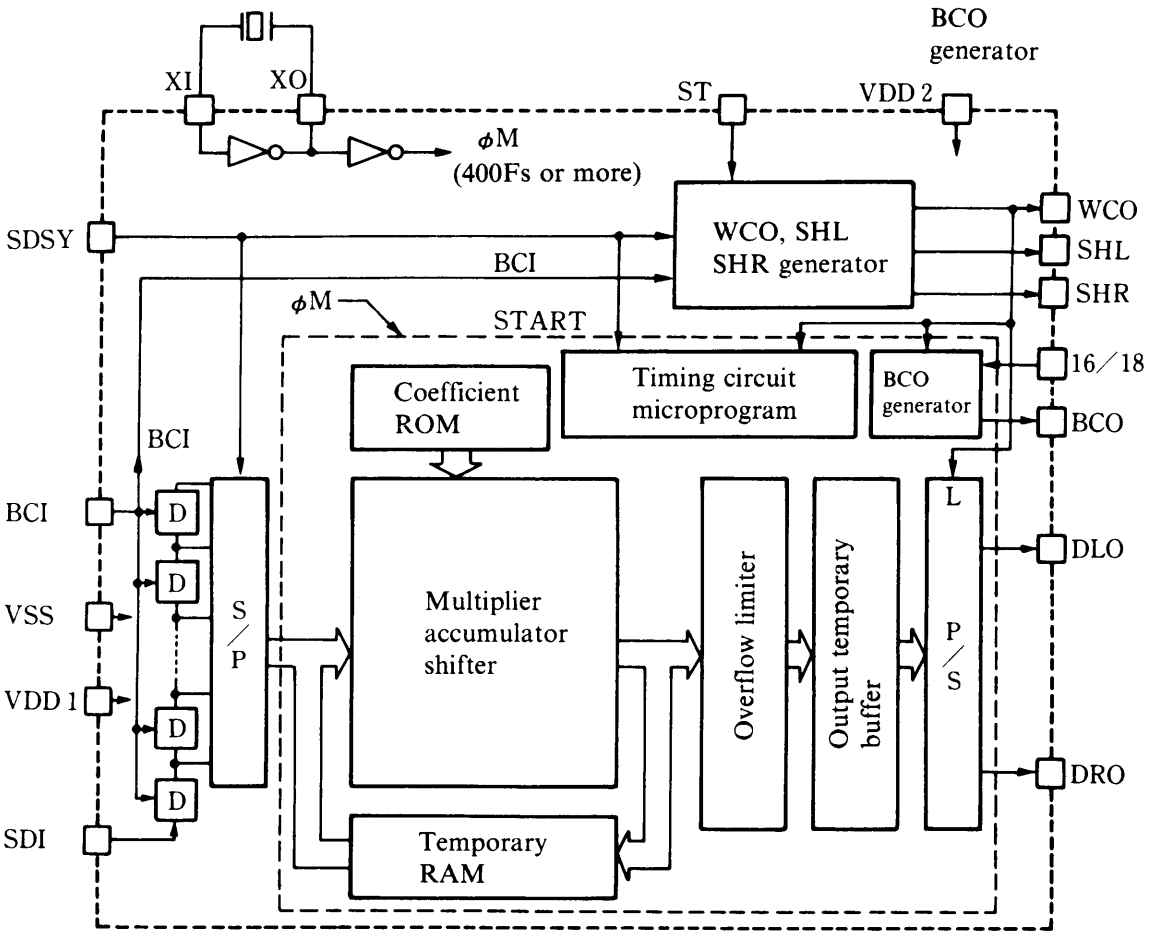


TOP VIEW

■ PIN DESCRIPTION

Terminal name	I/O	Function
SHL	O	1 DAC (ST = 'L'): L channel deglitcher signal 2 DAC (ST = 'H'): L/R channel deglitcher signal
XO XI	O I	Crystal oscillation between XI and XO Clock can be input directly to XI
VDD2	—	+5V power supply for crystal oscillator and deglitcher signal
BCI	I	Bit clock input terminal
SDSY	I	L/R clock input terminal
SDI	I	Data input terminal
VDD1	—	+5V power supply
DLO	O	1 DAC (ST = 'L'): L/R channel data output terminal 2 DAC (ST = 'H'): L channel data output terminal
DRO	O	R channel data output terminal
WCO	O	Word clock output terminal for DLO, DRO output data
BCO	O	Bit clock output terminal for DLO, DRO output data
VSS	—	GND terminal
ST	I	1 DAC/2 DAC switching terminal (1 DAC = 'L', 2 DAC = 'H')
16/18	I	16 bit/18 bit output switching terminal (16 bits = 'L', 18 bits = 'H')
SHR	O	1 DAC (ST = 'L'): R channel deglitcher signal

■ BLOCK DIAGRAM



■ OUTLINE OF FUNCTIONS

- The digital data signal input to the SDI is set in the S/P (serial/parallel) converter based on the synchronized BCI and SDSY signals.
- Generation of the output word clock (WCO) and deglitcher signals (SHL,SHR) is accomplished by counting the input bit clock (BCI) during 1 input word clock (SDSY) cycle.
  If the BCI of 1 SDSY cycle is a multiple of 16 which comes between 32 and 192 ticks, the BCI jitter can be generated so the rate is the same as that of the WCO, SHL, and SHR. However, caution is advised because when any changes take place in the BCI input duty, these are reflected in changes in the WCO, SHR, and SHL as well.
- The digital filter processor operates based on the clock input from the XI terminal.
  Directly after the SDSY change, the XI timing is used to begin the sum of products computation process, and the results are stored in the output temporary buffer.
  When the computation process has been completed, a wait mode is entered until the next SDSY change. Even if the SDSY cycle (sampling frequency) changes, operation will be carried out with the same XI clock.

400 is the minimum number of ticks required from the XI clock for 1 SDSY cycle. However, when there are more than 400 ticks, this will have an affect on the waiting period. (This can also be used with the 384 tick synchronized cycle.)
Data output to the DLO and DRO originates with the timing computed at the SDSY and BCI and is carried out during 1/2 an XI clock cycle, so the timing will be sufficient for the operation of the DA convertor.

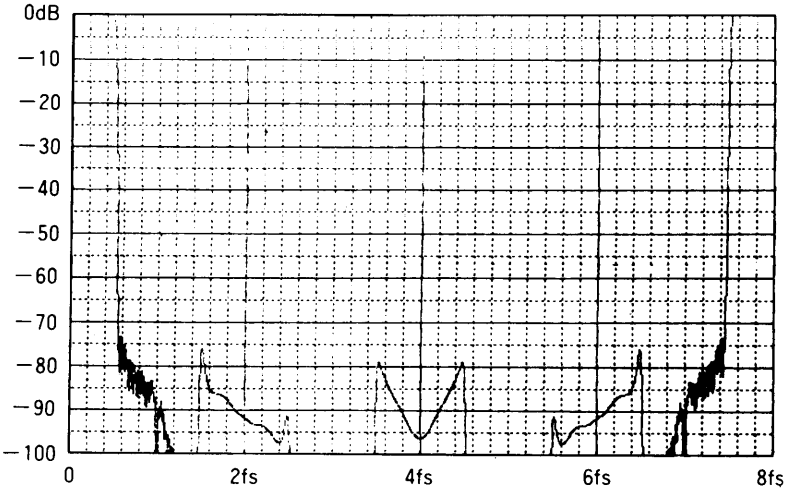
- In the manner described above, this LSI chip works with the signal processor at the previous step without the need for both to be connected to a synchronized clock. In fact, the XI clock does not change according to the sampling frequency, which makes this an interface which acts as a highly reliable digital filter.
- Exceptional performance is obtained from the three section in line filter arrangement, with a linear phase type 161 next FIR filter acting as the initial filter, a linear phase type 33 next FIR filter as the second filter, and a linear phase type 17 next FIR filter as the third filter.
- Given 16 bit 2 channel MSB first input data, input signals at any of the following frequencies can be processed: 32 Fs, 48 Fs, 64 Fs, 80 Fs, 96 Fs, 112 Fs, 128 Fs, 144 Fs, 160 Fs, 176 Fs, 192 Fs
- A 384 tick synchronous clock input sampling frequency (Fs) can be used, just as with the YM3434.
- Through switching done at the ST terminal, output data can be processed in either a 2 DAC (8×) or 1 DAC (4×) format. 16 or 18 bit output data can be switched using the 16/18 bit terminal.

■ FILTER CHARACTERISTICS (Theoretical characteristics)

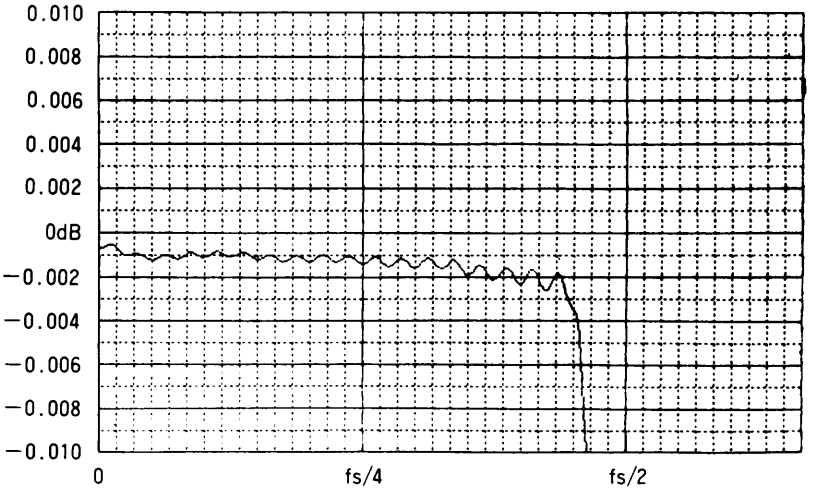
● Filter features (theoretical value)

		at 8 times (2 DAC)	at 4 times (1 DAC)
Passband features	Passband	0 ~ 0.435 × Fs	0 ~ 0.435 × Fs
	Passband ripple	within ±0.002dB	within ±0.002dB
Cutoff band features	Cutoff band	0.5465 × Fs ~ 7.4535 × Fs	0.5465 × Fs ~ 3.4535 × Fs
	Cutoff band reduced capacity	−70dB or more	−70dB or more

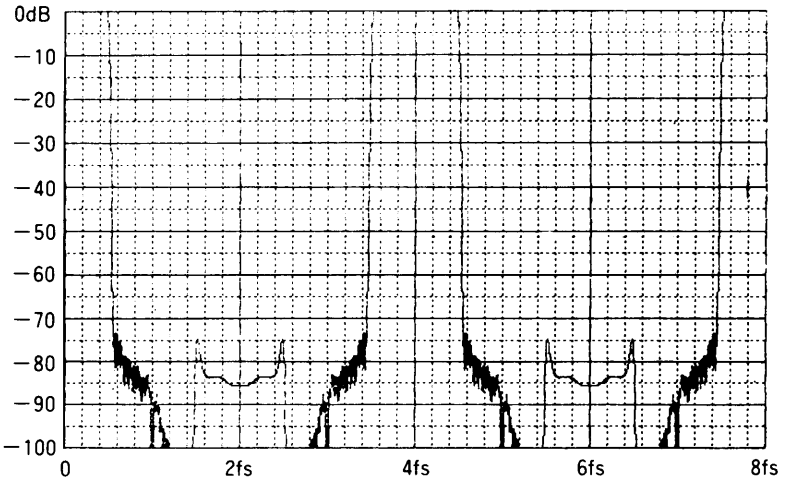
● 8 × (2 DAC)



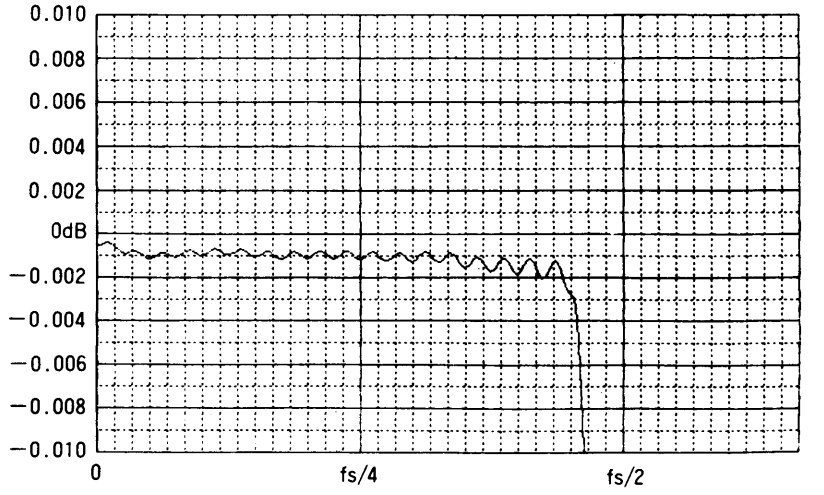
Pass Band Characteristic



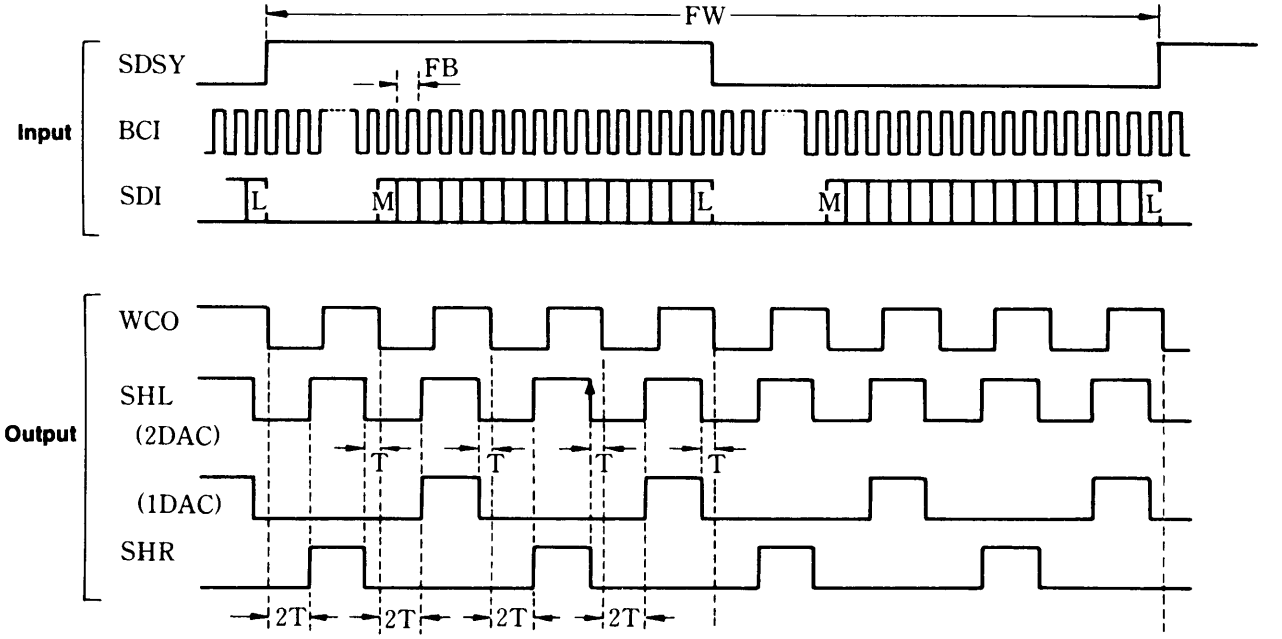
- **4 × (1 DAC)**



Pass Band Characteristic

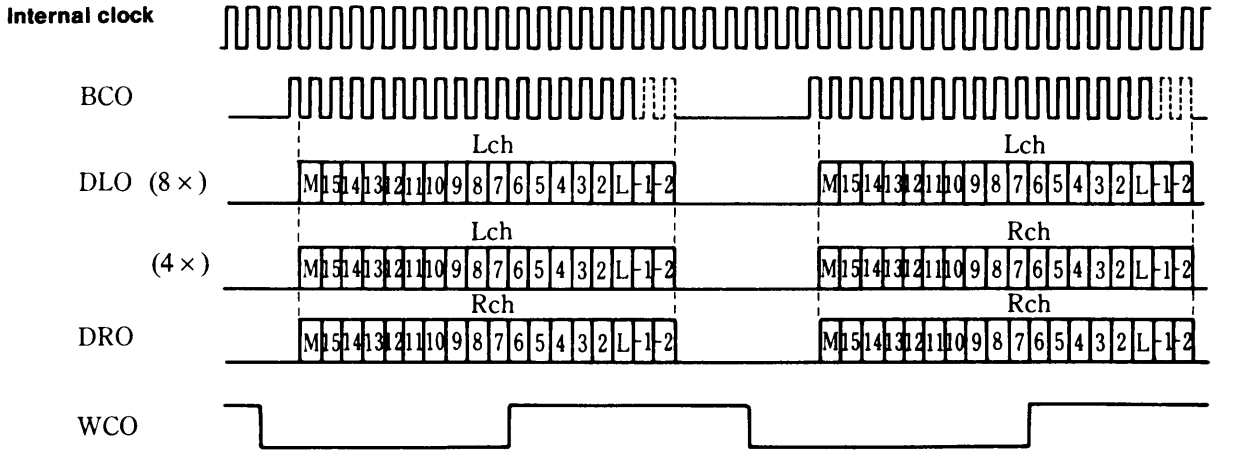


■ SERIAL INPUT TIMING and WCO, SHL, SHR OUTPUT TIMING



- T/2T cycles 32Fs input: T = FB/2: 2T = FB
  48Fs ~ 112 Fs input: T = FB: 2T = 2 × FB
  128Fs ~ input: T = 2 × FB: 2T = 4 × FB
- The required cycle number of the FB during FW must be a multiple of 16 between 32 and 192 ticks. [(32, 48, 64, 80, 96, 112, 128, 144, 160, 176, 192) step]
- The SDSY, BCI, and SDI must be synchronized. WCO, SHL, and SHR output is synchronous. However, the former and the latter groups are not synchronized with each other.

■ SERIAL OUTPUT TIMING



- BCO, DLO, and DRO are synchronous.
- BCO, DLO, DRO, and WCO are not synchronized, but the WCO falling edge is always generated during the period between BCO pulses.
- Appropriate 18 bit output (bit determined by the BCO) for the DLO and DRO −1 and −2 is determined by the high/low selection of the 16/18 bit terminal.
- The BCO clock rate is a 2 part XI input clock cycle.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	V_I	−0.3	V_{DD}+0.5	V
Operating temperature	T_{OP}	−40	85	°C
Storage temperature	T_{STG}	−50	+125	°C

● Recommended Operating Conditions

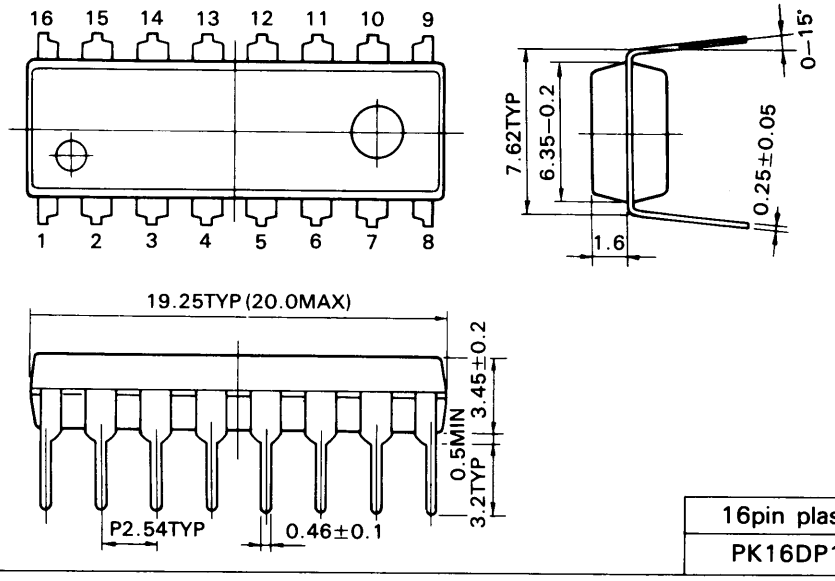
Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Clock frequency	X_{IN}	12.2	(400Fs)	20.0	MHz
Operating temperature	T_{OP}	0	25	70	°C

● Electrical Characteristics (Ta = 25°C, V_{DD} = 5.0V)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Power consumption	W	X_{IN} = 20.0MHz		150	240	mW
High input voltage (XI, 16/18, ST)	V_{IH}		3.5		V_{DD}	V
(BCI, SDSY, SDI)			2.7		V_{DD}	V
Low input voltage	V_{IL}		0		0.8	V
High output voltage	V_{OH}	I_{OH} = 50μA	4.0		V_{DD}	V
Low output voltage	V_{OL}	I_{OL} = 1mA	0		0.4	V
DLO, DRO setup time			15			nS
DLO, DRO hold time			15			nS
Input data setup time (BCI leading edge)			50			nS
Input data hold time (BCI leading edge)			20			nS
XI ON/OFF time (Duty)				50		%
BCI ON/OFF time (Duty)				50		%

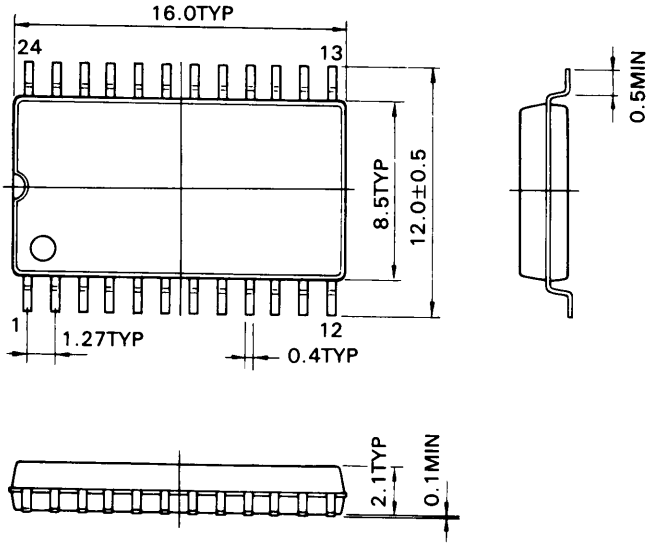
■ EXTERNAL DIMENSIONS

YM3433B-D



16pin plastic DIP
PK16DP1-05-3

YM3433B-F



24pin plastic SOP
PK24SO1-01-1

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