YAMAHA LSI

YSS243B

AC3F

AC-3 5.1ch Full decoder

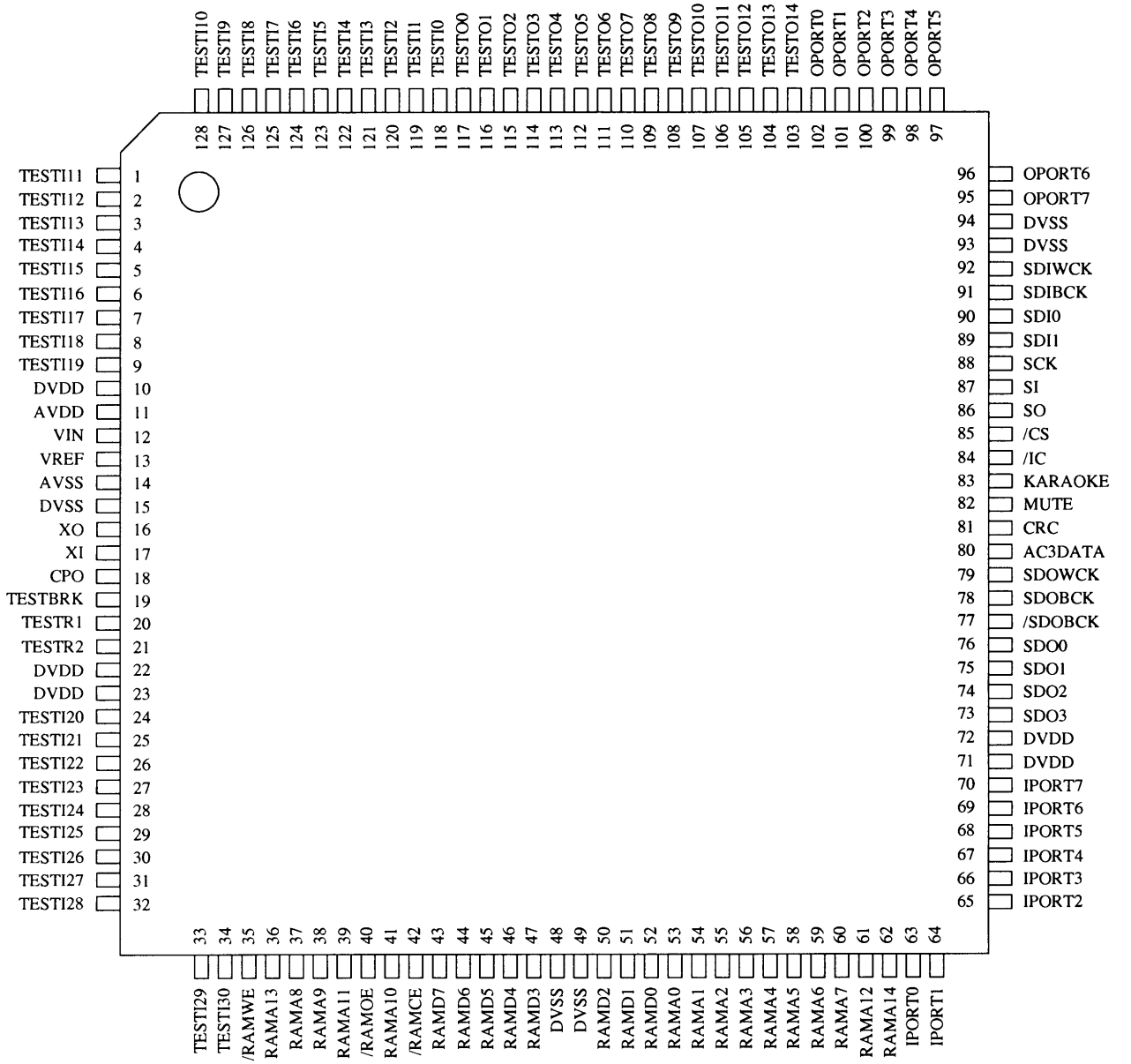
■OUTLINE

YSS243B(AC3F) is a Dolby AC-3 5.1 channel full decoder LSI which decodes the signal that has been coded as prescribed in IEC958 interface standard and outputs PCM data conforming to the Dolby AC-3 specification.
This LSI provides very accurate PCM data, because the decoding process uses 24 bit DSP.
Use of low frequency clock(20 MHz) for its operation achieves low power consumption. Thus, it is not necessary to consider radiation of heat when designing an AC-3 decoding system.

■FEATURES

- Both AC-3 and PCM data can be accepted for input data format. Output channel(s) can be selected from monaural to various down-mixing modes, or 5.1channels of PCM data.
- Processes Dolby AC-3 data at the rate of up to 640 kbps.
- Operates in AC-3 karaoke mode.
- Has a built-in buffer for input data. Has data interface terminals for connection of external SRAM.
  Note:It is necessary to add an external SRAM (256K bits) to be used for buffering the output data.
- Has a built-in PLL oscillation circuit to generate its own operating clock(20 MHz). Thus the frequency of an operating clock generated by the crystal oscillator, or of an external clock, can be selected in the range between 2.5 and 40 MHz.
- Interface formats for input data and output data can be specified independently.
- Processes one selected language data decoding from multi-language encoded data (possible to decode based on data stream number).
- Generates either pink noise or white noise as specified in the control register.
- Has two more mixed signal output channels in addition to 5.1 PCM data output channels.
- Controls time delay of signals at center and surround channels with respect to the left and right channel signals.
- One of four types of dynamic range compression methods recommended by Dolby, can be selected.
- Compression of dynamic range for high amplitude signals and low level signals can be made independently by setting the control register.
- Reads AC-3 bitstream information through the microprocessor interface.
- The delay time for processing AC-3 data decoding is fixed to three audio blocks(768 samples).
- 5V single power supply, Si-gate CMOS process.
- 128 pin QFP (YSS243B-F)

■PIN CONFIGURATION



< 128 pin QFP top view >

■PIN FUNCTION

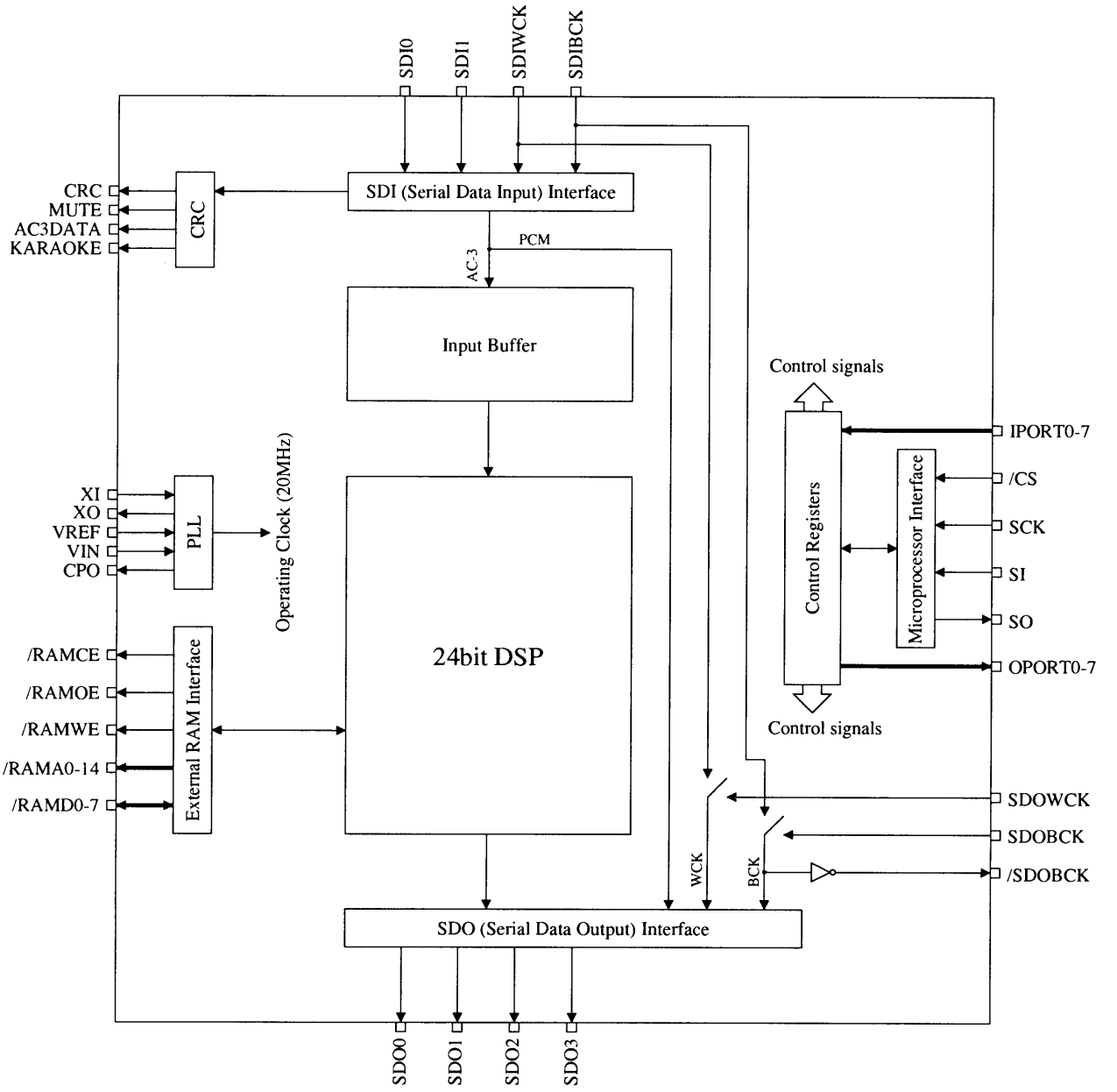
No.	NAME	I/O	FUNCTION
1	TESTI11	I+	LSI test terminal (To be open in use)
2	TESTI12	I+	LSI test terminal (To be open in use)
3	TESTI13	I+	LSI test terminal (To be open in use)
4	TESTI14	I+	LSI test terminal (To be open in use)
5	TESTI15	I+	LSI test terminal (To be open in use)
6	TESTI16	I+	LSI test terminal (To be open in use)
7	TESTI17	I+	LSI test terminal (To be open in use)
8	TESTI18	I+	LSI test terminal (To be open in use)
9	TESTI19	I+	LSI test terminal (To be open in use)
10	DVDD	-	+5V power supply (for digital circuit)
11	AVDD	-	+5V power supply (for PLL circuit)
12	VIN	AI	Input terminal for PLL circuit Connect with CPO terminal through the external analog filter.
13	VREF	AI	Input terminal for PLL circuit Connect with AVDD through the external analog filter.
14	AVSS	-	Ground (for PLL circuit)
15	DVSS	-	Ground (for digital circuit)
16	XO	O	Connect with crystal oscillator
17	XI	I	Connect with crystal oscillator or input external clock (2.5M～40.0MHz)
18	CPO	AO	Output terminal for PLL circuit Connect with VIN terminal through the external analog filter.
19	TESTBRK	I+	LSI test terminal (To be open in use)
20	TESTR1	I+	LSI test terminal (To be open in use)
21	TESTR2	I+	LSI test terminal (To be open in use)
22	DVDD	-	+5V power supply (for digital circuit)
23	DVDD	-	+5V power supply (for digital circuit)
24	TESTI20	I+	LSI test terminal (To be open in use)
25	TESTI21	I+	LSI test terminal (To be open in use)
26	TESTI22	I+	LSI test terminal (To be open in use)
27	TESTI23	I+	LSI test terminal (To be open in use)
28	TESTI24	I+	LSI test terminal (To be open in use)
29	TESTI25	I+	LSI test terminal (To be open in use)
30	TESTI26	I+	LSI test terminal (To be open in use)
31	TESTI27	I+	LSI test terminal (To be open in use)
32	TESTI28	I+	LSI test terminal (To be open in use)
33	TESTI29	I+	LSI test terminal (To be open in use)
34	TESTI30	I+	LSI test terminal (To be open in use)
35	/RAMWE	O	External SRAM Interface /WE
36	RAMA13	O	External SRAM Interface address
37	RAMA8	O	External SRAM Interface address
38	RAMA9	O	External SRAM Interface address
39	RAMA11	O	External SRAM Interface address
40	/RAMOE	O	External SRAM Interface /OE
41	RAMA10	O	External SRAM Interface address
42	/RAMCE	O	External SRAM Interface /CE
43	RAMD7	I/O	External SRAM Interface data
44	RAMD6	I/O	External SRAM Interface data
45	RAMD5	I/O	External SRAM Interface data
46	RAMD4	I/O	External SRAM Interface data
47	RAMD3	I/O	External SRAM Interface data

No.	NAME	I/O	FUNCTION
48	DVSS	-	Ground (for digital circuit)
49	DVSS	-	Ground (for digital circuit)
50	RAMD2	I/O	External SRAM Interface data
51	RAMD1	I/O	External SRAM Interface data
52	RAMD0	I/O	External SRAM Interface data
53	RAMA0	O	External SRAM Interface address
54	RAMA1	O	External SRAM Interface address
55	RAMA2	O	External SRAM Interface address
56	RAMA3	O	External SRAM Interface address
57	RAMA4	O	External SRAM Interface address
58	RAMA5	O	External SRAM Interface address
59	RAMA6	O	External SRAM Interface address
60	RAMA7	O	External SRAM Interface address
61	RAMA12	O	External SRAM Interface address
62	RAMA14	O	External SRAM Interface address
63	IPORT0	I+	Input port for general purpose
64	IPORT1	I+	Input port for general purpose
65	IPORT2	I+	Input port for general purpose
66	IPORT3	I+	Input port for general purpose
67	IPORT4	I+	Input port for general purpose
68	IPORT5	I+	Input port for general purpose
69	IPORT6	I+	Input port for general purpose
70	IPORT7	I+	Input port for general purpose
71	DVDD	-	+5V power supply (for digital circuit)
72	DVDD	-	+5V power supply (for digital circuit)
73	SDO3	O	PCM output terminal (MIX0, MIX1)
74	SDO2	O	PCM output terminal (C, LFE)
75	SDO1	O	PCM output terminal (LS, RS)
76	SDO0	O	PCM output terminal (L, R)
77	/SDOBCK	O	Output terminal of inverted SDOBCK
78	SDOBCK	I+	Bit clock for SDO output
79	SDOWCK	I+	Word clock for SDO output
80	AC3DATA	O	Detection of AC-3 bitstream data
81	CRC	O	Detection of CRC error (when AC-3 bitstream data is decoded)
82	MUTE	O	Detection of output data mute
83	KARAOKE	O	Detection of AC-3 karaoke data
84	/IC	Is	Initial clear
85	/CS	Is	Microprocessor interface Chip select
86	SO	O	Microprocessor interface Serial data output
87	SI	Is	Microprocessor interface Serial data input
88	SCK	Is	Microprocessor interface Clock
89	SDI1	I	AC-3 bitstream (or PCM) data input terminal
90	SDI0	I	AC-3 bitstream (or PCM) data input terminal
91	SDIBCK	I	Bit clock for SDI input
92	SDIWCK	I	Word clock for SDI input
93	DVSS	-	Ground (for digital circuit)
94	DVSS	-	Ground (for digital circuit)
95	OPORT7	O	Output port for general purpose
96	OPORT6	O	Output port for general purpose
97	OPORT5	O	Output port for general purpose
98	OPORT4	O	Output port for general purpose
99	OPORT3	O	Output port for general purpose

No.	NAME	I/O	FUNCTION
100	OPORT2	O	Output port for general purpose
101	OPORT1	O	Output port for general purpose
102	OPORT0	O	Output port for general purpose
103	TESTO14	O	LSI test terminal (To be open in use)
104	TESTO13	O	LSI test terminal (To be open in use)
105	TESTO12	O	LSI test terminal (To be open in use)
106	TESTO11	O	LSI test terminal (To be open in use)
107	TESTO10	O	LSI test terminal (To be open in use)
108	TESTO9	O	LSI test terminal (To be open in use)
109	TESTO8	O	LSI test terminal (To be open in use)
110	TESTO7	O	LSI test terminal (To be open in use)
111	TESTO6	O	LSI test terminal (To be open in use)
112	TESTO5	O	LSI test terminal (To be open in use)
113	TESTO4	O	LSI test terminal (To be open in use)
114	TESTO3	O	LSI test terminal (To be open in use)
115	TESTO2	O	LSI test terminal (To be open in use)
116	TESTO1	O	LSI test terminal (To be open in use)
117	TESTO0	O	LSI test terminal (To be open in use)
118	TESTI0	I+	LSI test terminal (To be open in use)
119	TESTI1	I+	LSI test terminal (To be open in use)
120	TESTI2	I+	LSI test terminal (To be open in use)
121	TESTI3	I+	LSI test terminal (To be open in use)
122	TESTI4	I+	LSI test terminal (To be open in use)
123	TESTI5	I+	LSI test terminal (To be open in use)
124	TESTI6	I+	LSI test terminal (To be open in use)
125	TESTI7	I+	LSI test terminal (To be open in use)
126	TESTI8	I+	LSI test terminal (To be open in use)
127	TESTI9	I+	LSI test terminal (To be open in use)
128	TESTI10	I+	LSI test terminal (To be open in use)

NOTE) Is : Schmidt input terminal
I+ : Input terminal with a pull-up resistor
AI : Analog input terminal
AO : Analog output terminal

■BLOCK DIAGRAM



■FUNCTION DESCRIPTION

1. Clocks **XI, XO, VREF, CPO**

XI and XO terminals are used to form a crystal oscillation circuit. The oscillation frequency is 40 MHz that is divided by 2 internally to provide the operating clock of 20 MHz.
To make clock signal, use XI and XO terminals and perform a self oscillation or feed an external clock signal to the XI terminal.
This LSI operates in a PLL oscillation mode as well. When PLL oscillating mode is chosen and a frequency lower than 20MHz clock signal to the XI terminal is applied to utilize multiplier, an external analog filter has to be connected between VIN, VREF, and CPO terminals.

2. Data Interface **SDIBCK, SDIWCK, SDI0, SDI1, SDOBCK, SDOWCK, /SDOBCK, SDO0-3**

AC-3 bitstream data or PCM data has to be fed from either SDI0 or SDI1 terminal. This signal has to be synchronized with SDIBCK(bit clock) and SDIWCK(word clock).
PCM data are outputted from the terminals SDO0 to SDO3.
Synchronization of PCM output data with input data of SDIBCK / SDIWCK, or with those clocks inputted from SDOBCK / SDOWCK terminals can be selected according to the setting of the control register.
One of the following parameters can be selected according to the setting of the control register: SDI0 or SDI1 port selection, phase of bit and word clocks, input and output data formats, numbers of data bits.
Please refer to "INPUT/OUTPUT DATA FORMAT" section for detail of interface and serial data format. (page 9)

3. Input Data Status **AC3DATA, MUTE, CRC, KARAOKE**

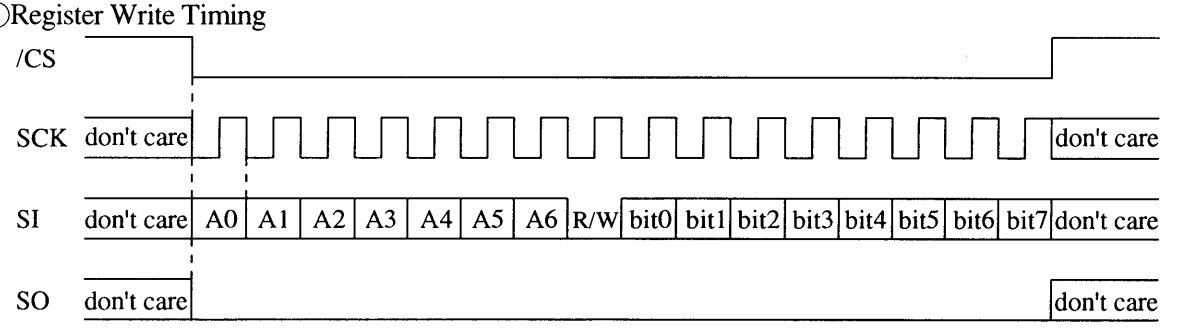
Status of SDI input signal can be known by monitoring signals outputted from the AC3DATA, MUTE, CRC, and KARAOKE terminals. Their levels become high when the conditions are met. These status also can be known by reading address 5F of the control registers.

AC3DATA	Detects whether SDI input is AC-3 bitstream data.
MUTE	Detects whether output signals of SD0 to SD3 are muted.
CRC	Detects CRC error in the AC-3 bitstream data.
KARAOKE	Detects whether SDI input is AC-3 karaoke data.

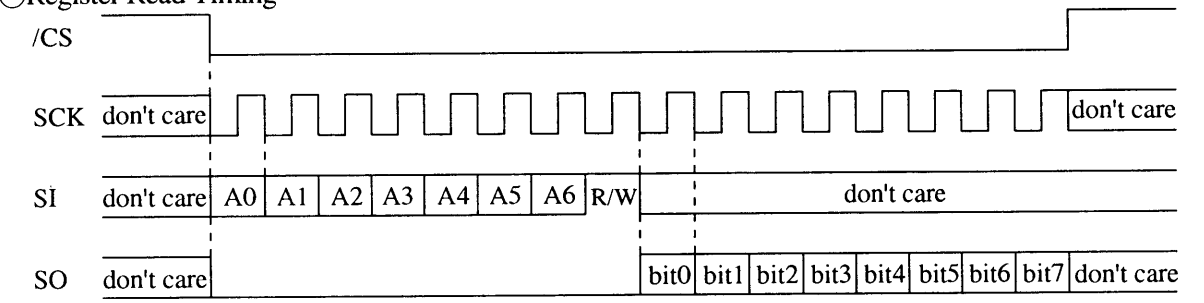
4. Microprocessor Interface **/CS, SCK, SI, SO**

The control register can be read / written via microprocessor interface. Four terminals /CS, SCK, SI and SO are used for this purpose.
Please refer to the following format chart for the details of read / write timing.

○Register Write Timing



○Register Read Timing



Data read / write method
When writing data:
Set the address bits (A0 to A6) for the first 7 bits of the SI terminal, then set the R/W bit to "0" for writing. Data should be entered from the SI terminal following R/W bit.

When reading data:
Set the address bits (A0 to A6) for the first 7 bits of the SI terminal, then set the R/W bit to "1" for reading. Register data will be outputted from the SO terminal with bits 9 to 16 that synchronize with SCK clock.

Note: Both address bits and data bits should be inputted with LSB first.

5. General Purpose I/O ports **OPORT7-0, IPORT7-0**

OPORT7 to 0 terminals are data output ports. Data written on the control register (address $06) is outputted from these terminals.
IPORT7 to 0 terminals are data input ports. Data entry to the control register (address $07) should be made from these terminals.

6. External RAM **/RAMCE, /RAMOE, /RAMWE, RAMA0-14, RAMD0-7**

This LSI requires an external SRAM for outputting the PCM data.
The specifications for the SRAM should be:
Capacity: 256Kbit (32Kwordx8bit)
Access time: 35 nsec or less

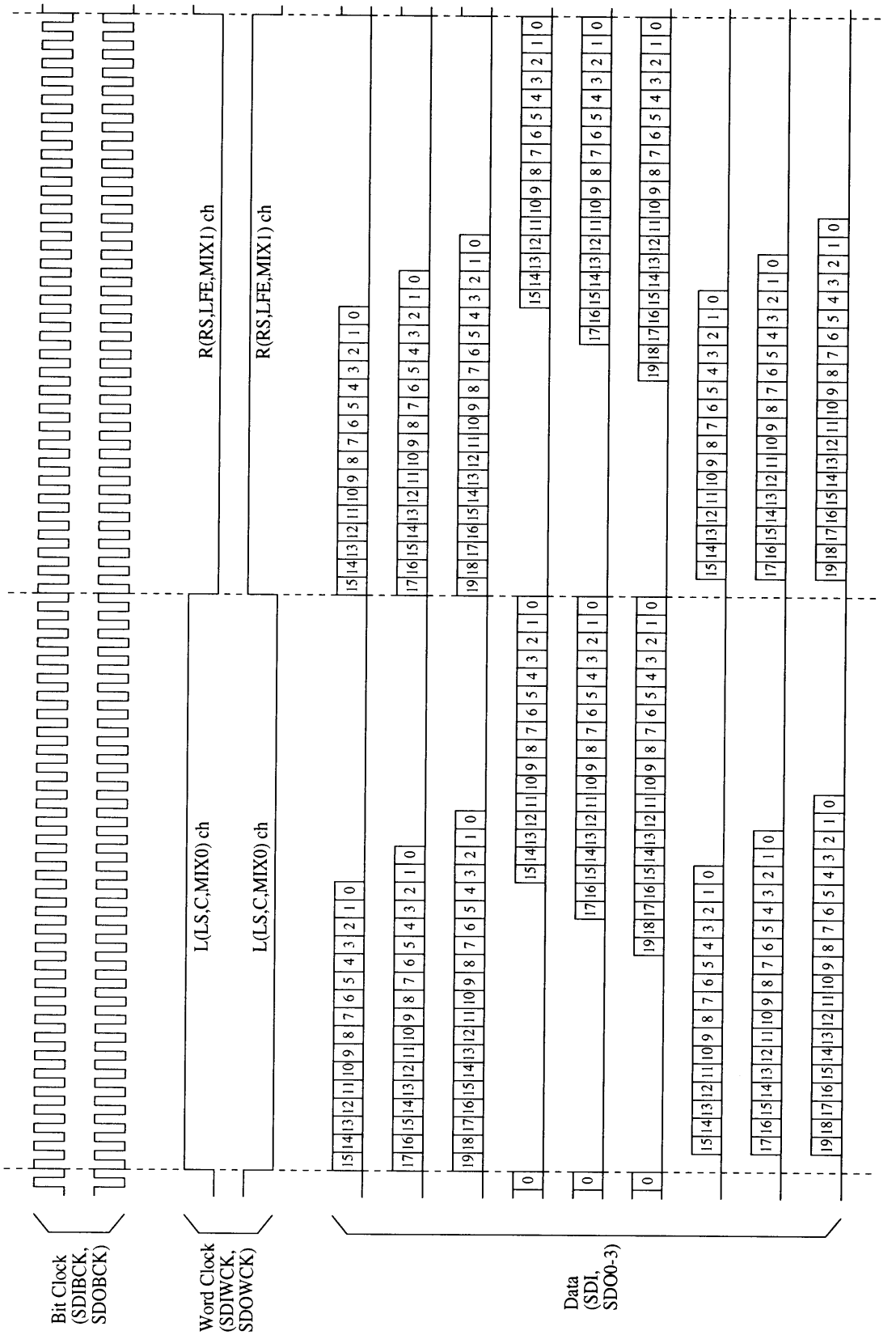
7. Initial Clear **/IC**

This LSI requires initial clear when turning on the power.

8. LSI Test Terminals **TESTI0-30, TESTO0-14, TESTR1-2, TESTBRK**

TESTI0-30, TESTO0-14, TESTR1-2 and TESTBRK are LSI test terminals. They must be open in normal use.

■INPUT/OUTPUT DATA FORMAT



■CONTROL REGISTER

The AC-3 decoding system is controlled by reading and writing the control registers through microprocessor interface (/CS, SCK, SI, SO).

※ All bits are set to "0" by initial clear except for PLL0 (bit 3) of PLL register ($00).

REGISTER MAP (1)
The following addresses ($00～$47) are registers which can read and write.

addr	NAME	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$00	PLL register	PLLUSE	PLL3 - 0				AC3/PCM	AMOFF	SDISEL
$01	DSN register	PLL8X	don't care			DSNIGN	DSN2 - 0		
$02	Mute register	LMUTEN	CMUTEN	RMUTEN	RSMUTEN	LSMUTEN	LFEMUTEN	M0MUTEN	M1MUTEN
$03	SDI register	don't care		SDIFMT1 - 0		SDIBIT1 - 0		SDIWP	SDIBP
$04	SDO register	SDOCKSEL	don't care	SDOFMT1 - 0		SDOBIT1 - 0		SDOWP	SDOBP
$05	SDO3 register	KROKON	don't care	SDO3FMT1 - 0		SDO3BIT1 - 0		SDO3WP	don't care
$06	OPORT register	OPORT7 - 0							
$07	IPORT register	IPORT7 - 0 (Unable to write to this register)							
$08 : $1D	(not used)	These registers are not assigned. (All "0" out when read)							
$1E	Test register 0	This register is for LSI test. Do not write.							
$1F	Test register 1	This register is for LSI test. Do not write.							
$20	Noise register	NOISE	PN/WN	NFS1 - 0		don't care			
$21	Noise Level register	NOISELEV7 - 0							
$22	MIX0 L register	MIX0L7 - 0							
$23	MIX1 L register	MIX1L7 - 0							
$24	MIX0 C register	MIX0C7 - 0							
$25	MIX1 C register	MIX1C7 - 0							
$26	MIX0 R register	MIX0R7 - 0							
$27	MIX1 R register	MIX1R7 - 0							
$28	MIX0 LS register	MIX0LS7 - 0							
$29	MIX1 LS register	MIX1LS7 - 0							
$2A	MIX0 RS register	MIX0RS7 - 0							
$2B	MIX1 RS register	MIX1RS7 - 0							
$2C	MIX0 LFE register	MIX0LFE7 - 0							
$2D	MIX1 LFE register	MIX1LFE7 - 0							
$2E	Center Delay register	don't care				CDELAY3 - 0			
$2F	Surround Delay register	don't care				SRDELAY3 - 0			
$30 : $3F	(not used)	These registers are not assigned. (All "0" out when read)							
$40	Compression register	don't care				P11OFF	DIALOFF	COMPMOD1 - 0	
$41	HDYNRNG register	HDYNRNG7 - 0							
$42	LDYNRNG register	LDYNRNG7 - 0							
$43	Output Mode register	don't care			DUALMOD1 - 0		OUTMOD2 - 0		
$44	PCM register H	PCMSFH7 - 0							
$45	PCM register L	PCMSFL7 - 0							
$46	Dither register	don't care							DITHOFF
$47	(not used)	don't care							

REGISTER MAP (2)

The following addresses ($48～$7F) are read only registers. Unable to write to these registers.

addr	NAME	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$48	Bitstream register 0	fscod		frmsizecod					
$49	Bitstream register 1	bsid					bsmod		
$4A	Bitstream register 2	acmod			cmixlev		surmixlev		lfeon
$4B	Bitstream register 3	dsurmod		copyrightb	origbs	0	0	0	0
$4C	Bitstream register 4	0	0	0	dialnorm				
$4D	Bitstream register 5	0	0	0	dialnorm2				
$4E	Bitstream register 6	audprodie	mixlevel					roomtyp	
$4F	Bitstream register 7	audprodi2e	mixlevel2					roomtyp2	
$50	Bitstream register 8	timecod1e	0	timecod1					
$51	Bitstream register 9	timecod1							
$52	Bitstream register 10	timecod2e	0	timecod2					
$53	Bitstream register 11	timecod2							
$54	Bitstream register 12	langcode	langcod2e	compre	compr2e	0	0	0	0
$55	Bitstream register 13	langcod							
$56	Bitstream register 14	langcod2							
$57	Bitstream register 15	compr							
$58	Bitstream register 16	compr2							
$59	Bitstream register 17	dynrng							
$5A	Bitstream register 18	dynrng2							
$5B : $5E	(not used)	These registers are not assigned. (All "0" out when read)							
$5F	Status register	0	0	0	0	KARAOKE	MUTE	CRC	AC3DATA
$60 : $7F	(not used)	These registers are not assigned. (All "0" out when read)							

■ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	-0.5 ~ 7.0	V
Input Voltage	V_I	-0.5 ~ V_{DD} + 0.5	V
Operating Temperature	Top	-20 ~ 75	℃
Storage Temperature	Tstg	-50 ~ 125	℃

2. Recommended Operating Conditions

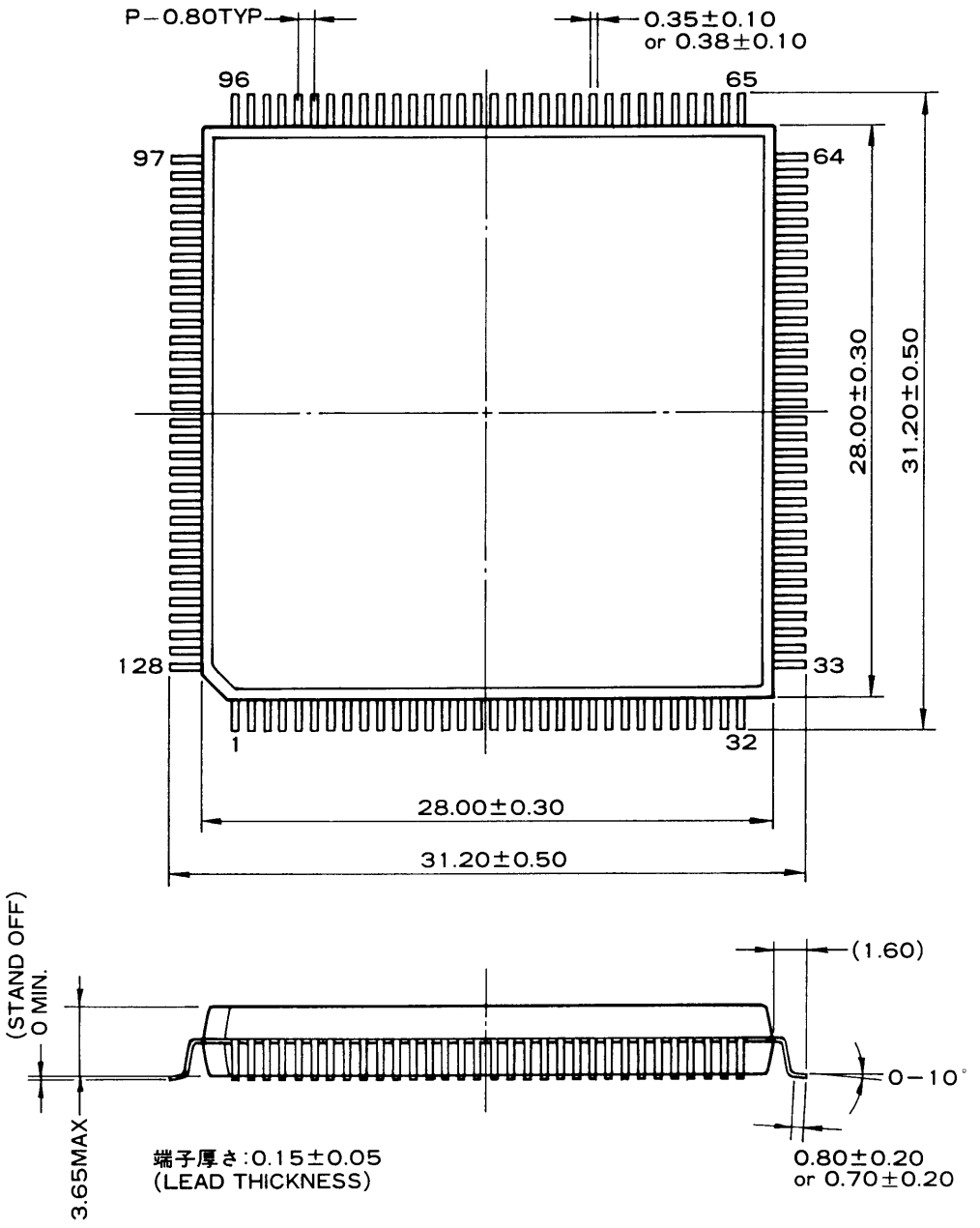
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	4.75	5.00	5.25	V
Operating Temperature	Top	0	25	70	℃

3. DC Characteristics (under recommended operating condition)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Consumption	W	V_{DD} = 5.0V		500		mW
Input Voltage H Level (1)	V_{IH1}	*1)	3.5			V
Input Voltage H Level (2)	V_{IH2}	*2)	2.0			V
Input Voltage L Level (1)	V_{IL1}	*1)			1.0	V
Input Voltage L Level (2)	V_{IL2}	*2)			0.8	V
Output Voltage H Level	V_{OH}	I_{OH} = 80 μA	V_{DD}-1.0			V
Output Voltage L Level	V_{OL}	I_{OL} = 1.6mA			0.4	V
Input Leakage Current	I_{LI}		-10		10	μA
Pull-up Resistor	R_P		50		400	kΩ

*1) Applicable to XI and /IC terminals.
*2) Applicable to input terminals except XI and /IC terminals.

■EXTERNAL DIMENSIONS



モールドコーナー形状は、この図面と若干異なるタイプのものもあります
カッコ内の寸法値は参考値とする
モールド外形寸法はバリを含まない
単位(UNIT):mm

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

Note: The LSIs for surface mount need especial consideration on storage and soldering condisions. For derailed information, please contact your nearest agent of yamaha.

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