# YAMAHA L 5 I

# **YSS222**

# **KPB**Karaoke Processor B

#### OUTLINE

YSS222(KPB) is an audio signal processing LSI for the key control function of one channel. The key of -1800 cent to +1200 cent can be managed in each 100 cent.

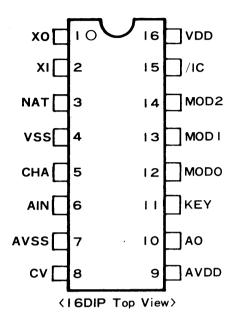
As A/D, D/A converter and RAM for the key control are built-in, it is the best for the voice key shift of the analog signal equipments such as the tape-recorder, the VTR, and microphones.

The amount of the key shift can be controlled even by the pulse input with the switch and the analog voltage input. Therefore, the microprocessor is unnecessary. It will be possible to develop and to make products in a shorter time at a lower cost.

#### FEATURES

- Key control of −1800 cent to +1200 cent by 100 cent.
- 14-bit floating A/D and D/A converter are built-in to cope with analog signal.
- Sampling frequency of the internal signal processing is 16kHz.
- Sampling frequency of A/D and D/A converter is 32kHz.
- RAM for the key control processing is built-in.
- Three selective modes for specifying the amount of the key shift.
  - 1. Analog voltage mode: Specification by analog voltage.
  - 2. Switch pulse mode: Specification by pulse input from switch.
  - 3. Microprocessor pulse mode: Specification by pulse input from microprocessor.
- Master clock is 768kHz(48fs).
- 5V single power supply and Si-gate CMOS process.
- 16-pin DIP(YSS222-D)

# **■ PIN CONFIGURATION**

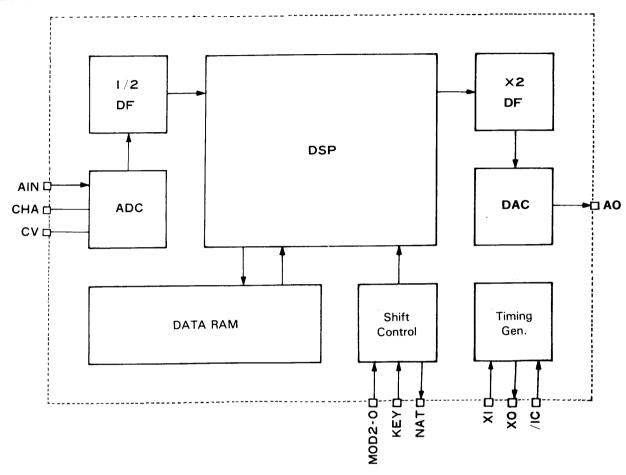


# ■ PIN DESCRIPTION

No. 16D	Name	I/O	Function
1	XO	0	Oscillator Connection Terminal
2	XI	I	Oscillator Connecting Terminal or External Clock Input (768kHz)
3	NAT	О	Key Shift Status Output ('H'=Non-Shift state)
4	$\mathbf{v}_{\mathbf{s}\mathbf{s}}$	_	Ground (Digital Block)
5	CHA	- A	Sample/Hold Capacitor Connecting Terminal for AIN signal
6	AIN	IA	Analog Audio Signal ADC Input
7	AVss	- A	Ground (Analog Block)
8	CV	- A	Center Voltage terminal of Internal ADC
9	AVDD	- A	+5V Power Supply (Analog Block)
10	AO	OA	Analog Audio Signal DAC Output
11	KEY	IA	Key Shift Control Input
12	MOD0	I	Control Mode Select 0
13	MOD1	I	Control Mode Select 1
14	MOD2	I	Control Mode Select 2
15	/IC	Is	Initial Clear Input
16	Vdd	_	+5V Power Supply (Digital Block)

(Note) Is; Schmitt-Trigger Input Terminal, A; Analog Terminal

#### ■ BLOCK DIAGRAM



#### ■ FUNCTION DESCRIPTION

#### 1. Clocks XI, XO

Using XI and XO terminals, the oscillation circuit is composed.

The oscillation frequency is 768kHz(48fs).

It is also possible to input an external clock to the XI terminal.

#### 2. Audio Signal I/O AIN, CHA, CV, AO

An analog audio signal is input from AIN terminal. The signal is A/D converted at 32kHz, is decimated to 16kHz with 1/2 under sampling filter, and is digital-processed.

Connect to CHA terminal the sample/hold capacitor for A/D conversion of AIN signal.

CV terminal indicates a center voltage of internal ADC. With a stabilization capacitor connected, bias the AIN signal by this voltage.

After digital key shift processing, audio signal is over-sampled to 32kHz with 2 times over-sampling filter and after D/A conversion, it is output from AO terminal.

With a sample/hold capacitor connected to AO terminal, execute the signal by the buffer with a high impedance input.

#### 3. Key control KEY, MOD2-0, NAT

The method of specifying the amount of the key shift is selected with MOD2-MOD0 terminals. The KEY terminal is an input terminal to control the amount of the key shift. However, the input method is different depending on the specified mode.

The NAT terminal becomes 'H' when key is 'Non-shift' (It is displayed in every mode description as <NAT>).

When the key has changed, (All modes contain ±0.0 cent), NAT the terminal becomes 'L'.

MOD2	MOD1	MOD0	Mode	Key Shift Range [cent]
Н	Н	Н	Microprocessor Pulse Mode	$-1800 \sim +1200$ (by 100 cent)
Н	Н	L	Switch Pulse Mode 1	$-1200 \sim +1200$ (by 100 cent)
Н	$\mathbf{L}$	H	Switch Pulse Mode 2	$-600 \sim +600 \text{ (by } 100 \text{ cent)}$
Н	L	L	Switch Pulse Mode 3	$-400 \sim +400 \text{ (by } 100 \text{ cent)}$
L	Н	Н	Analog Voltage Mode 1	$-1800 \sim +1200$ (by 100 cent)
L	H	L	Analog Voltage Mode 2	-1600~+1200 (by 200 cent)

#### (1) Analog voltage mode

The KEY terminal voltage is divided into 32 levels between VDD-VSS, and keys are provided according to the KEY terminal voltage.

As for the analog voltage mode, there are two kinds and the shift resolution is different.

KEY Terminal Voltage [V]		Key Shif	t [cent]	KEY Terminal Voltage [V] Ke		Key Shif	t [cent]
* VDD	VDD=5.0	Mode 1	Mode 2	* Vdd	VDD=5.0	Mode 1	Mode 2
32~31/32	5.00~4.84	+1200	±1900	16~15/32	2.50~2.34	-400	-400
31 ~ 30/32	4.84~4.69	+1100	+1200	15~14/32	2.34~2.19	-500	-400
$30 \sim 29/32$	4.69~4.53	+1000	+1000	$14 \sim 13/32$	2.19~2.03	-600	-600
29~28/32	4.53~4.38	+900	T1000	$13 \sim 12/32$	2.03~1.88	-700	- 600
$28 \sim 27/32$	4.38 ~ 4.22	+800	+800	$12 \sim 11/32$	$1.88 \sim 1.72$	-800-	-800
$27 \sim 26/32$	4.22~4.06	+700	T 600	$11 \sim 10/32$	$1.72 \sim 1.56$	-900	- 800
$26 \sim 25/32$	4.06 ~ 3.91	+600	+600	10~ 9/32	$1.56 \sim 1.41$	-1000	-1000
$25 \sim 24/32$	3.91 ~ 3.75	+500	+600	9~ 8/32	1.41 ~ 1.25	-1100	- 1000
24~23/32	3.75~3.59	+400	+400	8~ 7/32	$1.25 \sim 1.09$	-1200	-1200
$23 \sim 22/32$	3.59~3.44	+300	<b>∓400</b>	7 ~ 6/32	1.09~0.94	-1300	- 1200
$22 \sim 21/32$	3.44~3.28	+200	+200	6~ 5/32	$0.94 \sim 0.78$	-1400	-1400
$21 \sim 20/32$	3.28~3.13	+100	T 200	5 ~ 4/32	$0.78 \sim 0.63$	- 1500	- 1400
20~19/32	3.13~2.97	±0	+0	4~ 3/32	$0.63 \sim 0.47$	-1600	-1600
19~18/32	2.97 ~ 2.81	-100	±0	3~ 2/32	$0.47 \sim 0.31$	-1700	- 1600
18~17/32	2.81~2.66	- 200	200	2~ 1/32	0.31~0.16	- 1800	<nat></nat>
17~16/32	2.66~2.50	- 300	-200	1~ 0/32	$0.16 \sim 0.00$	<nat></nat>	(NAI)

(Note) < NAT>: The key becomes non-shift.

#### (2) Switch pulse mode

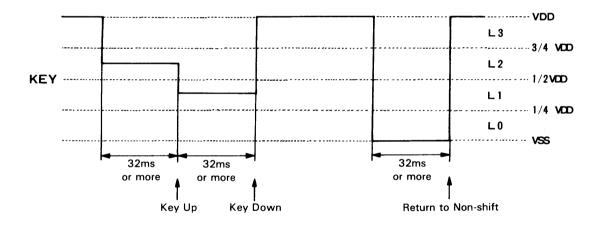
The key changes 100 cent by every pulse to KEY terminal according to the voltage level of the pulse.

The width of the pulse is required to be 32ms or more, and the pulse shorter than 32ms is disregarded.

As for the switch pulse mode, there are three kinds and the variable range of the key is different. The pulse which specifies more than the maximum variable range is disregarded.

MEN Manager 1 Malkage 170	Oti	Maximum Variable Range			
KEY Terminal Voltage [V]	Operation	Mode 1	Mode 2	Mode 3	
L3= VDD ( VDD~3/4 VDD) L2=5/8 VDD (3/4 VDD~2/4 VDD) L1=3/8 VDD (2/4 VDD~1/4 VDD)	No Change Key Shift Up (100 cent) Key Shift Down (100 cent)	+6 -6	+3	+2 -2	
L0 = Vss (1/4 Vdd - Vss)	Return to Non-shift < NAT>			_	

#### [Example]



#### (3) Microprocessor pulse mode

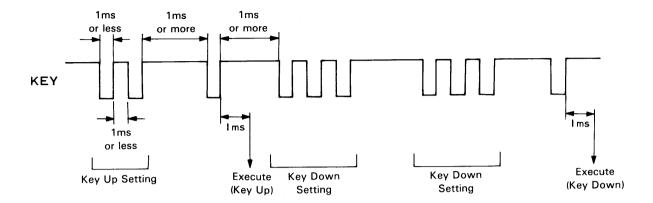
The amount of the key shift is specified according to the number of the pulse input to KEY terminal.

Each code is identified by the number of the pulse inputs at intervals of 1ms or less, and the delimitation between codes by a pulse interval of 1ms or more. Set the width of the pulse as 1ms or less.

In this mode, unless 'one pulse' code is input to KEY terminal, actual key shift will not be executed.

Pulse Code	Operation			
One Pulse	Execute			
Two Pulse	Setting of Key Up (100 cent)			
Three Pulse	Setting of Key Down (10	00 cent)		
Four Pulse	Setting of Non shift	<NAT $>$		

# [Example]



#### 4. Reset /IC

It is necessary to reset this LSI when the power is turned on.

## ■ ELECTRICAL CHARACTERISTICS

#### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDD	-0.5~7.0	V
Input Voltage	Vı	$-0.5 \sim V_{DD} + 0.5$	V
Output Current	Io	-20~20	mA
Operating Temperature	Тор	0~70	°C
Storage Temperature	Tstg	<b>−50 ~125</b>	°C

#### 2. Recommended Operating Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit
Power Supply Voltage	VDD	4.5	5.0	5.5	V
Operating Temperature	Top	0	25	70	°C

#### 3. DC Characteristics

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Power Supply Current	IDD	VDD=5.0V		9		mA
Input Voltage H Level	VIL	*1			0.3VDD	v
Input Voltage L Level	Vih	*1	0.7Vdd			V
Input Leakage Current	Ili	*2			10	μΑ
Input Capacitance	Cı	*1			8	pF
Output Voltage L Level	Vol	IoL=1.6mA, *3			0.4	v
Output Voltage H Level	Vон	IOH = -0.4mA, *3	VDD - 0.4			v
Output Capacitance	Co	*3			10	pF

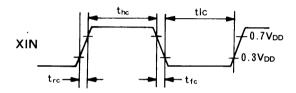
<sup>\*1)</sup> Applicable to XI, MOD0, MOD1, MOD2, /IC terminals.

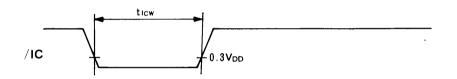
<sup>\*2)</sup> Applicable to input terminals except analog terminals and pulled up terminals.

<sup>\*3)</sup> Applicable to all output terminals except analog terminals.

## 4. AC Characteristics

	Parameter	Symbol	Min.	Typ.	Max.	Unit
XIN	Clock Frequency	fc	690	768	845	kHz
	H Level Time	thC	390			ns
	L Level Time	tic	390			ns
	Rise Time	trC		50	200	ns
	Fall Time	tfC		50	200	ns
/IC	Pulse Width	ticw	13			μS





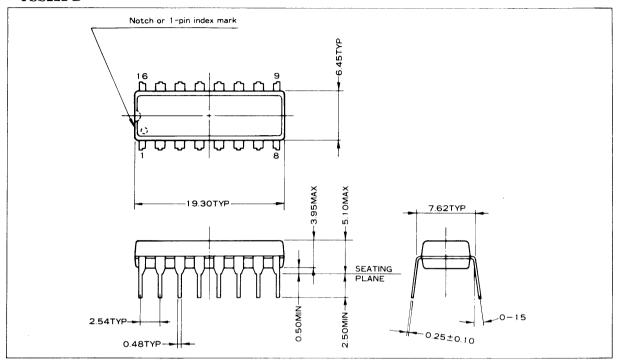
# 5. Analog Characteristics (VDD=5.0V, Top=25°C)

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Analog Input Voltage (1)	VIA1	AIN Terminal	0.05VDD		0.95VDD	V
Analog Input Voltage (2)	VIA2	KEY Terminal	0		VDD	V
Analog Output Voltage	Voa	AO Terminal	0.02VDD		0.98VDD	V
CV Center Voltage	Vc	CV Terminal		$0.5 V_{\mathrm{DD}}$		V
Total Harmonic Distortion	THD+N	1kHz, 0dB, *1			1.0	%
		1kHz, -30dB, *1			1.5	%
Signal to Noise Ratio	S/N	S=0dB, *1	75	80		dB

<sup>\*1)</sup>  $0dB=4.5Vpp, A/D \rightarrow D/A through$ 

## **■ EXTERNAL DIMENSIONS**

#### • YSS222-D



Plastic body dimensions do not include burr of resin  $UNIT:\ mm$ 

Note: The LSIs for surface mount need especial consideration on strage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

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