YAMAHA LSI

YTD436

ISTC

ISDN BRI controller with S/T ref. pt. analog D/R

YTD436 is a high-performance communication LSI for the ISDN BRI user-network interface function (digital four-wire time-division full-duplex operation), supporting D channel layer 1 and layer 2 functions in one 100-pin SQFP chip.

YTD436 supports layer 1 (physical layer) control function conforming to ITU-T Recommendation I.430 and fully supports layer 2 (LAPD protocol) function conforming to ITU-T Recommendations Q.920 and Q.921. ETSI (European Telecommunication Standards Institute) and North American standard operating modes are also supported.

In addition, YTD436 includes layer 3 processor interface function which operate in DMA transfer mode or I/O transfer mode. This gives a great advantage for mounting and functional designing of both “active” (CPU on board) terminal equipment and “passive” (no CPU on board) PC cards.

The layer 1 function has a built-in S/T reference point analog driver/receiver to support the S/T reference point interface. In order to support the U interface, YTD436 also has a TTL interface (no built-in analog driver/receiver) suitable for connecting to an NT1 chip or a DSU module.

YAMAHA CORPORATION

YTD436 CATALOG
CATALOG No.:4TD436A3
1999.11

Features

1. Layer 1 function

- Conforms to ITU-T Recommendation I.430 (1992 edition) and TTC Standard JT-I430 (1997 edition) (default)
  - 192 kbps transmission rate
  - Interface structure : 2B + D (B = 64 kbps, D = 16 kbps)
  - Frame assembling and disassembling function
  - Collision control (built-in random number (Ri) reset), priority control (built-in retransmission control), and state transition control
  - Programmable T3 and T4 timers
- Supports ETSI ETS 300 012 (April 1992) and ANSI T1.605 operating modes
- Leased line capability (JT-I430-a)
- Built-in driver and receiver
  - TTL interface (when the driver / receiver is disconnected)
  - No external relay or common-mode choke needed
  - Supports 1-to-2 pulse transformer
- Abundant Test functions (for testing and maintenance)
  - Demo mode in which no switch simulator is needed.
  - Three kinds of loop-back modes (Loop-back 1 to 3)
  - INFO signals output for testing
  - Test pulse output for pulse shape check
- Multiframing capability
- INFO1 transmission and INFO4 reception monitor pins
- Power down monitor pin
- I.430 transmission frame phase adjustment function

2. Layer 2 function

- Conforms to ITU-T Recommendation Q.920 (1992 edition) and Q.921 (1997 edition) and TTC Standard JT-Q920 (1993 edition) and JT-Q921 (1998 edition)
  - HDLC frame control (Flag control, FCS generation/checking, Automatic zero insertion/deletion, Abort pattern transmission/detection, etc.)
  - LAPD status control (Sequence control, Flow control, SAPI control)
  - Built-in timer for time-out check
- Supports ETSI ETS 300 125 (September 1991), National ISDN-1/2, AT&T 5ESS 5E9 and Nortel DMS-100 S208-6 operating modes
- Multilink capability (circuit switching $\times$ 2 links, packet switching/teleaction communications $\times$ 2 links)
- Automatic assigned TEI/non-automatic assigned TEI (VC/PVC)
- Leased line mode (disable layer 2 function)

3. Layer 3 interface function

- Connects to 8-bit or 16-bit microprocessor
  (8086 family, Z80 family, 6800 family, 68000 family)
- Operates in one of two data transfer modes :
  - DMA transfer mode (with the built-in 16-bit address DMA controller)
  - I/O transfer mode (with the built-in FIFO)
- Primitive logical interface

4. B channel interface

- Data rate setting : 64 k, 56 k and 32 kbps
- Serial mode
  - B channel I/O clock selection function
    - Internal clock mode
      Inputs/outputs the B channel data with 64 k, 56 k or 32 kHz internal clock
    - External clock mode (PCM Highway mode)
      Inputs/outputs the B channel data with a 128 k to 2048 kHz external clock
  - B channel selection function
    - Internal clock mode
      Selects/switches B channel I/O pins
    - External clock mode (PCM Highway mode)
      Selects/switches B channel time slots
- Parallel mode
  - LSB/MSB switching function
  - Bit shift function
  - Data transfer mode
    - DMA transfer mode with the DMA request function
    - I/O transfer mode with the built-in FIFO

5. Low-power operation
   (Host processor clock control function, LSI internal clock freezing function)
6. High-performance CMOS technology
7. 100-pin SQFP
8. Single +5 volt supply

Applications

- ISDN telephone
- Video telephone
- Telemeter
- PBX
- Terminal adapter (TA)
- Other ISDN terminals

Functional Comparison of YAMAHA ISDN S/T Reference Point Interface LSIs

			YTD410	YM7405B	YTD418	YTD423	YTD436
Layer 1	ITU-T Recommendation	I.430	1992 edition	1992 edition	1992 edition	1992 edition	1992 edition
	TTC Standard	JT-I430	1993 edition	1993 edition	1993 edition	1993 edition	1997 edition
Layer 2 (LAPD)	ITU-T Recommendation	Q.920 Q.921	1992 edition	1992 edition	1992 edition	1992 edition	1992 edition 1997 edition
	TTC Standard	JT-Q920 JT-Q921	1993 edition	1993 edition	1993 edition	1993 edition	1993 edition 1998 edition
ETSI ETS 300 012, ETS 300 125				√	√	√	√
North American Switchs National ISDN-1/2, AT&T 5ESS, Nortel DMS-100						√	√
S/T Reference Point Analog Driver / Receiver			Internal	Internal	External [YTD421]	External [YTD421]	Internal
Maximum D Channel Links	Cricuit Switching		1	2	2	2	2
	Dch Packet Switching (Teleaction Communication)		1	2	2	2	2 (2)
D Channel Layer 3 Data Transfer Method			DMA Transfer	DMA Transfer	DMA Transfer	DMA Transfer or I/O Transfer	DMA Transfer or I/O Transfer
HDLC Controller and DMA Controller for B Channel Data			External	External	External	Internal	External
B Channel Data Transfer Method			—	—	—	DMA Transfer or I/O Transfer	DMA Transfer or I/O Transfer (Note 1)
B Channel Internal Clock Mode (kHz)			56, 64	64	64	32, 56, 64	32, 56, 64
B Channel External Clock Mode				√	√	√	√
Clock Output Function for CPU			√			√	√
Signal Output Function for Testing			√			√	√
Power Consumption during Operation (typ.)			65	125	75	85	75
Power Consumption during Sleep (typ.)			2	30	21	1	4 0.6 (Note 2)
Package			80pin QFP 100pin TQFP	80pin QFP 100pin TQFP	80pin QFP	100pin SQFP	100pin SQFP

Note1: DMA transfer : Request function only
I/O transfer : 4-byte FIFO

Note2: State at Line interface disconnection + Power down (SLEEP state)

BLOCK DIAGRAM

User Network Interface Block Diagram

YTD436 is the most-suited LSI for terminal equipment such as ISDN telephones and video telephones and for PHS base stations.

YTD436 contains layer 1 and layer 2 functions, analog driver/receiver for the S/T reference point, DMA request function for B channel data transfer, and DMA controller for D channel data transfer. Because of this, terminal equipment can be optimally configured by adding few circuits such as the layer 3 control processor.

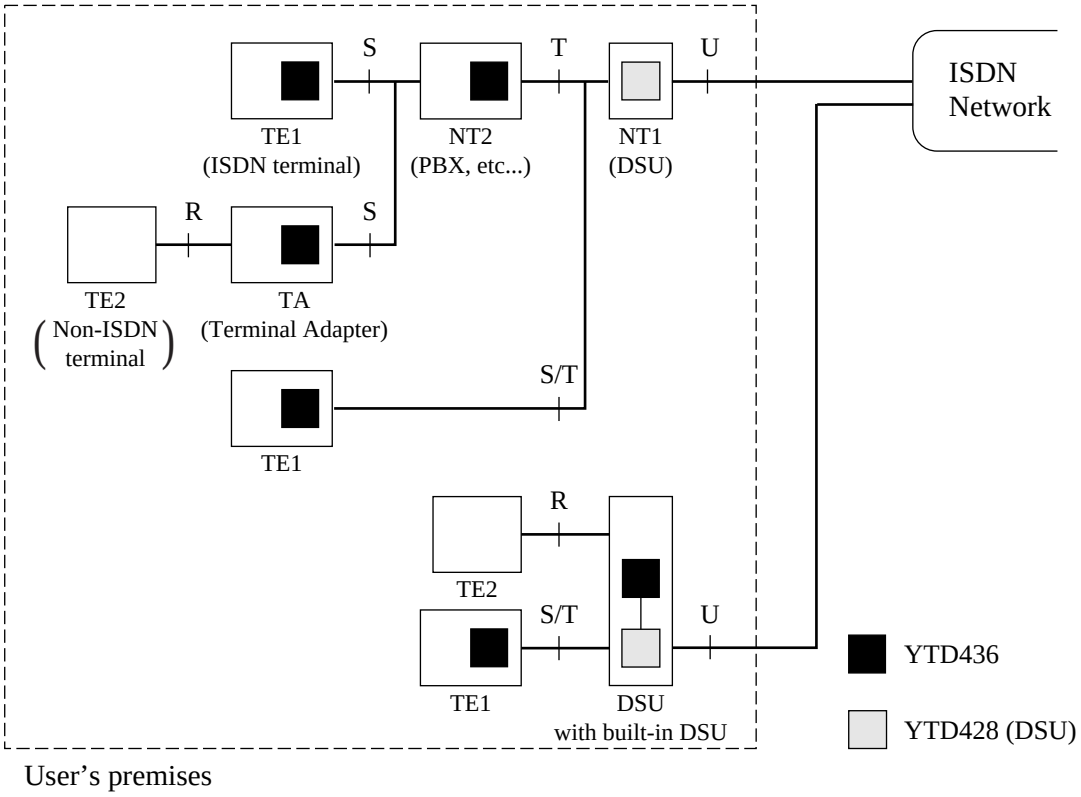


Figure : User-Network Interface Block Diagram

YTD436 Peripheral LSI Interface Block Diagram

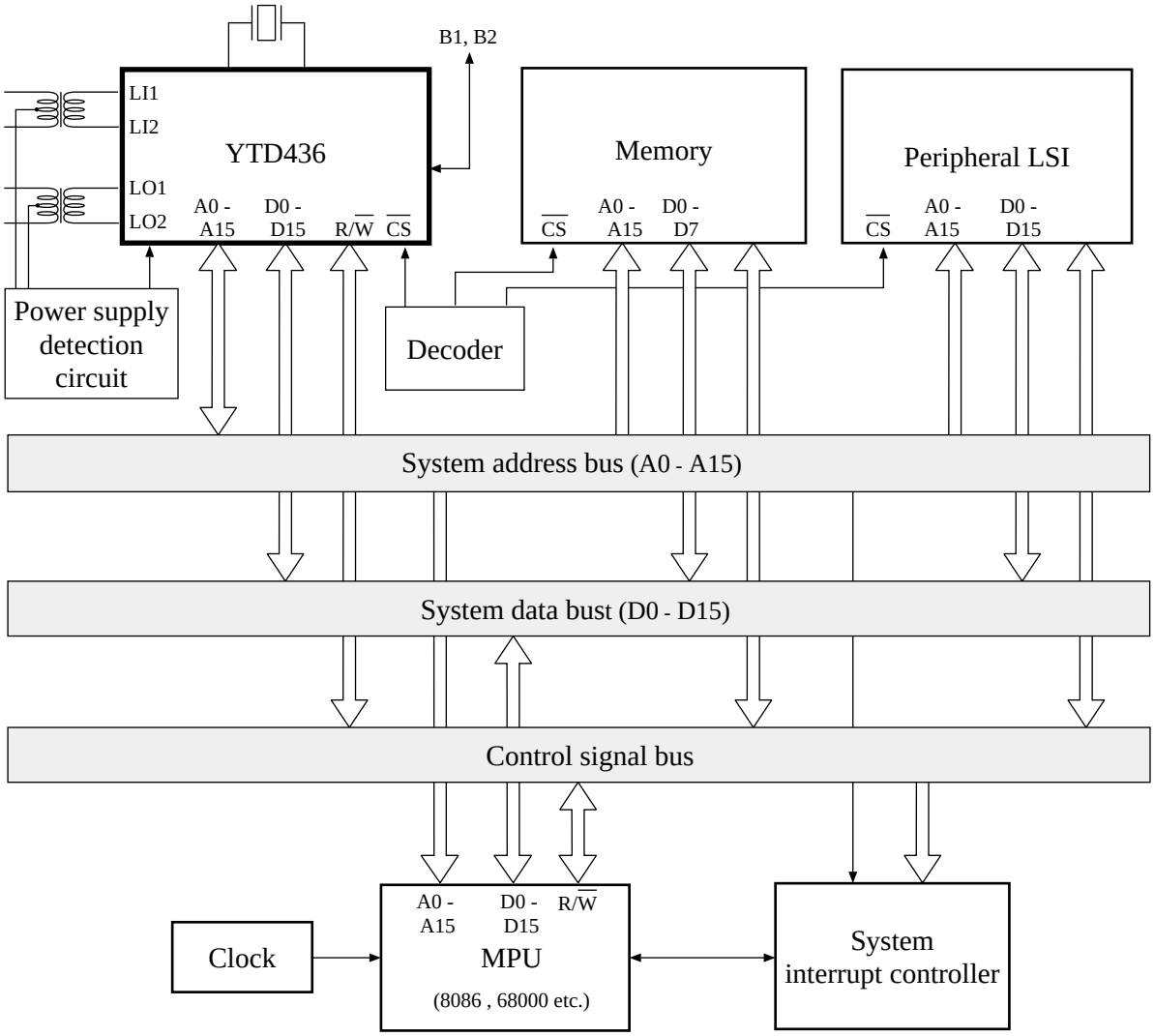


Figure : YTD436 Peripheral LSI Interface Block Diagram

YTD436 Internal Block Diagram

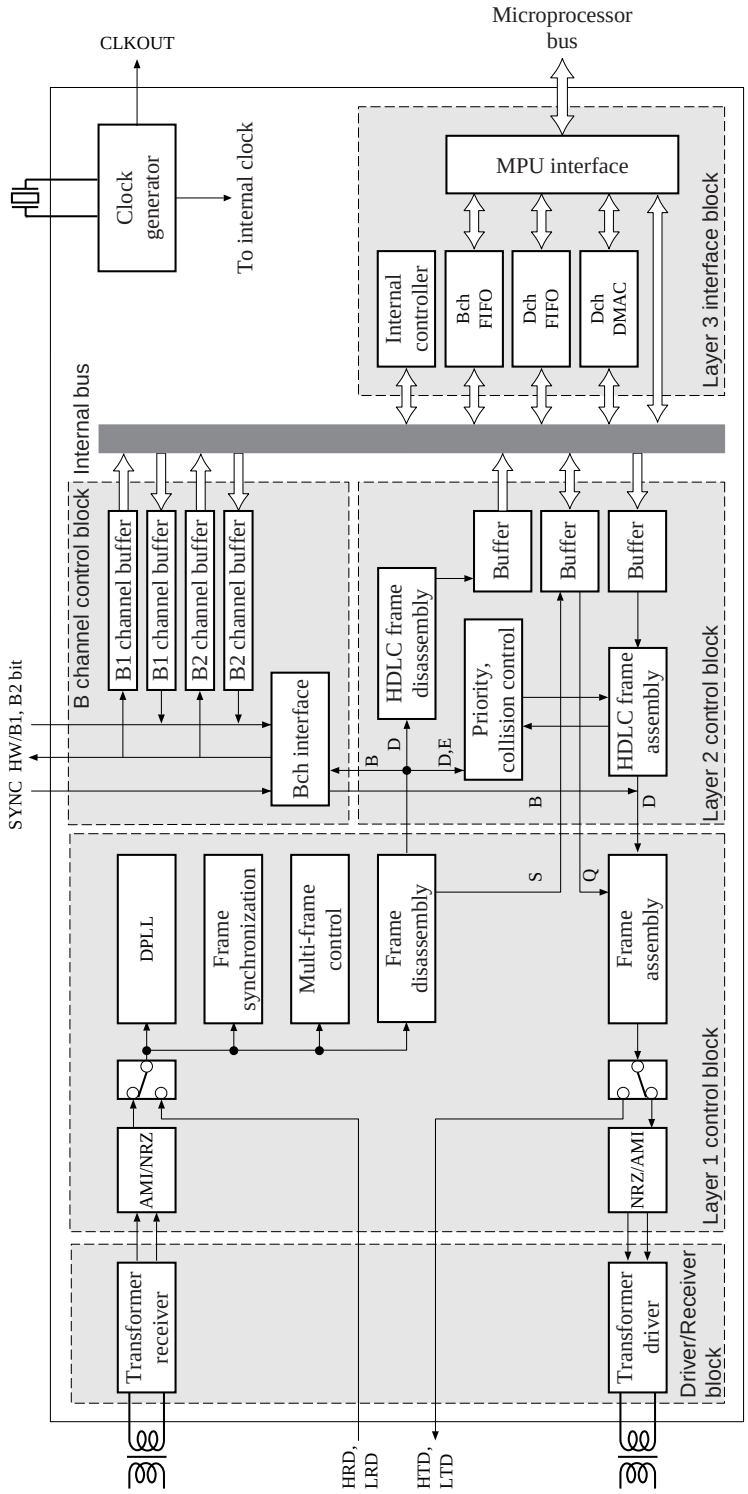


Figure : YTD436 Internal Block Diagram

Pin Assignments

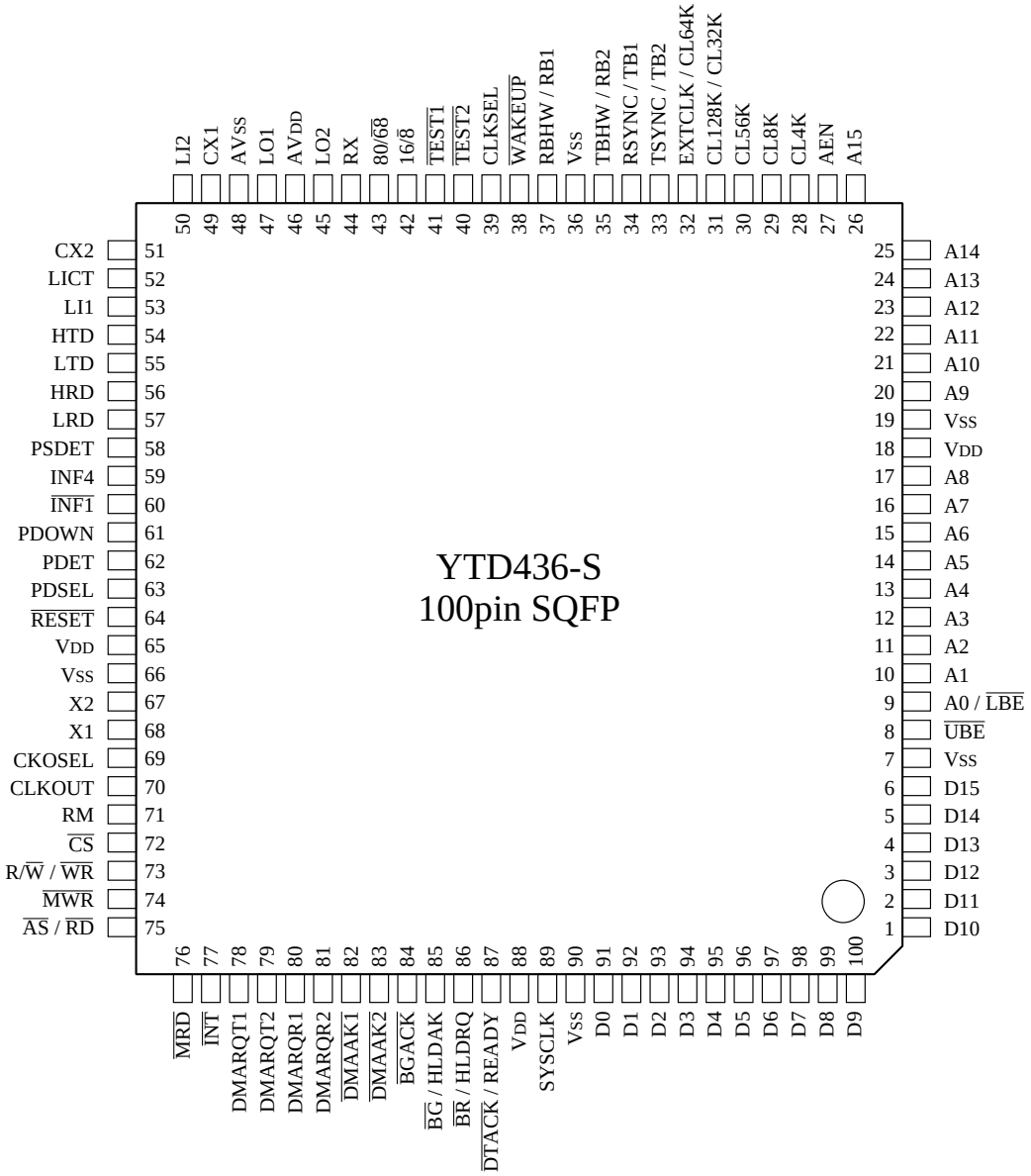


Figure : YTD436-S (100-pin SQFP) Pin Assignments [Top View]

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	- 0.3	+ 7.0	V
Input Voltage	V_{IN}	- 0.3	V_{DD} + 0.3	V
Operating Temperature	T_{op}	0	+ 70	ºC
Storage Temperature	T_{stg}	- 50	+ 125	ºC

(Based on Vss = 0.0 V)

Recommended Operating Conditions

Supply Voltage	5 V ± 5 %
Operating Temperature	0 - 70 ºC

(Based on Vss = 0.0 V)

DC Characteristics

(V_{DD} = 5 V ± 5 %, T_{op} = 0 - 70 ºC)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage	(CMOS)	V_{IH}	(Note 1)	0.8V_{DD}			V
Low-Level Input Voltage	(CMOS)	V_{IL}	(Note 1)			0.2V_{DD}	V
High-Level Input Voltage	(TTL)	V_{IH}	(Note 2)	2.2			V
Low-Level Input Voltage	(TTL)	V_{IL}	(Note 2)			0.8	V
High-Level Output Voltage	(CMOS)	V_{OH}	$\|I_{OH}\|$ < 10 µA	V_{DD} - 0.4			V
Low-Level Output Voltage	(CMOS)	V_{OL}	$\|I_{OL}\|$ < 10 µA			V_{DD} + 0.4	V
High-Level Output Voltage	(TTL)	V_{OH}	(Note 3)	2.7			V
Low-Level Output Voltage	(TTL)	V_{OL}	(Note 3)			0.4	V
Low-Level Output Voltage	(Open-D)	V_{OL}	(Note 4)			0.4	V
Leakage Current		I_L		-10		10	µA
Off-State Leakage Current		I_{LZ}	(Note 5)	-10		10	µA
Power Supply Current		I_{DD}	(Note 6) (Note 7) (Note 8)		15 800 120		mA µA µA

Note 1: With respect to X1, PSDET, PDET, PDSEL, $\overline{\text{WAKEUP}}$, $\overline{\text{RESET}}$, CLKSEL, $\overline{\text{TEST1}}$, $\overline{\text{TEST2}}$ pins (except for the analog pins).

Note 2: With respect to other pins (except for the analog pins).

Note 3: CLKOUT pin Test condition: I_{OH} = - 1.0 mA, I_{OL} = 2.0 mA

other output pins Test condition: I_{OH} = - 0.4 mA, I_{OL} = 1.2 mA

Note 4: HTD, LTD, $\overline{\text{INT}}$ pin Test condition : I_{OL} = 1.2 mA

INF1 pin Test condition : I_{OL} = 3 mA

RBHW pin Test condition : I_{OL} = 0.8 mA, R_L = 500 Ω

Note 5: With respect to cases in which D0 - D15, and A0 - A15 pins are in the input state and $\overline{\text{MWR}}$ and $\overline{\text{MRD}}$ pins are in Hi-Z state.

Note 6: RUN state (connecting with a B channel, transferring all “0”, SYSCLK = 8 MHz, using internal driver/receiver, assuming as V_{IH} = V_{DD}, H_{IL} = V_{SS})

Note 7: SLEEP state

Note 8: SLEEP state + Line interface disconnection

AC Characteristics

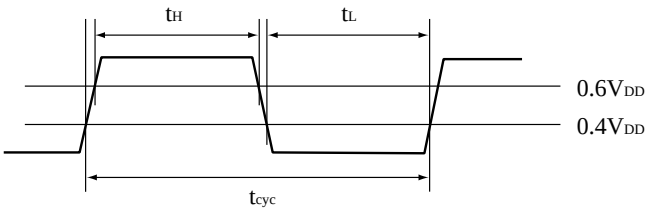
(V_{DD} = 5 V ± 5 %, T_{op} = 0 - 70 ºC)

Clocks

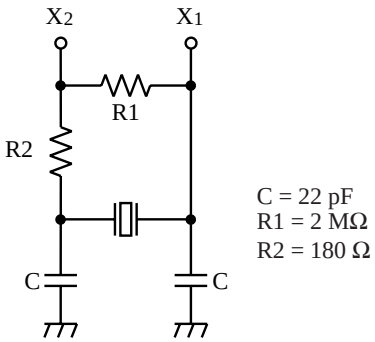
1. Main clock

External input or Crystal oscillation

Parameter	Symbol	Min.	Typ.	Max.	Units
Main Clock Frequency	f_M	- 100 ppm	12.288	+ 100 ppm	MHz
Clock Duty	t_{DUTY}	40	50	60	%



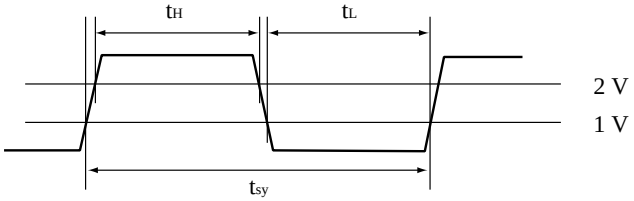
$$t_{DUTY} = \frac{t_H}{t_{cyc}} \text{ or } \frac{t_L}{t_{cyc}}$$



C = 22 pF
R1 = 2 MΩ
R2 = 180 Ω

2. System Clock

Parameter	Symbol	Min.	Typ.	Max.	Units
System Clock Frequency	f_{sy}	1.5		12.5	MHz
High Level Pulse Width	t_H	30			ns
Low Level Pulse Width	t_L	30			ns



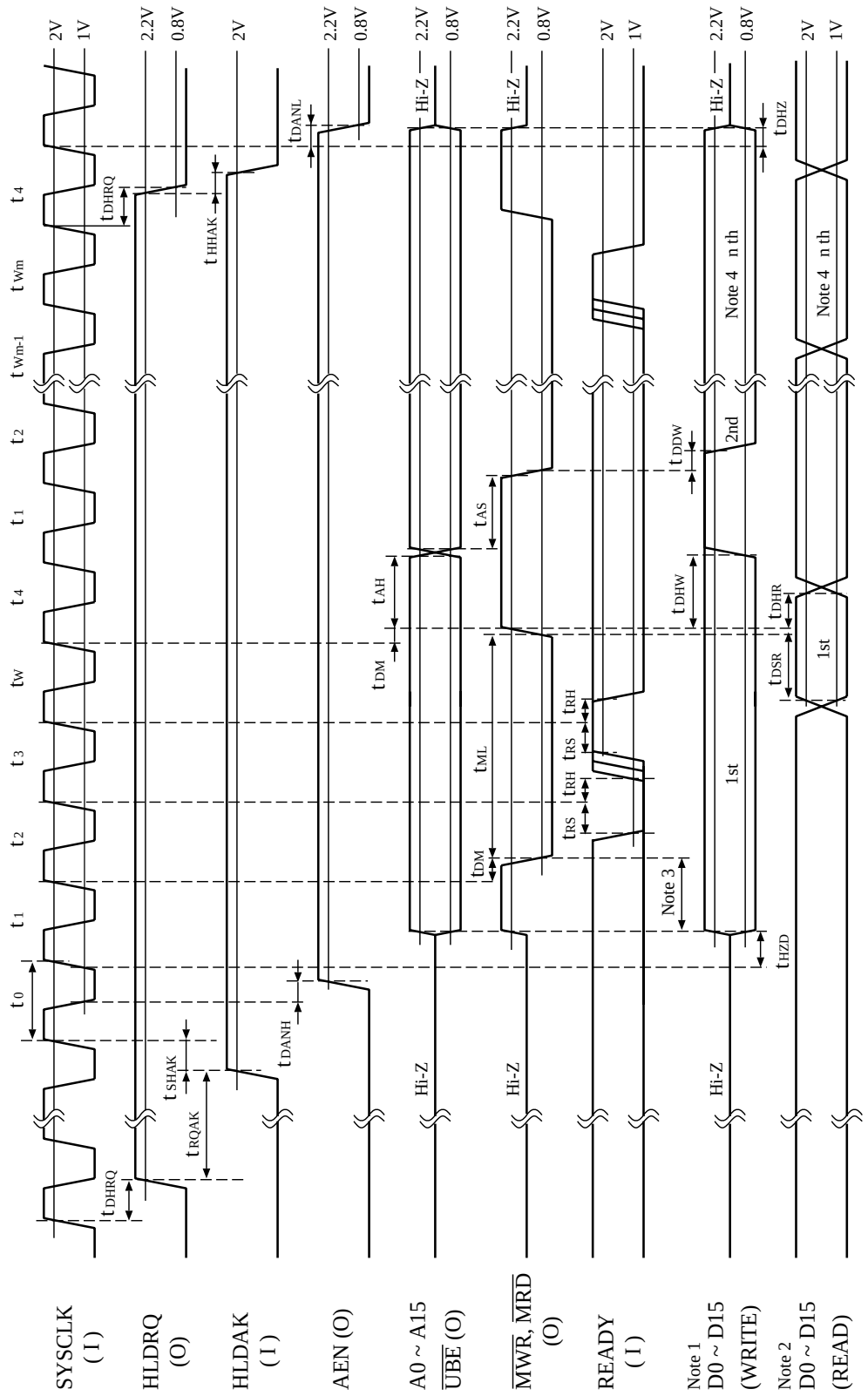
$$t_{sy} = \frac{1}{f_{sy}}$$

Microprocessor Interface

1. During Bus Master (DMAC)(C_L = 80 pF)

Parameter	Symbol	Min.	Typ.	Max.	Units
HLDRQ Delay Tim	t_{DHRQ}			80	ns
HLDAK Setup Time	t_{SHAK}	10			ns
HLDAK Hold Time	t_{HHAK}	0			ns
AEN HIGH Delay Time	t_{DANH}			80	ns
AEN LOW Delay Time	t_{DANL}			80	ns
Hi-Z to DRIVEN Time	t_{HZD}			70	ns
DRIVEN to Hi-Z Time	t_{DHZ}			80	ns
A15 - A0 UBE Setup Time	t_{AS}		1		t_{sy}
A15 - A0 UBE Hold Time	t_{AH}	$1t_{sy} - 50$			ns
$\overline{MWR}$ $\overline{MRD}$ Delay Time	t_{DM}			40	ns
$\overline{MWR}$ $\overline{MRD}$ Low Time	t_{ML}	$2t_{sy} - 30$			ns
READY Setup Time	t_{RS}	10			ns
READY Hold Time	t_{RH}	40			ns
Data Delay Time (WRITE)	t_{DDW}			70	ns
Data Hold Time (WRITE)	t_{DHW}		1		t_{sy}
Data Setup Time (READ)	t_{DSR}	40			ns
Data Hold Time (READ)	t_{DHR}	12			ns
HLDAK Response Time	t_{RQAK}			0.4	ms

Note: $tsy = \frac{1}{fsy}$ is the system clock cycle.



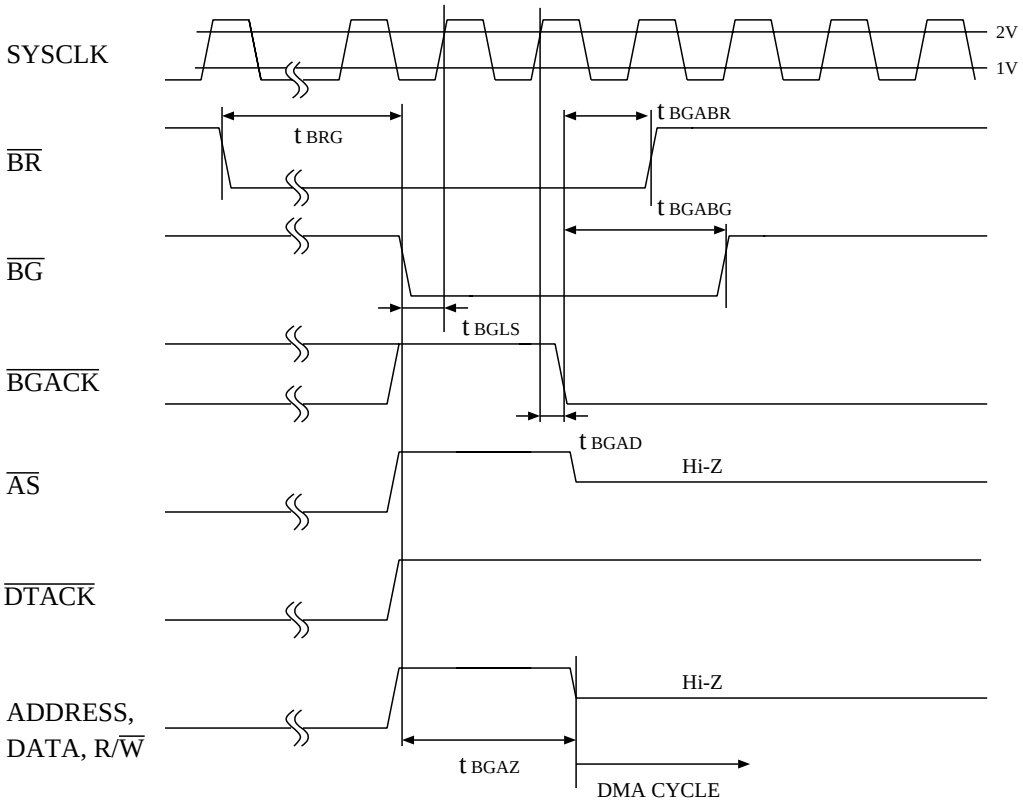
Note 1: When $\overline{UBE}$ ($\overline{LBE}$) is "H", D8 ~ D15 (D0 ~ D7) are high-impedance.
Note 2: $\overline{UBE}$ ($\overline{LBE}$) is "H", D8 ~ D15 (D0 ~ D7) are "Don't Care".
Note 3: Only 1st-DATA is output baout 1 tsy earlier than $\overline{MWR}$.
Note 4: n : $1 \leq n \leq 4$

Figure : Microprocessor Interface during Bus Master

2. During Bus Master (68000 DMA Transfer Specified in REG1)(C_L = 80 pF)

Parameter	Symbol	Min.	Typ.	Max.	Units
$\overline{BG}$ Setup Time	t_{BGLS}	10			ns
$\overline{BGACK}$ Delay Time	t_{BGAD}			80	ns
$\overline{BGACK}$ = "L" → $\overline{BR}$ = "H" Delay Time	t_{BGABR}		1		tsy
$\overline{BGACK}$ = "L" → $\overline{BG}$ = "H" Delay Time	t_{BGABG}	1.5		4.5	tsy
Bus Float Delay Time	t_{BGAZ}			80	ns
Control Signal Delay Time	t_{DM}			40	ns
Hi-Z to DRIVEN Time	t_{HZD}			80	ns
DRIVEN to Hi-Z Time	t_{DHZ}			80	ns
$\overline{DTACK}$ Setup Time	t_{RS}	10			ns
$\overline{DTACK}$ Hold Time	t_{RH}	40			ns
Data Delay Time (WRITE)	t_{DDW}			70	ns
Data Hold Time (WRITE)	t_{DHW}	10			ns
Data Setup Time (READ)	t_{DSR}	40			ns
Data Hold Time (READ)	t_{DHR}	0			ns
A15 - A0, $\overline{UBE}$ Setup Time	t_{AS}		1		tsy
A15 - A0, $\overline{UBE}$ Hold Time	t_{AH}	10			ns
$\overline{BG}$ Response Time	t_{BRG}			0.4	ms

Note: $tsy = \frac{1}{fsy}$ is the system clock cycle.



Note: Hi-z is indicating the 68000 pin condition.
The timing is based on the following:
V_{thH} = 2 V, V_{thL} = 1 V for the input pins, V_{thH} = 2.2 V, V_{thL} = 0.8 V for the output pins.

Figure : 68000 Interface during Bus Master 1

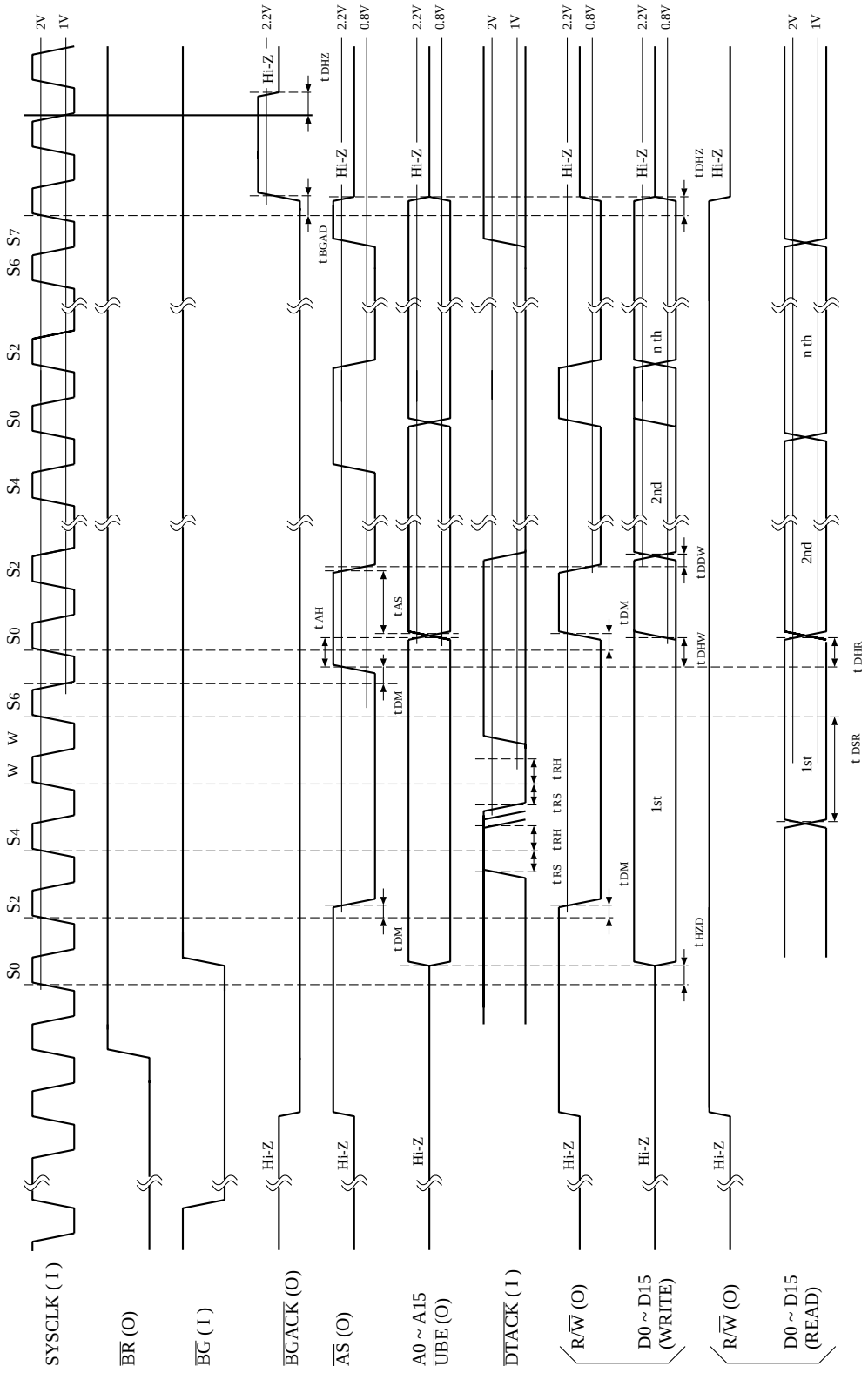


Figure : 68000 Interface during Bus Master 2

3. During Bus Slave (I/O Register)(C_L = 80 pF)

(80 family microprocessor)

Parameter		Symbol	Min.	Max.	Units
Read/Write On Time	**Note 1**	t_{WL}	100		ns
Read/Write Off Time (1)		t_{WH1}	100		ns
Read/Write Off Time (2)	**Note 2**	t_{WH2}	3		t_{sy}
Read/Write Rise or Fall Time		t_r, t_f		30	ns
Address Setup Time		t_{AS}	15		ns
Address Hold TIme		t_{AH}	10		ns
Data Setup Time		t_{DS}	40		ns
Data Hold Time		t_{DH}	10		ns
Data Delay Time		t_{DD}		60	ns

Note 1: Write On Time signifies the time in which both WR and $\overline{CS}$ are “L”. Read On Time signifies the time in which both $\overline{RD}$ and $\overline{CS}$ are “L”.

Note 2: tsy is the system clock cycle.
t_{WH2} is (1) the **READ Cycle of Status Data** register (REG6), (2) WRITE cycle of the **Command Data** (REG5), (3) the READ Cycle of the **Transmit/Receive Status** register (REG4) from Status Data or Command Data.

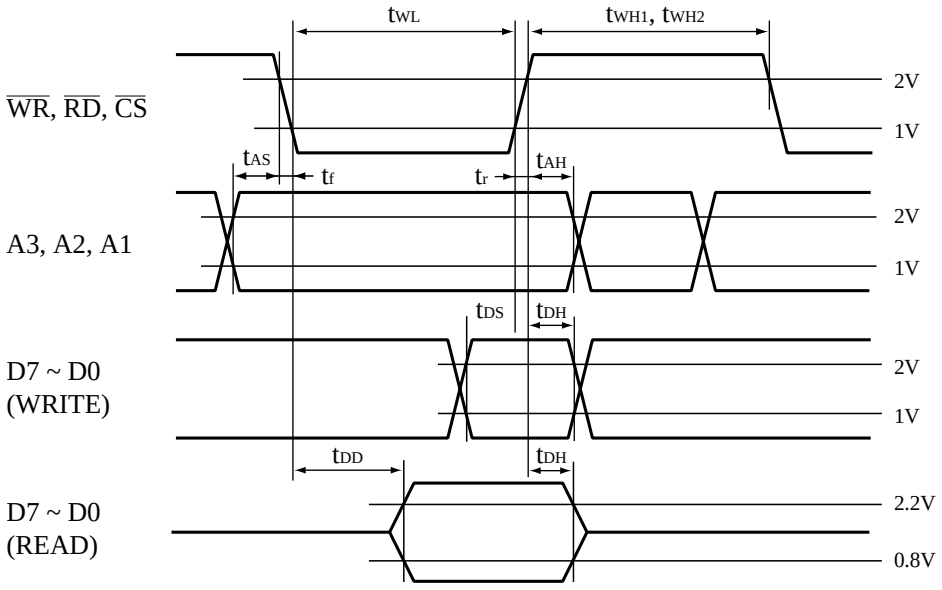


Figure : 80 Family Microprocessor

(68 Family Microprocessor)

Parameter		Symbol	Min.	Max.	Units
Read/Write On Time	**Note 1**	t_{WL}	100		ns
Read/Write Off Time (1)		t_{WH1}	100		ns
Read/Write Off Time (2)	**Note 2**	t_{WH2}	3		t_{sy}
Read/Write Rise or Fall Time		t_r, t_f		30	ns
Address Setup Time		t_{AS}	15		ns
Address Hold TIme		t_{AH}	10		ns
Data Setup Time		t_{DS}	40		ns
Data Hold Time		t_{DH}	10		ns
Data Delay Time		t_{DD}		60	ns

Note 1: Write On Time signifies the time in which $\overline{AS}$ ($\overline{E}$), $\overline{CS}$, and R/$\overline{W}$ are all “L”. Read On Time signifies the time in which both $\overline{AS}$ ($\overline{E}$) and $\overline{CS}$ are “L” and R/$\overline{W}$ is “H”.

Note 2: t_{sy} is the system clock cycle. t_{WH2} is (1) the READ cycle of the **Status Data register** (REG6), (2) the WRITE cycle of Command Data (REG5), (3) the READ cycle of the **Transmit/Receive Status** register (REG4) from Status Data or Command Data.

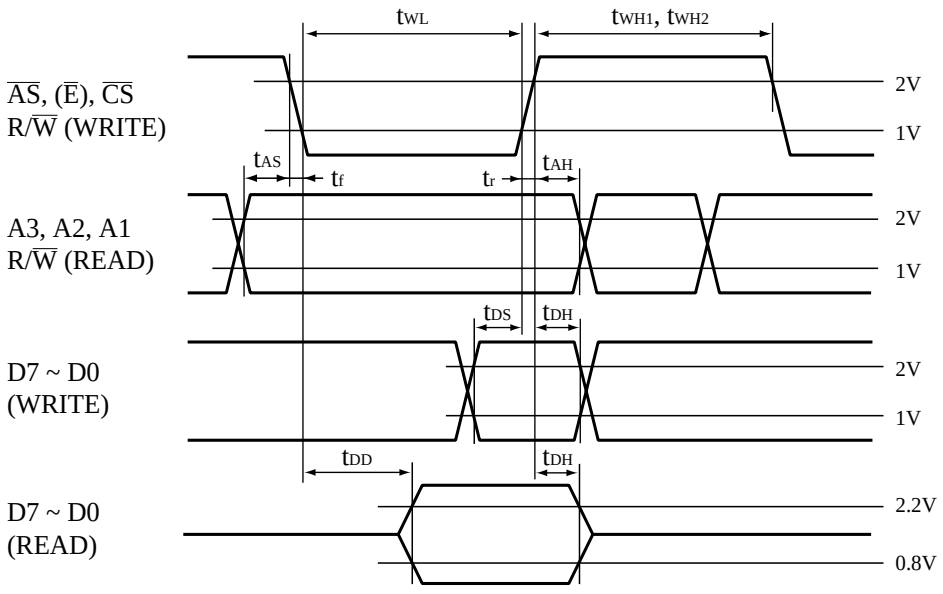
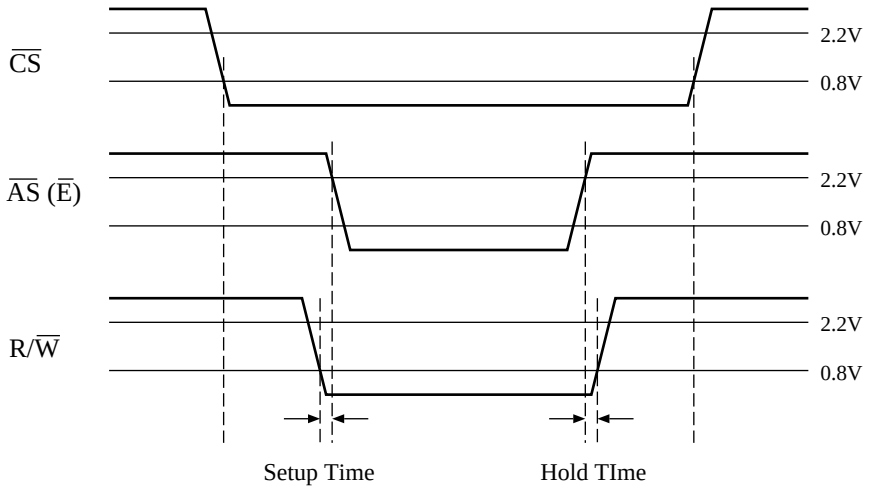


Figure : 68 Family Microprocessor

Note 3: Provide at least 0 ns for R/$\overline{W}$ Setup Time and Hold Time before and after the time in which both $\overline{AS}$ ($\overline{E}$) and $\overline{CS}$ are “L”. When the Setup Time and Hold Time are negative, be careful of the condition $\overline{AS}$ ($\overline{E}$) = “L”, $\overline{CS}$ = “L”, and R/$\overline{W}$ = “H” which causes the register data to be read.



B Channel Data DMA Controller Interface

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Request Delay Time	t_{DREQD}				50	ns
WR, RD, Pulth Width	t_{WH}		100			ns
Acknowledge Setup Time	t_{DACKS}		0			ns
Acknowledge Hold Time	t_{DACKH}		0			ns

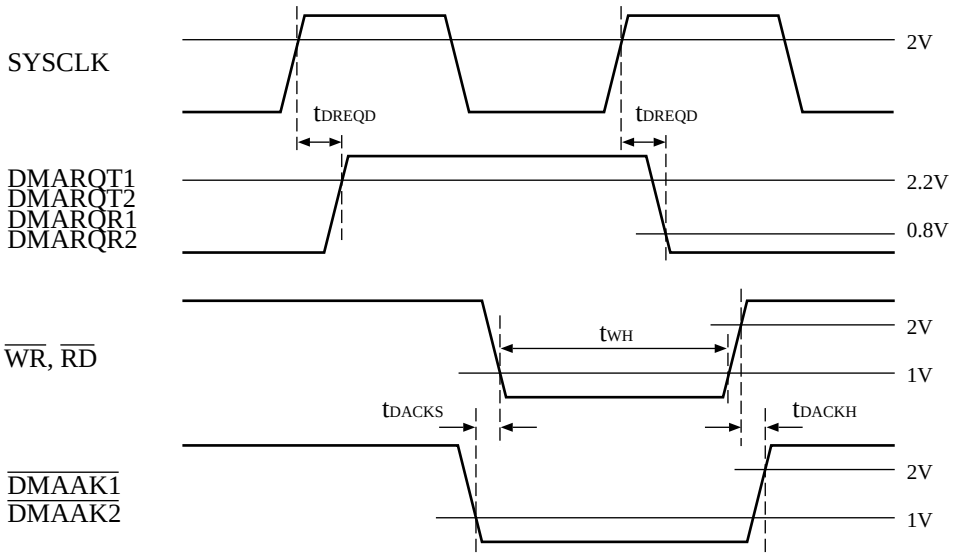


Figure : B Channel Data DMA Control Interface Timing

I.430 TTL Interface

(C_L = 80 pF)

Parameter	Symbol	Min.	Typ.	Max.	Units
Receive Pulse High-Level Period	t_{HRW}	4.95	5.21	5.46	µs
F Bit Transmission Delay Time	t_{RTD}		10.41		µs
Transmit Pulse Width	t_{HTW}	4.95	5.21	5.46	µs
Hi-Z to DRIVEN Time	t_{THZD}			50	ns
Transmit Pulse Phase Delay Time	t_{TPD}		50		ns
Timing Extract Jitter	j_{TT}	-7		+7	%

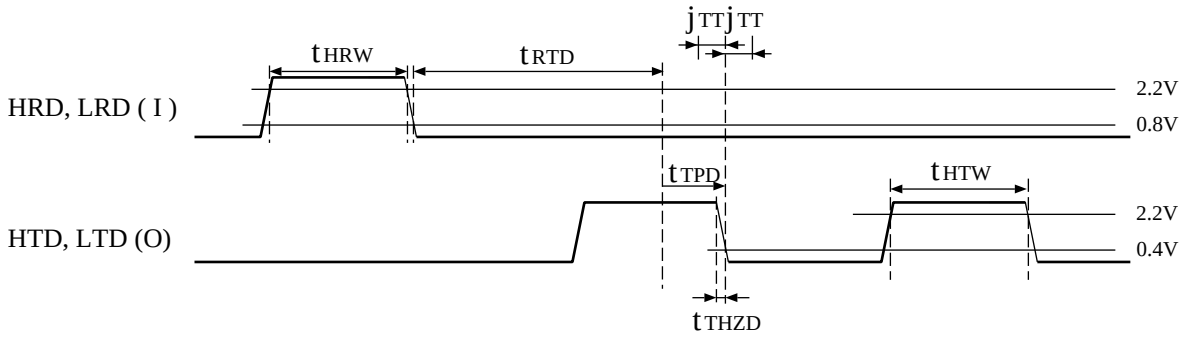


Figure : DSU Interface

Note 1: The F bit position transmitted from a TE towards the NT shall be delayed, nominally by two bit periods with respect to the F bit of the received frame.

Note 2: Though, this pin is either an output or an open drain pin, it is prescribed by the condition during the output.

Transformer Interface

1. Receive block

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Receive Input Impedance	Z_{Li}	Li	50			kΩ

2. Transmit block

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Transmit Output Impedance	Z_{Lo0}	When binary "0" is output		15		Ω
Transmit Output Impedance	Z_{Lo1}	When binary "1" is output	50			kΩ

3. Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Input Bit Rate	B_R	Refer to ITU-T I.430, 5.4.1		192		kbps
Timing Extract Jitter	J_{TT}	Refer to ITU-T I.430, 8.2.2	- 7		+ 7	%
Input/Output Phase Difference	P_D	Refer to ITU-T I.430, 8.2.3	- 7		+ 15	%

B Channel Interface (Internal Clock Mode : Normal)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
CL64K Output Frequency	f_{CL64K}	fx = 12.228 MHz		64		kHz
CL8K Synchronizing Frequency	f_{CL8K}	fx = 12.228 MHz		8		kHz
Clock Phase Difference	t_{CD}	fx = 12.228 MHz			12	ns
Receive Bch Data Output Delay Time	t_{BD}				200	ns
Transmit Bch Data Setup Time	t_{BS}		70			ns
Transmit Bch Data Hold Time	t_{BH}		10			ns

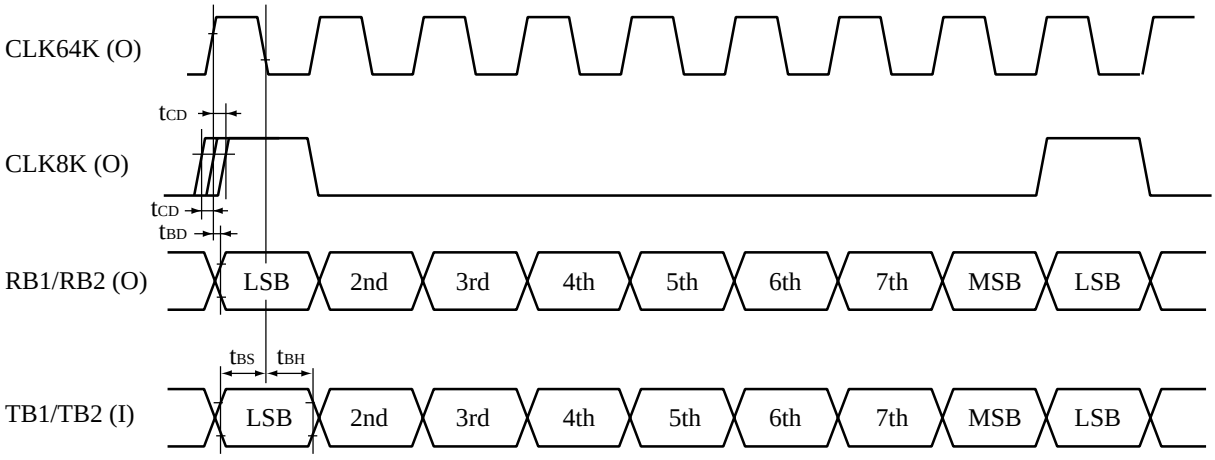


Figure : B Channel Input/Output Timing (Internal Clock Mode)

B Channel Interface (Internal Clock Mode : 56 kbps)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
CL56K Output Frequency	f_{CL56K}	fx = 12.228 MHz		56		kHz
CL8K Synchronizing Frequency	f_{CL8K}	fx = 12.228 MHz		8		kHz
Clock Phase Difference	t_{CD}	fx = 12.228 MHz			12	ns
Receive Bch Data Output Delay Time	t_{BD}				200	ns
Transmit Bch Data Setup Time	t_{BS}		70			ns
Transmit Bch Data Hold Time	t_{BH}		10			ns

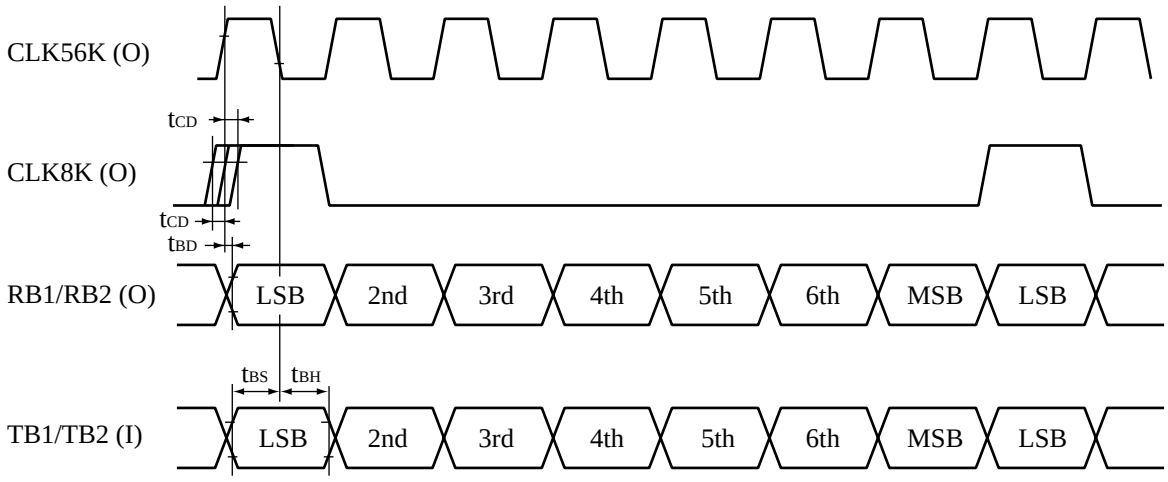


Figure : B Channel Input/Output Timing (56 kbps Interface)

B Channel Interface (Internal Clock Mode : 32 kbps)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
CL32K Output Frequency	f_{CL32K}	fx = 12.228 MHz		32		kHz
CL8K Synchronizing Frequency	f_{CL8K}	fx = 12.228 MHz		8		kHz
Clock Phase Difference	t_{CD}	fx = 12.228 MHz			12	ns
Receive Bch Data Output Delay Time	t_{BD}				200	ns
Transmit Bch Data Setup Time	t_{BS}		70			ns
Transmit Bch Data Hold Time	t_{BH}		10			ns

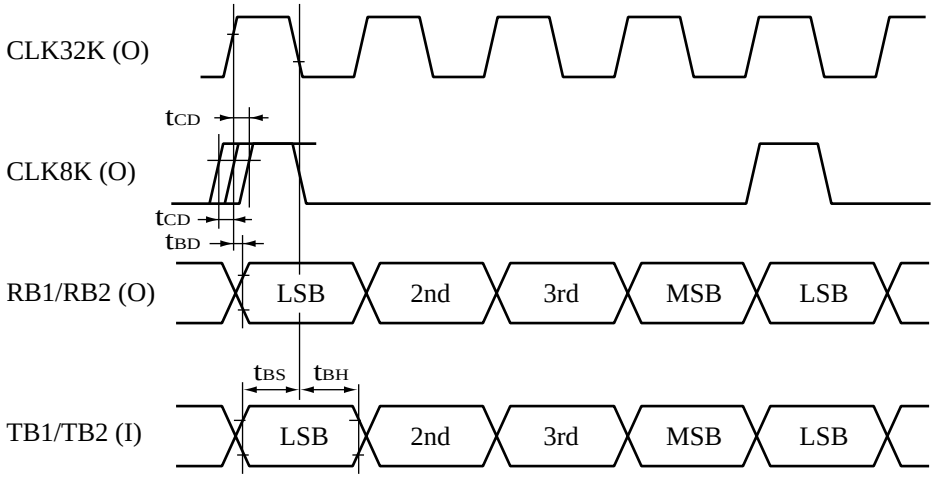


Figure: B Channel Input/Output Timing (32 kbps Interface)

B Channel Interface (External Clock Mode)

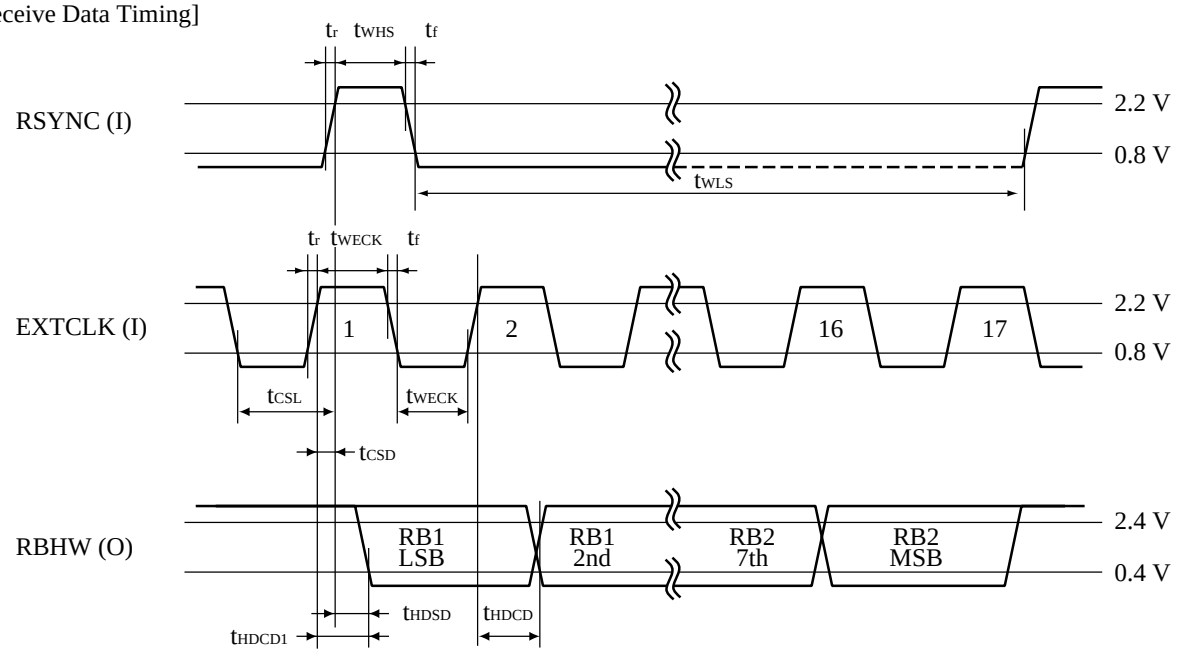
Test Condition: t_r, t_f = 5 ns

Parameter		Symbol	Min.	Typ.	Max.	Units
Clock Frequency		f_{ECK}	128		2048	kHz
Clock Cycle Period		t_{WECK}	200			ns
SYNC Frequency		t_{SYNC}		8		kHz
SYNC High-Level Period		t_{WHS}	200			ns
SYNC Low-Level Period		t_{WLS}	8			µs
Digital Input Rise Time		t_r			50	ns
Digital Input Fall Time		t_f			50	ns
SYNC Timing to Clock		t_{CSL}	40			ns
		t_{CSD}			100	ns
Data Output Delay Time to Clock	**Note 1, Note 2**	t_{HDCD1}			170	ns
Data Output Delay TIme to SYNC	**Note 1, Note 2**	t_{HDSD}			170	ns
Data Output Delay TIme	**Note 1**	t_{HDCD}			180	ns
Data Input Setup Time		t_{HDS}	65			ns
Data Input Hold Time		t_{HDH}	120			ns

Note 1: Load Condition for Data Output Delay Time R_L = 500 Ω, C_L = 165 pF,
I_{OL} = 0.8 mA, I_{OH} = -150 µA

Note 2: Based on the later point between EXTCLK or SYNC.

[Receive Data Timing]



[Transmit Data Timing]

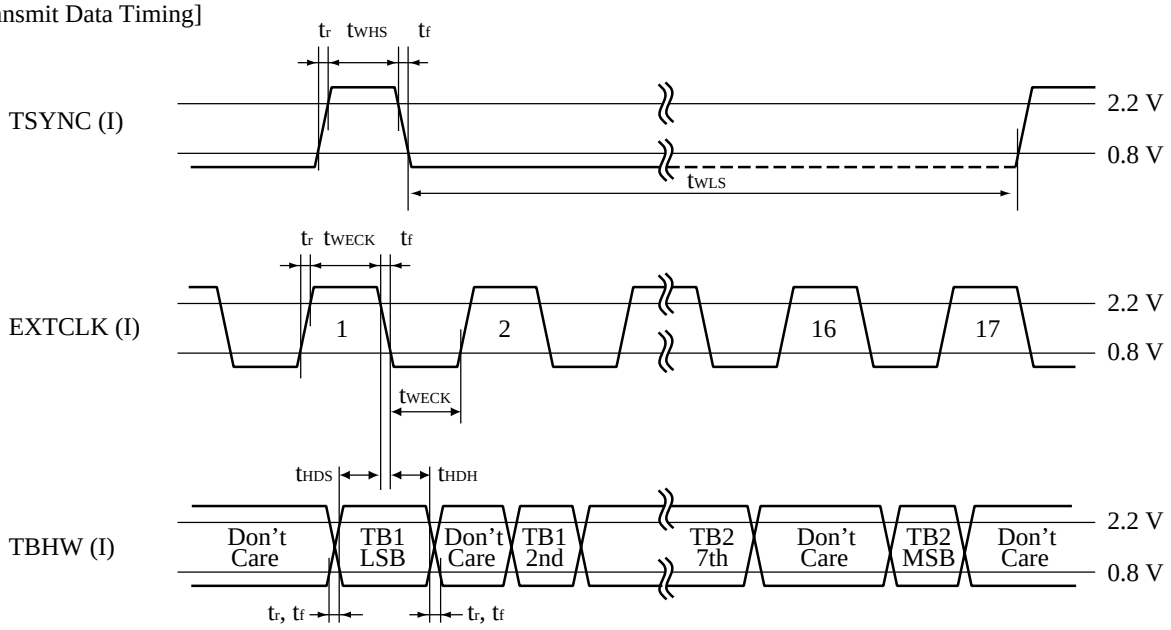


Figure : B Channel Input/Output Timing (External Clock Mode)

Bit Interface for Multiframing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
CL4K Output Frequency	f_{CL4K}	fx = 12.228 MHz		4		kHz
Received M Bit Output Dealy TIme	t_{MD}			130.2		µs

Note: Multiframing Bits are matched to the timing of each bit of the frame structure at the S/T reference point.

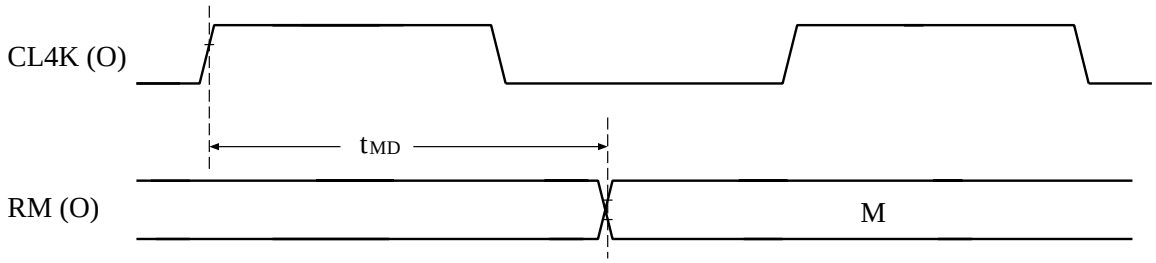


Figure : Input/Output Timing for Multiframing

$\overline{\text{WAKEUP}}$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
WAKEUP High Setup Time	t_{WKH}		100			ns
WAKEUP Low Hold Time	t_{WKL}		120			ns

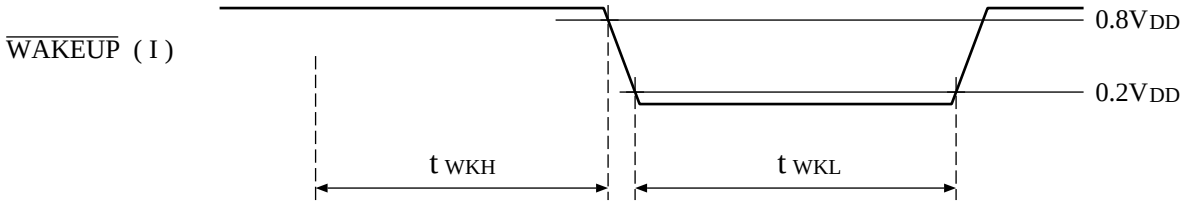


Figure : WAKEUP Time

$\overline{\text{RESET}}$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
RESET Time	t_{WRL}		250			µs

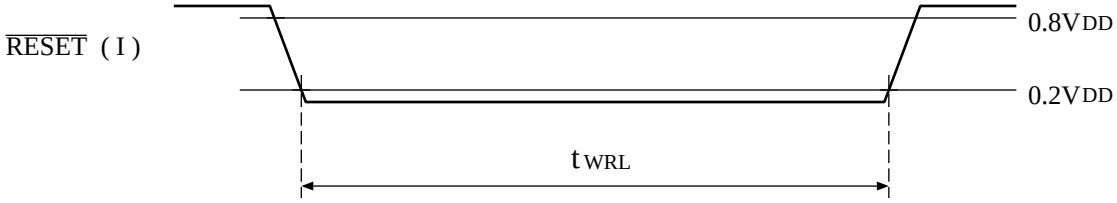
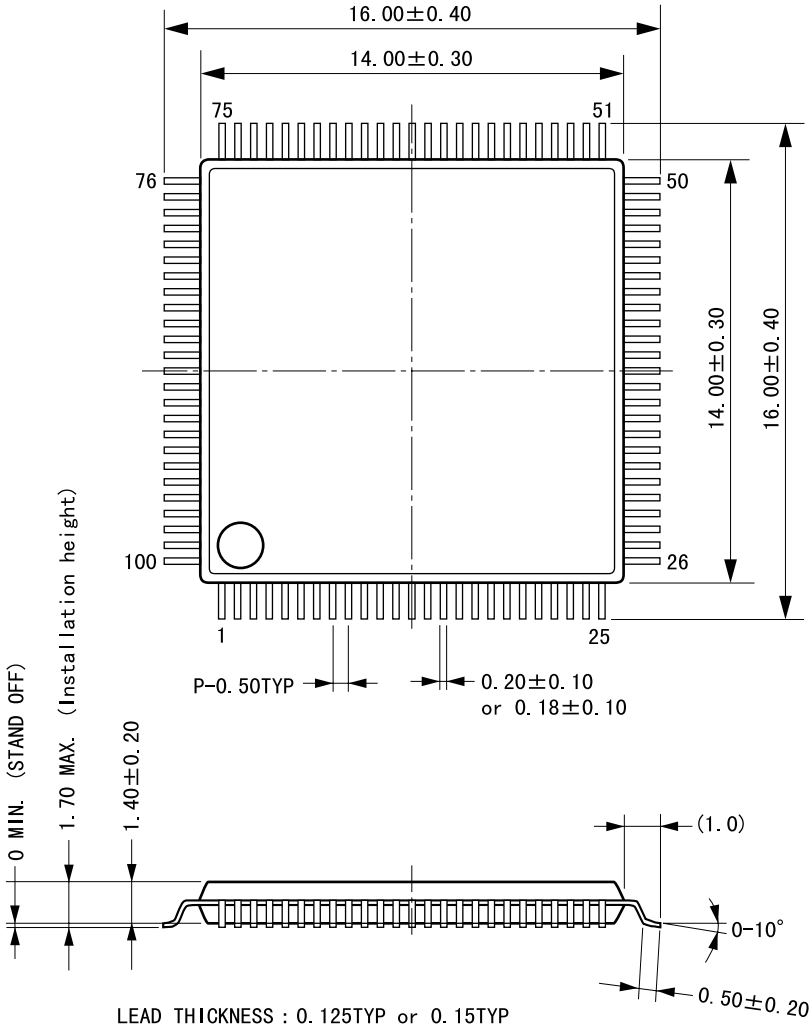


Figure : Reset Time

PACKAGE OUTLINE

C-PK100SP-1



(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

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