FAROUDJA Laboratories

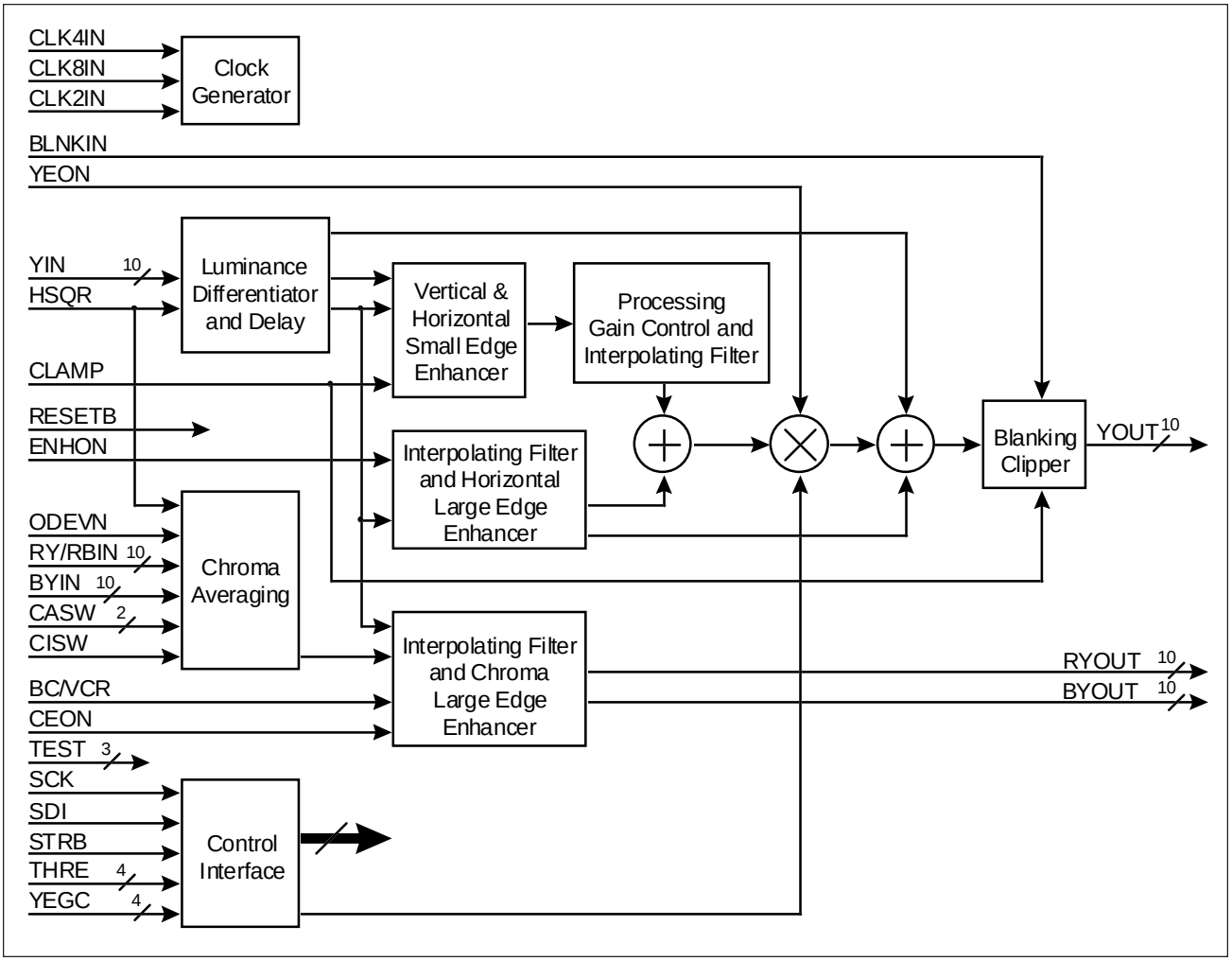
YCP 101 Digital Video Enhancer

The YCP 101 Digital Video Enhancer uses Faroudja Labs' patented nonlinear luma and chroma processing technology to enhance the quality of a YUV video signal derived either from a component source or separated from an NTSC or PAL source. The signals are all interpolated at appropriate points in their paths to double the sampling rates. This prevents the bandwidth expansion caused by nonlinear processing from introducing aliasing distortion. In the luma path, small edges above the programmable noise threshold and large edges are processed independently in a manner which gives optimum edge enhancement overall. In the chroma path only large edge enhancement is done, using a luma component factor in the chroma processing. Most of the parameters involved in the process are programmable via the serial control bus, although the built-in default values also allow the device to be used without any external control processor. All I/O paths are 10 bits wide and the internal signal processing is consistent with this.

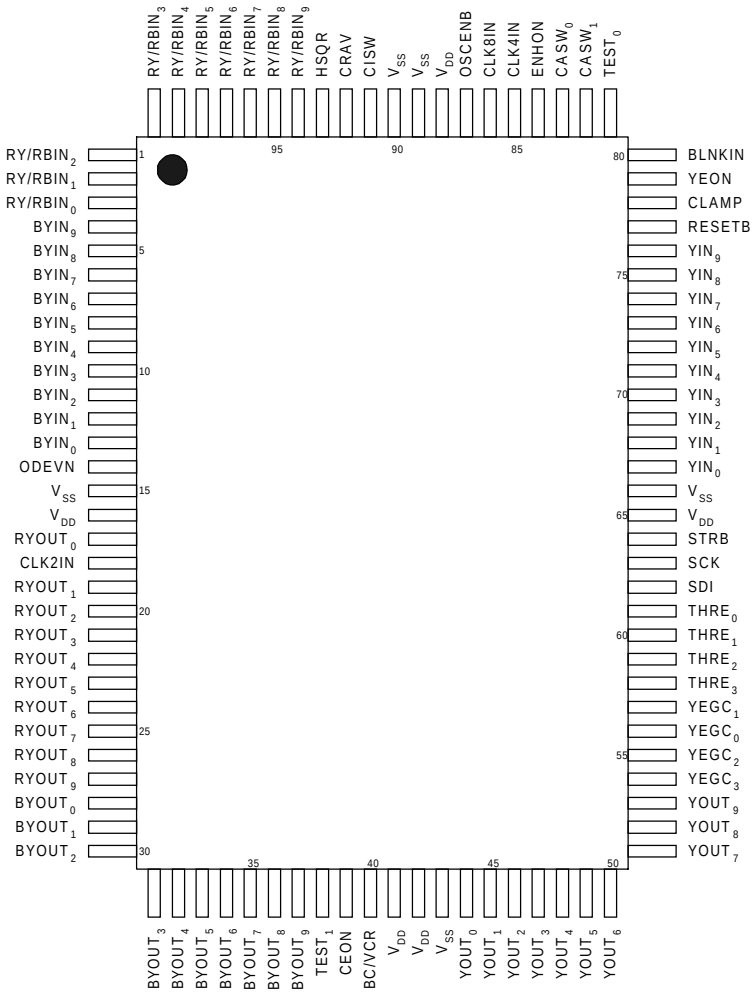
Features:

- Digital Luminance and Chrominance Enhancement consistent with 10-bit digital I/O
- Digital YUV outputs
- Input luminance sampling rates up to 30 MHz, output luminance rates up to 60 MHz
- Up to 1150 pixels/line
- Adaptive Digital Averager to reduce cross color with NTSC signal sources and eliminate Hanover blinds with PAL sources
- Can be used in conjunction with FRE 201 Digital Line Doubler as a pre- or post-processor
- Horizontal and Vertical Detail Processors
- 3-Wire Serial Control bus
- 0.5 watts typical power dissipation

Simplified Block Diagram



Packaging and Pinout Information



Package: 100-pin PQFP. θ_{ja} = xx °C/watt

Pin Connections and Functions

Pin #	Name	Description
Control Signals		
58-61	$THRE_{3-0}$	Detail processor threshold control. The levels set on these inputs allow the threshold used in the detail processor circuit to be adjusted. The levels can be changed asynchronously as long as the serial control bus is not used. The value can also be set via the serial control interface; any value written in this way will override the value set with the $THRE_{3-0}$ inputs. A rising edge on the STRB input transfers control to the serial bus and the device must be reset to re-activate the $THRE_{3-0}$ inputs.
79	YEON	Luminance enhancement on. When this input is set high the luminance enhancement function will be turned on. When it is set low the function will be turned off.
54, 55, 57, 56	$YEGC_{3-0}$	Luminance large-edge enhancement gain control. The levels set on these inputs allow the gain of the luminance small-edge enhancement circuit to be adjusted. The levels can be changed asynchronously as long as the serial control bus is not used. The value can also be set via the serial control interface; any value written in this way will override the value set with the $YEGC_{3-0}$ inputs. A rising edge on the STRB input transfers control to the serial bus and the device must be reset to re-activate the $YEGC_{3-0}$ inputs.
84	ENHON	Luminance large-edge enhancement on. When this input is set high this function will be turned on. When it is set low the function will be turned off.
14	ODEVN	Odd or even number of pixels/line. This input should be set high for applications with an even number of pixels/line, such as NTSC sampled at $4 \cdot f_{SC}$. It should be set low for applications with an odd number of pixels/line, such as PAL sampled at $4 \cdot f_{SC}$.
39	CEON	Chrominance enhancement on. When this input is set high the chrominance enhancement function will be turned on. When it is set low the function will be turned off.
92	CRAV	Chroma averager on. When this input is set high the 2-line chroma averager is turned on. This funtion should be used with PAL signals only if there is no other chroma averager in the system. When this input is set low the chroma averager is turned off.
81, 38	$TEST_{1-0}$	Test inputs. These pins should be set high for normal operation.
82-83	$CASW_{1-0}$	Chroma averager mode select. These inputs select the output of the chrominance averaging circuit. The selections are shown in Table 1.
40	BC/VCR	Broadcast/VCR signal processing control. When the input signal source is of broadcast quality this input should be set high for optimum processing. When the input source is of typical consumer VCR quality this input should be set low for optimum processing.
91	CISW	Chroma input mode switch. When this input is set high, multiplexed R-Y and B-Y signals are input on the $RY/RBIN_{9-0}$ bus at the luminance clock rate and the $BYIN_{9-0}$ bus is not used. When this input is set low the R-Y signal is input on the $RY/RBIN_{9-0}$ bus and the B-Y signal is input on the $BYIN_{9-0}$ bus.
77	RESETB	Reset. When this input is set low it will reset all the internal registers to the default states. Refer to the section on the control registers for details of these states. The device must be reset after it is powered-up.
63	SCK	3-wire serial control bus clock input. Refer to the section on the serial port for timing details.
62	SDI	3-wire serial control bus data input. Data can be written to the control registers via this pin. Refer to the section on the serial port for timing and format details and to the section on the registers for programming information.
64	STRB	3-wire serial control bus strobe input. Refer to the section on the serial port for timing details.

Pin #	Name	Description
Input Signals		
87	OSCENB	Internal oscillator enable input. This pin should be tied high during normal operation. If the external clocks should be stopped during operation this input should be set low to enable the oscillator. This will provide an internal clock to prevent damage occurring to the device.
76-67	YIN_{9-0}	10-bit luminance signal input bus. This signal is sampled on the rising edges of the CLK4IN clock.
94-100 1-3	$RY/RBIN_{9-0}$	10-bit R-Y or multiplexed R-Y and B-Y signal input bus. When CISW is set low the R-Y signal is input on the $RY/RBIN_{9-0}$ bus. In this mode the chroma signals are sampled on the rising edges of the CLK2IN clock. When the CISW input is set high, multiplexed R-Y and B-Y signals are input on the $RY/RBIN_{9-0}$ bus. In this mode the chroma signals are sampled on the rising edges of the CLK4IN clock.
4-13	$BYIN_{9-0}$	10-bit B-Y signal input bus. When CISW is set low the B-Y signal is input on the $BYIN_{9-0}$ bus. In this mode the chroma signals are sampled on the rising edges of the CLK2IN clock. When the CISW input is set high $BYIN_{9-0}$ bus is not used and these pins should be tied low.
86	CLK8IN	Clock input at 2 times the luminance sampling rate. This clock is used for the internal signal processing and output signal timing. Refer to the timing diagrams for the relationships between the clocks.
85	CLK4IN	Clock input at the luminance sampling rate. This clock is used for the luma signal timing. Refer to the timing diagrams for the relationships between the clocks.
18	CLK2IN	Clock input at the chroma sampling rate. This clock is used for the chroma signal timing. Refer to the timing diagrams for the relationships between the clocks.
93	HSQR	Horizontal frequency square wave input. This signal should be synchronized to the horizontal scanning frequency. The rising edge is used to reset the internal line memory counter.
80	BLNKIN	Blanking input. This signal indicates the blanking period of the composite input signal.
78	CLAMP	Clamp input. This signal should go low during the back porch period of each line.
Output Signals		
53-44	$YOUT_{9-0}$	Luminance output bus. The luminance (Y) output signal is available at these pins. The signal is clocked out on the rising edges of the CLK8IN clock.
27-19, 17	$RYOUT_{9-0}$	R-Y chrominance output bus. The R-Y (U) chrominance output signal is available at these pins. The signal is clocked out on the rising edges of the CLK4IN clock.
37-28	$BYOUT_{9-0}$	B-Y chrominance output bus. The R-Y (V) chrominance output signal is available at these pins. The signal is clocked out on the rising edges of the CLK4IN clock.
Power Supply Connections (not shown on Block diagram)		
See list	V_{SS}	Ground connections. Connect to the digital ground plane. Pins: 15, 43, 66, 89, 90
See list	V_{DD}	Power connections. Connect to the digital 5.0 volt power supply and decouple to the digital ground plane. Pins: 16, 41, 42, 65, 88

Description of Functional Blocks

Clock Generation Block

The internal clocks are derived from the three input clocks, CLK2IN, CLK4IN and CLK8IN, using gating circuits. CLK4IN is used to sample the luminance input and the multiplexed chrominance inputs when CISW is set high. CLK2IN is used to sample the chrominance inputs when CISW is set low. CLK8IN is used for the luminance output clock and CLK4IN is used for the chrominance output clock.

Serial Interface Block

The serial Interface block consists of a 3-wire input decoder and a number of control and status registers. When the STRB input is set low the SCK (clock) and SDI (data) inputs are enabled and data is clocked serially through a 64-bit shift register. When the STRB input goes high the first 8 bits of the last 64 bits to enter the register are examined for a valid address (AD_H). If the address is valid the remaining data is latched into the control registers. Refer to the section on the serial port for timing and format details and to the section on the registers for programming information.

Luminance Differentiator and Delay Block

The luminance signal is first resampled with the CLK8IN clock and interpolated up to that sampling rate. It is then processed in the Luminance Differentiator and Delay Block to generate the small- and large-edge functions required in the lumina edge enhancer circuits. This block also contains the delays necessary to time-align the various outputs of the block.

Vertical and Horizontal Small-Edge Enhancer Block

The outputs of the differentiator block are passed into the vertical and horizontal small-edge enhancer block. The processing of the vertical (line-to-line) and horizontal (pixel-to-pixel) edges is carried out in two separate sub-blocks inside this block. Only small edges are processed in this block. The nonlinear transfer function of the processor eliminates all large edges, which are processed separately in the Large-Edge Enhancer Block. An adjustable threshold also prevents the enhancement of very small edges to eliminate luma noise enhancement.

Processing Gain control and Low-Pass Filter

The output of the small-edge enhancer is passed into the gain control and low-pass filter block. The gain control circuit allows the amplitude of the signal to be controlled manually. The signal is then interpolated to double the sapling rate to match the output of the horizontal large-edge enhancer block.

Horizontal Large-Edge Enhancer Block

The outputs of the differentiator block are passed into the horizontal large-edge enhancer block. Only the horizontal i.e., pixel-to-pixel, edges are processed in this way. The nonlinear transfer function of the processor eliminates all small edges and expands the bandwidth of the signal. Consequently, the sampling rate is first doubled with an interpolating filter to prevent the introduction of aliasing distortion. The output of this block is then summed with the output of the small-edge enhancer/low-pass filter and a delayed version of the direct-path signal in such a way as to provide a seamless integration of the two processing paths and the direct path, resulting in optimum overall enhancement of the luminance signal.

Blanking Clipper

The blanking clipper is used to make corrections to the blanking level before the final output of the luma signal.

Chroma Adaptive Averager Block

The chrominance signals are first resampled with the CLK4IN clock and interpolated up to that sampling rate. The signals are then multiplexed if the input is set to separate R-Y and B-Y inputs (CISW set low) an passed into the Adaptive Averaging Filter. The filter is time multiplexed between the R-Y and B-Y signals and averages odd and even lines to eliminate Hanover blinds in signals from PAL coded sources. The transfer function of the averaging filter is adaptively controlled to minimize its effect on horizontal chroma edges. Although the averager can also be used with signals from NTSC coded sources it can be disabled by means of the $CASW_{1-0}$ inputs, as shown in Table 1, below:

Mode	$CASW_{1-0}$	Output of Adaptive Averager Block
1	00	Averager input with 0 line delay
2	01	Averager input with 2 line delay
3	10	Averager input with 1 line delay
4	11	Averager output

Since the averager has a 1 line delay, which matches the delay in the luma path, the normal operating modes will be 3 for (NTSC) and 4 (for PAL).

Chroma Large-Edge Enhancer Block

The outputs of the chroma averager block are passed into the chroma large-edge enhancer block, where the R-Y and B-Y signals are demultiplexed to be independently processed. Only the horizontal i.e., line-to-line, chroma edges are processed. The nonlinear transfer function of the processor eliminates all small edges and only the large edges are enhanced to eliminate chroma noise enhancement. Consequently, the sampling rate is first doubled with an interpolating filter to prevent the introduction of aliasing distortion. Consequently, the sampling rate is first doubled with an interpolating filter to prevent the introduction of aliasing distortion. The chroma enhancement process is modulated by the luma signal since major chroma changes are invariably accompanied by luminance changes. The enhanced signals are then added to a delayed version of the direct-path signal to generate the R-Y and R-B output signals.

Memory Map

Register Addr.	Name	Bits 7	6	5	4	3	2	1	0	Default Value
0_H	ADDR	$Device\_Address_{7-0}$								AD_H
1_H	HDR	$Header_{7-0}$								00_H
2_H	THA	$Threshold\_Offset_{4-0}$								00_H
3_H	CG	$Chroma\_Gain_{3-0}$								60_H
4_H	DPA	$Detail\_Enhancement_{3-0}$								$B0_H$
5_H	CAT	$Chroma\_Av\_Thesh_{3-0}$								$C0_H$
6_H	DPT	$Detail\_Thresh_{5-0}$								$X0_H$*
7_H	YEG	$Luma\_Enh\_Gain_{3-0}$								$Y0_H$**

Notes: * The value X of $Detail\_Thresh_{5-2}$ is determined by the setting of the $THRE_{3-0}$ pins after reset.

** The value Y of $Luma\_Enh\_Gain_{3-0}$ is determined by the setting of the $YEGC_{3-0}$ pins after reset.

All registers are write only.

Register Details

Note: All values are binary except for those with an H suffix, which are hexadecimal.

Address 00_H: ADDR. Default value AD_H

The eight bits in the ADDR register identify the address of the device:

Bit	7	6	5	4	3	2	1	0
Mnemonic	$Address_7$	$Address_6$	$Address_5$	$Address_4$	$Address_3$	$Address_2$	$Address_1$	$Address_0$
Address value	1	0	1	0	1	1	0	1

The device will only respond to the current 8-byte sequence if the first byte corresponds to the device address, AD_H.

Address 01_H: HDR. Default value 00_H

The eight bits in the HDR register set the operating mode of the device:

Bit	7	6	5	4	3	2	1	0
Mnemonic	$Address_7$	$Address_6$	$Address_5$	$Address_4$	$Address_3$	$Address_2$	$Address_1$	$Address_0$
Default value	0	0	0	0	0	0	0	0

The device will only operate correctly if this byte is set to the default mode, 00_H. Other values will put the device into test modes.

Register Details

Note: All values are binary except for those with an H suffix, which are hexadecimal.

Address 02_H: THA. Default value 00_H

The five most significant bits in the THA register set the threshold offset between the vertical and horizontal small edge (detail) enhancement circuits, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	$Thr\_O'set_4$	$Thr\_O'set_3$	$Thr\_O'set_2$	$Thr\_O'set_1$	$Thr\_O'set_0$	0	0	0
Default value	0	0	0	0	0	0	0	0

$Thr\_O'set_{4-0}$: These bits set the threshold offset between the vertical and horizontal detail enhancement circuits, as follows:

00_H* = Zero threshold offset.
10_H = Maximum negative threshold offset.
$0F_H$ = Maximum positive threshold offset.

This 5-bit number is a 2's complement value. This allows the threshold for vertical small edge enhancement to be made larger (positive offset) or smaller (negative threshold) than that for horizontal small edge enhancement. Refer to the description of the DPT and YEG registers (addresses 6_H and 7_H) for more details.

Bits 2-0 are not used in normal operation and must always be set to 000.

Address 03_H: CG. Default value 60_H

The eight bits in the CG register set the chroma large edge enhancement gain level, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	Chr_Gain_3	Chr_Gain_2	Chr_Gain_1	Chr_Gain_0	0	0	0	0
Default value	0	1	1	0	0	0	0	0

Chr_Gain_{3-0}: These bits set the chroma large edge enhancement gain level, as follows:

00_H = Zero chroma large edge enhancement gain.
60_H* = Default detail chroma large edge enhancement gain.
FF_H = Maximum detail chroma large edge enhancement gain.

Address 04_H: DPA. Default value $B0_H$

The eight bits in the DPA register set the luma small edge (detail) enhancement gain level, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	Det_Enh_3	Det_Enh_2	Det_Enh_1	Det_Enh_0	0	0	0	0
Default value	1	0	1	1	0	0	0	0

Det_Enh_{3-0}: These bits set the small edge (detail) enhancement gain level relative to the overall enhancement level set by the YEG register (or the YEGC3-0 pins), as follows:

00_H = Zero detail enhancement gain.
$B0_H$* = Default detail enhancement gain.
FF_H = Maximum detail enhancement gain.

* Indicates default value

Address 05_H: CAT. Default value $C0_H$

The eight bits in the CAT register set the chroma averager threshold level, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	Chr_Av_3	Chr_Av_2	Chr_Av_1	Chr_Av_0	0	0	0	0
Default value	1	1	0	0	0	0	0	0

Chr_Av_{3-0}: These bits set the chroma averager threshold level, used to set the edge level above which the averager is switched into the signal path, as follows:

00_H = Zero threshold.

$C0_H$* = Default threshold.

FF_H = Maximum threshold.

This is only effective when $CASW_{1-0}$ is set to 11, for signals from PAL coded sources.

Address 06_H: DPT. Default value set by pins $THRE_{3-0}$

The eight bits in the DPT register set the detail enhancement threshold level, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	Det_Thr_5	Det_Thr_4	Det_Thr_3	Det_Thr_2	Det_Thr_1	Det_Thr_0	0	0
Default value	$THRE_3$	$THRE_2$	$THRE_1$	$THRE_0$	0	0	0	0

Det_Thr_{5-0}: These bits set the detail enhancement threshold level, used to set the level below which no enhancement is made, on the assumption that the detail is noise, as follows:

00_H = Zero detail enhancement threshold.

FF_H = Maximum detail enhancement threshold.

The default value of the detail enhancement threshold is determined by the settings of the $THRE_{3-0}$ pins. In this way it is possible to use the device in its default mode, without the need for any programming, and still have control over the detail enhancement threshold. A value of 60_H is recommended. A rising edge on the STRB input transfers control to the serial bus and the device must be reset to re-activate the $THRE_{3-0}$ inputs.

Address 07_H: YEG. Default value set by pins $YEGC_{3-0}$

The eight bits in the YEG register set the overall luminance enhancement gain, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	$Luma\_Enh_3$	$Luma\_Enh_2$	$Luma\_Enh_1$	$Luma\_Enh_0$	0	0	0	0
Default value	$YEGC_3$	$YEGC_2$	$YEGC_1$	$YEGC_0$	0	0	0	0

$Luma\_Enh_{3-0}$: These bits set the overall luminance enhancement gain level, which controls the overall enhancement of the luma signal, both small and large edges, as follows:

00_H = Zero luminance enhancement gain.

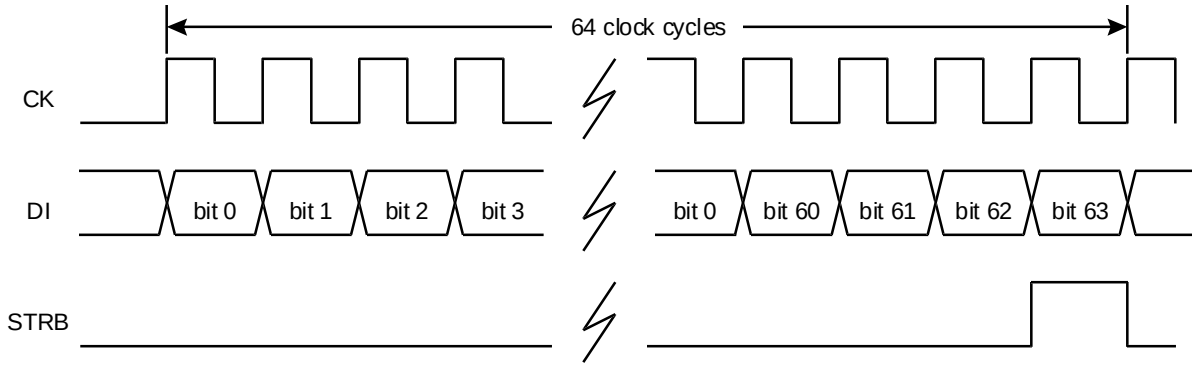
FF_H = Maximum luminance enhancement gain.

The default value of the overall enhancement is determined by the settings of the $YEGC_{3-0}$ pins. In this way it is possible to use the device in its default mode, without the need for any programming, and still have control over the detail enhancement level. A value of 80_H is recommended. A rising edge on the STRB input transfers control to the serial bus and the device must be reset to re-activate the $YEGC_{3-0}$ inputs.

* Indicates default value

Serial Control Bus Operation and Protocol

The YCP101 is programmed by means of a 3-wire serial bus. If the device is not programmed after a reset it will operate with the default parameter values shown in the register descriptions. The programming protocol requires 8 bytes of data to be written into the device via the DI pin, as shown in the timing diagram below. The bit sequence of each byte is LSB first, MSB last. During the final cycle of the 64 clock cycles the STRB line is pulsed high to latch the 8 bytes of data into the registers. The first byte is the device address, AD_H, and this is followed by the header byte, 00_H, and then the six data bytes, as shown in the diagram below. The data values shown are the default values automatically set up after the device is reset. After the sequence is complete the clock may be stopped or the sequence may be repeated continuously. The maximum clock speed is 14.4 kHz.

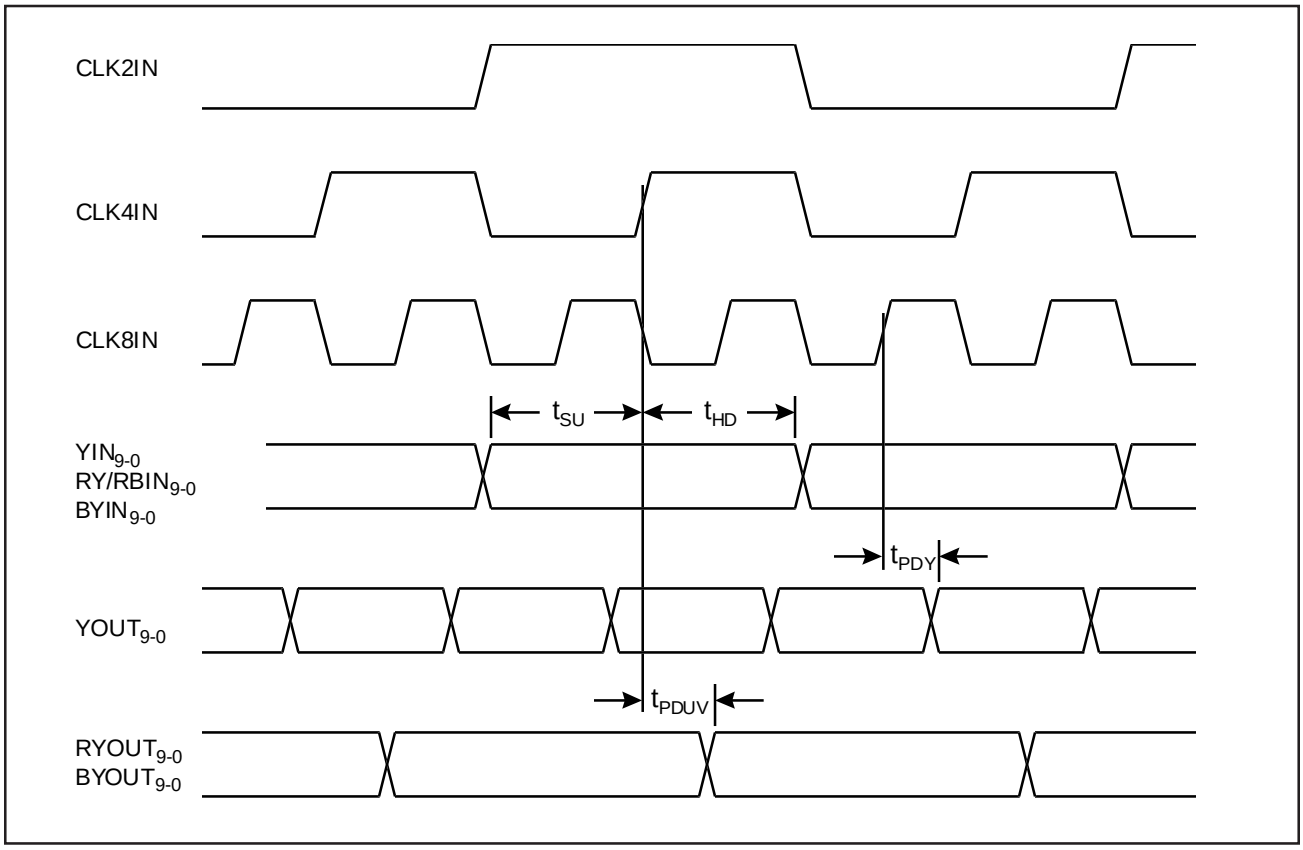


Bits 0-7	Bits 8-15	Bits 16-23	Bits 24-31	Bits 32-39	Bits 40-47	Bits 48-55	Bits 56-63
Device Address (10101101)	Header (00000000)	THA (00000000)	CG (01100000)	DPA (10110000)	CAT (11000000)	DPT (XXXX0000) See note 1	YEG (YYYY0000) See note 2

Note 1: The values of the 4 MSBs of DPT (XXXX) are determined by the settings of the $THRE_{3-0}$ pins after reset.

Note 1: The values of the 4 MSBs of YEG (YYYY) are determined by the settings of the $YEGC_{3-0}$ pins after reset.

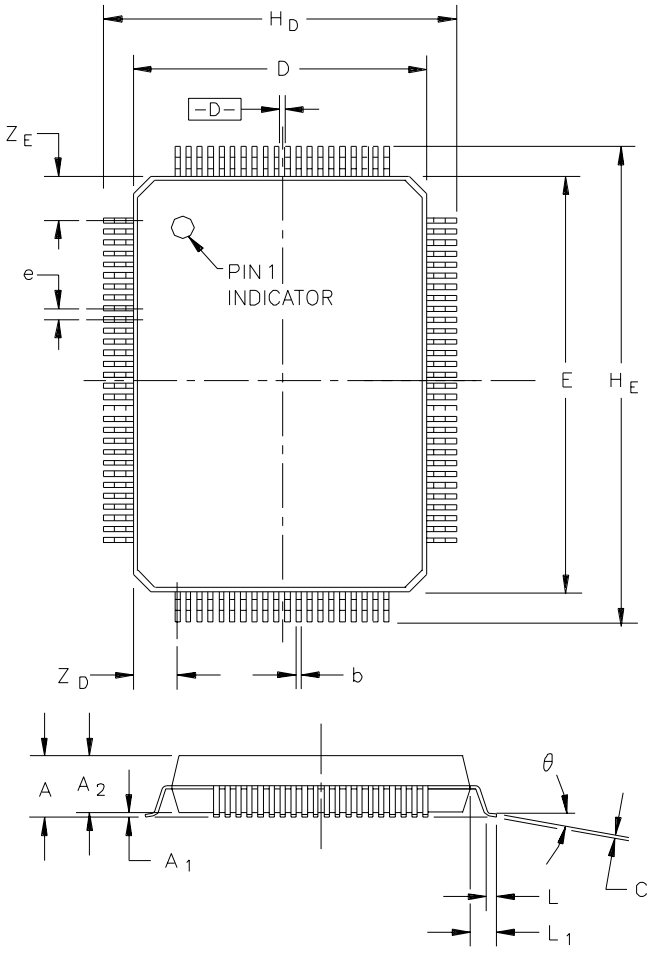
Input and Output Signal Timing



Input and Output Signal Timing

Symbol	Description	Min.	Nom.	Max.	Units	Conditions
Input Signal Timing						
f_{CLK4IN}	Input clock frequency			30	MHz	
f_{CLK8IN}	Output clock frequency			60	MHz	
t_{SU}	Input to clock setup	TBD			nsec.	
t_{HD}	Input to clock hold	TBD			nsec.	
Output Signal Timing						
t_{PDD}	CLK8IN to $YOUT_{9-0}$ propagation delay			TBD	nsec.	
t_{PDA}	Clock to $RY/BYOUT_{9-0}$ propagation delay			TBD	nsec.	

Package Dimensions



Ref.	Millimeters Min.	Typ.	Max.	Inches Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55		3.05	0.100		0.120
b	0.23		0.38	0.009		0.015
C	0.13		0.23	0.005		0.009
D	13.90		14.10	0.547		0.555
E	19.90		20.10	0.783		0.791
e		0.65			0.0256	
H_D	16.95		17.45	0.667		0.687
H_E	22.95		23.45	0.904		0.923
L	0.65		0.95	0.025		0.037
L1		1.60			0.063	
Z_D		0.5			0.02	
Z_E		0.5			0.02	
θ	0°		7°	0°		7°

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