YA28

2.5 Gb/s 1:4 Demultiplexer with Clock and Data Recovery

Features

Meets or exceeds all relevant ANSI, ITU and Bellcore specifications

Fully balanced, differential architecture

Differential CML data input accepts signals of 2.5 Gb/s data rate

Loss of lock signal

4-bit 622 Mb/s Low Voltage Differential Signal (LVDS) outputs

Single 3.3 V supply for simplified system integration

Industry standard 48-pin LQFP package

Applications

SONET/SDH-based transmission systems, test equipment and modules

OC-48 fibre optic modules and line termination

WDM for OC-48 SONET applications

ATM over SONET/SDH

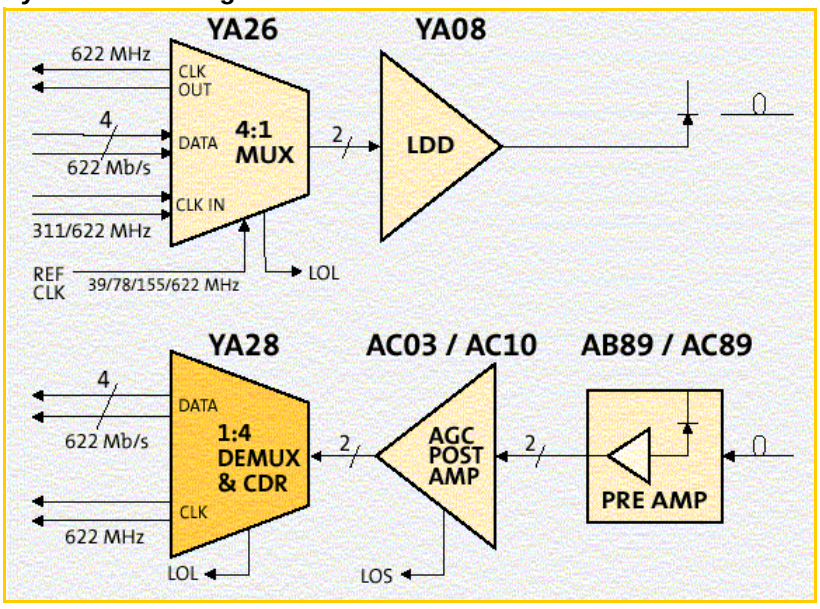
Section repeaters, muxes, terminators, broadband cross-connects

The Nortel Networks YA28 1:4 Demultiplexer and clock recovery circuit is a bipolar monolithic demultiplexer that accepts a nominal 2.5 Gb/s data stream and extracts a 2.5 GHz clock and retimes the 2.5 Gb/s datastream. This data is then multiplexed to 4-bit parallel data at 622 Mb/s, which is output with a data clock at 622 MHz.

Nortel Networks offers a portfolio of optical networking ICs for use in high-performance optical transmitter and receiver functions. The YA28 provides for power and chip-count savings that translate into better utilization of board real estate and ultimately cost savings to the designer of fiber-based Datacom or Telecom solutions.

The YA28 is fabricated using a high yield silicon bipolar process. It is available in a 48-lead LQFP package.

System block diagram



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Functional description

The YA28 uses phase lock loop techniques to recover a high frequency dock from NRZ binary data presented to pins RXD_INP and RXD_INN at nominally 2.5 Gb/s. The recovered clock retimes the data which is then demultiplexed into four 622 Mb/s data streams on LVDS compatible outputs. For SONET/SDH applications the device is tuned during manufacture to provide a VCO center frequency close to 2.488 GHz. This coarse tuning is performed during production and no additional trimming is required for VCO alignment. For normal operation, the only external components required are decoupling capacitors and loop filter components.

System inputs

Inputs RXD_INP and RXD_INN are fully differential CML inputs designed to receive AC coupled signals from a post amplifier. Normally, this would be the Nortel Networks AC03/ AC10 Automatic Gain Control (AGC) Amplifier. These inputs include on-chip termination resistors of nominally 50 Ω.

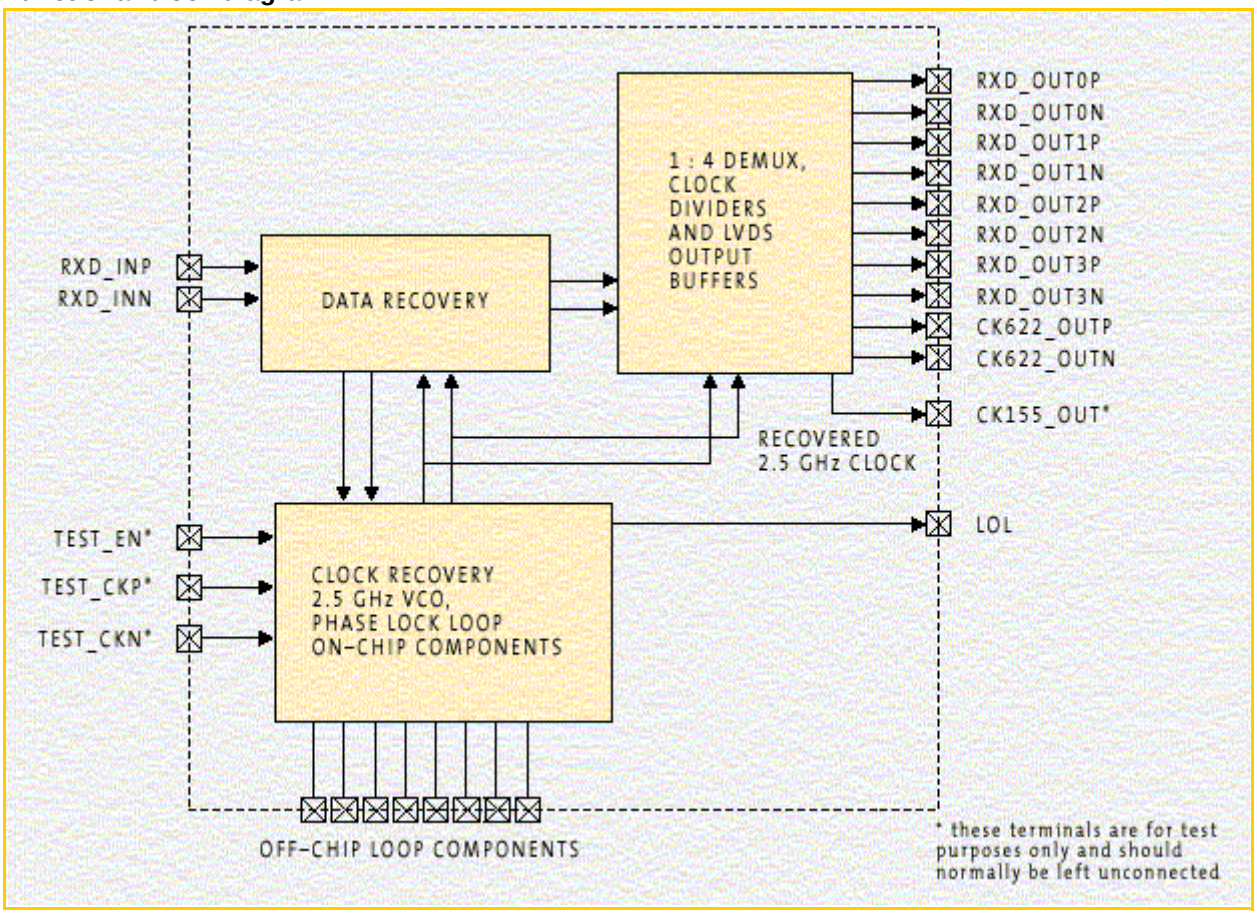
Phase locked loop

The PLL used in the YA28 is a fully balanced differential design, similar to that used in the YA18 Clock and Data Recovery function, comprising VCO and phase/frequency detector. The VCO has been designed to minimize jitter and the effects of temperature and supply voltage ripple. The VCO center frequency is digitally programmed during manufacture to minimize the effect of process variations.

System outputs

The recovered clock from the CDR section is divided down to 622 MHz and output on CK622_OUTP and CK622_OUTN. The retimed data is demultiplexed to 622 Mb/s and output on RXD_OUTnP and RXD_OUTnN (n=0 to 3). The data output transitions are retimed to the falling edge of the recovered clock (i.e. the falling edge of pin CK622_OUTP).

Functional block diagram



Loss of lock

The loss of lock indicator is an open-collector output (active low) which functions by monitoring cycle slips of the input relative to the VCO. The output sinks a maximum current of 10 mA. It will be active for at least 2.5 µs after the most recent frequency correction pulse, by which time the loop is assumed to be in phase lock and data is assumed to be valid. The loss of lock signal may be extended with external circuitry if required. The frequency correction current pulse is emitted if two successive samples of clock by data transitions show a slip of the phase of the clock signal either in the forward or reverse directions with respect to the data edges. An input signal compliant with the tolerance requirements of Bellcore GR-253 will not trigger the LOL output after the 10 ms allotted for loop acquisition.

Test inputs and outputs

A number of test inputs are provided for production testing at low speeds. These unterminated inputs bypass the internal VCO and are left unconnected under normal operation.

A divided version of the 2.5 GHz VCO output at 155 MHz is delivered as a single-ended low power PECL output at pin CK155_OUT. The CK155_EN pin can be used to enable this functionality.

Note: Under normal operation leave these pins unconnected.

Absolute maximum ratings

These are stress ratings only Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device Avoid operating the device outside the recommended operating conditions defined below.

Symbol	Parameter	Min	Max	Units
VCC	Supply voltage - any VCC/VCC_OUT/VCC_VCO pin	-0.7	6.0	V
VIcml	CML data input voltage - single-ended wrt GND	0	VCC+0.5	V
IOlvds	LVDS output current		50	
VIlvpecl	LVPECL single ended input voltage	-0.5	VCC+0.5	V
VIlvcmos	LVCMOS single ended input voltage	-0.5	VCC+0.5	V
VOoc	Open Collector output voltage	-0.5	VCC+0.5	V
Tstg	Storage Temperature	-65	135	°C

Recommended operating conditions

Symbol	Parameter	Min	Typical	Max	Units
VCC	Supply voltage - any VCC pin	3.135	3.30	3.465	V
Vripple	VCC supply voltage noise and ripple			15	mV rms
VIDcml	CML differential input voltage (peak-to-peak)	100	400	500	mV pk-pk
Vicml	CML input voltage, recommended overall range	2.15		VCC	V
VIHpecl	PECL input HIGH voltage	VCC -1.165		VCC -0.88	V
VILpecl	PECL input LOW voltage	VCC -1.81		VCC -1.475	V
VIHcmos	Input voltage high, LVCMOS input	2.0		VCC	V
VILcmos	Input voltage low, LVCMOS input	0		0.8	V
Tj	Junction temperature	-40		125	°C
Tamb	Ambient temperature	-40		85	°C

All voltages are with respect to GND (0 V) unless otherwise stated.

The specified VCC levels include all supply rail variations except ripple and noise, which are specified as Vripple.

DC electrical characteristics

Symbol	Parameter	Min	Typical	Max	Units
IIHlvpecl	LVPECL i/p high current, at VIH = VCC -0.88			100	µA
IILlvpecl	LVPECL i/p low current, at VIL = VCC -1.81			50	µA
VOHpecl	LVPECL output HIGH voltage	VCC -1.065		VCC -0.88	V
VOLpecl	LVPECL output LOW voltage	VCC -1.81		VCC -1.62	V
I ih	Input current high, LVCMOS input			10	µA
I il	Input current low, LVCMOS input			-10	µA
VOL oc	Open Collector O/P Low voltage at IOL = 1mA			0.4	V
IOH oc	Open Collector O/P High leakage current at VOH = VCC			1	µA
VMAX oc	Open Collector Pull-up Voltage			VCC	V
IOL oc	Open Collector O/P Low Current			5	mA
Icc max	Current drawn from the VCC supply		315	398	mA
PD max	Device power dissipation		1.2	1.5	W

Over recommended operating conditions unless otherwise noted.

AC characteristics

Parameter	Min	Typical	Max	Units
VCO loop aquisition time			10	ms
Jitter Tolerance at RXD_INP/N inputs, bandwidth from 10 to 600 Hz	15			UI pk-pk
from 600 Hz to 6 kHz	20 dB/dec			UI pk-pk
from 6 kHz to 100 kHz	1.5			UI pk-pk
from 100 kHz to 1 MHz	20 dB/dec			UI pk-pk
above 1 MHz	0.15			UI pk-pk
Jitter generated at TXD_OUTP/N outputs, bandwidth 12 kHz to 20 MHz			0.0075	UI rms
Jitter gain from RXD_INP/N to CKOP/N			0.1	dB
LOL asserted pulse width	1		10	µs

Over recommended operating conditions unless otherwise noted, output load 50 Ω.

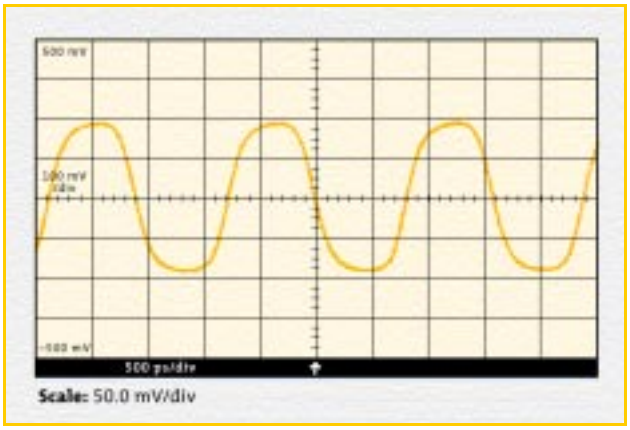
LVDS output DC electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Voh	Output voltage high, Voa or Vob	R load = 100 Ω	Vol +125	1475	mV
Vol	Output voltage low, Voa or Vob	R load = 100 Ω	925	Voh-125	mV
[Vod]	Output differential voltage	R load = 100 Ω	250	400	mV
Vos	Output offset voltage	R load = 100 Ω	1125	1275	mV
Ro	Output impedance, single ended	Vcm = 1.0 V and l.4 V	40	140	Ω
ΔRo	Ro mismatch between A and B	Vcm = 1.0 V and l.4 V		10	%
[ΔVod]	Change in [Vod] between “0” and “1”	R load = 100 Ω		25	mV
ΔVos	Change in Vos between “0” and “1”	R load = 100 Ω		25	mV
Isa, Isb	Output current	Driver shorted to ground		40	mA
Isab	Output current	Driver shorted to ground		12	mA

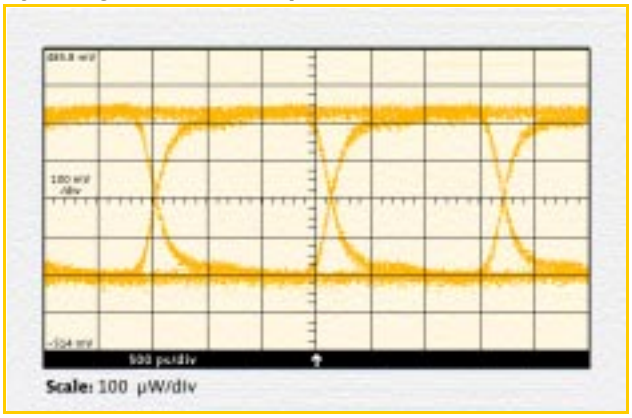
LVDS output AC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t fall	Vod fall time, 20% to 80%		100	500	ps
t risel	Vod rise time, 20% to 80%		100	500	ps
Clock	Clock signal duty cycle	622 MHz	45	55	%

CK622_OUT waveform



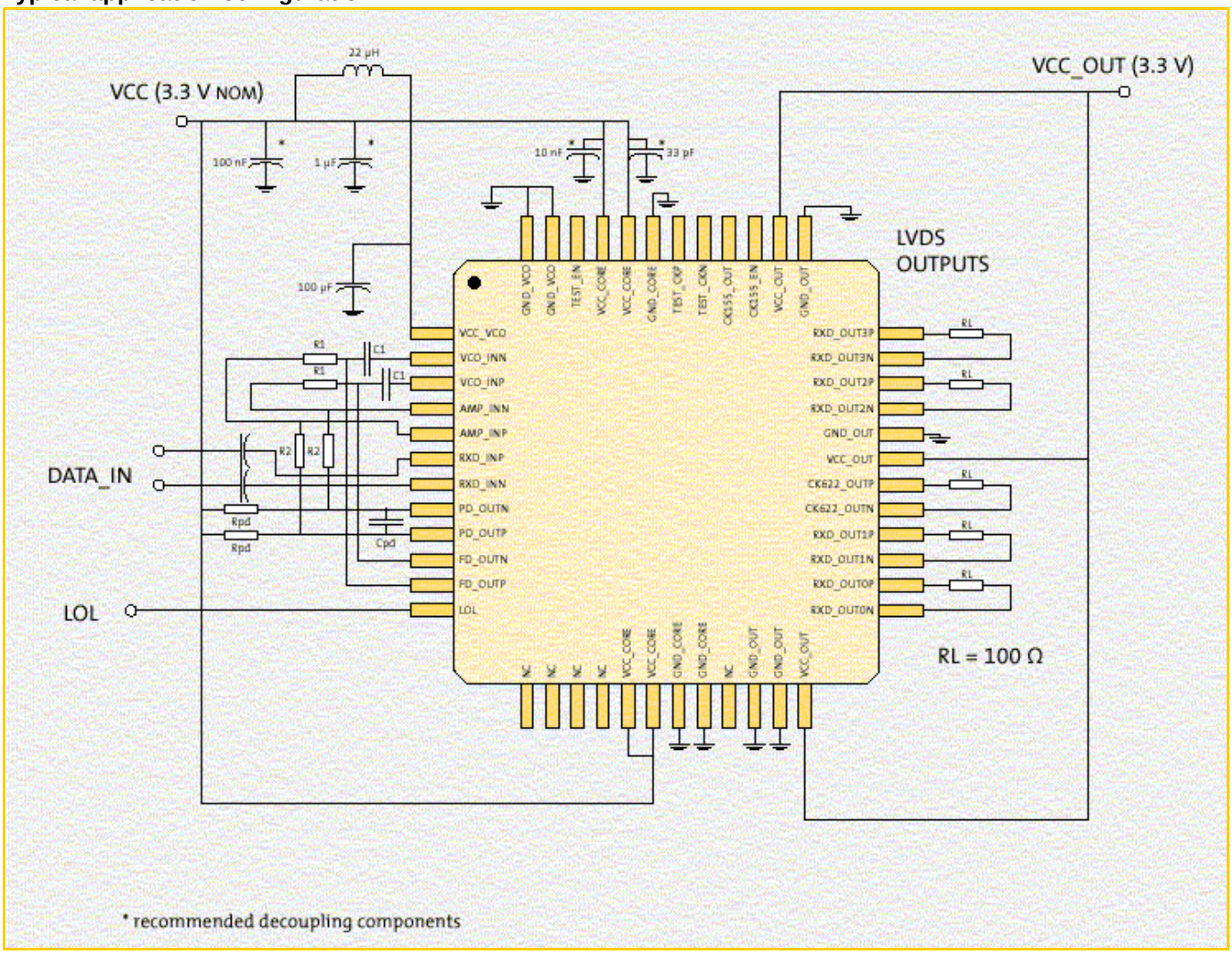
Eye diagram - data outputs



Additional design and applications information

The application diagram “Typical application configuration” shows the configuration for using the YA28 in a 2.5 Gb/s OC-48/STM-16 system. This shows all required external components, including supply decoupling capacitors.

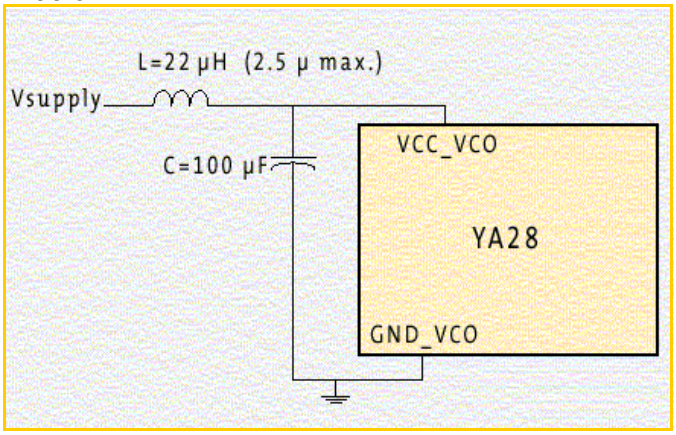
Typical application configuration



Power supply noise

Although the device has been designed to maximize supply noise rejection, it is recommended that you use an LC filter network, shown in “Supply filter circuit” below, between the supply and pin 1, VCC_VCO. Using this configuration, the device will function within the jitter specification with a maximum supply noise of 50 mVpp, over a frequency range from 6 kHz to 2 MHz, on the supply. The effective series resistance of the network must not exceed 2.5 Ω.

Supply filter circuit

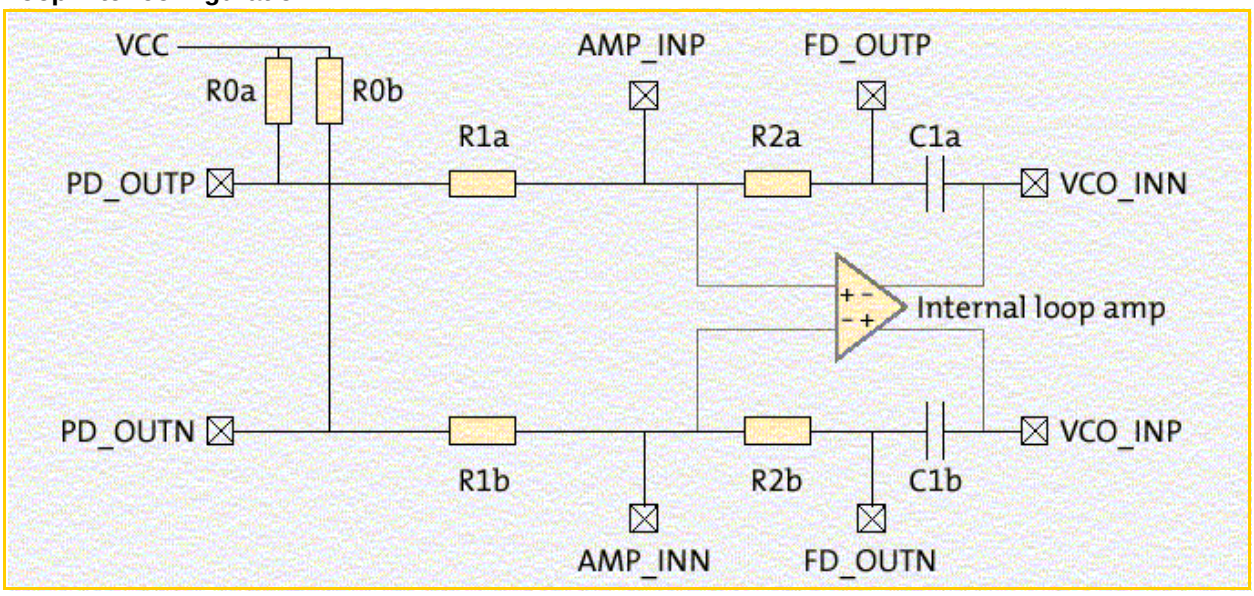


Setting the loop filter

The YA28 is designed for regenerator and receiver applications. Its integrated PLL is a fully differential design with loop bandwidth set by an external network. The configuration of this network is shown in “Loop filter configuration” with typical component values listed in the typical loop filter component values table.

These components are surface mount parts of 0603 size, with ±2% tolerance for resistors up to 2 MΩ, ±5% tolerance for capacitors up to 10 nF, and ±10% tolerance for capacitors from 10 nF to 100 nF. The typical loop filter component values table defines a set of typical values for the loop filter components for a given bandwidth. Alternative values can be determined by using the standard PLL performance equations.

Loop filter configuration



Typical loop filter component values

Loop bandwidth (kHz)	R0 a, b (Ω)	R1 a, b (kΩ)	R2 a, b (kΩ)	C1 a, b (nF)
1800	82	8.2	1.0	100

Pin assignment

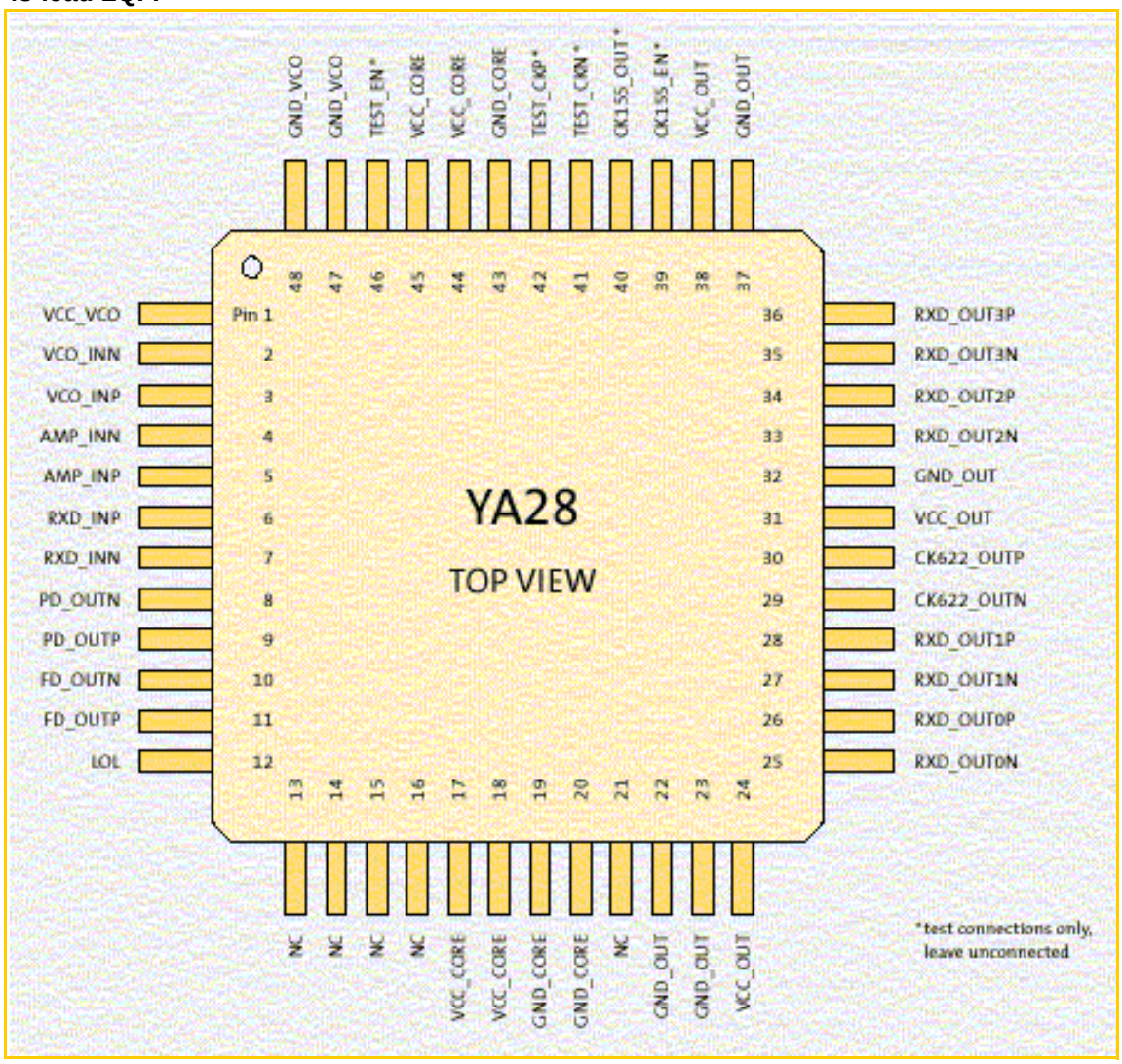
Pin No.	Pin Name	Type	Description	Function
1	VCC_VCO	P		VCC for voltage controlled oscillator
2	VCO_IN	O/I	Analog	Voltage controlled oscillator positive input
3	VCO_IP	O/I	Analog	Voltage controlled oscillator negative input
4	AMP_INN	I	Analog	Input to loop filter op amp
5	AMP_INP	I	Analog	Input to loop filter op amp
6	RXD_INP	I	Analog	Positive differential data input
7	RXD_INN	I	Analog	Negative differential data input
8	PD_OUTN	O	Analog	Loop preamplifier negative output
9	PD_OUTP	O	Analog	Loop preamplifier positive output
10	FD_OUTN	O	Analog	Frequency detector positive output
11	FD_OUTP	O	Analog	Frequency detector negative output
12	LOL	O	Open Collector	Lock flag (Active low)
13, 14, 15, 16, 21	N/C			No connection
17, 18, 44, 45	VCC_CORE	P		VCC for core sections of chip
19, 20, 43	GND_CORE	P		GND for core sections of chip
22, 23, 32, 37	GND_OUT	P		VGND for data and clock output buffers
24, 31, 38	VCC_OUT	P		+3.3 V supply rail for clock and data output buffers
25	RXD_OUT0N	O	LVDS	Retimed data differential negative output (4)
26	RXD_OUT0P	O	LVDS	Retimed data differential positive output (4)
27	RXD_OUT1N	O	LVDS	Retimed data differential negative output (4)
28	RXD_OUTlP	O	LVDS	Retimed data differential positive output (4)
29	CK622_OUTN	O	LVDS	Recovered and divided clock differential negative output
30	CK622_OUTP	O	LVDS	Recovered and divided clock differential positive output
33	RXD_OUT2N	O	LVDS	Retimed data differential negative output (4)
34	RXD_OUT2P	O	LVDS	Retimed data differential positive output (4)
35	RXD_OUT3N	O	LVDS	Retimed data differential negative output (4)
36	RXD_OUT3P	O	LVDS	Retimed data differential positive output (4)
39	CK155_EN	I	DC	Enable pin for test clock output (leave unconnected)
40	CK155_OUT	O	PECL	155 MHz divided clock test output (leave unconnected)
41	TEST_CKN	I	PECL	External test clock input (leave unconnected)
42	TEST_CKP	I	PECL	External test clock input (leave unconnected)

Pin No.	Pin Name	Type	Description	Function
46	TEST_EN	I	CMOS	Test enable input for test clock (leave unconnected)
47, 48	GND_VCO	P		VGND for VCO

Package pin configuration

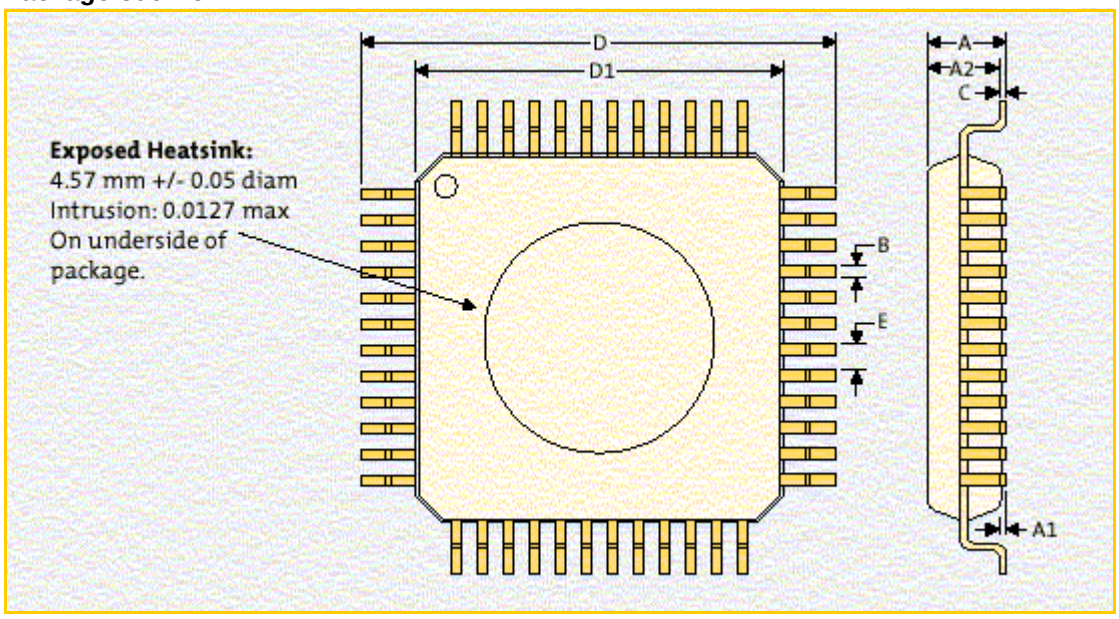
The device is packaged in a 48-lead plastic low-profile quad flat pack (LQFP). To achieve the required thermal resistance, the package contains a heat slug that must be soldered directly to the circuit board.

48-lead LQFP



Package outline drawing and dimensions

Package outline



Dimension	Min (mm)	Nom (mm)	Max (mm)
Lead Pitch (E)		0.50	
Body Size (Dl)		7.00	
Component Tip-to-Tip (D)		9.00	
Component Height (A)			1.60
Component Standoff (A1)	0.05		0.15
Body Thickness (A2)	1.35	1.40	1.45
Lead Width, plated (B)	0.17	0.22	0.27
Lead Thickness, plated (C)	0.09		0.20

Ordering information

Please quote the Product Code from Table below when ordering as this is the identification that appears on the part when shipped.

Product ordering information

Product Code	Product Name
A0774011 (QMV1080-1AF5)	YA28 2.5 Gb/s Demultiplexer with Clock and Data Recovery

For additional information on Nortel Networks products and services offered, please contact your local representative.

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