Preliminary

YA26

2.5 Gb/s 4:1 Multiplexer and Clock Generator

Data Sheet

Features

Meets or exceeds all relevant ANSI, ITU and Bellcore specifications

LVDS inputs accept signals of 622 Mb/s data rate

Differential data outputs provide CML signals at 2.5 Gb/s with 3.3 V or 5 V interface capability

Internally synthesized 2.5 GHz clock accepts four different reference frequencies

622.08 MHz clock output with selectable delay locked loop for simplified clocking schemes

PLL loss of lock signal

Single 3.3 V supply for simplified system integration

Typical power dissipation of 1 W (750 mW without DLL)

Industry standard 48-pin LQFP package

Applications

SONET / SDH-based transmission systems, test equipment and modules

OC-48 fibre optic modules and line termination

WDM for OC-48 SONET applications

ATM over SONET / SDH

Section repeaters, muxes, terminators, broadband cross-connects

The Nortel Networks YA26 Multiplexer and Clock Generator multiplexes 4-bit parallel input data at 622 Mb/s into a single, serial output data stream at 2.5 Gb/s.

An on-chip phase locked loop generates a 2.5 GHz clock from a choice of external stable references. Particular care has been taken in the design of the input interfacing of the device to simplify the task of correctly synchronizing the clock and data. The CML output of the YA26 is configured to interface directly with the Nortel Networks YA08 Laser Diode Driver or any other devices accepting differential CML signals.

The Microelectronics Group of Nortel Networks offers a portfolio of optical networking ICs for use in high-performance optical transmitter and receiver functions. The YA26 provides for power and chip-count savings to the designer of fibre-based datacom or telecom solutions.

The YA26 is fabricated using Nortel Networks' NT25 high yield silicon bipolar process. It is available in a 48-lead LQFP package.

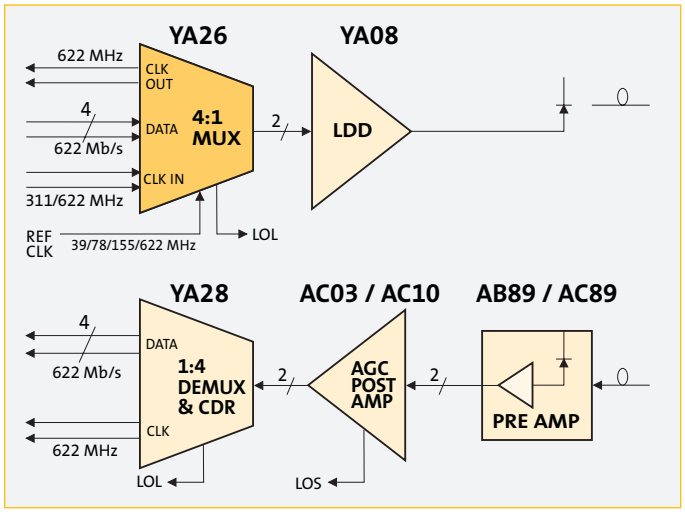

Figure 1: System Block Diagram

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Functional description

The YA26 Multiplexer takes 4-bit parallel data at 622 Mb/s and multiplexes it to a single serial output data stream at 2.5 Gb/s. The device features an on-chip 2.5 GHz VCO and associated multiplying PLL that locks to a received reference clock. To aid flexibility of the device for various systems, the reference clock inputs can accept 38.88 MHz, 77.76 MHz, 155.52 MHz and 622.08 MHz inputs, controlled by a simple digital interface.

To simplify the synchronizing of input clock and data at rates of 622 Mb/s, the device provides an output clock at 622 MHz for clocking of the 4-bit parallel 622 Mb/s data from a pre-processor. This clocking is available in two forms. The first uses a delay locked loop (DLL) to automatically adjust the alignment of the incoming data relative to the on-chip VCO. The second bypasses the DLL and provides a fixed phase output clock requiring data to be available at the chip input within a fixed time window relative to this clock.

For further flexibility there is a timing scheme synchronized to the reference clock that does not use the clock output. This requires the data to be at the chip input in a defined time window relative to the clock. In this case the DLL circuitry is not required and can be powered down.

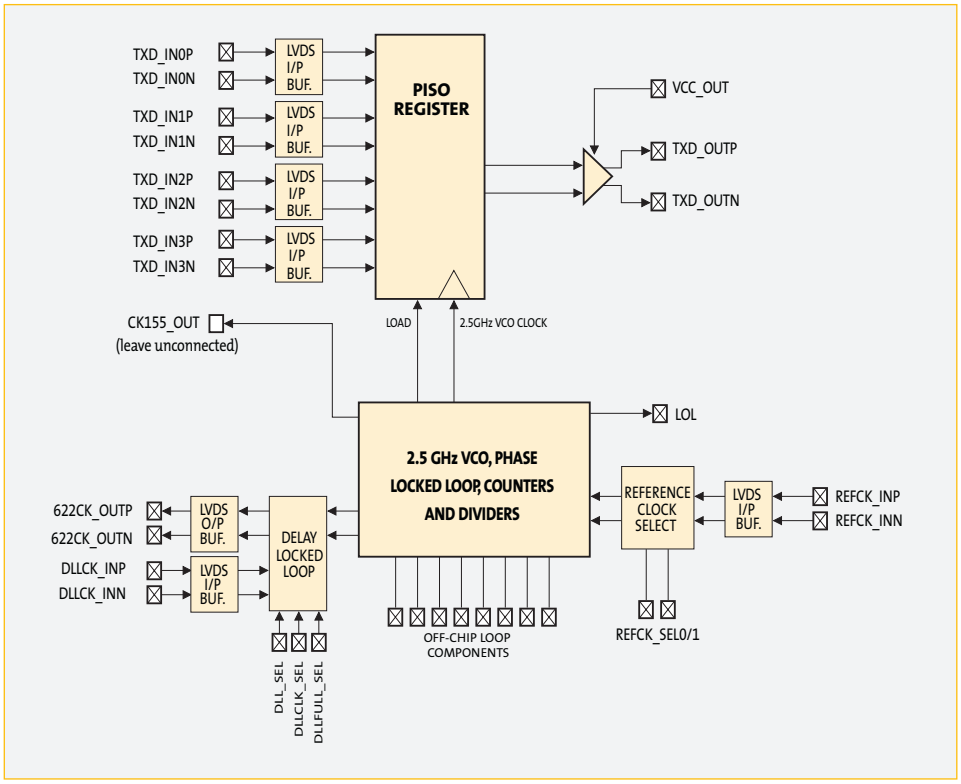

Figure 2: Functional Block Diagram

System Inputs

All 4-bit parallel data inputs on pins TXD_IN0P/N to TXD_IN3P/N are LVDS inputs and include 100 Ω differential on-chip termination resistors. An LVDS interface is also provided for the reference clock inputs on pins REFCK_INP/N, see Fig 2. This clock input can also be driven from LVPECL signals with the addition of suitable external resistors.

In the DLL data synchronization scheme, a 311 MHz or 622 MHz return clock (DLLCK_INP/N) is required from the interfacing device, aligned with the incoming data.

System Outputs

The serial 2.5 Gb/s data output on pins TXD_OUTP/N is a differential current mode logic (CML) output designed to drive 50 Ω loads. The two output pins are provided with a local supply rail (VCC_OUT) that should be connected to VCC for 3.3 V compatible output levels, or can be connected to a separate 5 V supply if 5 V compatible output levels are required. Data bits are mapped on to a serial output stream with DATA_0 transmitted before DATA_1 and so on. No framing manipulation is included within the device.

The clock output 622 CK_OUTP/N used for clocking of data from the pre-processor is an LVDS output running at 622 MHz. If the DLL select pin (DLL_SEL) is set, then the phase of this clock, relative to the derived input clock DLLCK_INP/N, is controlled by the delay locked loop. If the DLL select pin is not set then a clock with fixed phase is output.

Clocked DLL Data Synchronization

The delay locked loop (DLL) allows arbitrary propagation delay between the multiplexer and the data source. The write clock for the data source is supplied by the YA26 with a phase relative to the reference clock to ensure alignment of the received data with the on-chip clock. The loop is designed to continuously track slow movement, for example due to temperature, and to reacquire lock after a loop break.

The block diagram for the DLL operation is shown in Figure 3. In this scheme, a clock (622 CK_OUT) is provided by the YA26 to clock out the 4-bit wide data from the pre-processor. To provide correct alignment of the input clock and data relative to the on-chip clock, the DLL adjusts the phase of the 622 CK_OUT signal relative to the on-chip clock.

Three LVCMOS inputs control the DLL operating mode as shown in Table 1. Setting DLL_SEL to 0 activates the DLL bypass mode when the 622 MHz clock signal is available at 622 CK_OUT without any delay adjustment. In this mode, the user must ensure correct alignment of the data relative to the clock. Setting DLLCK_SEL to 0 allows the DLL phase detector to work with a 311 MHz returned clock signal. DLLFULL_SEL should normally be set to 1 for full DLL operation. If set to 0 this restricts the DLL to tracking only through +/-180 degrees. In this configuration, which should not normally be required, the DLL may not lock to a 311 MHz returned clock.

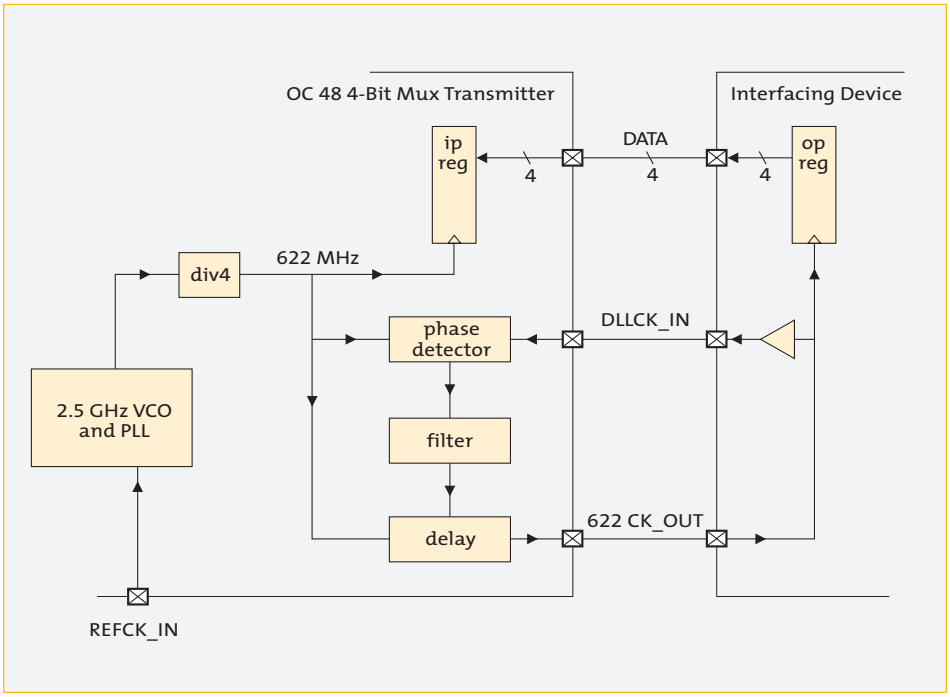

Figure 3: DLL Functional Block Diagram

DLL Mode Select Truth Table

DLL_SEL	DLLFULL_SEL	DLLCK_SEL	Effect
0	X	X	DLL bypassed
1	1	1	Full DLL at 622 MHz
1	1	0	Full DLL at 311 MHz
1	0	1	Limited DLL at 622 MHz
1	0	0	Not permitted

Table 1: DLL Mode Select Truth Table

X = Don't care

Clocked DLL Data Synchronization (continued)

A timing diagram showing the returned clock and the required data window is shown in Figure 4, with all timings taken at the pins of the YA26. From the timing diagram, it can be seen that the data valid period is 1100 ps centered 215 ps from the rising edge of the returned clock. This takes account of all of the possible contributions in uncertainty of the clock and data alignment. This includes random contributions such as jitter and DLL offset, etc., but also contributions due to the interface specification requirements have been included. The LVDS interface for which this scheme is specified, allows large skew and rise time differences, for example, the returned clock rise time may be 100 ps and the data rise time may be 400 ps. For more closely matched clock and data waveforms the required alignment may be relaxed.

The clocked DLL data synchronization option is enabled by setting the DLL selection pin (DLL_SEL) to a logic 1, see Table 1.

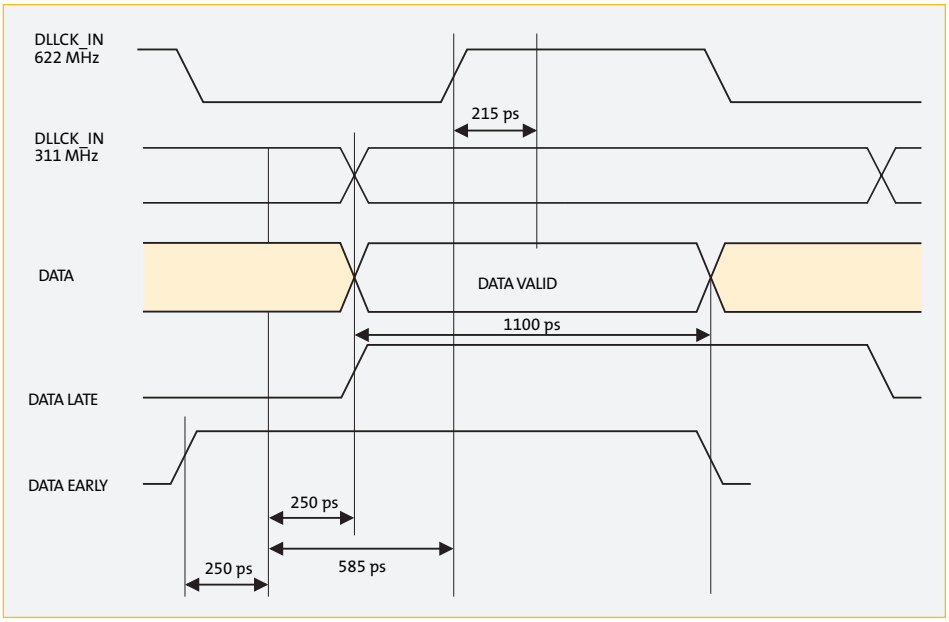

Figure 4: DLL Data Synchronization Timing

Fixed Clock Data Synchronization

In the alternative fixed clocked scheme, the delay locked loop is bypassed and a fixed phase 622 MHz clock is generated at the 622CK_OUT pins. The incoming data now has to meet the stated timing requirements relative to this clock. Figure 5 shows the fixed clock data synchronization timing diagram. For the same reason as the DLL scheme, the data valid window is quite large to account for all the possible contributions to uncertainty that arise with the potential variations allowed for the LVDS interface standard.

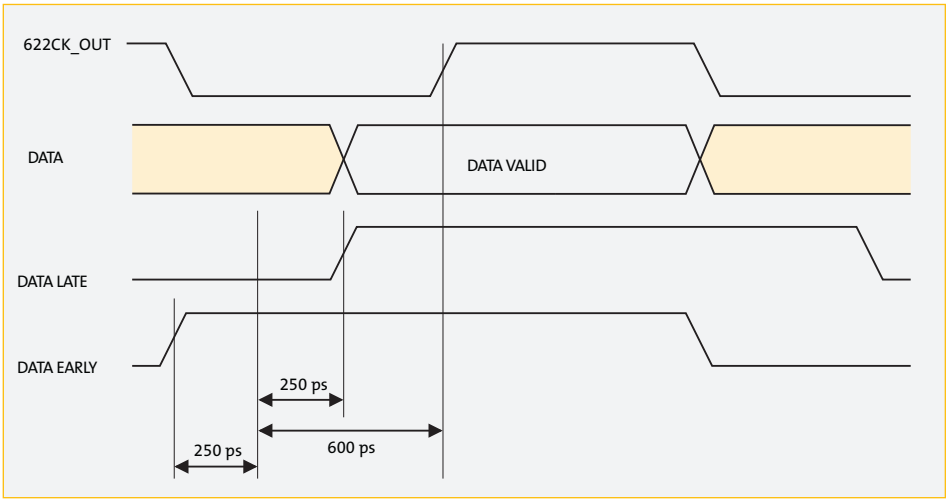

Figure 5: Fixed Clock Data Synchronization Timing

The fixed clock data synchronization option is enabled by setting the DLL selection pin (DLL_SEL) to a logic 0, see Table 1.

Reference Clock Data Synchronization

In this scheme no additional clock is required as the incoming data is timed relative to the master reference clock. When this scheme is used, the incoming 4-bit 622 Mb/s data will be clocked into the device relative to the reference clock on the REFCK_IN input. This scheme is intended to be used with a 155 MHz reference clock but can be applied for other clock frequencies. The timing diagram for this scheme is shown in Figure 6. The data valid window assumes that the clock and data have the same rise/fall time and amplitude, and there is no skew between data channels at the chip inputs, and no differential skew. If this is not the case, additional timing allowances must be made.

The use of this clocking scheme removes the need for the DLL function, which can be powered down with a typical power dissipation saving of 250 mW. To achieve this power down it is nessesary to leave the following pins unconnected: VCC_DLL, DLL_SEL, DLLCK_SEL and DLLFULL_SEL. It is important for reliable operation that all of these pins are left unconnected.

Reference Clock Selection

The YA26 device is designed to interface to a range of different devices and systems. For this reason the capability to use different reference clocks is included. The reference clock selection circuitry is controlled using two LVCMOS input pins REFCK_SEL0 and REFCK_SEL1, see Table 2.

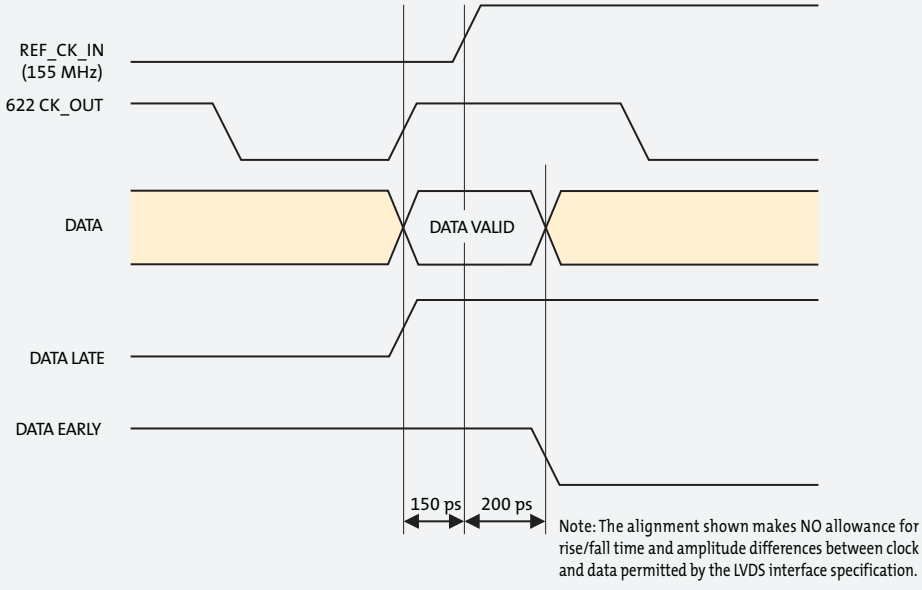

Figure 6: Reference Clock Data Synchronization Timing

Reference Clock Selection Truth Table

REFCK_SEL1	REFCK_SEL0	REF Freq
0	0	622 MHz
0	1	155 MHz
1	0	78 MHz
1	1	39 MHz

Table 2: Reference Clock Selection Truth Table

Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of, the device. Avoid operating the device outside the recommended operating conditions defined below.

Symbol	Parameter	Min	Max	Units
VCC	Supply voltage - any VCC_CORE/VCC_OUT pin	–0.7	6.0	V
VI lvpecl	LVPECL single ended input voltage	0	VCC +0.5	V
IO lvpecl	LVPECL output current		50	mA
IO cml	CML output current		50	mA
VI lvds	LVDS single ended input voltage	-0.5	VCC +0.5	V
IO lvds	LVDS output current		50	mA
VI lvcmos	LVCMOS single ended input voltage	-0.5	VCC +0.5	V
VO oc	Open Collector output voltage	-0.5	VCC +0.5	V
Tstg	Storage temperature	-65	150	˚C
Tj	Junction temperature	-40	120	˚C

Table 3: Absolute Maximum Ratings

Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Units
VCC	Supply voltage (all VCC's except VCC_OUT)	3.13	3.30	3.47	V
VCC_OUT	Supply voltage for data output	3.13	3.3 or 5.0	5.50	V
Vripple	VCC supply voltage noise and ripple			15	mVrms
V ih	Input voltage high, LVCMOS input	2.0		VCC	V
V il	Input volt low, LVCMOS input	0		0.8	V
VIHIvpecl	LVPECL i/p HIGH voltage	VCC -1.165		VCC -0.88	V
VILIvpecl	LVPECL i/p LOW voltage	VCC -2.1		VCC -1.475	V
VMAX oc	Open Collector Pull-up Voltage			VCC	V
Tj	Junction temperature	-40		125	°C
Tamb	Ambient temperature	-40		85	°C

Table 4: Recommended Operating Conditions

All voltages are with respect to GND (0 V) unless otherwise stated. The specified VCC levels include all supply rail variations except ripple and noise which are specified as Vripple.

DC Electrical Characteristics

Symbol	Parameter	Min	Typical	Max	Units
IIHlvpecl	LVPECL i/p high current, at VIH = VCC -0.88			100	µA
IILlvpecl	LVPECL i/p low current, at VIL = VCC -1.81			50	µA
VOHpecl	LVPECL output HIGH voltage	VCC -1.065		VCC -0.88	V
VOLpecl	LVPECL output LOW voltage	VCC -1.81		VCC -1.62	V
VOHcml	Output HIGH voltage, high Z load	VCC -0.01	VCC	VCC +0.01	V
VOLcml	Output LOW voltage, high Z load	VCC -1.1	VCC -0.90	VCC -0.70	V
VOHcml	Output HIGH voltage, 50 Ω load	VCC -0.01	VCC	VCC +0.01	V
VOLcml	Output LOW voltage, 50 Ω load	VCC -0.55	VCC -0.45	VCC -0.35	V
I ih	Input current high, LVCMOS input			500	µA
I il	Input current low, LVCMOS input			-100	µA
VOL oc	Open Collector O/P Low voltage at IOL = 1 mA			0.4	V
IOH oc	Open Collector O/P High leakage current at VOH = VCC			1	µA
IOL oc	Open Collector O/P Low Current			5	mA
Icc max	Current drawn from the VCC supply (fully powered)		315	398	mA
PD max	Device power dissipation (fully powered)		1.05	1.38	W
Icc	Current drawn from the VCC supply (DLL unconnected)		233	300	mA
PD	Device power dissipation (DLL unconnected)		0.77	1.04	W

Table 5: DC Electrical Characteristics

AC Characteristics

Symbol	Parameter	Min	Typical	Max	Units
	2.5 GHz VCO loop acquisition time			10	ms
	Jitter generated at TXD_OUTP/N outputs, Bandwidth 12 kHz to 20 MHz, max ref clock jitter + 1 ps rms			0.0075	UI rms
	Jitter bandwidth	0.7	1.5	2.5	MHz
	Peak Jitter gain	0.1		0.3	dB
	LOL asserted pulse width	1		10	µs
TRpecl	LVPECL test output rise time	0.25		1.5	ns
TFpecl	LVPECL test output fall time	0.25		1.5	ns
CK155msr	CK155_OUT mark to space ratio	45		55	%
CKlvpecl_msr	REFCK_IN (LVPECL) mark to space ratio	45		55	%
TRcml	CML output rise time	50		125	ps
TFcml	CML output fall time	50		125	ps

Table 6: AC Characteristics

These max and min DC and AC Characteristics apply over the recommended operating conditions, output load 50 Ω.
All typical values are quoted at 3.3 V and 25° C.

LVDS Input/output DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
VI	Input Voltage Range, V ia or V ib	|V gpd|<50 mV	825	1575	mV
Vidth	Input differential threshold	|V gpd|<50 mV	-100	+100	mV
Vhyst	Input differential hysteresis Vidthh - Vidthl		25		mV
Rin	Receiver differential input impedance		80	120	Ω
Voh	Output voltage high, Voa or Vob	R load = 100 Ω		1475	mV
Vol	Output voltage low, Voa or Vob	R load = 100 Ω	925		mV
|Vod|	Output differential voltage	R load = 100 Ω	250	400	mV
Vos	Output offset voltage	R load = 100 Ω	1125	1275	mV
Ro	Output impedance, single ended	V cm = 1.0 V and 1.4 V	40	140	Ω
ΔRo	Ro mismatch between A and B	V cm = 1.0 V and 1.4 V		10	%
|ΔVod|	Change in |Vod| between '0' and '1'	R load = 100 Ω		25	mV
ΔVos	Change in Vos between '0' and '1'	R load = 100 Ω		25	mV
Isa, Isb	Output current	Driver shorted to ground		40	mA
Isab	Output current	Driver shorted to ground		12	mA

Table 7: LVDS Input / Output DC Electrical Characteristics

LVDS Input/output AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
t fall	V od fall time, 20% to 80%		100	400	ps
t risel	V od rise time, 20% to 80%		100	400	ps
t skew1	Differential skew	Any differential pair on package		50	ps
t skew2	Channel to Channel skew	Any two differential signals on package		50	ps
ck lvds_msr	REFCK_IN LVDS mark to space ratio		45	55	%
Clock	Clock signal duty cycle	622 MHz	45	55	%

Table 8: LVDS Input / Output AC Characteristics

Note Signal naming and definitions are in accordance with IEEE Std 1596.3-1996 – IEE standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI).

Typical Operating Characteristics

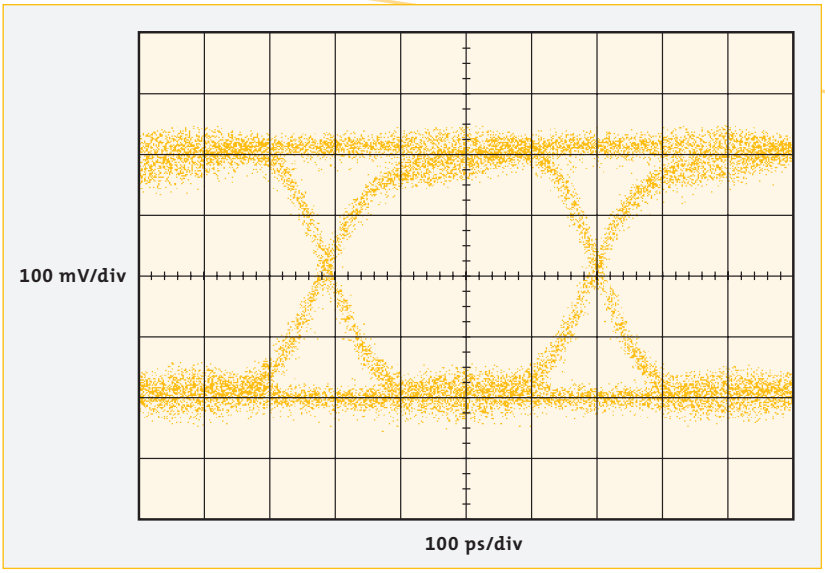

Figure 7 - Data Eye Diagram

Additional Design and Applications Information

The application diagram in Figure 8 shows the configuration for using the YA26 in a 2.5 Gb/s OC-48/ STM-16 system with full implementation of the delay lock loop. This shows all required external components, including supply decoupling capacitors.

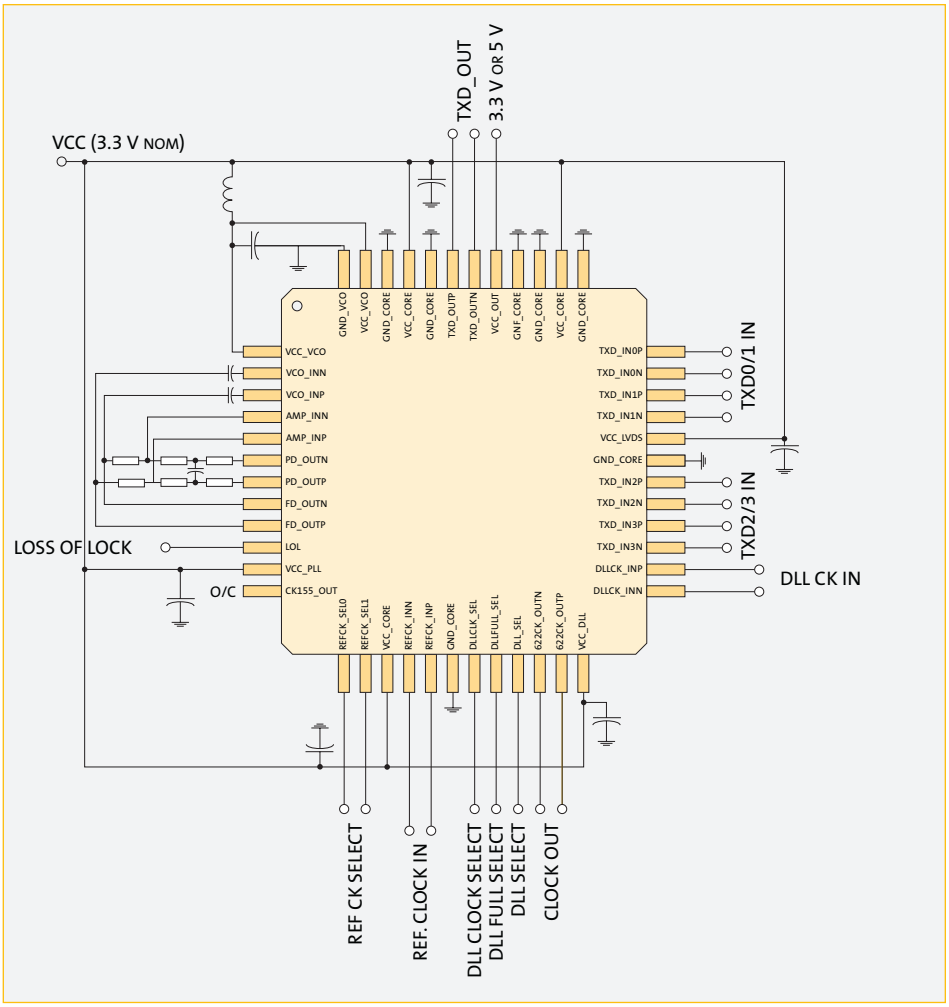

Figure 8: Typical Application cicuit

Loss of Lock Output Characteristics

A loss of lock signal is generated from the raw frequency detector outputs of the VCO loop and is asserted each time a cycle slip is observed by a frequency detector. It is an open collector output with internal circuitry to pulse stretch the signal. The pulse width of the loss of lock signal is between 1 and 10 µs.

Power Supply Noise

Although the device has been designed to maximize supply noise rejection, it is recommended that an LC filter network is used, shown in Figure 9, between the supply and pins 1 and 47 VCC_VCO. Using this configuration, the device will function within the jitter specification with a maximum supply noise of 15 mVrms, over a frequency range from 6 kHz to 2 MHz, on the supply. The effective series resistance of the network must not exceed 2.5 Ω.

PLL Performance

The internally generated 2.5 GHz VCO clock signal is divided down and phase locked to the rising edge of the REFCK_INP input.

The YA26 is designed for regenerator and receiver applications. Its integrated PLL is a fully differential design with loop bandwidth set by an external network. The configuration of this network is shown in Figure 10 with typical component values listed in Table 9.

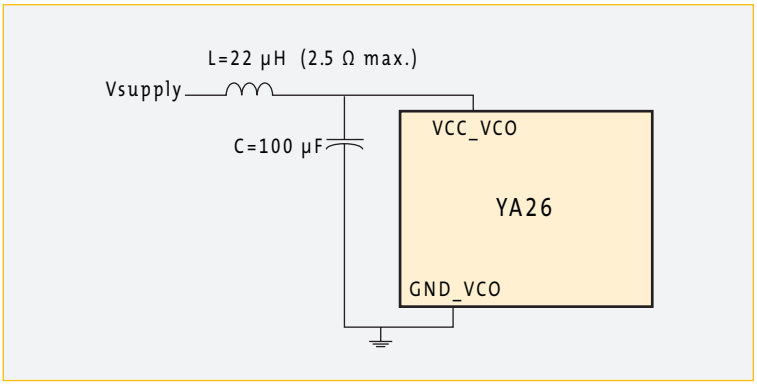

Figure 9: Supply filter circuit

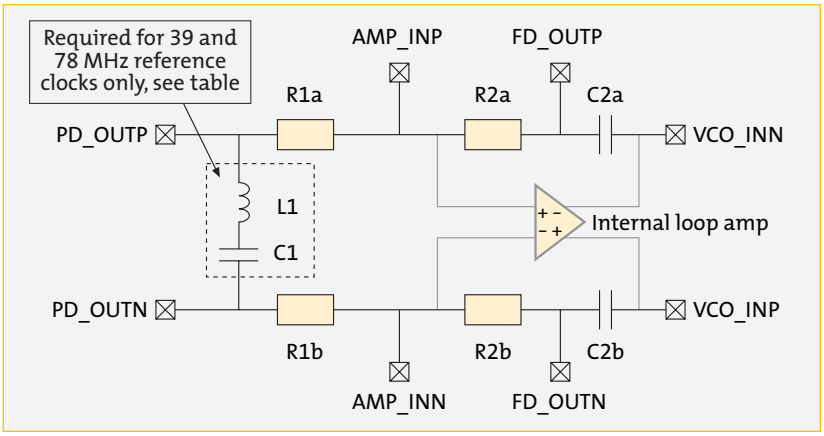

Figure 10: Loop filter configuration

All components should be surface mount devices of 0603 size, with ±2% tolerance for resistors and ±5% tolerance for capacitors. Table 9 defines nominal values for the loop filter components for different reference clock frequencies. Alternative values can be determined by using the standard PLL performance equations.

Ref. Freq (MHz)	R1a,b (KΩ)	R2a,b (KΩ)	C2a,b (nF)	C1 (pF)	L 1 (uH)
39	3.0	4.7	2.2	5.0	3.3
78	6.2	4.7	2.2	4.2	1.0
155	12	4.7	2.2	–	–
622	12	4.7	2.2	–	–

Table 9: Typical Loop filter component values

CML Interface

As with the other members of the family, the high-speed serial output of the YA26 is configured as a fully differential CML signal pair as shown in Figure 11. Although the YA26 is designed to interface with the Nortel Networks YA08 Laser Diode Driver by providing a nominal peak differential output voltage of 400 mV, the outputs are such that it is possible to drive a wide range of similar CML inputs. If you need to drive a single-ended input, you must AC couple the unused output to a 50 Ω termination. If the receiving device with CML inputs is a 5 V part, then the separate output supply (VCC_OUT) can be connected to a 5 V rail.

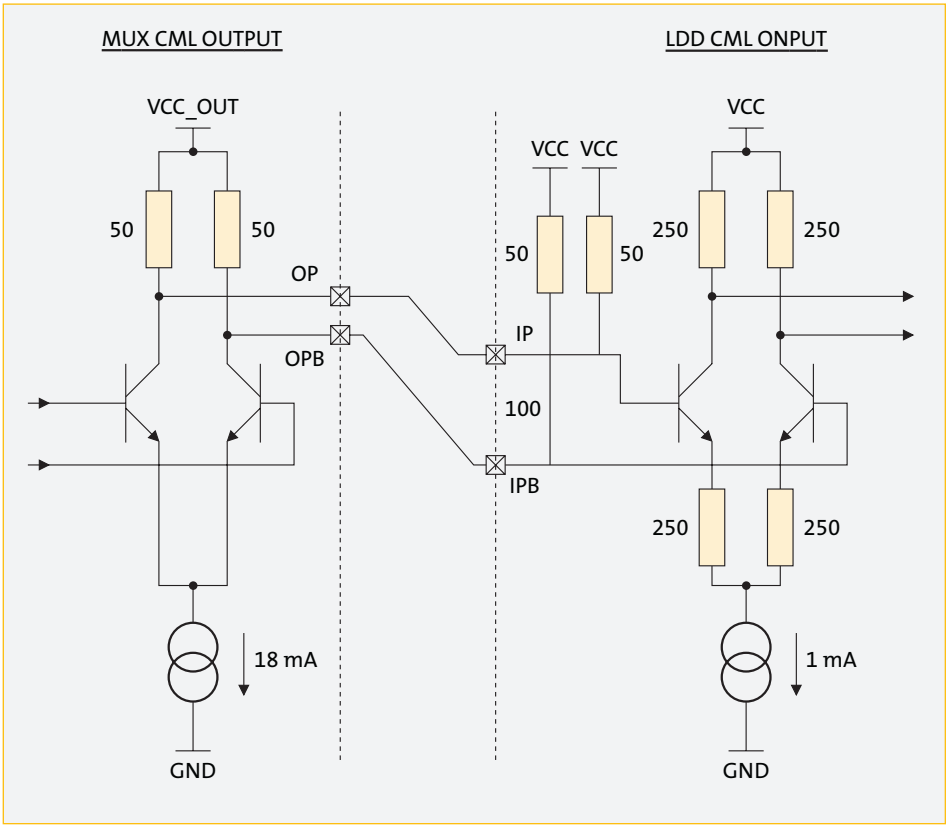

Figure 11: CML output/input interface

Pin Assignment

Pin No.	Pin Name	Type	Description	Function
1	VCC_VCO	P	Supply	+3.3 V supply rail for VCO
2	VCO_INN	I	Analog	Voltage controlled oscillator -ve input
3	VCO_INP	I	Analog	Voltage controlled oscillator +ve input
4	AMP_INN	I	Analog	Loop amplifier -ve input
5	AMP_INP	I	Analog	Loop amplifier +ve input
6	PD_OUTN	O	Analog	Loop phase detector -ve output
7	PD_OUTP	O	Analog	Loop phase detector +ve output
8	FD_OUTN	O	Analog	Loop frequency detector -ve output
9	FD_OUTP	O	Analog	Loop frequency detector +ve output
10	LOL	O	Open Collector	PLL loss of lock output
11	VCC_PLL	P	Supply	+3.3 V supply rail for PLL
12	CK155_OUT	O	PECL 100k	VCO divided clock test output (leave unconnected)
13	REFCK_SEL0	I	LVCMOS	Reference clock frequency select bit 0
14	REFCK_SEL1	I	LVCMOS	Reference clock frequency select bit 1
15, 38, 45	VCC_CORE	P	Supply	+3.3 V supply rail
16	REFCK_INN	I	LVDS	Reference clock -ve input
17	REFCK_INP	I	LVDS	Reference clock +ve input
18, 31, 37, 39, 40, 44, 46	GND_CORE	P	Supply	0 V supply rail
19	DLLCK_SEL	I	LVCMOS	DLL 622/311 MHz clock select input
20	DLLFULL_SEL	I	LVCMOS	DLL partial/full select input
21	DLL_SEL	I	LVCMOS	DLL select input
22	622 CK_OUTN	O	LVDS	622 MHz Output clock for data clocking -ve
23	622 CK_OUTP	O	LVDS	622 MHz Output clock for data clocking +ve
24	VCC_DLL	P	Supply	+3.3 V supply rail for DLL
25	DLLCK_INN	I	LVDS	622/311 MHz return clock for DLL -ve input
26	DLLCK_INP	I	LVDS	622/311 MHz return clock for DLL +ve input
27	TXD_IN3N	I	LVDS	Parallel data differential -ve input
28	TXD_IN3P	I	LVDS	Parallel data differential +ve input
29	TXD_IN2N	I	LVDS	Parallel data differential -ve input
30	TXD_IN2P	I	LVDS	Parallel data differential +ve input

Pin Assignment (continued)

Pin No.	Pin Name	Type	Description	Function
32	VCC_LVDS	P	Supply	+3.3 V supply rail for input LVDS buffers
33	TXD_IN1N	I	LVDS	Parallel data differential -ve input
34	TXD_IN1P	I	LVDS	Parallel data differential +ve input
35	TXD_IN0N	I	LVDS	Parallel data differential -ve input
36	TXD_IN0P	I	LVDS	Parallel data differential +ve input
41	VCC_OUT	P	Supply	+3.3 / 5.0 V supply rail for CML data output
42	TXD_OUTN	O	CML	Serial data differential -ve output
43	TXD_OUTP	O	CML	Serial data differential +ve output
47	VCC_VCO	P	Supply	+3.3 V supply rail for VCO
48	GND_VCO	P	Supply	0 V supply rail for VCO

Package Pin Configuration

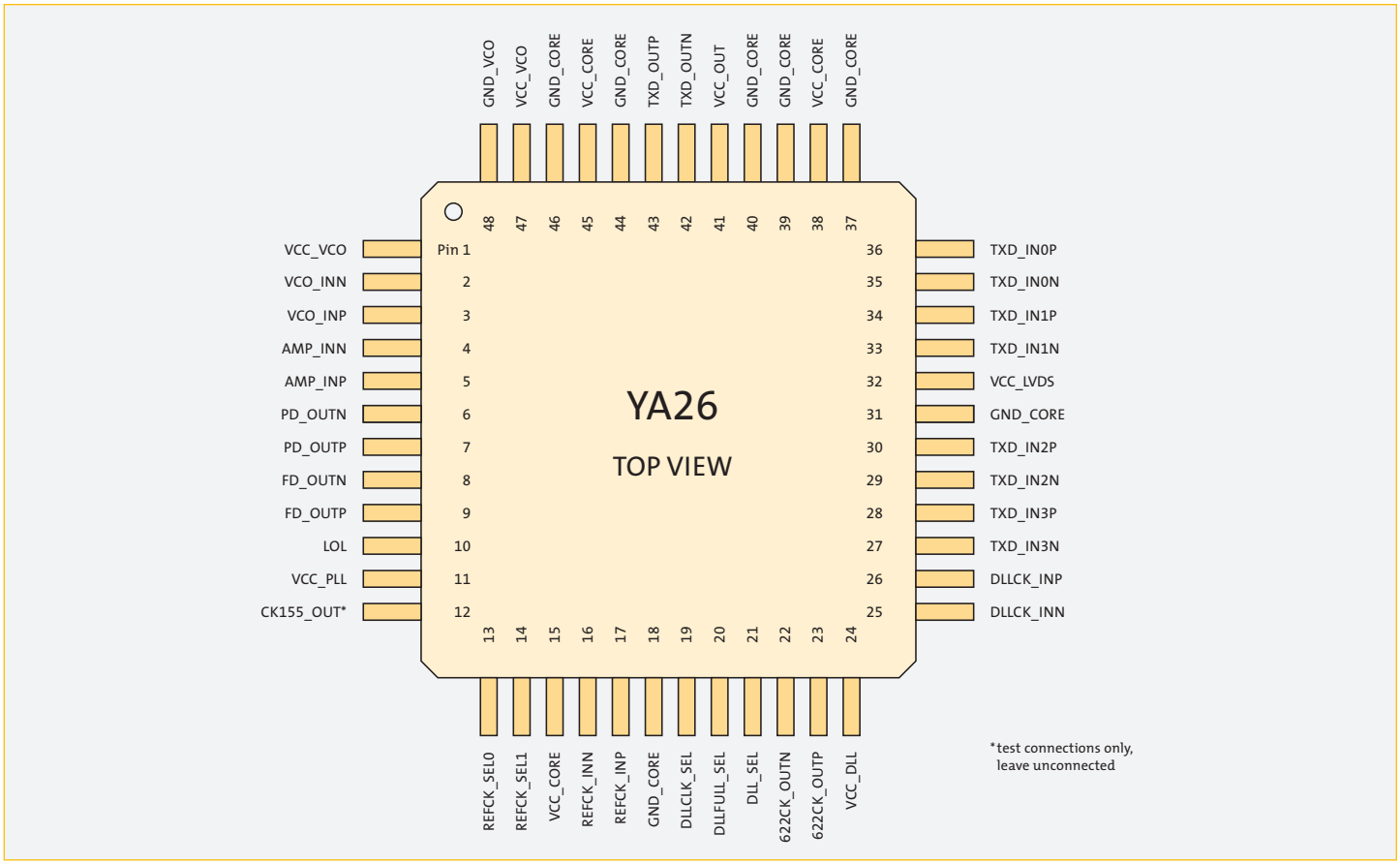

Figure 12: 48-lead LQFP

Package Outline Drawing and Dimensions

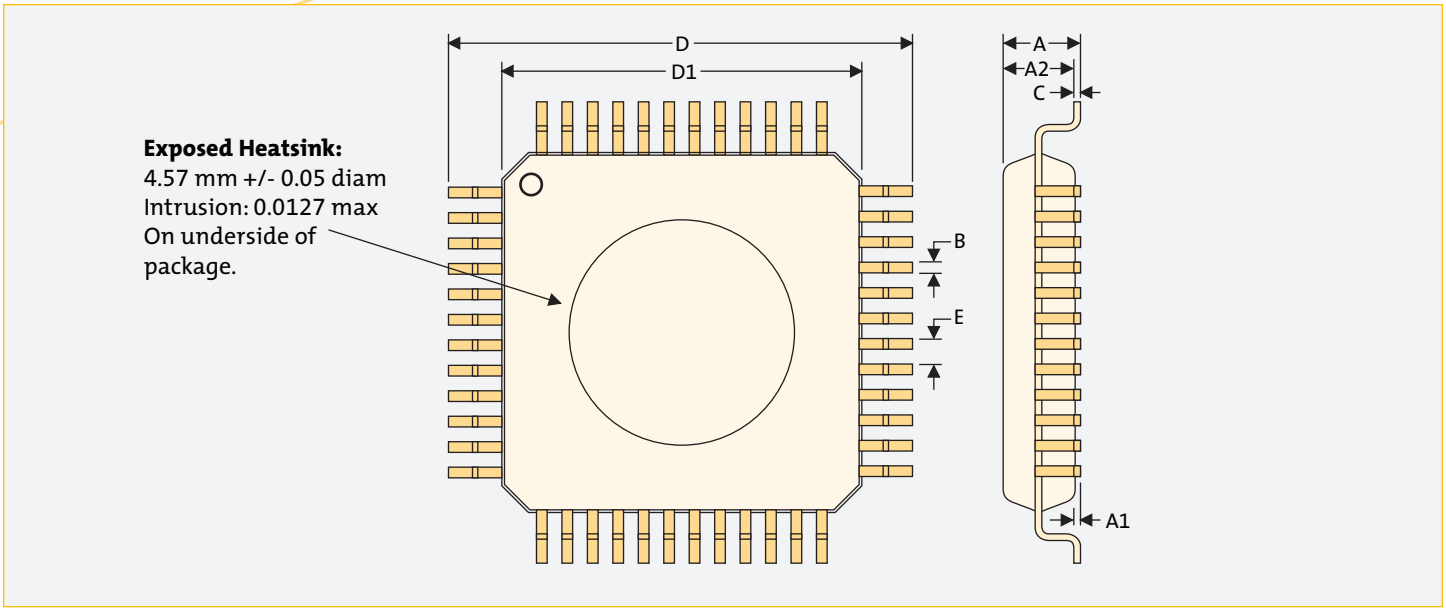

Figure 13: Package Outline

Dimension	Min (mm)	Nom (mm)	Max (mm)
Lead Pitch (E)		0.50	
Body Size (D1)		7.00	
Component Tip-to-Tip (D)		9.00	
Component Height (A)			1.60
Component Standoff (A1)	0.05		0.15
Body Thickness (A2)	1.35	1.40	1.45
Lead Width, plated (B)	0.17	0.22	0.27
Lead Thickness, plated (C)	0.09		0.20

Notes:

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