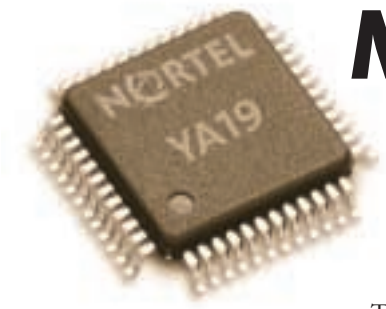
YA19

2.5 Gb/s 16:1 Multiplexer and ClockGenerator



Data Sheet

Features

Meets or exceeds all relevant ANSI, ITU and Bellcore specifications

LVPECL 100 k inputs accept signals of 155 Mb/s data rate

Differential data outputs provide CML signals at 2.5 Gb/s with 3.3 V or 5 V interface capability

Internally synthesized 2.5 GHz clock removes the need for external high speed reference

Single 3.3 V supply for simplified system integration

Typical power dissipation of less than 1 W

Industry standard LQFP package or high-density flip-chip for module applications

Manufactured using the high performance, high yield bipolar process

The Nortel Networks YA19 Multiplexer and Clock Generator multiplexes 16-bit parallel input data at 155 Mb/s into a single, serial output stream at 2.5 Gb/s. An on-chip phase locked loop generates a 2.5 GHz clock from either the incoming 155MHz data clock or from an external stable reference. The CML outputs of the YA19 are configured to interface directly with the Nortel Networks YA08 Laser Diode Driver.

The YA19 is part of our family of 2.5 Gb/s components, which provides for power and chip-count savings that translate into better utilization of board real-estate and ultimately cost savings to the designer of fibre-based datacom or telecom solutions.

The device is fabricated using a high yield, silicon bipolar process. Each product is available in industry-standard packaging or as flip chip, for high density modules.

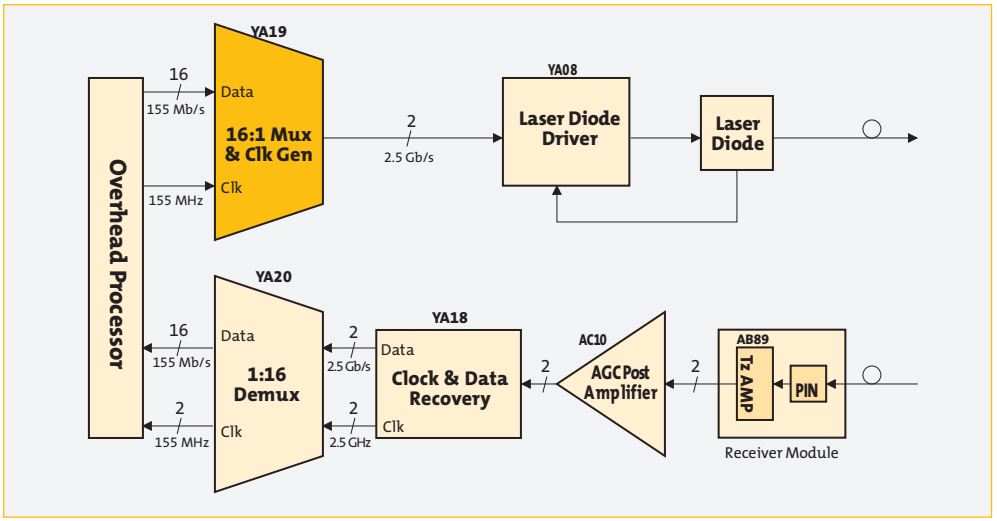


Figure 1: System Block Diagram

NORTEL NETWORKS™

Functional Description

The YA19 multiplexes 16-bit parallel input data at 155 Mb/s into a single serial output data stream at 2.5 Gb/s. For normal operation the device takes the input data clock at 155 MHz and generates a synchronous 2.5 GHz clock using an on-chip PLL.

The device requires a single 3.3 V (±5%) power supply. The CML data outputs can deliver levels suitable for input to a 3.3 V or 5 V device. In the latter case a +5 V (±10%) supply is also required.

System Inputs

The 16-bit data bus on pins TXD_IN0-15 uses single-ended 100 k LVPECL inputs while the 155 MHz clock on pins CK155_INP/N uses similar differential inputs. These inputs do not include on-chip termination.

The 16 data inputs are clocked into the device on the falling edge of CK155_INP during the time window when the transmit bus is guaranteed to be stable.

System Outputs

The multiplexed data is output at 2.5 Gb/s on pins TXD_OUTP/N which are differential CML designed to drive 50 ohm. These output pins are provided with a local supply rail connected to pin VCC_OUT, which can be connected to VCC for 3.3 V compatible output levels, or can be connected to a separate 5 V supply if 5 V compatible output levels are required. Data bits are mapped onto the serial output stream in conventional order, with bit0 transmitted before bit1, etc.

Loss of Lock (LOL) Output

A Loss Of Lock output, LOL, is generated from the raw frequency detector output of the VCO. It is asserted each time a cycle slip is observed by the frequency detector. LOL is a single ended open-collector output which requires external pulse stretching circuitry and is LOW if either loop is out of lock.

Test Inputs and Outputs

To enable testing at low speeds, various test inputs are made available. These inputs, which are not internally terminated, bypass the on-chip VCO. Under normal operation test input TEST_R must be connected to GND and inputs TEST_DIS and TEST_CK connected to VCC.

A divider is included to divide the 2.5 GHz VCO output down to 155 MHz, which is delivered as a single-ended PECL output at pin CK155_OUT. Under normal operation this output should be left unconnected.

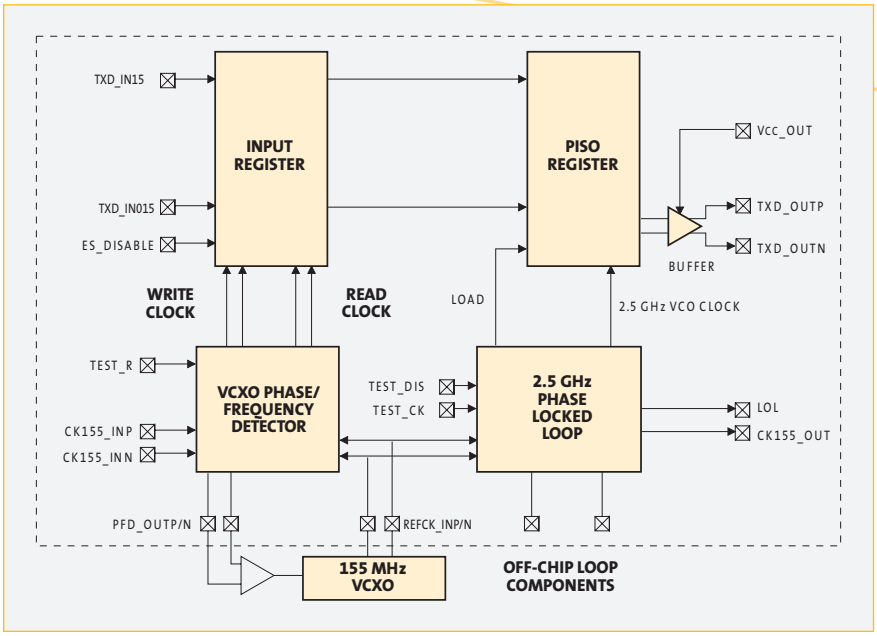


Figure 2: Functional Block Diagram

Absolute Maximum Ratings

These are stress ratings only: Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of, the device. Avoid operating the device outside the recommended operating conditions defined below.

Symbol	Parameter	Min	Max	Unit
Vcc	Supply voltage – any Vcc/Vcc_OUT pin	-1.0	6.0	V
VIpecl	LVPECL single ended input voltage	0	Vcc+0.5	V
Io	Output current – LVPECL or CML		-50	mA
Vooc	Open collector output voltage - LOL output	-0.5	Vcc+0.5	V
Tstg	Storage temperature	-65	135	˚C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Vcc	Supply voltage – any Vcc pin	3.14	3.3	3.46	V
Vcc_OUT	Supply voltage for data outputs	3.14		5.50	V
Vripple	Vcc supply noise and ripple	-25		25	mV
VIHPECL	LVPECL INPUT HIGH VOLTAGE	Vcc-1.165		Vcc-0.88	V
VILPECL	LVPECL INPUT LOW VOLTAGE	Vcc-2.100		Vcc-1.475	V
	Maximum input jitter on CK155_INP/N input (1)			0.1	UI rms
Tamb	Ambient operating temperature	-40		85	˚C

DC Electrical Characteristics

Over recommended operating conditions, output load 50 ohm, VX =VCC_OUT for CML outputs.

Symbol	Parameter	Min	Typ	Max	Unit
IIHpecl	Input HIGH current - PECL input (VIH=VCC-0.88V)			100	µA
IILpecl	Input LOW current - PECL input (VIL=VCC-1.81V)			50	µA
VOdiff	CML differential output voltage (peak value)	375	400	425	mV
VOHcml	CML output HIGH voltage, referenced to VCC_OUT	VX-0.01	VX	VX+0.01	V
VOLcml	CML output LOW voltage, referenced to VCC_OUT	VX-0.42	VX-0.40	VX-0.38	
VOHpecl	Output HIGH voltage - PECL output	VCC -1.065		VCC -0.88	V
VOLpecl	Output LOW voltage - PECL output	VCC -1.81		VCC - 1.62	V
VOHLOL	Output HIGH voltage - Loss of Lock output	VCC -0.2		VCC	V
VOLLOL	Output LOW voltage - Loss of Lock output			VCC - 1.1	V
Icc	Supply Current (VCC and VCC_OUT)		250	375	mA
Pd	Device power dissipation		0.825	1.3	W

AC Characteristics

Over recommended operating conditions, output load 50 ohm.

Symbol	Parameter	Min	Max	Unit
	2.5 GHz loop acquisition time		10	ms
	155 Mhz VCXO loop acquisition time		10	s
	Jitter generated at TXD_OUTP/N outputs, bandwidth 12 kHz to 20 MHz		0.0075	UI rms
	Jitter gain from CK155_INP/N to TXD_OUTP/N at any frequency		0.1	dB
TRcml	Output rise time - CML output	50	125	ps
TFcml	Output fall time - CML output	50	125	ps
TSUdi	Data input SETUP time wrt CK155_INP falling edge		1.0	ns
THdi	Data input HOLD time wrt CK155_INP falling edge		1.0	ns

Design Procedure and Applications Information

The application diagram in Figure 3 shows the configuration for usage of the YA19 in a 2.5 Gb/s OC-48/ STM-16 system. This shows required external components, including supply decoupling capacitors but not including the Loss of Lock circuitry defined in Figure 4.

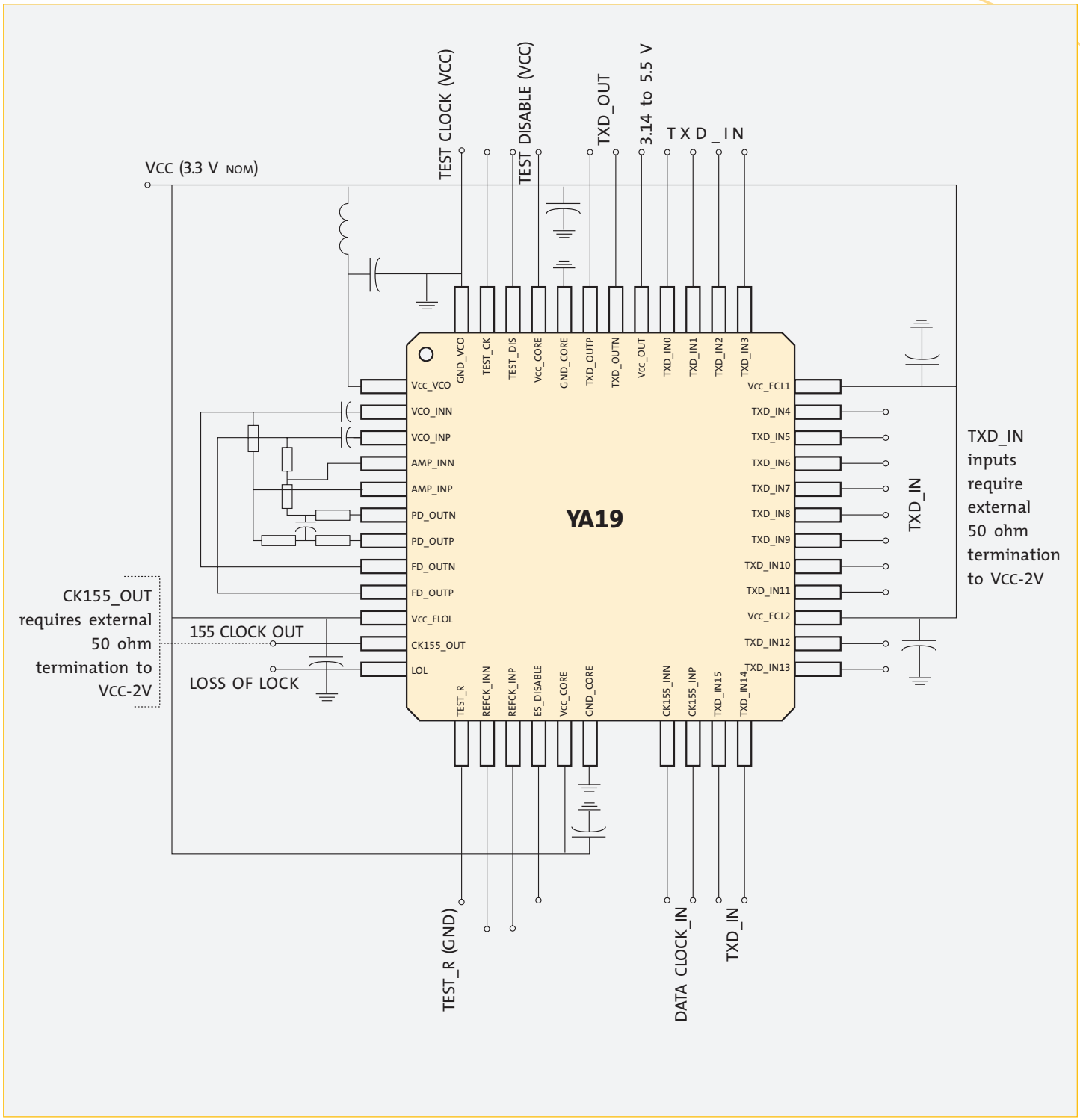


Figure 3: Typical Application Configuration

Loss of Lock Output Characteristics

A loss of lock signal is generated from the raw frequency detector output of the VCO loop and is asserted each time a cycle slip is observed by a frequency detector. It is a single ended CML output which requires the external circuitry shown in Figure 4 to pulse stretch the signal and generate an open collector output.

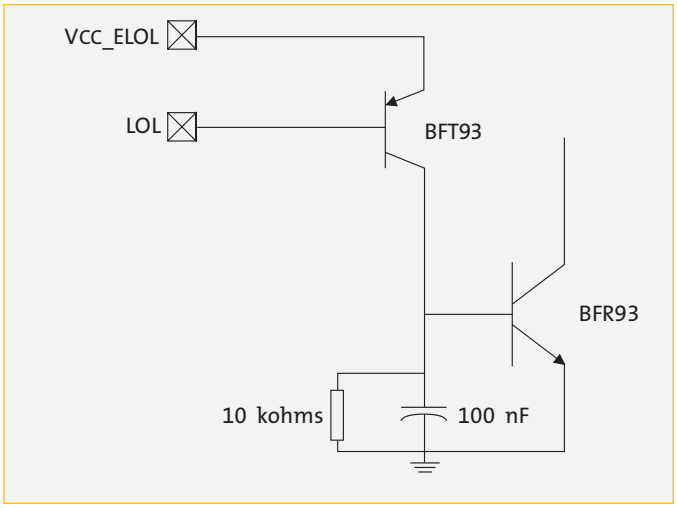


Figure 4: LOL External Pulse Stretching Circuit

Power Supply Noise

Although the device has been designed to maximize supply noise rejection, it is recommended that you use an LC filter network, shown in Figure 5, between the supply and pin 35 VCC_VCO. Using this configuration, the device will function within the jitter specification with a maximum supply noise of 50 mVpp, over a frequency range from 6 kHz to 2 MHz, on the supply. The effective series resistance of the network must not exceed 2.5 ohm.

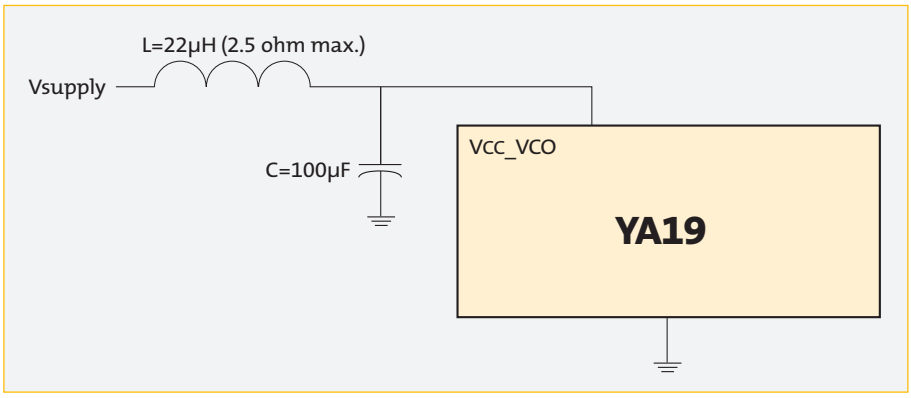


Figure 5: Supply Filter Circuit

PLL Performance

The internally generated 2.5 GHz VCO clock signal is divided by 16 and then phase locked to the falling edge of the REFCK_INP input. The 2.5 Gb/s PLL is phase locked to the falling edge of C455 INP.

For the device to meet Bellcore specifications, it is necessary for the data clock to achieve phase noise of better than -90 dBc/Hz at a frequency offset of 1 kHz.

Setting the Loop Filter

The YA19 is designed for regenerator and receiver applications. Its integrated PLL is a fully differential design with loop bandwidth set by a pair of identical external networks. The configuration of these networks is shown in Figure 6 with typical component values listed in Table 1. These components should be surface mount parts of 0603 size, with ±2% tolerance for resistors up to 2 Mohm, ±5% tolerance for capacitors up to 10 nF, and ±10% tolerance for capacitors from 10 nF to 100 nF. The transistors are BFT93 or equivalent.

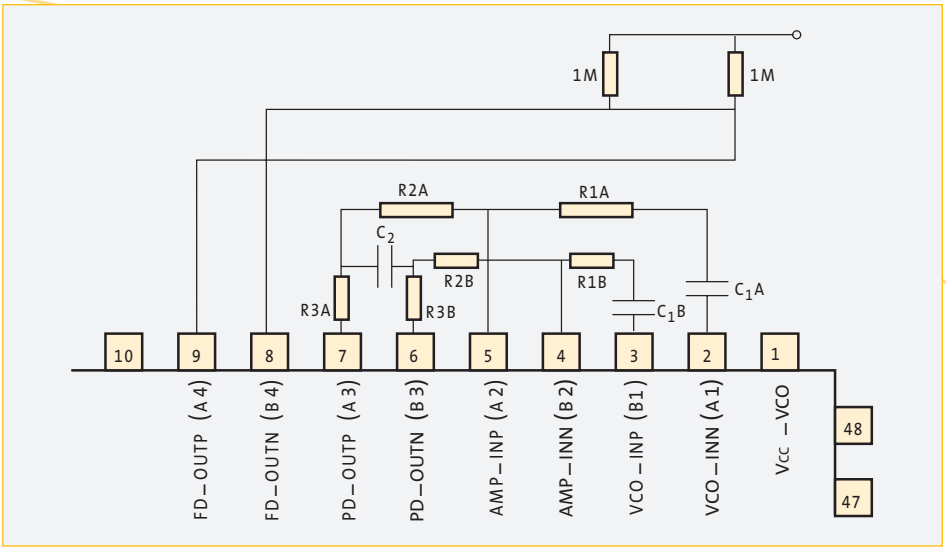


Figure 6: Loop Filter Configuration

The table below defines a set of values for the loop filter components for a given bandwidth and damping factor. Alternative values can be determined by using the standard PLL performance equations.

Loop bandwidth	Damping factor	C_1	C_2	R1	R2	R3
2000 kHz	5	1 nF	2 pF	8.2 Kohm	3.3 Kohm	3.3 Kohm

Table 1: Typical Loop Filter Component Values

Output Interfacing

As with other members of the OC-48/STM-16 electro-optic interface family, the high speed (2.5 Gb/s) output of the YA19 is configured as a fully differential CML signal pair as shown in Figure 7.

Although the YA19 is specifically designed to interface with the Nortel Networks YA08 Laser Diode Driver by providing a nominal peak differential output voltage of 400 mV, the outputs are such that it is possible to drive a wide range of similar CML inputs. If you need to drive a single-ended input, you must AC couple the unused output to a 50 ohm termination.

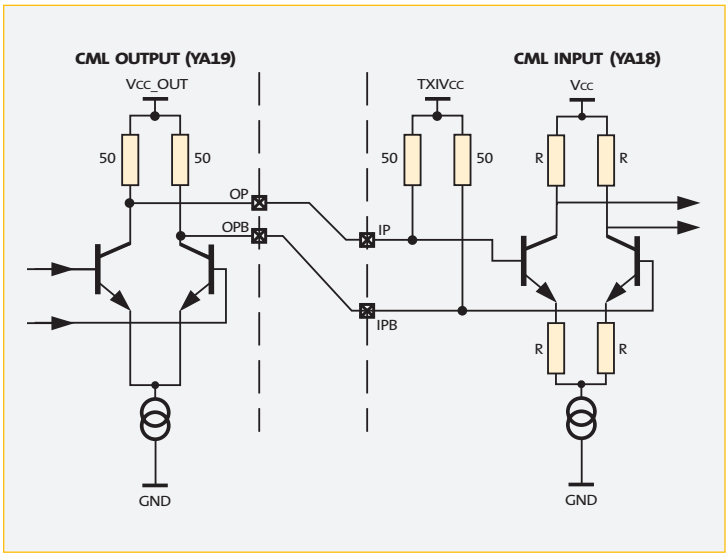


Figure 7: CML Input and Output Configurations

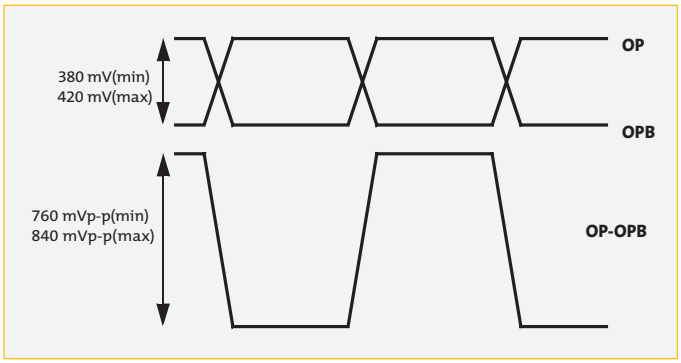


Figure 8: CML Output Differential Voltage Levels

Pin Assignment

Pin No	Symbol	Type	Description	Function
1	VCC_VCO	P		3.3 V supply rail for VCO
2	VCO_INN	I	Analog	Loop filter pin A1
3	VCO_INP	I	Analog	Loop filter pin B1
4	AMP_INN	I	Analog	Loop filter pin B2
5	AMP_INP	I	Analog	Loop filter pin A2
6	PD_OUTN	O	Analog	Loop filter pin B3
7	PD_OUTP	O	Analog	Loop filter pin A3
8	FD_OUTN	O	Analog	Loop filter pin B4
9	FD_OUTP	O	Analog	Loop filter pin A4
10	VCC_ELOL	P		3.3 V supply rail for PECL output and LOL
11	CK155_OUT	O	PECL 100 k	VCO divided clock output
12	LOL	O	CML	PLL loss of lock output
13	TEST_R	I	LVCMOS	Test reset input (connect to GND for normal operation)
14	REFCK_INN	I	PECL 100 k	155 MHz reference clock negative differential input
15	REFCK_INP	I	PECL 100 k	155 MHz reference clock positive differential input
17, 45	VCC_CORE	P		3.3 V supply rail for digital core
18, 44	GND_CORE	P		Supply ground for digital core
21	CK155_INN	I	PECL 100 k	155 MHz data clock negative differential input
22	CK155_INP	I	PECL 100 k	155 MHz data clock positive differential input
23, 24, 25, 26, 28, 29, 30, 31, 32, 33, 34, 35, 37, 38, 39, 40	TXD_IN15 to TXD_IN0	I	PECL 100 k	Parallel data input, bit 15, LSB to bit 0, MSB

Pin Assignment (continued)

Pin No	Symbol	Type	Description	Function
27	VCC_ECL2	P		3.3 V supply pin for PECL inputs <8:15>
36	VCC_ECL1	P		3.3 V supply pin for PECL inputs <0:7>
41	VCC_OUT	P		3.3 V or 5 V supply pin for CML data output
42	TXD_OUTN	O	CML	Serial data negative differential output
43	TXD_OUTP	O	CML	Serial data positive differential output
46	TEST_DIS	I	LVCMOS	Test disable input (connect to VCC for normal operation)
47	TEST_CK	I	PECL 100 k	Test clock input (connect to VCC for normal operation)
48	GND_VCO	P		Supply ground for VCO

Package Pin Configuration

The device is packaged in a 48-lead plastic low-profile quad flat pack (LQFP). To achieve the required thermal resistance, the package contains a heat slug which must be soldered directly to the circuit board.

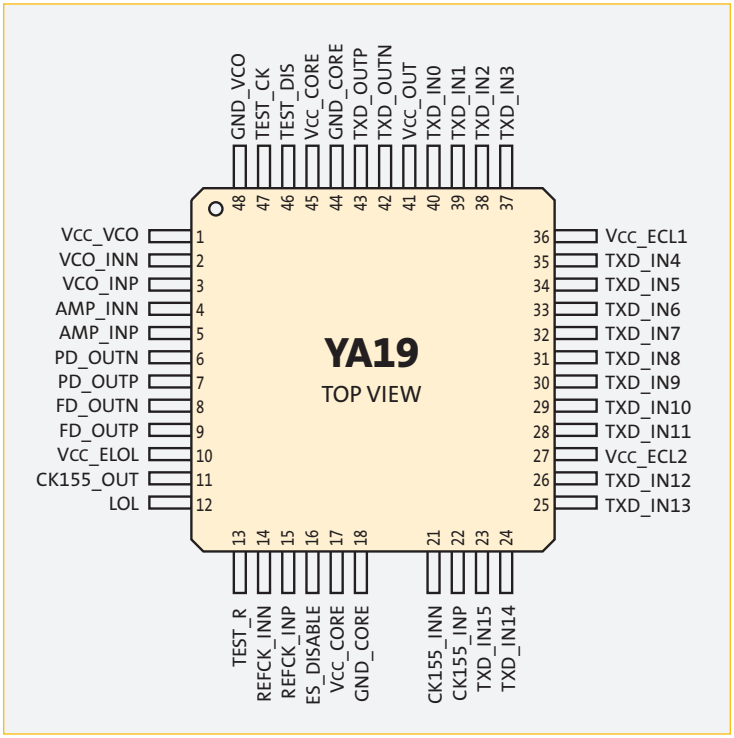


Figure 9: 48-lead LQFP

Package Outline and Dimensions

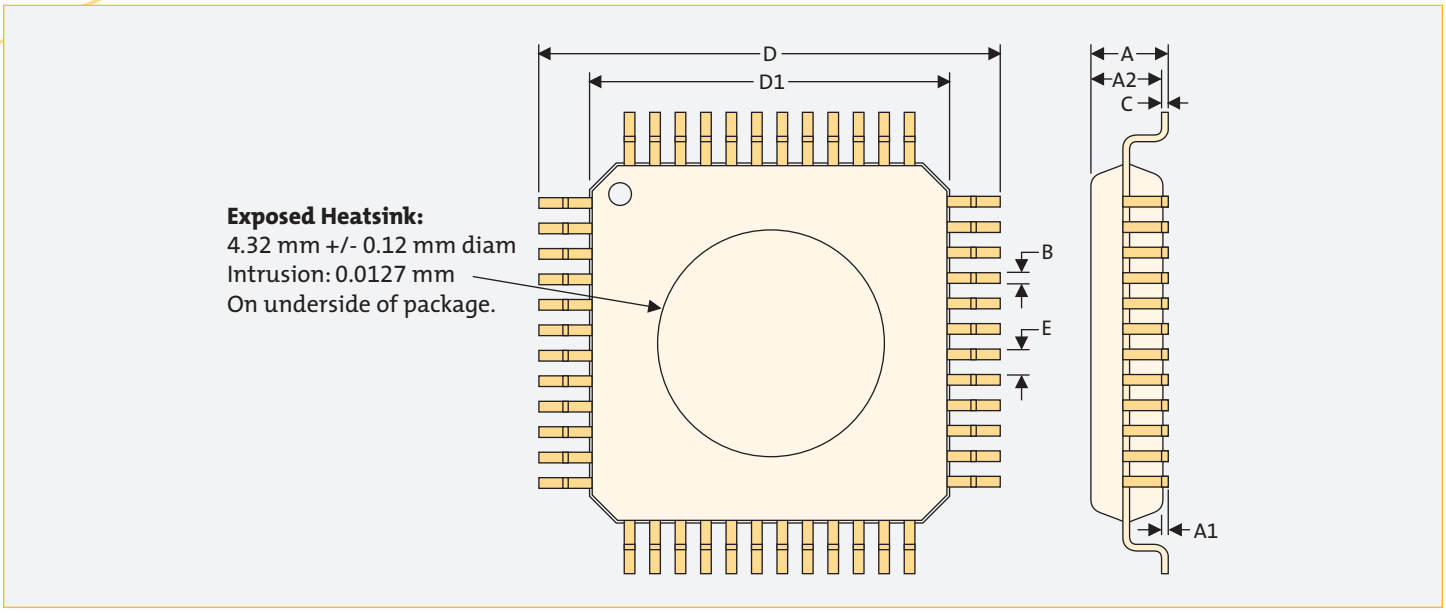


Figure 10: Package Outline

	Min (mm)	Nom (mm)	Max (mm)
Lead pitch (E)		0.50	
Body size (D1)		7.00	
Component tip-to-tip (D)		9.00	
Component height (A)			1.60
Component standoff (A1)	0.05		0.15
Body thickness (A2)	1.35	1.40	1.45
Lead width, plated (B)	0.17	0.22	0.27
Lead thickness, plated (C)	0.09		0.20

Notes:

Ordering information

Please quote the Product Code from Table 2 below when ordering as this is the identification that appears on the part when shipped.

Table 2: Product ordering information

Product Code	Product Name
A0742167 (QMV1051-1AF5)	YA19 2.5 Gb/s 16:1 Multiplexer and Clock Generator

For additional information on Nortel Networks products and services offered, please contact your local representative.

Nortel Networks
High Performance Optical Component Solutions
attn: Marketing Department
2745 Iris Street
6th Floor
Ottawa, Ontario
Canada K2C 3V5

Tel: 1-800-4 NORTEL
Fax: 1-613-763-8416

Email: opticalcomponents@nortelnetworks.com

www.nortelnetworks.com/hpocs

Publication # 84001.37/03-01 Issue 2

Issued: 5 March 2001