Key Features

- Resolutions Up To UXGA 85Hz
- 250ps Long Term Jitter
- 64 Phase Choices
- Zero Offset Error/Offset Drift

X98024

240MHz Triple Video Digitizer with Digital PLL

PRELIMINARY INFORMATION

FEATURES

- **240MSPS maximum conversion rate**
- **64 interpixel sampling positions**
- **Low long-term PLL clock jitter (250ps p-p @ 240MSPS)**
- **Programmable input bandwidth (100MHz to 780MHz)**
- **2 channel input multiplexer**
- **RGB and YUV 4:2:2 output formats**
- **4 embedded voltage regulators allow operation from single 3.3V supply and enhance performance, isolation**
- **Completely independent 8 bit gain/10 bit offset control**
- **CSYNC and SOG support**
- **Trilevel Sync detection**
- **1150mW typical PD @ 240MSPS**

APPLICATIONS

- **LCD Monitors and Projectors**
- **Digital TVs**
- **Plasma Display Panels**
- **RGB Graphics Processing**
- **Scan Converters**

DESCRIPTION

The X98024 3-channel, 8-bit Analog Front End (AFE) contains all the components necessary to digitize analog RGB or YUV graphics signals from personal computers, workstations and video set-top boxes. The fully differential analog design provides high PSRR and dynamic performance to meet the strigent requirements of the graphics display industry. The 240MSPS conversion rate supports resolutions up to UXGA at 85Hz refresh rate, while the front end's high input bandwidth ensures sharp images at the highest resolution.

To minimize noise, the X98024's analog section features 2 sets of pseudo-differential RGB inputs with programmable input bandwidth, as well as internal DC restore clamping (including mid-scale clamping for YUV signals). This is followed by the programmable gain/offset stage and the three 240MSPS Analog-to-Digital Converters (ADCs). All necessary reference voltages are internally generated.

The X98024's digital PLL generates a pixel clock from the analog source's HSYNC or SOG (Sync-On-Green) signals. Pixel clock output frequencies range from 10MHz to 240MHz with long-term clock jitter less than 250ps peak to peak.

BLOCK DIAGRAM