**New Features**

- Monitor Voltages: 5V to 0.9V
- Memory Security
- Independent Core Voltage Monitor

# 4Kbit EEPROM X40430/X40431/X40434/X40435

## Triple Voltage Monitor with Integrated CPU Supervisor

### FEATURES

- **Triple voltage detection and reset assertion**
  - **—Standard reset threshold settings. See selection table on page 2.**
  - **—Adjust low voltage reset threshold voltages using special programming sequence**
  - **—Reset signal valid to $V_{CC}$ = 1V**
  - **—Monitor three separate voltages**
- **Fault detection register**
- **Selectable power on reset timeout (0.05s, 0.2s, 0.4s, 0.8s)**
- **Selectable watchdog timer interval (25ms, 200ms, 1.4s or off)**
- **Debounced manual reset input**
- **Low power CMOS**
  - **—25µA typical standby current, watchdog on**
  - **—6µA typical standby current, watchdog off**
- **4Kbits of EEPROM**
  - **—16 byte page write mode**
  - **—5ms write cycle time (typical)**
- **Built-in inadvertent write protection**
  - **—Power-up/power-down protection circuitry**
  - **—Block lock protect 0, or 1/2, of EEPROM**
- **400kHz 2-wire interface**
- **2.7V to 5.5V power supply operation**
- **Available packages**
  - **—14-lead SOIC, TSSOP**

### APPLICATIONS

- **Communication Equipment**
  - **—Routers, Hubs, Switches**
  - **—Disk Arrays, Network Storage**
- **Industrial Systems**
  - **—Process Control**
  - **—Intelligent Instrumentation**
- **Computer Systems**
  - **—Computers**
  - **—Network Servers**

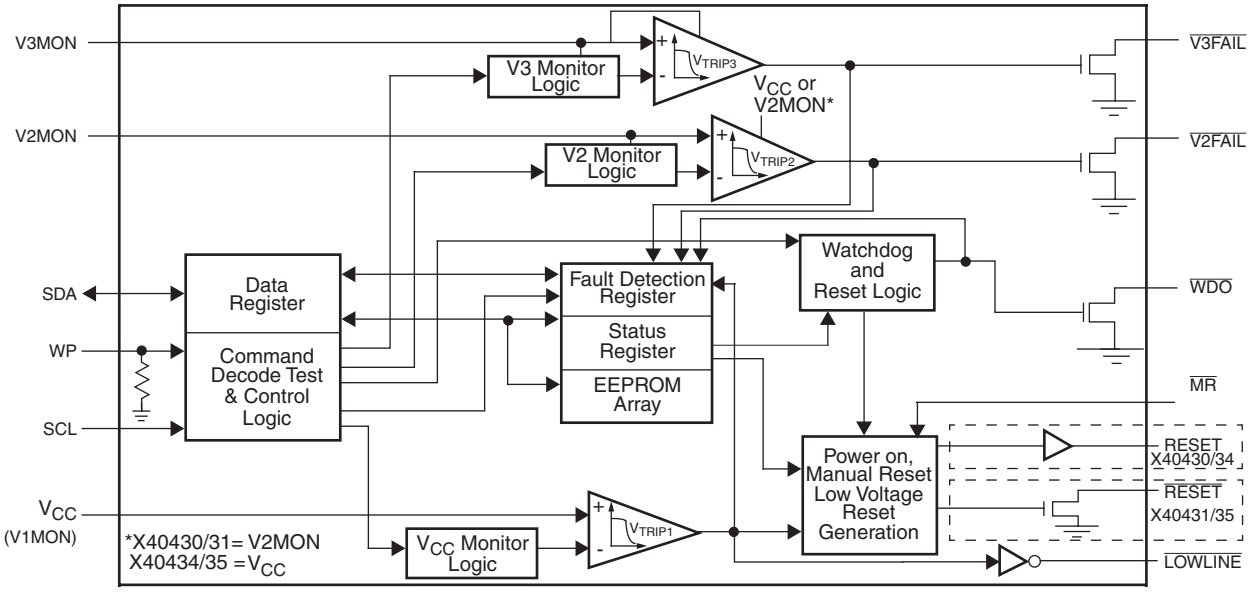
### DESCRIPTION

The X40430/31/34/35 combines power-on reset control, watchdog timer, supply voltage supervision, second and third voltage supervision, manual reset, and Block Lock™ protect serial EEPROM in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying voltage to $V_{CC}$ activates the power on reset circuit which holds RESET/$\overline{\text{RESET}}$ active for a period of time. This allows the power supply and system oscillator to stabilize before the processor can execute code.

Low $V_{CC}$ detection circuitry protects the user's system from low voltage conditions, resetting the system when $V_{CC}$ falls below the minimum $V_{TRIP1}$ point. RESET/$\overline{\text{RESET}}$ is active until $V_{CC}$ returns to proper operating

### BLOCK DIAGRAM



level and stabilizes. A second and third voltage monitor circuit tracks the unregulated supply to provide a power fail warning or monitors different power supply voltage. Three common low voltage combinations are available. However, Xicor's unique circuits allows the threshold for either voltage monitor to be reprogrammed to meet specific system level requirements or to fine-tune the threshold for applications requiring higher precision.

A manual reset input provides debounce circuitry for minimum reset component count.

The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{WDO}$ signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

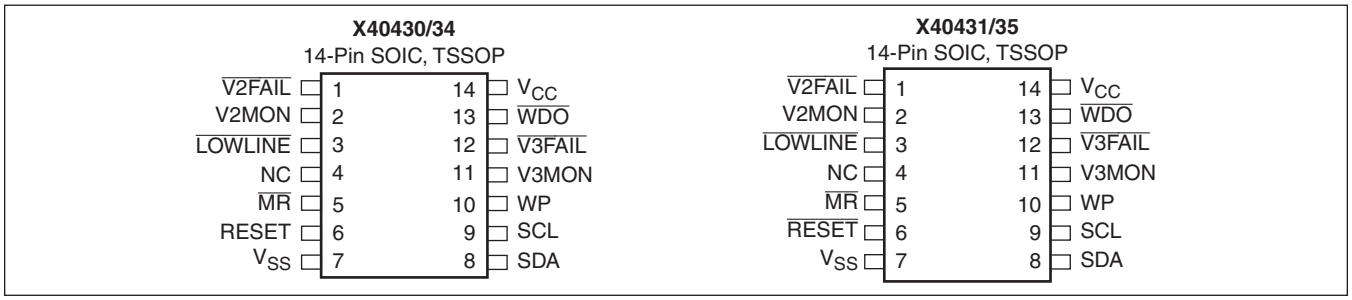
The memory portion of the device is a CMOS Serial EEPROM array with Xicor's Block Lock protection. The array is internally organized as x 8. The device features a 2-wire interface and software protocol allowing operation on an $I^2C$ bus.

The device utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

| Device | Expected System Voltages | Vtrip1(V) | Vtrip2(V) | Vtrip3(V) | POR (system) |
|---|---|---|---|---|---|
| X40430/31 | | 2.0–4.75* | 1.70–4.75 | 1.70–4.75 | |
| -A | 5V; 3V or 3.3V; 1.8V | 4.55–4.65* | 2.85–2.95 | 1.65–1.75 | $\overline{RESET}$ = X40430 |
| -B | 5V; 3V; 1.8V | 4.35–4.45* | 2.55–2.65 | 1.65–1.75 | $\overline{RESET}$ = X40431 |
| -C | 3.3V; 2.5V; 1.8V | 2.95–3.05* | 2.15–2.25 | 1.65–1.75 | |
| X40434/35 | | 2.0–4.75* | 0.90–3.50* | 1.70–4.75 | |
| -A | 5V; 3.3V; 1.5V | 4.55–4.65* | 1.25–1.35* | 3.05–3.15 | $\overline{RESET}$ = X40434 |
| -B | 5V; 3V or 3.3V; 1.5V | 4.55–4.65* | 1.25–1.35* | 2.85–2.95 | $\overline{RESET}$ = X40435 |
| -C | 5V; 3 or 3.3V; 1.2V | 4.55–4.65* | 0.95–1.05* | 2.85–2.95 | |

*Voltage monitor requires Vcc to operate. Others are independent of Vcc.

## PIN CONFIGURATION




## PIN DESCRIPTION

| Pin | Name | Function |
|---|---|---|
| 1 | $\overline{V2FAIL}$ | **V2 Voltage Fail Output.** This open drain output goes LOW when V2MON is less than $V_{TRIP2}$ and goes HIGH when V2MON exceeds $V_{TRIP2}$. There is no power up reset delay circuitry on this pin. |
| 2 | V2MON | **V2 Voltage Monitor Input.** When the V2MON input is less than the $V_{TRIP2}$ voltage, $\overline{V2FAIL}$ goes LOW. This input can monitor an unregulated power supply with an external resistor divider or can monitor a second power supply with no external components. Connect V2MON to $V_{SS}$ or $V_{CC}$ when not used. The V2MON comparator is supplied by V2MON (X40430/31) or by the $V_{CC}$ input (X40434/35). |
| 3 | $\overline{LOWLINE}$ | **Early Low $V_{CC}$ Detect.** This CMOS output signal goes LOW when $V_{CC} < V_{TRIP1}$ and goes high when $V_{CC} > V_{TRIP1}$. |
| 4 | NC | **No connect.** |
| 5 | $\overline{MR}$ | **Manual Reset Input.** Pulling the $\overline{MR}$ pin LOW initiates a system reset. The RESET/$\overline{RESET}$ pin will remain HIGH/LOW until the pin is released and for the $t_{PURST}$ thereafter. |

**PIN DESCRIPTION** (Continued)

| Pin | Name | Function |
|---|---|---|
| 6 | $\overline{\text{RESET}}$/ RESET | **$\overline{\text{RESET}}$ Output.** (X40431/35) This open drain pin is an active LOW output which goes LOW whenever $V_{CC}$ falls below $V_{TRIP1}$ voltage or if manual reset is asserted. This output stays active for the programmed time period ($t_{PURST}$) on power up. It will also stay active until manual reset is released and for $t_{PURST}$ thereafter.<br>**RESET Output.** (X40430/34) This pin is an active HIGH CMOS output which goes HIGH whenever $V_{CC}$ falls below $V_{TRIP1}$ voltage or if manual reset is asserted. This output stays active for the programmed time period ($t_{PURST}$) on power up. It will also stay active until manual reset is released and for $t_{PURST}$ thereafter. |
| 7 | $V_{SS}$ | Ground |
| 8 | SDA | **Serial Data.** SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. This pin requires a pull up resistor and the input buffer is always active (not gated).<br>**Watchdog Input.** A HIGH to LOW transition on the SDA (while SCL is toggled from HIGH to LOW and followed by a stop condition) restarts the Watchdog timer. The absence of this transition within the watchdog time out period results in $\overline{\text{WDO}}$ going active. |
| 9 | SCL | **Serial Clock.** The Serial Clock controls the serial bus timing for data input and output. |
| 10 | WP | **Write Protect.** WP HIGH prevents writes to any location in the device (including all the registers). It has an internal pull down resistor (>10MΩ typical). |
| 11 | V3MON | **V3 Voltage Monitor Input.** When the V3MON input is less than the $V_{TRIP3}$ voltage, $\overline{\text{V3FAIL}}$ goes LOW. This input can monitor an unregulated power supply with an external resistor divider or can monitor a third power supply with no external components. Connect V3MON to $V_{SS}$ or $V_{CC}$ when not used. The V3MON comparator is supplied by the V3MON input. |
| 12 | $\overline{\text{V3FAIL}}$ | **V3 Voltage Fail Output.** This open drain output goes LOW when V3MON is less than $V_{TRIP3}$ and goes HIGH when V3MON exceeds $V_{TRIP3}$. There is no power up reset delay circuitry on this pin. |
| 13 | $\overline{\text{WDO}}$ | **$\overline{\text{WDO}}$ Output.** $\overline{\text{WDO}}$ is an active LOW, open drain output which goes active whenever the watchdog timer goes active. |
| 14 | $V_{CC}$ | Supply Voltage |

## PRINCIPLES OF OPERATION

### Power On Reset

Applying power to the X40430/31/34/35 activates a Power On Reset Circuit that pulls the RESET/$\overline{\text{RESET}}$ pins active. This signal provides several benefits.

– It prevents the system microprocessor from starting to operate with insufficient voltage.

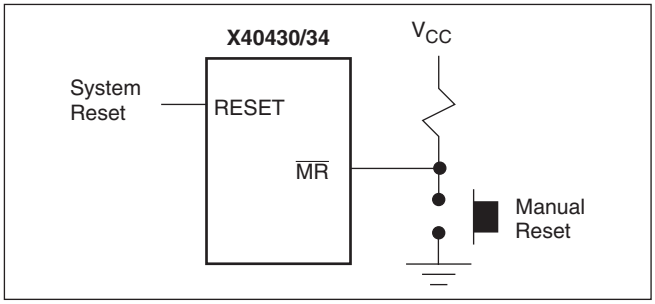
– It prevents the processor from operating prior to stabilization of the oscillator.

– It allows time for an FPGA to download its configuration prior to initialization of the circuit.

– It prevents communication to the EEPROM, greatly reducing the likelihood of data corruption on power up.

When $V_{CC}$ exceeds the device $V_{TRIP1}$ threshold value for $t_{PURST}$ (selectable) the circuit releases the $\overline{\text{RESET}}$ (X40431/35) and RESET (X40430/34) pin allowing the system to begin operation.

**Figure 1. Connecting a Manual Reset Push-Button**




### Manual Reset

By connecting a push-button directly from $\overline{\text{MR}}$ to ground, the designer adds manual system reset capability. The $\overline{\text{MR}}$ pin is LOW while the push-button is closed and RESET/$\overline{\text{RESET}}$ pin remains HIGH/LOW until the push-button is released and for $t_{PURST}$ thereafter.

### Low Voltage $V_{CC}$ (V1 Monitoring)

During operation, the X40430/31/34/35 monitors the $V_{CC}$ level and asserts RESET/$\overline{\text{RESET}}$ if supply voltage falls below a preset minimum $V_{TRIP1}$. The RESET/$\overline{\text{RESET}}$ signal prevents the microprocessor from operating in a power fail or brownout condition. The RESET/$\overline{\text{RESET}}$ signal remains active until the voltage drops below 1V. It also remains active until $V_{CC}$ returns and exceeds $V_{TRIP1}$ for $t_{PURST}$.

### Low Voltage V2 Monitoring

The X40430 also monitors a second voltage level and asserts $\overline{\text{V2FAIL}}$ if the voltage falls below a preset minimum $V_{TRIP2}$. The $\overline{\text{V2FAIL}}$ signal is either ORed with RESET to prevent the microprocessor from operating in a power fail or brownout condition or used to interrupt the microprocessor with notification of an impending power failure.

For the X40430 and X40431 the $\overline{\text{V2FAIL}}$ signal remains active until the V2MON drops below 1V (V2MON falling). It also remains active until V2MON returns and exceeds $V_{TRIP2}$. This voltage sense circuitry monitors the power supply connected to V2MON pin. If $V_{CC}$ = 0, V2MON can still be monitored.

For the X40434 and X40435, the $\overline{\text{V2FAIL}}$ signal remains active until $V_{CC}$ drops below 1V and remains active until V2MON returns and exceeds $V_{TRIP2}$. This sense circuitry is powered by $V_{CC}$. If $V_{CC}$=0, V2MON cannot be monitored.

### Low Voltage V3 Monitoring

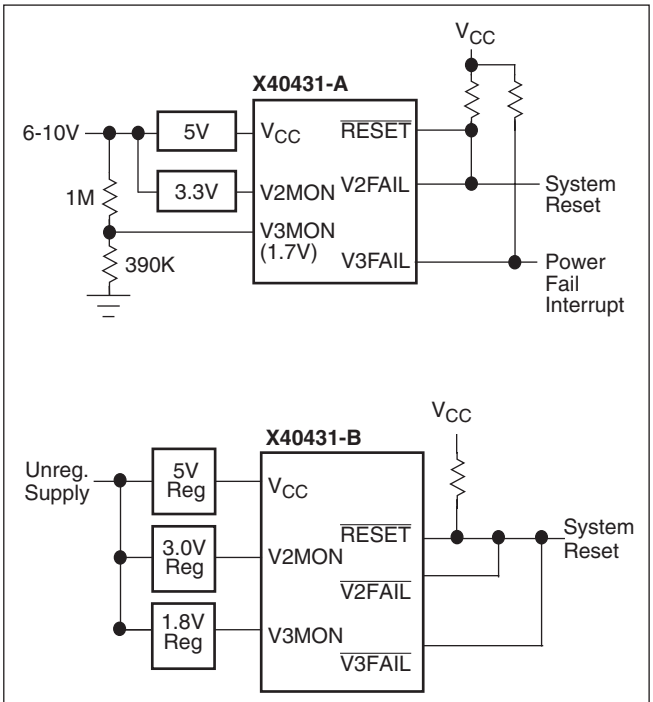
The X40430/31/34/35 also monitors a third voltage level and asserts $\overline{\text{V3FAIL}}$ if the voltage falls below a preset minimum $V_{TRIP3}$. The $\overline{\text{V3FAIL}}$ signal is either ORed with RESET to prevent the microprocessor from operating in a power fail or brownout condition or used to interrupt the microprocessor with notification of an impending power failure. The $\overline{\text{V3FAIL}}$ signal remains active until the V3MON drops below 1V (V3MON falling). It also remains active until V3MON returns and exceeds $V_{TRIP3}$.

This voltage sense circuitry monitors the power supply connected to V3MON pin. If $V_{CC}$ = 0, V3MON can still be monitored.

### Early Low $V_{CC}$ Detection ($\overline{\text{LOWLINE}}$)

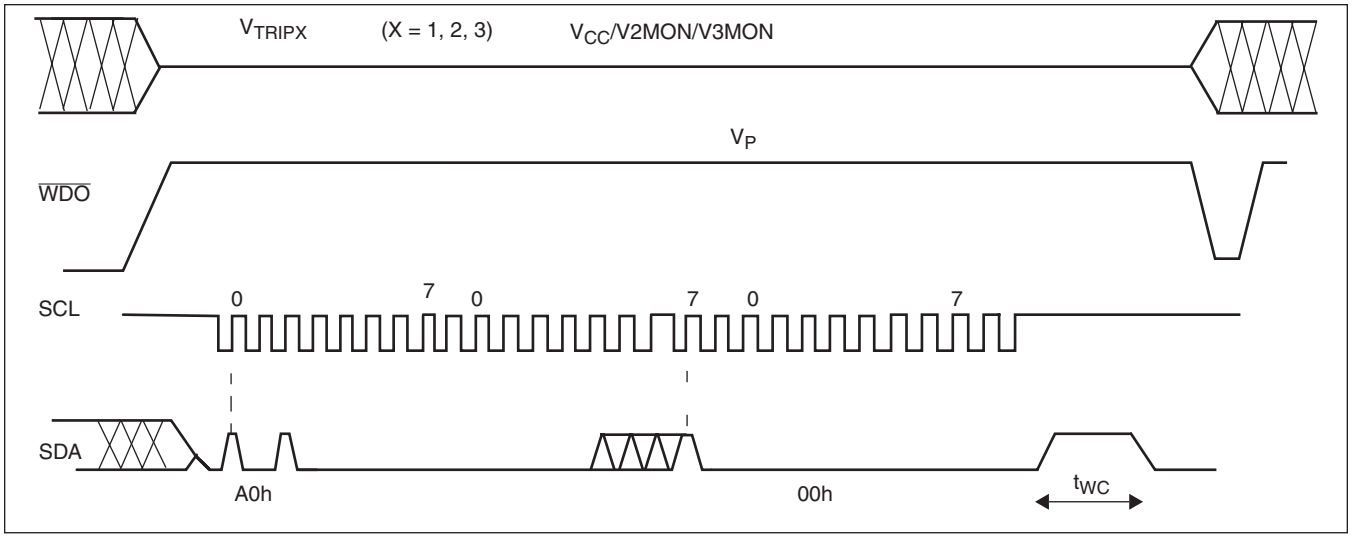
This CMOS output goes LOW earlier than RESET/$\overline{\text{RESET}}$ whenever $V_{CC}$ falls below the $V_{TRIP1}$ voltage and returns high when $V_{CC}$ exceeds the $V_{TRIP1}$ voltage. There is no power up delay circuitry ($t_{PURST}$) on this pin.

**Figure 2. Two Uses of Multiple Voltage Monitoring**




**Notice:** No external components required to monitor three voltages.

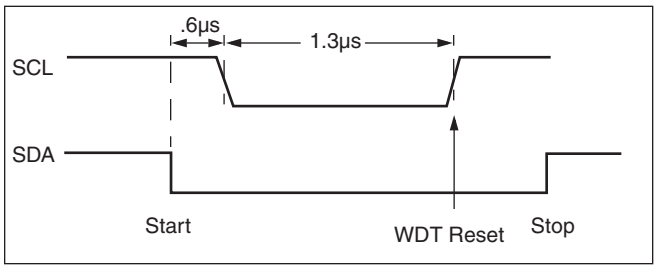
**Figure 3. $V_{TRIPX}$ Set/Reset Conditions**




## WATCHDOG TIMER

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the SDA and SCL pins. A standard read or write sequence to any slave address byte restarts the watchdog timer and prevents the $\overline{WDO}$ signal going active. A minimum sequence to reset the watchdog timer requires four microprocessor instructions namely, a Start, Clock Low, Clock High and Stop. The state of two nonvolatile control bits in the Status Register determine the watchdog timer period. The microprocessor can change these watchdog bits by writing to the X40430/31/34/35 control register (also refer to page 20).

**Figure 4. Watchdog Restart**




## V1, V2 AND V3 THRESHOLD PROGRAM PROCEDURE (OPTIONAL)

The X40430 is shipped with standard V1, V2 and V3 threshold ($V_{TRIP1}$, $V_{TRIP2}$, $V_{TRIP3}$) voltages. These values will not change over normal operating and storage conditions. However, in applications where the standard thresholds are not exactly right, or if higher precision is needed in the threshold value, the X40430/31/34/35 trip points may be adjusted. The procedure is described below, and uses the application of a high voltage control signal.

### Setting a $V_{TRIPx}$ Voltage (x=1, 2, 3)

There are two procedures used to set the threshold voltages ($V_{TRIPx}$), depending if the threshold voltage to be stored is higher or lower than the present value. For example, if the present $V_{TRIPx}$ is 2.9 V and the new $V_{TRIPx}$ is 3.2 V, the new voltage can be stored directly into the $V_{TRIPx}$ cell. If however, the new setting is to be lower than the present setting, then it is necessary to "reset" the $V_{TRIPx}$ voltage before setting the new value.

### Setting a Higher $V_{TRIPx}$ Voltage (x=1, 2, 3)

To set a $V_{TRIPx}$ threshold to a new voltage which is higher than the present threshold, the user must apply the desired $V_{TRIPx}$ threshold voltage to the corresponding input pin Vcc(V1MON), V2MON or V3MON. Then, a programming voltage (Vp) must be applied to the $\overline{WDO}$ pin before a START condition is set up on SDA. Next, issue on the SDA pin the Slave Address A0h, followed by the Byte Address 01h for $V_{TRIP1}$, 09h for $V_{TRIP2}$, and 0Dh for $V_{TRIP3}$, and a 00h Data Byte in order to program $V_{TRIPx}$. The STOP bit following a valid write operation initiates the programming sequence. Pin $\overline{WDO}$ must then be brought LOW to complete the operation. To check if the $V_{TRIPX}$ has been set, set VXMON to a value slightly greater than $V_{TRIPX}$ (that was previously set). Slowly ramp down VXMON and observe when the corresponding outputs ($\overline{LOWLINE}$, $\overline{V2FAIL}$ and $\overline{V3FAIL}$) switch. The voltage at which this occurs is the $V_{TRIPX}$ (actual).

### Case A

Now if the desired $V_{TRIPX}$ is greater than the $V_{TRIPX}$ (actual), then add the difference between $V_{TRIPX}$ (desired) – $V_{TRIPX}$ (actual) to the original $V_{TRIPX}$ desired. This is your new $V_{TRIPX}$ that should be applied to VXMON and the whole sequence should be repeated again (see Figure 5).

### Case B

Now if the $V_{TRIPX}$ (actual), is higher than the $V_{TRIPX}$ (desired), perform the reset sequence as described in the next section. The new $V_{TRIPX}$ voltage to be applied to VXMON will now be: $V_{TRIPX}$ (desired) – ($V_{TRIPX}$ (actual) – $V_{TRIPX}$ (desired)).

**Note:** This operation does not corrupt the memory array.

### Setting a Lower $V_{TRIPx}$ Voltage (x=1, 2, 3)

In order to set $V_{TRIPx}$ to a lower voltage than the present value, then $V_{TRIPx}$ must first be "reset" according to the procedure described below. Once $V_{TRIPx}$ has been "reset", then $V_{TRIPx}$ can be set to the desired voltage using the procedure described in "Setting a Higher $V_{TRIPx}$ Voltage".

### Resetting the $V_{TRIPx}$ Voltage

To reset a $V_{TRIPx}$ voltage, apply the programming voltage (Vp) to the $\overline{WDO}$ pin before a START condition is set up on SDA. Next, issue on the SDA pin the Slave Address A0h followed by the Byte Address 03h for $V_{TRIP1}$, 0Bh for $V_{TRIP2}$, and 0Fh for $V_{TRIP3}$, followed by 00h for the Data Byte in order to reset $V_{TRIPx}$. The STOP bit following a valid write operation initiates the programming sequence. Pin $\overline{WDO}$ must then be brought LOW to complete the operation.

After being reset, the value of $V_{TRIPx}$ becomes a nominal value of 1.7V or lesser.

**Notes:** 1. This operation does not corrupt the memory array.
2. Set $V_{CC} \cong 1.5$(V2MON or V3MON), when setting $V_{TRIP2}$ or $V_{TRIP3}$ respectively.

## CONTROL REGISTER

The Control Register provides the user a mechanism for changing the Block Lock and Watchdog Timer settings. The Block Lock and Watchdog Timer bits are nonvolatile and do not change when power is removed.

The Control Register is accessed with a special preamble in the slave byte (1011) and is located at address 1FFh. It can only be modified by performing a byte write operation directly to the address of the register and only one data byte is allowed for each register write operation. Prior to writing to the Control Register, the WEL and RWEL bits must be set using a two step process, with the whole sequence requiring 3 steps. See "Writing to the Control Registers" on page 7.

The user must issue a stop, after sending this byte to the register, to initiate the nonvolatile cycle that stores WD1, WD0, PUP1, PUP0, and BP. The X40430/31/34/35 will not acknowledge any data bytes written after the first byte is entered.

The state of the Control Register can be read at any time by performing a random read at address 1FFh, using the special preamble. Only one byte is read by each register read operation. The master should supply a stop condition to be consistent with the bus protocol.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PUP1 | WD1 | WD0 | BP | 0 | RWEL | WEL | PUP0 |

### RWEL: Register Write Enable Latch (Volatile)

The RWEL bit must be set to "1" prior to a write to the Control Register.

**Figure 5. Sample $V_{TRIP}$ Reset Circuit**

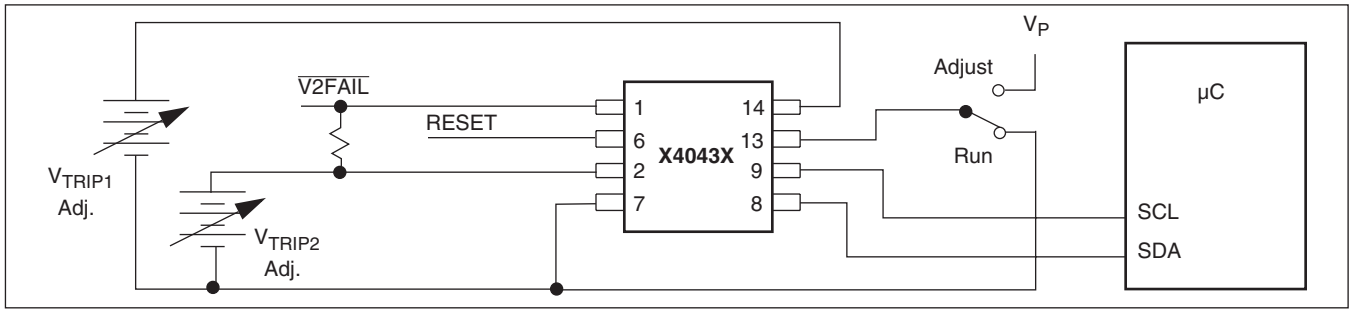
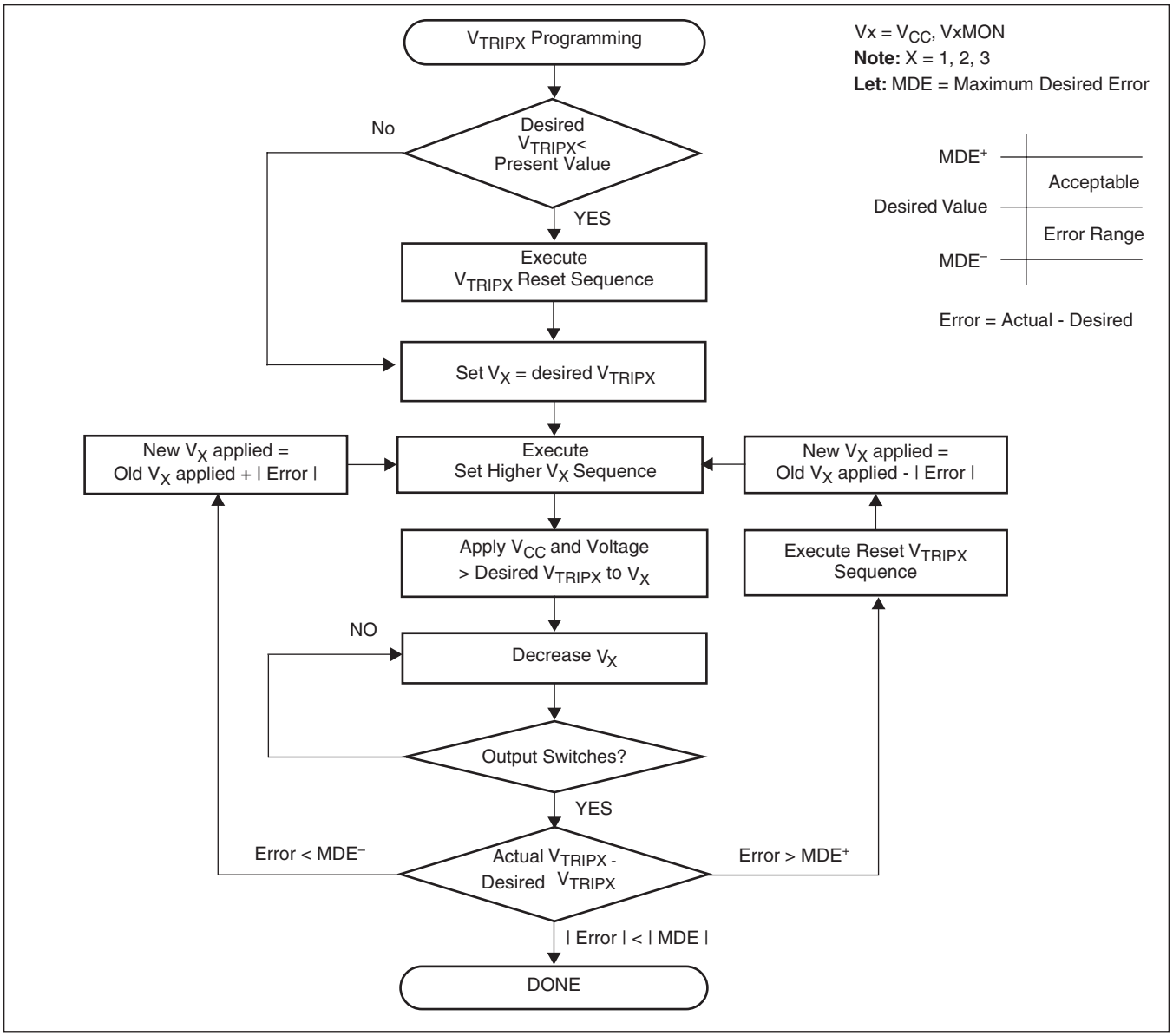


**Figure 6. $V_{TRIPX}$ Set/Reset Sequence (X = 1, 2, 3)**




### WEL: Write Enable Latch (Volatile)

The WEL bit controls the access to the memory and to the Register during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to any address, including any control registers will be ignored (no acknowledge will be issued after the Data Byte). The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the control register.

Once set, WEL remains set until either it is reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the control register) or until the part powers up again. Writes to the WEL bit do not cause a high voltage write cycle, so the device is ready for the next operation immediately after the stop condition.

### BP: Block Protect Bits (Nonvolatile)

The Block Protect Bit BP, determines which blocks of the array are write protected. A write to a protected block of memory is ignored. The block protect bit will prevent write operations to half or none of the array.

| BP | Protected Addresses (Size) | Memory Array Lock |
|---|---|---|
| 0 | None | None |
| 1 | 100h – 1FFh (256 bytes) | Upper Half of Memory Array |

### PUP1, PUP0: Power Up Bits (Nonvolatile)

The Power Up bits, PUP1 and PUP0, determine the $t_{PURST}$ time delay. The nominal power up times are shown in the following table.

| PUP1 | PUP0 | Power on Reset Delay ($t_{PURST}$) |
|---|---|---|
| 0 | 0 | 50ms |
| 0 | 1 | 200ms (factory setting) |
| 1 | 0 | 400ms |
| 1 | 1 | 800ms |

### WD1, WD0: Watchdog Timer Bits (Nonvolatile)

The bits WD1 and WD0 control the period of the Watchdog Timer. The options are shown below.

| WD1 | WD0 | Watchdog Time Out Period |
|---|---|---|
| 0 | 0 | 1.4 seconds |
| 0 | 1 | 200 milliseconds |
| 1 | 0 | 25 milliseconds |
| 1 | 1 | disabled (factory setting) |

### Writing to the Control Registers

Changing any of the nonvolatile bits of the control and trickle registers requires the following steps:

– Write a 02H to the Control Register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceded by a start and ended with a stop).

– Write a 06H to the Control Register to set the Register Write Enable Latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation proceeded by a start and ended with a stop).

– Write one byte value to the Control Register that has all the control bits set to the desired state. The Control register can be represented as *qxys* 001*r* in binary, where *xy* are the WD bits, *s* is the BP bit and *qr* are the power up bits. This operation proceeded by a start and ended with a stop bit. Since this is a nonvolatile write cycle it will take up to 10ms (max.) to complete. The RWEL bit is reset by this cycle and the sequence must be repeated to change the nonvolatile bits again. If bit 2 is set to '1' in this third step (*qxys* 011*r*) then the RWEL bit is set, but the WD1, WD0, PUP1, PUP0, and BP bits remain unchanged. Writing a second byte to the control register is not allowed. Doing so aborts the write operation and returns a NACK.

– A read operation occurring between any of the previous operations will not interrupt the register write operation.

– The RWEL bit cannot be reset without writing to the nonvolatile control bits in the control register, power cycling the device or attempting a write to a write protected block.

To illustrate, a sequence of writes to the device consisting of [02H, 06H, 02H] will reset all of the nonvolatile bits in the Control Register to 0. A sequence of [02H, 06H, 06H] will leave the nonvolatile bits unchanged and the RWEL bit remains set.

**Notes:** 1. $t_{PURST}$ is set to 200ms as factory default.
2. Watch Dog Timer bits are shipped disabled.

### FAULT DETECTION REGISTER

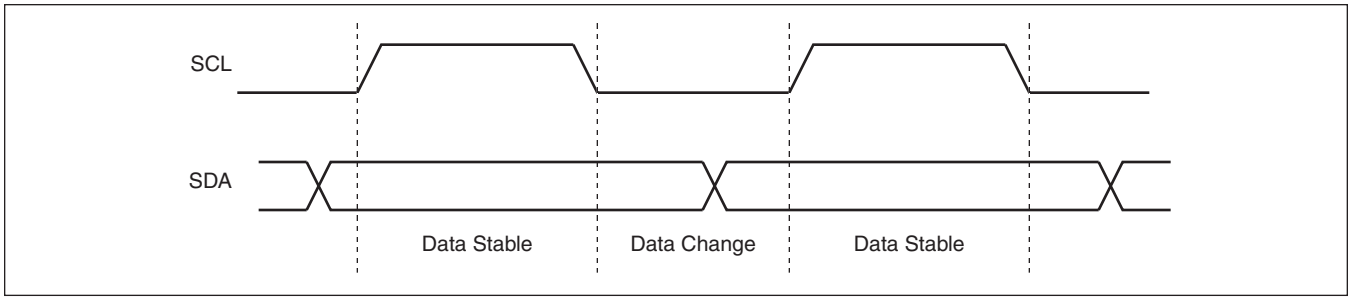
The Fault Detection Register (FDR) provides the user the status of what causes the system reset active. The Manual Reset Fail, Watchdog Timer Fail and Three Low Voltage Fail bits are volatile

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LV1F | LV2F | LV3F | WDF | MRF | 0 | 0 | 0 |

The FDR is accessed with a special preamble in the slave byte (1011) and is located at address 0FFh. It can only be modified by performing a byte write operation directly to the address of the register and only one data byte is allowed for each register write operation.

There is no need to set the WEL or RWEL in the control register to access this FDR.

**Figure 7. Valid Data Changes on the SDA Bus**




At power-up, the FDR is defaulted to all “0”. The system needs to initialize this register to all “1” before the actual monitoring can take place. In the event of any one of the monitored sources fail. The corresponding bit in the register will change from a “1” to a “0” to indicate the failure. At this moment, the system should perform a read to the register and note the cause of the reset. After reading the register the system should reset the register back to all “1” again. The state of the FDR can be read at any time by performing a random read at address 0FFh, using the special preamble.

The FDR can be read by performing a random read at 0FFh address of the register at any time. Only one byte of data is read by the register read operation.

### MRF, Manual Reset Fail Bit (Volatile)

The MRF bit will be set to “0” when Manual Reset input goes active.

### WDF, Watchdog Timer Fail Bit (Volatile)

The WDF bit will be set to “0” when the $\overline{WDO}$ goes active.

### LV1F, Low $V_{CC}$ Reset Fail Bit (Volatile)

The LV1F bit will be set to “0” when $V_{CC}$ (V1MON) falls below $V_{TRIP1}$.

### LV2F, Low V2MON Reset Fail Bit (Volatile)

The LV2F bit will be set to “0” when V2MON falls below $V_{TRIP2}$.

### LV3F, Low V3MON Reset Fail Bit (Volatile)

The LV3F bit will be set to “0” when the V3MON falls below $V_{TRIP3}$.

## SERIAL INTERFACE

### Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

### Serial Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 7.

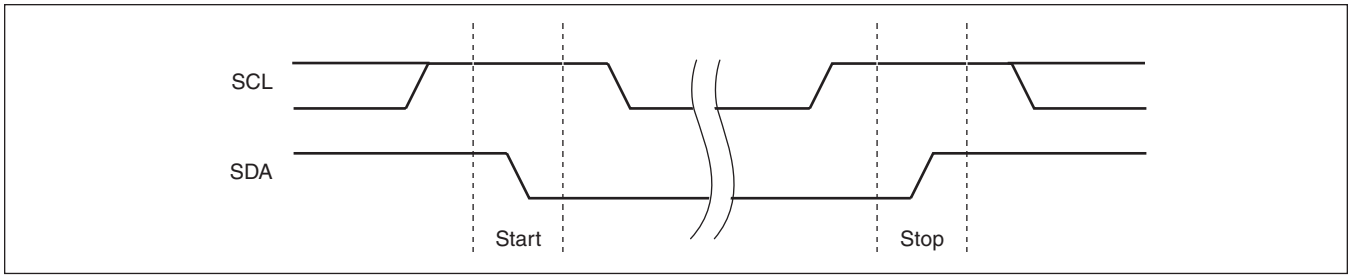
### Serial Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 8.

### Serial Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Figure 8.

**Figure 8. Valid Start and Stop Conditions**




### Serial Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. See Figure 9.

The device will respond with an acknowledge after recognition of a start condition and if the correct Device Identifier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for the Slave Address Byte when the Device Identifier and/or Select bits are incorrect.

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

### Serial Write Operations

### Byte Write

For a write operation, the device requires the Slave Address Byte and a Word Address Byte. This gives the master access to any one of the words in the array. After receipt of the Word Address Byte, the device responds with an acknowledge, and awaits the next eight bits of data. After receiving the 8 bits of the Data Byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. During this internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 10.

A write to a protected block of memory will suppress the acknowledge bit.

**Figure 9. Acknowledge Response From Receiver**

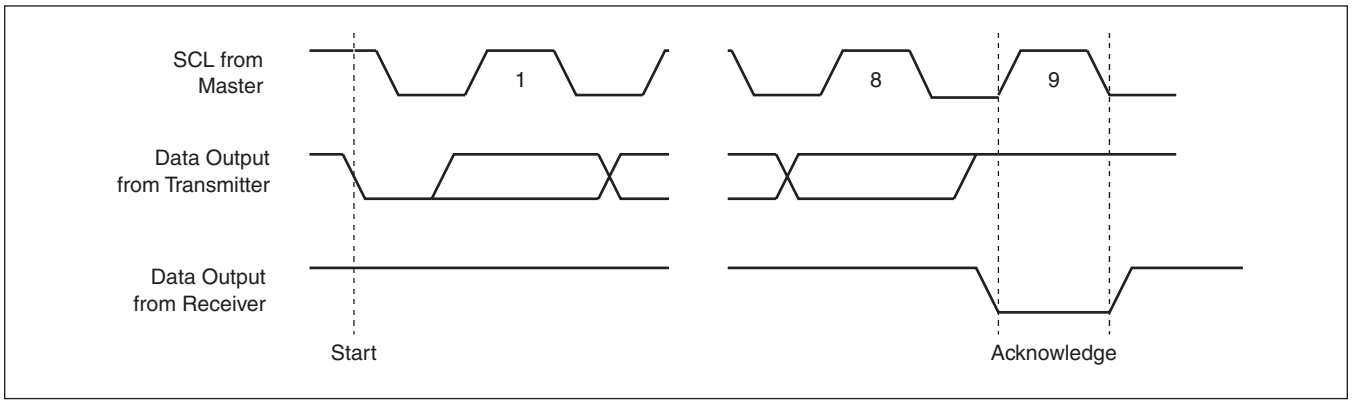
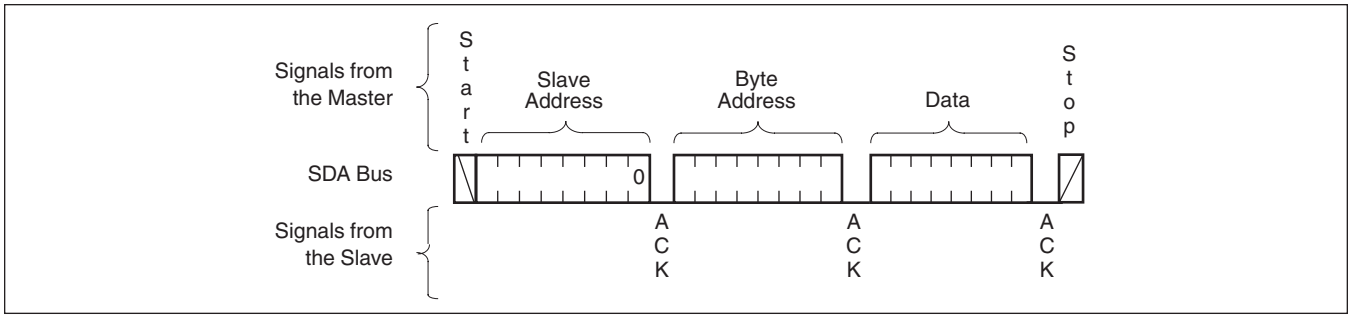


**Figure 10. Byte Write Sequence**




### Page Write

The device is capable of a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit an unlimited number of 8-bit bytes. After the receipt of each byte, the device will respond with an acknowledge, and the address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it "rolls over" and goes back to '0' on the same page.

This means that the master can write 16 bytes to the page starting at any location on that page. If the master begins writing at location 10, and loads 12 bytes, then the first 6 bytes are written to locations 10 through 15, and the last 6 bytes are written to locations 0 through 5. Afterwards, the address counter would point to location 6 of the page that was just written. If the master supplies more than 16 bytes of data, then new data overwrites the previous data, one byte at a time.

**Figure 11. Page Write Operation**

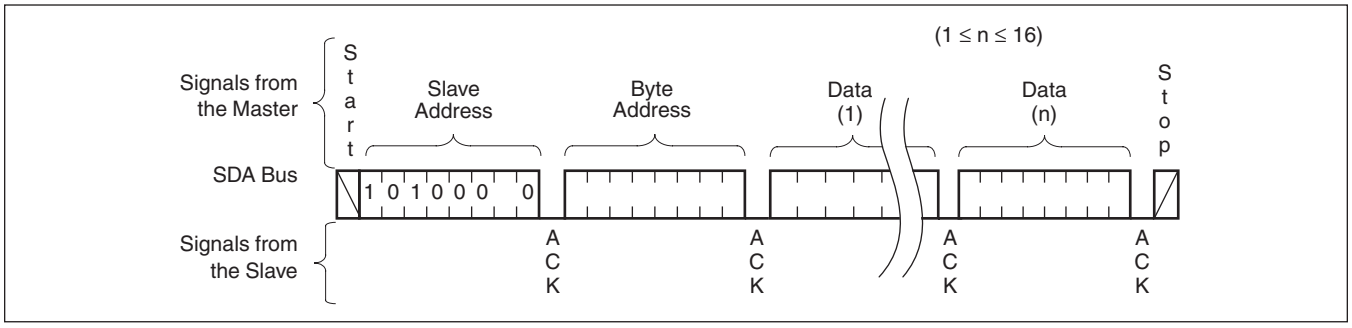
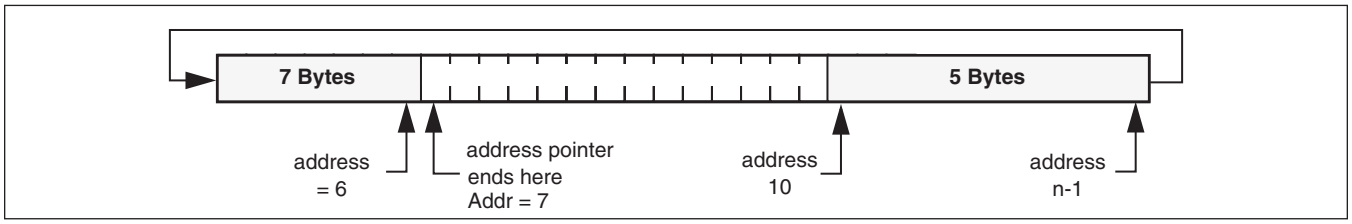



**Figure 12. Writing 12 bytes to a 16-byte page starting at location 10.**




The master terminates the Data Byte loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. See Figure 11 for the address, acknowledge, and data transfer sequence.

### Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte plus the subsequent ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte plus its associated ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be effected.

### Acknowledge Polling

The disabling of the inputs during high voltage cycles can be used to take advantage of the typical 5ms write cycle time. Once the stop condition is issued to indicate the end of the master's byte load operation, the device initiates the internal high voltage cycle. Acknowledge polling can be initiated immediately. To do this, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the high voltage cycle then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. See Figure 13.

### Serial Read Operations

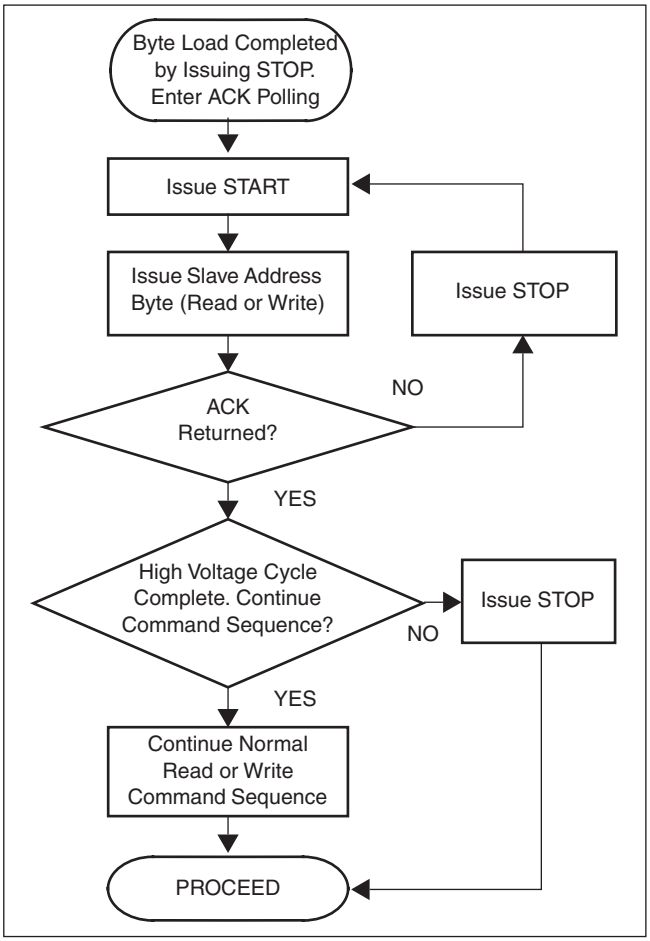
Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

### Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power up, the address of the address counter is undefined, requiring a read or write operation for initialization.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. See figure 15 for the address, acknowledge, and data transfer sequence.

**Figure 13. Acknowledge Polling Sequence**




It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

### Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition and the Slave Address Byte, receives an acknowledge, then issues the Word Address Bytes. After acknowledging receipts of the Word Address Bytes, the master immediately issues another start condition and the Slave Address Byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. See Figure 16 for the address, acknowledge, and data transfer sequence.

A similar operation called “Set Current Address” where the device will perform this operation if a stop is issued instead of the second start shown in Figure 15. The device will go into standby mode after the stop and all bus activity will be ignored until a start is detected. This operation loads the new address into the address counter. The next Current Address Read operation will read from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

### Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first Data Byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter “rolls over” to address 0000h and the device continues to output data for each acknowledge received. See Figure 17 for the acknowledge and data transfer sequence.

## SERIAL DEVICE ADDRESSING

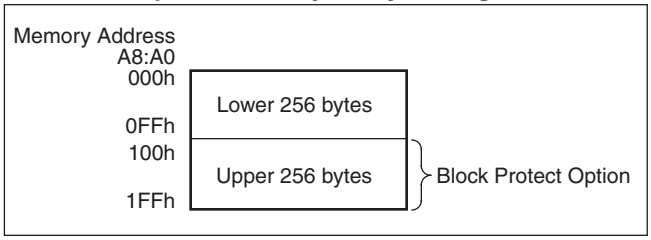
### Memory Address Map

CR, Control Register, CR7: CR0
Address: $1FF_{hex}$

FDR, Fault DetectionRegister, FDR7: FDR0
Address: $0FF_{hex}$

General Purpose Memory Organization, A8:A0
Address: 000h to 1FFh

### General Purpose Memory Array Configuration




### Slave Address Byte

Following a start condition, the master must output a Slave Address Byte. This byte consists of several parts:

– a device type identifier that is always ‘101x’. Where x=0 is for Array, x=1 is for Control Register or Fault Detection Register.

– next two bits are ‘0’.

– next bit that becomes the MSB of the address.

**Figure 14. X40430/31/34/35 Addressing**

| | Slave Byte | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| General Purpose Memory | 1 | 0 | 1 | 0 | 0 | 0 | A8 | R/$\overline{W}$ |
| Control Register | 1 | 0 | 1 | 1 | 0 | 0 | 1 | R/$\overline{W}$ |
| Fault Detection Register | 1 | 0 | 1 | 1 | 0 | 0 | 0 | R/$\overline{W}$ |

| | Word Address | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| General Purpose Memory | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Control Register | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Fault Detection Register | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Figure 15. Current Address Read Sequence**

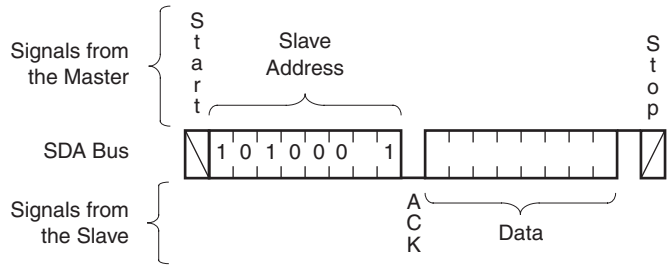
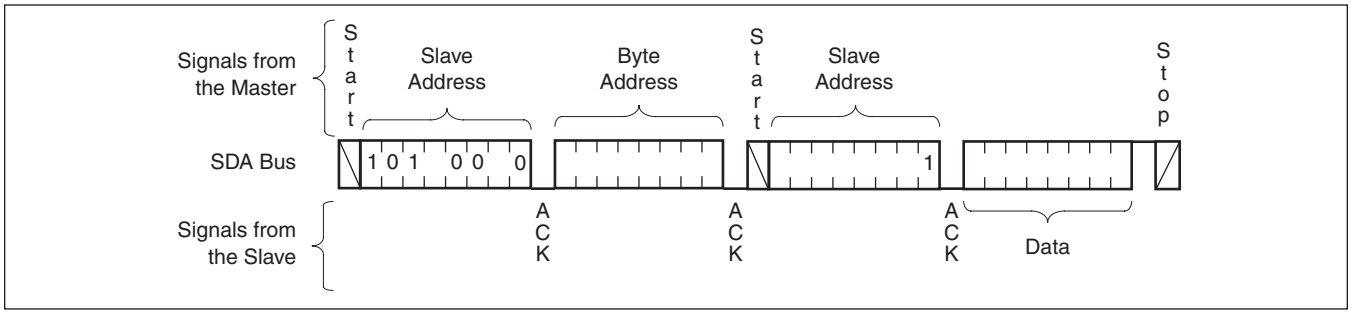


**Figure 16. Random Address Read Sequence**




– last bit of the slave command byte is a R/$\overline{W}$ bit. The R/$\overline{W}$ bit of the Slave Address Byte defines the operation to be performed. When the R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation.

### Word Address

The word address is either supplied by the master or obtained from an internal counter. The internal counter is undefined on a power up condition.

### Operational Notes

The device powers-up in the following state:

– The device is in the low power standby state.

– The WEL bit is set to '0'. In this state it is not possible to write to the device.

– SDA pin is the input mode.

– RESET/$\overline{RESET}$ Signal is active for $t_{PURST}$.

### Data Protection

The following circuitry has been included to prevent inadvertent writes:

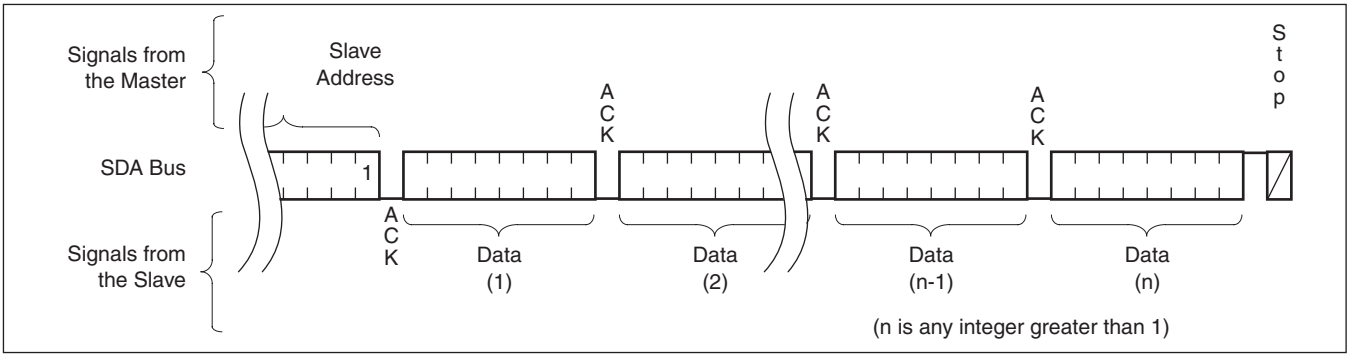
– The WEL bit must be set to allow write operations.

– The proper clock count and bit sequence is required prior to the stop bit in order to start a nonvolatile write cycle.

– A three step sequence is required before writing into the Control Register to change Watchdog Timer or Block Lock settings.

– The WP pin, when held HIGH, prevents all writes to the array and all the Register.

**Figure 17. Sequential Read Sequence**



### ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... –65°C to +135°C
Storage temperature ..... –65°C to +150°C
Voltage on any pin with
respect to $V_{SS}$ .....–1.0V to +7V
D.C. output current ..... 5mA
Lead temperature (soldering, 10 seconds)..... 300°C

### COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

| Temperature | Min. | Max. |
|---|---|---|
| Commercial | 0°C | 70°C |
| Industrial | –40°C | +85°C |

| Version | Chip Supply Voltage | Monitored* Voltages |
|---|---|---|
| X40430/31 | 2.7V to 5.5V | 1.7V to 5.5V |
| X40434/35 | 2.7V to 5.5V | 1.0V to 5.5V |

*See Ordering Info

### D.C. OPERATING CHARACTERISTICS

(Over the recommended operating conditions unless otherwise specified)

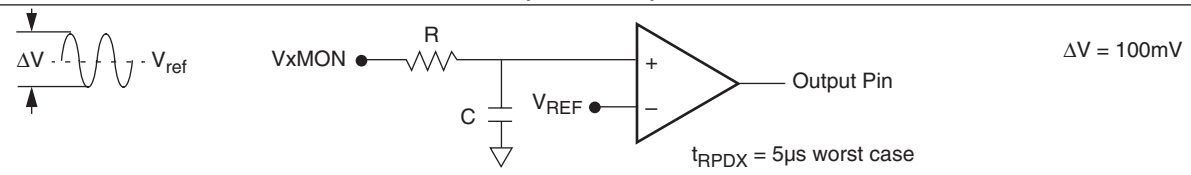
| Symbol | Parameter | Min. | Typ.(4) | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{CC1}$(1) | Active Supply Current ($V_{CC}$) Read | | | 1.5 | mA | $V_{IL} = V_{CC}$ x 0.1<br>$V_{IH} = V_{CC}$ x 0.9,<br>$f_{SCL}$ = 400kHz |
| $I_{CC2}$(1) | Active Supply Current ($V_{CC}$) Write | | | 3.0 | mA | |
| $I_{SB1}$(1)(6) | Standby Current ($V_{CC}$) AC (WDT off) | | 6 | 10 | µA | $V_{IL} = V_{CC}$ x 0.1<br>VIH = $V_{CC}$ x 0.9<br>$f_{SCL}$, $f_{SDA}$ = 400kHz |
| $I_{SB2}$(2)(6) | Standby Current ($V_{CC}$) DC (WDT on) | | 25 | 30 | µA | $V_{SDA} = V_{SCL} = V_{CC}$<br>Others = GND or $V_{CC}$ |
| $I_{LI}$ | Input Leakage Current (SCL, $\overline{MR}$, WP) | | | 10 | µA | $V_{IL}$ = GND to $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current (SDA, $\overline{V2FAIL}$, $\overline{V3FAIL}$, $\overline{WDO}$, $\overline{RESET}$) | | | 10 | µA | $V_{SDA}$ = GND to $V_{CC}$<br>Device is in Standby(2) |
| $V_{IL}$(3) | Input LOW Voltage (SDA, SCL, $\overline{MR}$, WP) | -0.5 | | $V_{CC}$ x 0.3 | V | |
| $V_{IH}$(3) | Input HIGH Voltage (SDA, SCL, $\overline{MR}$, WP) | $V_{CC}$ x 0.7 | | $V_{CC}$ + 0.5 | V | |
| $V_{HYS}$(6) | Schmitt Trigger Input Hysteresis<br>• Fixed input level<br>• $V_{CC}$ related level | <br>0.2<br>.05 x $V_{CC}$ | | | <br>V<br>V | |
| $V_{OL}$ | Output LOW Voltage (SDA, RESET/ $\overline{RESET}$, $\overline{LOWLINE}$, $\overline{V2FAIL}$, $\overline{V3FAIL}$, $\overline{WDO}$) | | | 0.4 | V | $I_{OL}$ = 3.0mA (2.7-5.5V)<br>$I_{OL}$ = 1.8mA (2.7-3.6V) |
| $V_{OH}$ | Output (RESET, $\overline{LOWLINE}$) HIGH Voltage | $V_{CC}$ – 0.8<br>$V_{CC}$ – 0.4 | | | V | $I_{OH}$ = -1.0mA (2.7-5.5V)<br>$I_{OH}$ = -0.4mA (2.7-3.6V) |

**D.C. OPERATING CHARACTERISTICS** (Continued)
(Over the recommended operating conditions unless otherwise specified)

| Symbol | Parameter | Min. | Typ.(4) | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| **$V_{CC}$ Supply** | | | | | | |
| $V_{TRIP1}$(5) | $V_{CC}$ Trip Point Voltage Range | 2.0 | | 4.75 | V | |
| | | 4.55 | 4.6 | 4.65 | V | X40430/31-A, X40434/35 |
| | | 4.35 | 4.4 | 4.45 | V | X40430/31-B |
| | | 2.85 | 2.9 | 2.95 | V | X40430/31-C |
| **Second Supply Monitor** | | | | | | |
| $I_{V2}$ | V2MON Current | | | 15 | µA | |
| $V_{TRIP2}$(5) | V2MON Trip Point Voltage Range | 1.7<br>0.9 | | 4.75<br>3.5 | V<br>V | x40430/31<br>x40434/35 |
| | | 2.85 | 2.9 | 2.95 | V | X40430/31-A |
| | | 2.55 | 2.6 | 2.65 | V | X40430/31-B |
| | | 2.15 | 2.2 | 2.25 | V | X40430/31-C |
| | | 1.25 | 1.3 | 1.35 | V | X40434/35-A&B |
| | | 0.95 | 1.0 | 1.05 | V | X40434/35-C |
| $t_{RPD2}$(6) | $V_{TRIP2}$ to $\overline{V2FAIL}$ | | | 5 | µs | |
| **Third Supply Monitor** | | | | | | |
| $I_{V3}$ | V3MON Current | | | 15 | µA | |
| $V_{TRIP3}$(5) | V3MON Trip Point Voltage Range | 1.7 | | 4.75 | V | |
| | | 1.65 | 1.7 | 1.75 | V | X40430/31 |
| | | 3.05 | 3.1 | 3.15 | V | X40434/35-A |
| | | 2.85 | 2.9 | 2.95 | V | X40434/35-B&C |
| $t_{RPD3}$(6) | $V_{TRIP3}$ to $\overline{V3FAIL}$ | | | 5 | µs | |

**Notes:** (1) The device enters the Active state after any start, and remains active until: 9 clock cycles later if the Device Select Bits in the Slave Address Byte are incorrect; 200ns after a stop ending a read operation; or $t_{WC}$ after a stop ending a write operation.
(2) The device goes into Standby: 200ns after any stop, except those that initiate a high voltage write cycle; $t_{WC}$ after a stop that initiates a high voltage cycle; or 9 clock cycles after any start that is not followed by the correct Device Select Bits in the Slave Address Byte.
(3) $V_{IL}$ Min. and $V_{IH}$ Max. are for reference only and are not tested.
(4) At 25°C, $V_{CC}$ = 3V
(5) See ordering information for standard programming levels. For custom programmed levels, contact factory.
(6) Based on characterization data.

**EQUIVALENT INPUT CIRCUIT FOR VxMON (x = 1, 2, 3)**

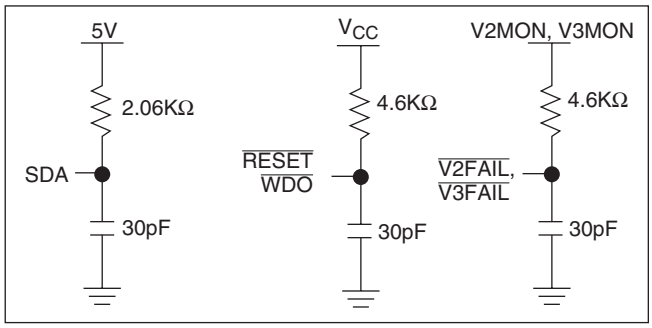



**CAPACITANCE**

| Symbol | Parameter | Max. | Unit | Test Conditions |
|---|---|---|---|---|
| $C_{OUT}$(1) | Output Capacitance (SDA, RESET/$\overline{RESET}$, $\overline{LOWLINE}$, $\overline{V2FAIL}$,$\overline{V3FAIL}$, $\overline{WDO}$) | 8 | pF | $V_{OUT}$ = 0V |
| $C_{IN}$(1) | Input Capacitance (SCL, WP, $\overline{MR}$) | 6 | pF | $V_{IN}$ = 0V |

**Note:** (1) This parameter is not 100% tested.

### EQUIVALENT A.C. OUTPUT LOAD CIRCUIT FOR $V_{CC}$ = 5V




### A.C. TEST CONDITIONS

| | |
|---|---|
| Input pulse levels | $V_{CC}$ x 0.1 to $V_{CC}$ x 0.9 |
| Input rise and fall times | 10ns |
| Input and output timing levels | $V_{CC}$ x 0.5 |
| Output load | Standard output load |

### SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from LOW to HIGH | Will change from LOW to HIGH |
| | May change from HIGH to LOW | Will change from HIGH to LOW |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

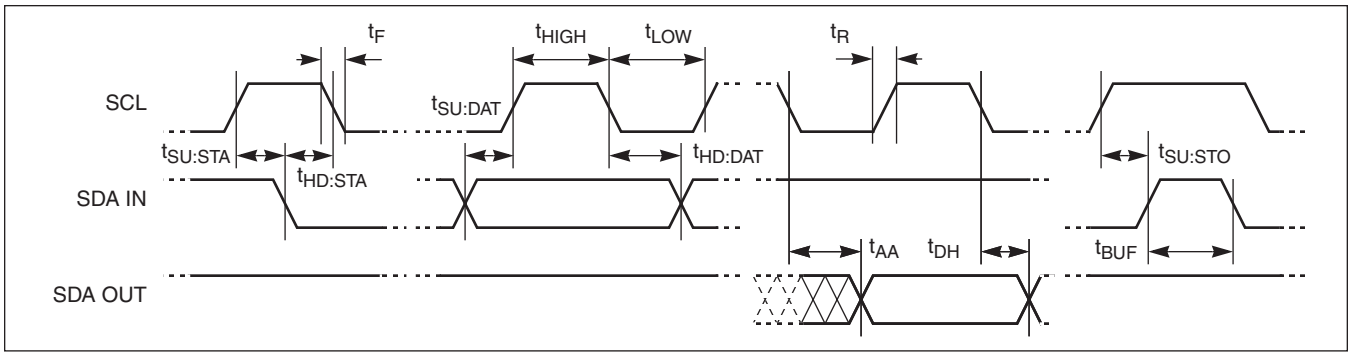
## A.C. CHARACTERISTICS

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $f_{SCL}$ | SCL Clock Frequency | | 400 | kHz |
| $t_{IN}$ | Pulse width Suppression Time at inputs | 50 | | ns |
| $t_{AA}$ | SCL LOW to SDA Data Out Valid | 0.1 | 0.9 | µs |
| $t_{BUF}$ | Time the bus free before start of new transmission | 1.3 | | µs |
| $t_{LOW}$ | Clock LOW Time | 1.3 | | µs |
| $t_{HIGH}$ | Clock HIGH Time | 0.6 | | µs |
| $t_{SU:STA}$ | Start Condition Setup Time | 0.6 | | µs |
| $t_{HD:STA}$ | Start Condition Hold Time | 0.6 | | µs |
| $t_{SU:DAT}$ | Data In Setup Time | 100 | | ns |
| $t_{HD:DAT}$ | Data In Hold Time | 0 | | µs |
| $t_{SU:STO}$ | Stop Condition Setup Time | 0.6 | | µs |
| $t_{DH}$ | Data Output Hold Time | 50 | | ns |
| $t_R$ | SDA and SCL Rise Time | 20 +.1Cb(1) | 300 | ns |
| $t_F$ | SDA and SCL Fall Time | 20 +.1Cb(1) | 300 | ns |
| $t_{SU:WP}$ | WP Setup Time | 0.6 | | µs |
| $t_{HD:WP}$ | WP Hold Time | 0 | | µs |
| Cb | Capacitive load for each bus line | | 400 | pF |

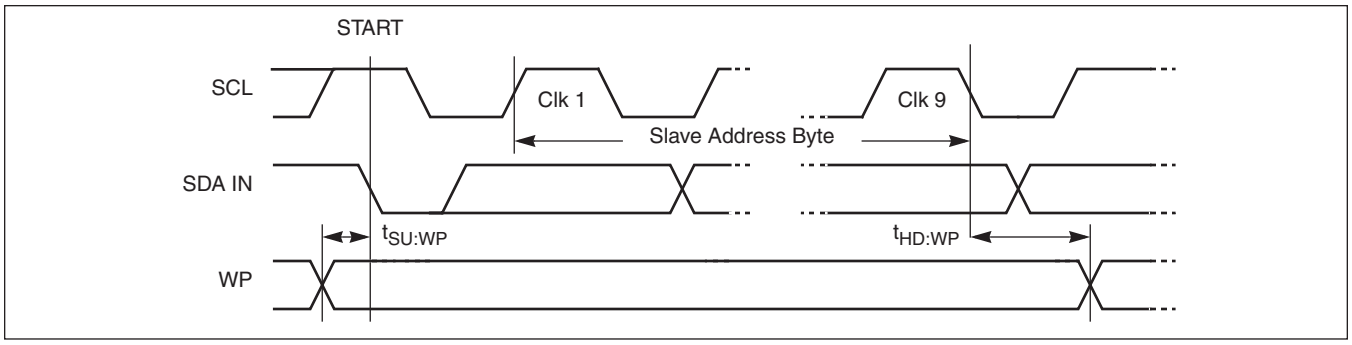
**Note:** (1) Cb = total capacitance of one bus line in pF.

## TIMING DIAGRAMS

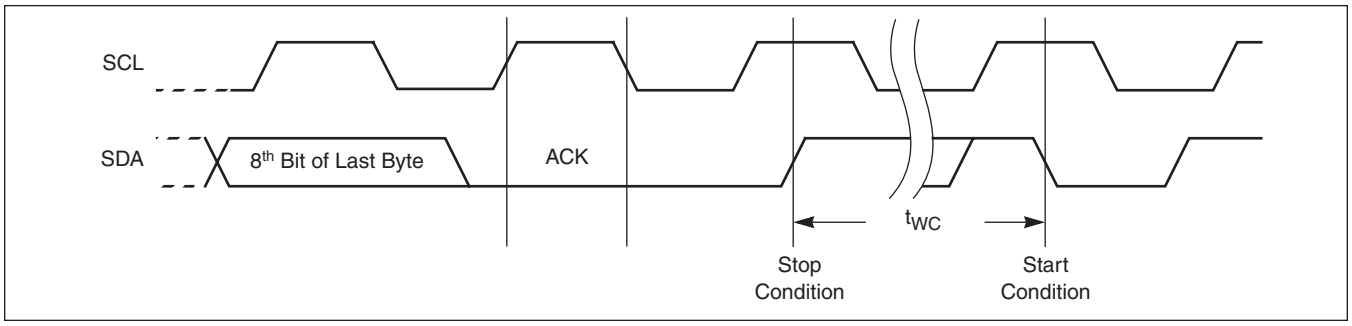
### Bus Timing



### WP Pin Timing




### Write Cycle Timing

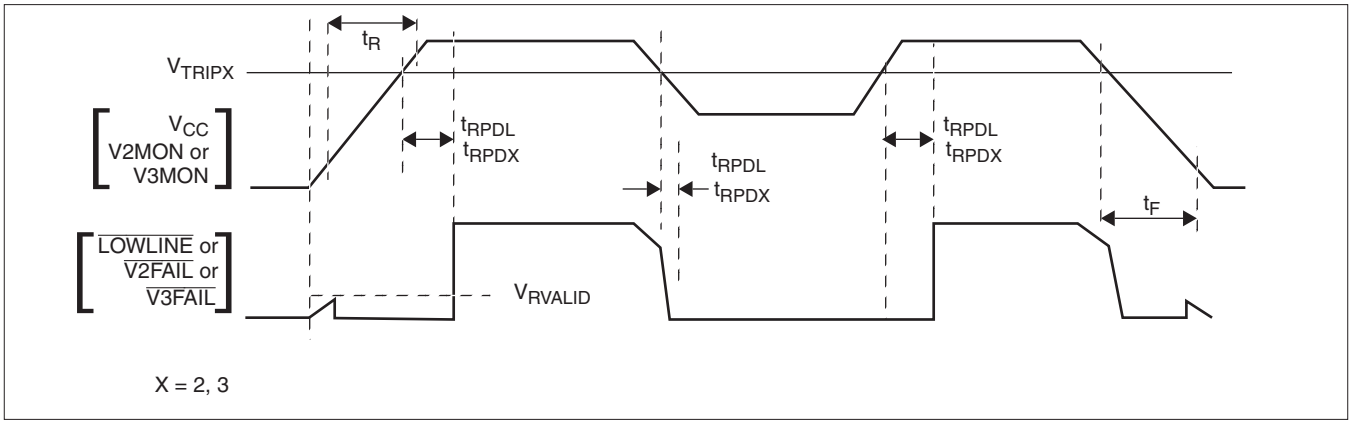



### Nonvolatile Write Cycle Timing

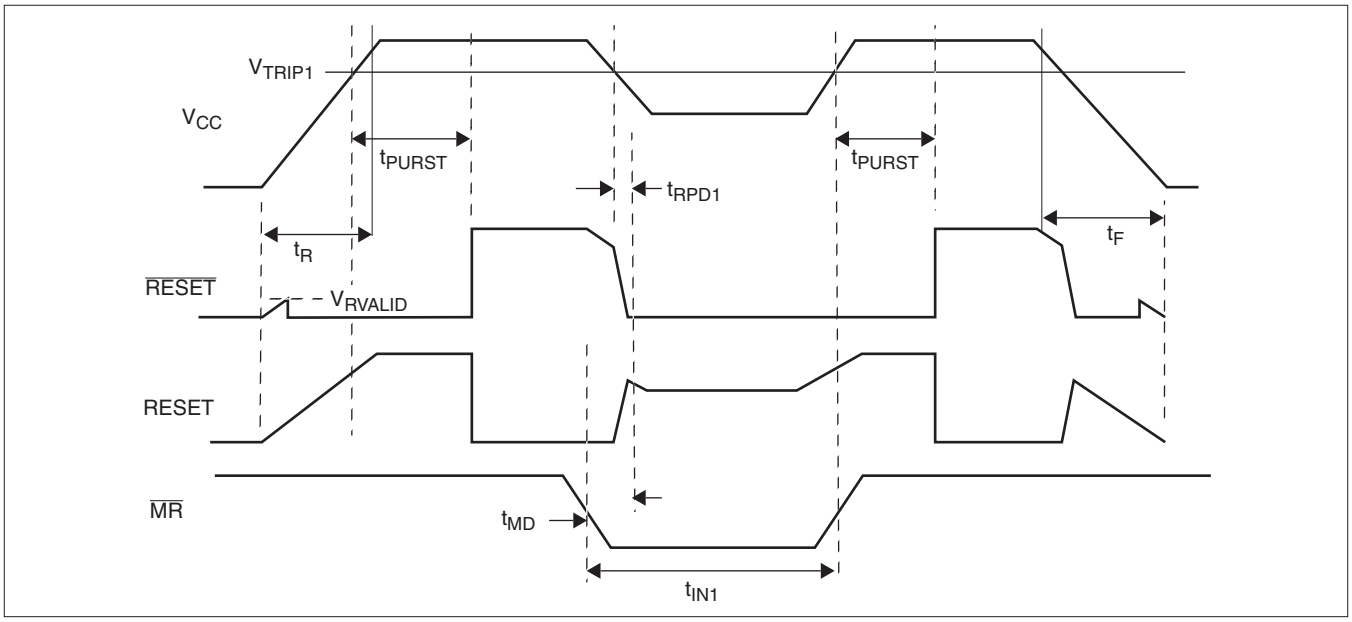
| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{WC}$(1) | Write Cycle Time | | 5 | 10 | ms |

**Note:** (1) $t_{WC}$ is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

### Power Fail Timings



### RESET/$\overline{\text{RESET}}$/$\overline{\text{MR}}$ Timings

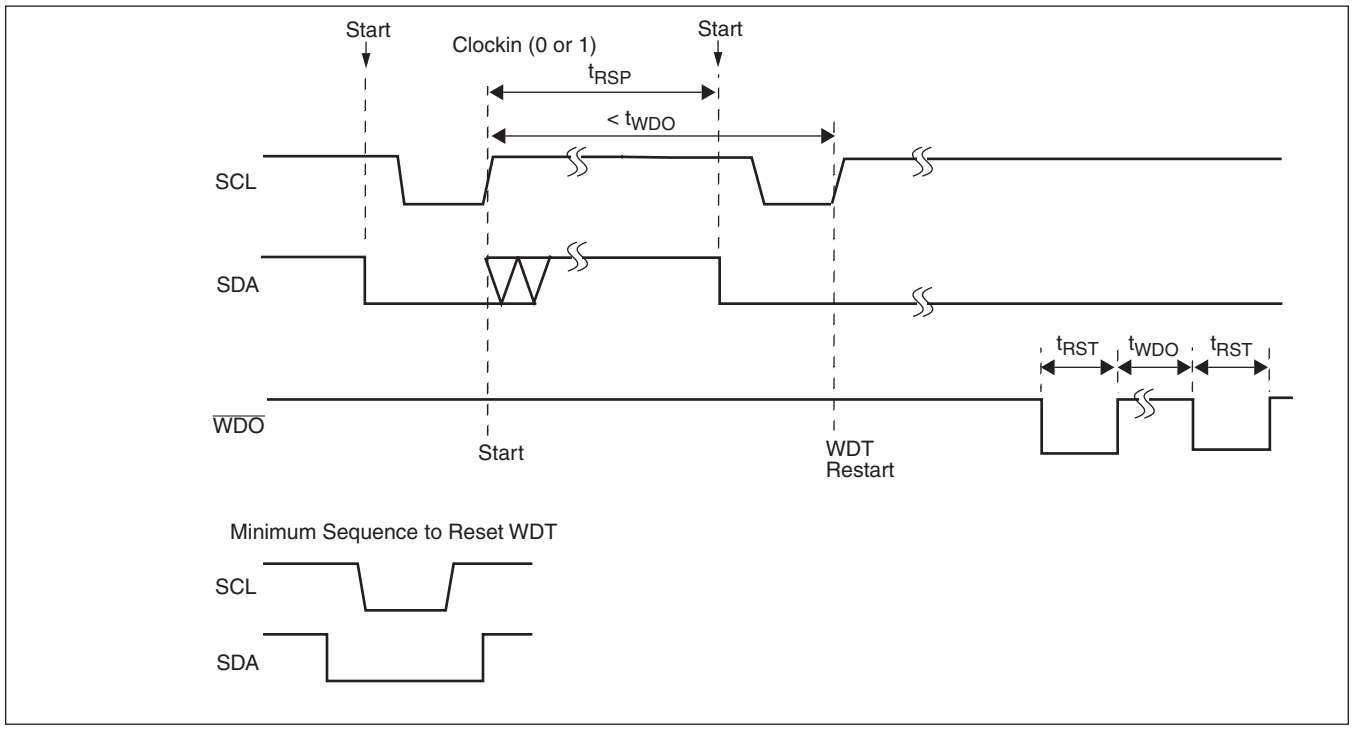



### LOW VOLTAGE AND WATCHDOG TIMINGS PARAMETERS (@25°C, $V_{CC}$ = 5V)

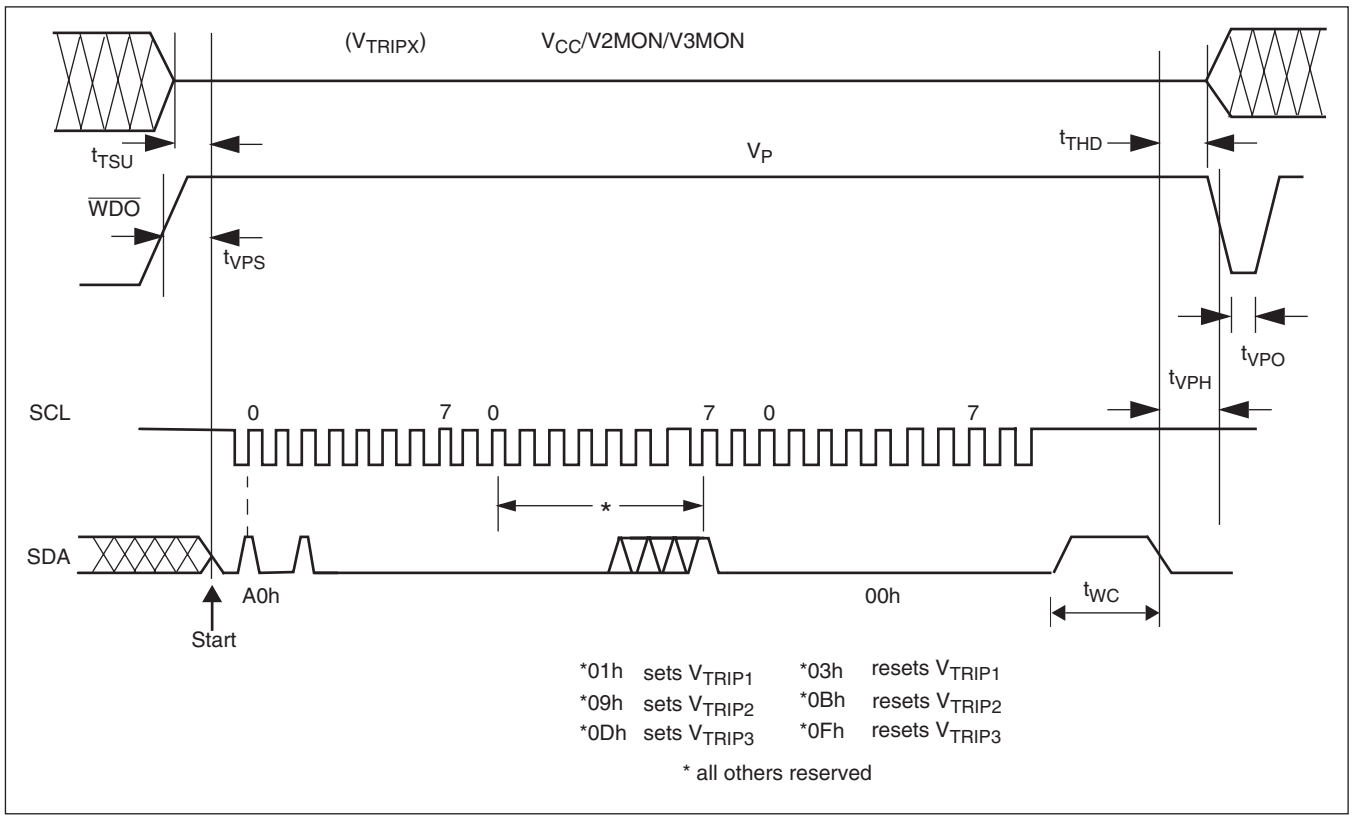
| Symbol | Parameters | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|
| $t_{RPD1}$(2)<br>$t_{RPDL}$ | $V_{TRIP1}$ to $\overline{\text{RESET}}$/RESET (Power down only)<br>$V_{TRIP1}$ to $\overline{\text{LOWLINE}}$ | | | 5 | µs |
| $t_{LR}$ | $\overline{\text{LOWLINE}}$ to RESET/$\overline{\text{RESET}}$ delay (Power down only) [= $t_{RPD1}$-$t_{RPDL}$] | | 500 | | ns |
| $t_{RPDX}$(2) | $V_{TRIP2}$ to $\overline{\text{V2FAIL}}$, or $V_{TRIP3}$ to $\overline{\text{V3FAIL}}$ (x = 2, 3) | | | 5 | µs |
| $t_{PURST}$ | Power On Reset delay:<br>PUP1=0, PUP0=0<br>PUP1=0, PUP0=1 (factory setting)<br>PUP1=1, PUP0=0<br>PUP1=1, PUP0=1 | | <br>50(2)<br>200<br>400(2)<br>800(2) | | <br>ms<br>ms<br>ms<br>ms |
| $t_F$ | $V_{CC}$, V2MON, V3MON, Fall Time | 20 | | | mV/µs |
| $t_R$ | $V_{CC}$, V2MON, V3MON, Rise Time | 20 | | | mV/µs |
| $V_{RVALID}$ | Reset Valid $V_{CC}$ | 1 | | | V |
| $t_{MD}$(2) | $\overline{\text{MR}}$ to RESET/ $\overline{\text{RESET}}$ delay (activation only) | 500 | | | ns |
| $t_{in1}$ | Pulse width for $\overline{\text{MR}}$ | 5 | | | µs |
| $t_{WDO}$ | Watchdog Timer Period:<br>WD1=0, WD0=0<br>WD1=0, WD0=1<br>WD1=1, WD0=0<br>WD1=1, WD0=1 (factory setting) | | <br>1.4(2)<br>200(2)<br>25<br>OFF | | <br>s<br>ms<br>ms |
| $t_{RST1}$ | Watchdog Reset Time Out Delay<br>WD1=0, WD0=0<br>WD1=0, WD0=1 | 100 | 200 | 300 | ms |
| $t_{RST2}$ | Watchdog Reset Time Out Delay WD1=1, WD0=0 | 12.5 | 25 | 37.5 | ms |
| $t_{RSP}$ | Watchdog timer restart pulse width | 1 | | | µs |

**Notes:** (1) $V_{CC}$ = 5V at 25°C.
(2) Values based on characterization data only.

### Watchdog Time Out For 2-Wire Interface




### $V_{TRIPX}$ Set/Reset Conditions

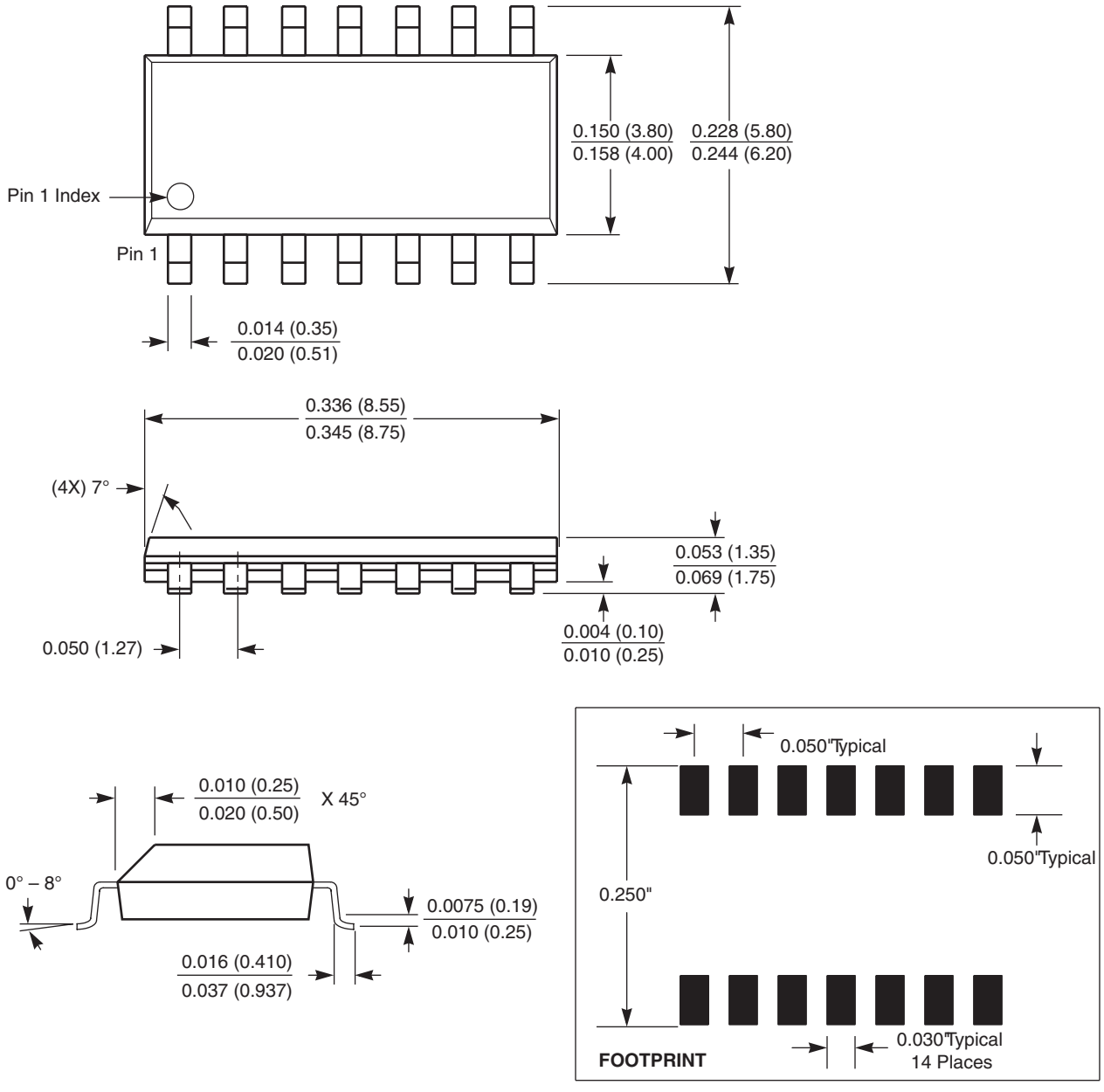


**$V_{TRIP1}$, $V_{TRIP2}$, $V_{TRIP3}$ Programming Specifications: $V_{CC}$ = 2.0–5.5V; Temperature = 25°C**

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{VPS}$ | $\overline{WDO}$ Program Voltage Setup time | 10 | | µs |
| $t_{VPH}$ | $\overline{WDO}$ Program Voltage Hold time | 10 | | µs |
| $t_{TSU}$ | $V_{TRIPX}$ Level Setup time | 10 | | µs |
| $t_{THD}$ | $V_{TRIPX}$ Level Hold (stable) time | 10 | | µs |
| $t_{WC}$ | $V_{TRIPX}$ Program Cycle | 10 | | ms |
| $t_{VPO}$ | Program Voltage Off time before next cycle | 1 | | ms |
| $V_P$ | Programming Voltage | 15 | 18 | V |
| $V_{TRAN1}$ | $V_{TRIP1}$ Set Voltage Range | 2.0 | 4.75 | V |
| $V_{TRAN2}$ | $V_{TRIP2}$ Set Voltage Range – X40430/31 | 1.7 | 4.75 | V |
| $V_{TRAN2A}$ | $V_{TRIP2}$ Set to Voltage Range – X40434/35 | 0.9 | 3.5 | V |
| $V_{TRAN3}$ | $V_{TRIP3}$ Set Voltage Range | 1.7 | 4.75 | V |
| $V_{tv}$ | $V_{TRIPX}$ Set Voltage variation after programming (-40 to +85°C). | -25 | +25 | mV |
| $t_{VPS}$ | $\overline{WDO}$ Program Voltage Setup time | 10 | | µs |

## PACKAGING INFORMATION

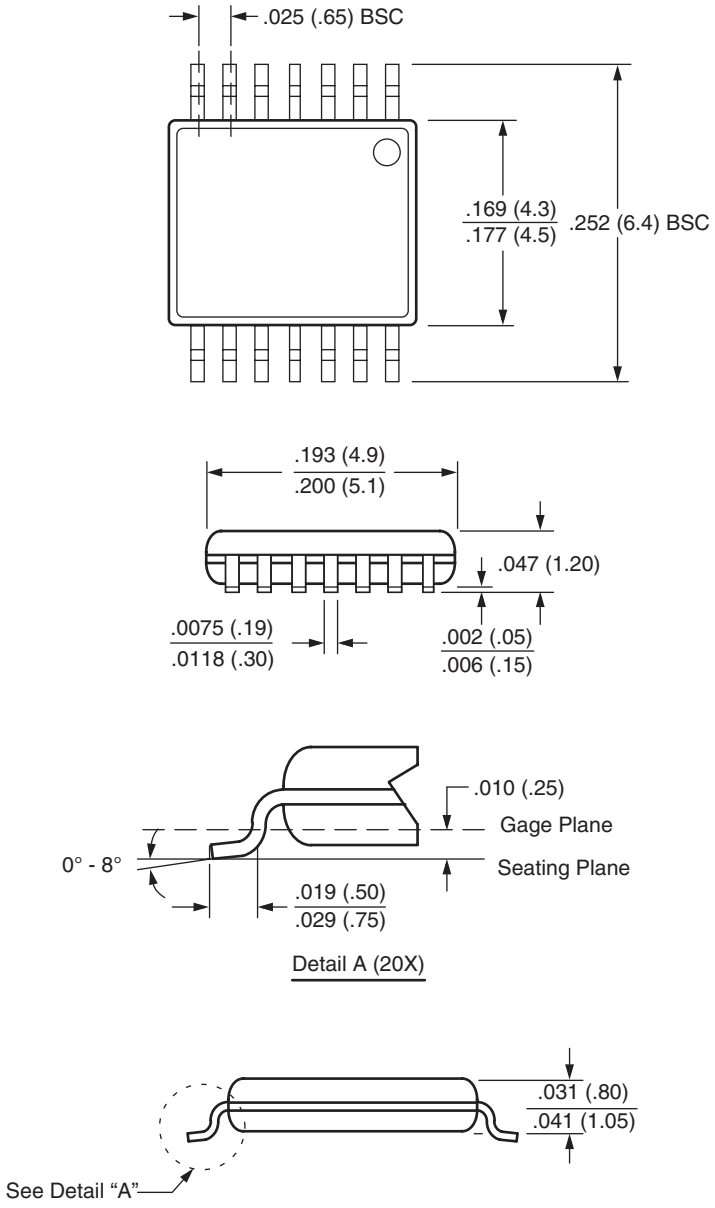
### 14-Lead Plastic Small Outline Gullwing Package Type S




**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

## PACKAGING INFORMATION

### 14-Lead Plastic, TSSOP, Package Type V




**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

## ORDERING INFORMATION

| Monitored $V_{CC}$ Supplies | $V_{TRIP1}$ Range | $V_{TRIP2}$ Range | $V_{TRIP3}$ Range | Package | Operating Temperature Range | Part Number with RESET | Part Number with $\overline{\text{RESET}}$ |
|---|---|---|---|---|---|---|---|
| 1.7-5.5 | 4.6V±50mV | 2.9V±50mV | 1.7V±50mV | 14L SOIC | 0ºC–70ºC | X40430S14-A | X40431S14-A |
| | | | | | -40ºC–85ºC | X40430S14I-A | X40431S14I-A |
| | | | | 14L TSSOP | 0ºC–70ºC | X40430V14-A | X40431V14-A |
| | | | | | -40ºC–85ºC | X40430V14I-A | X40431V14I-A |
| 1.7-5.5 | 4.4V±50mV | 2.6V±50mV | 1.7V±50mV | 14L SOIC | 0ºC–70ºC | X40430S14-B | X40431S14-B |
| | | | | | -40ºC–85ºC | X40430S14I-B | X40431S14I-B |
| | | | | 14L TSSOP | 0ºC–70ºC | X40430V14-B | X40431V14-B |
| | | | | | -40ºC–85ºC | X40430V14I-B | X40431V14I-B |
| 1.7-3.6 | 2.9V±50mV | 2.2V±50mV | 1.7V±50mV | 14L SOIC | 0ºC–70ºC | X40430S14-C | X40431S14-C |
| | | | | | -40ºC–85ºC | X40430S14I-C | X40431S14I-C |
| | | | | 14L TSSOP | 0ºC–70ºC | X40430V14-C | X40431V14-C |
| | | | | | -40ºC–85ºC | X40430V14I-C | X40431V14I-C |
| 1.3-5.5 | 4.6V±50mV | 1.3V±50mV | 3.1V±50mV | 14L SOIC | 0ºC–70ºC | X40434S14-A | X40435S14-A |
| | | | | | -40ºC–85ºC | X40434S14I-A | X40435S14I-A |
| | | | | 14L TSSOP | 0ºC–70ºC | X40434V14-A | X40435V14-A |
| | | | | | -40ºC–85ºC | X40434V14I-A | X40435V14I-A |
| 1.3-5.5 | 4.6V±50mV | 1.3V±50mV | 2.9V±50mV | 14L SOIC | 0ºC–70ºC | X40434S14-B | X40435S14-B |
| | | | | | -40ºC–85ºC | X40434S14I-B | X40435S14I-B |
| | | | | 14L TSSOP | 0ºC–70ºC | X40434V14-B | X40435V14-B |
| | | | | | -40ºC–85ºC | X40434V14I-B | X40435V14I-B |
| 1.0-5.5 | 4.6V±50mV | 1.0V±50mV | 2.9V±50mV | 14L SOIC | 0ºC–70ºC | X40434S14-C | X40435S14-C |
| | | | | | -40ºC–85ºC | X40434S14I-C | X40435S14I-C |
| | | | | 14L TSSOP | 0ºC–70ºC | X40434V14-C | X40435V14-C |
| | | | | | -40ºC–85ºC | X40434V14I-C | X40435V14I-C |

## PART MARK INFORMATION