APPLICATION NOTES
AVAILABLE
AN99 • AN115 • AN120 • AN124 • AN133 • AN134 • AN135

XICOR®

Low Noise/Low Power/2-Wire Bus

X9429

Single Digitally Controlled Potentiometer (XDCP™)

FEATURES

- **Single Voltage Potentiometer**
- **64 Resistor Taps**
- **2-wire Serial Interface for write, read, and transfer operations of the potentiometer**
- **Wiper Resistance, 150Ω Typical at 5V**
- **Non-Volatile Storage of Multiple Wiper Positions**
- **Power On Recall. Loads Saved Wiper Position on Power Up.**
- **Standby Current < 5µA Max**
- **V_{CC} : 2.7V to 5.5V Operation**
- **2.5KΩ, 10KΩ Total Pot Resistance**
- **Endurance: 100, 000 Data Changes per Bit per Register**
- **100 yr. Data Retention**
- **14-Lead TSSOP, 16-Lead SOIC**
- **Low Power CMOS**

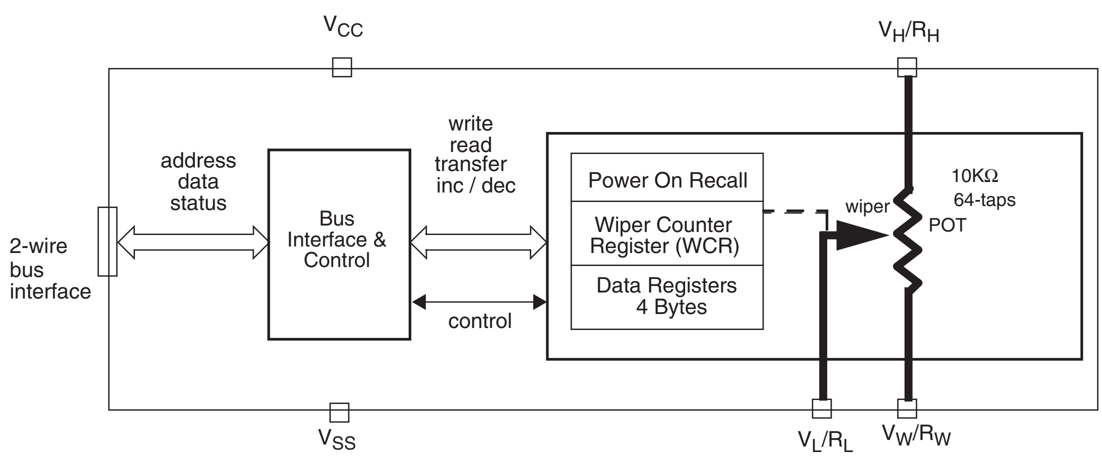
DESCRIPTION

The X9429 integrates a single digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

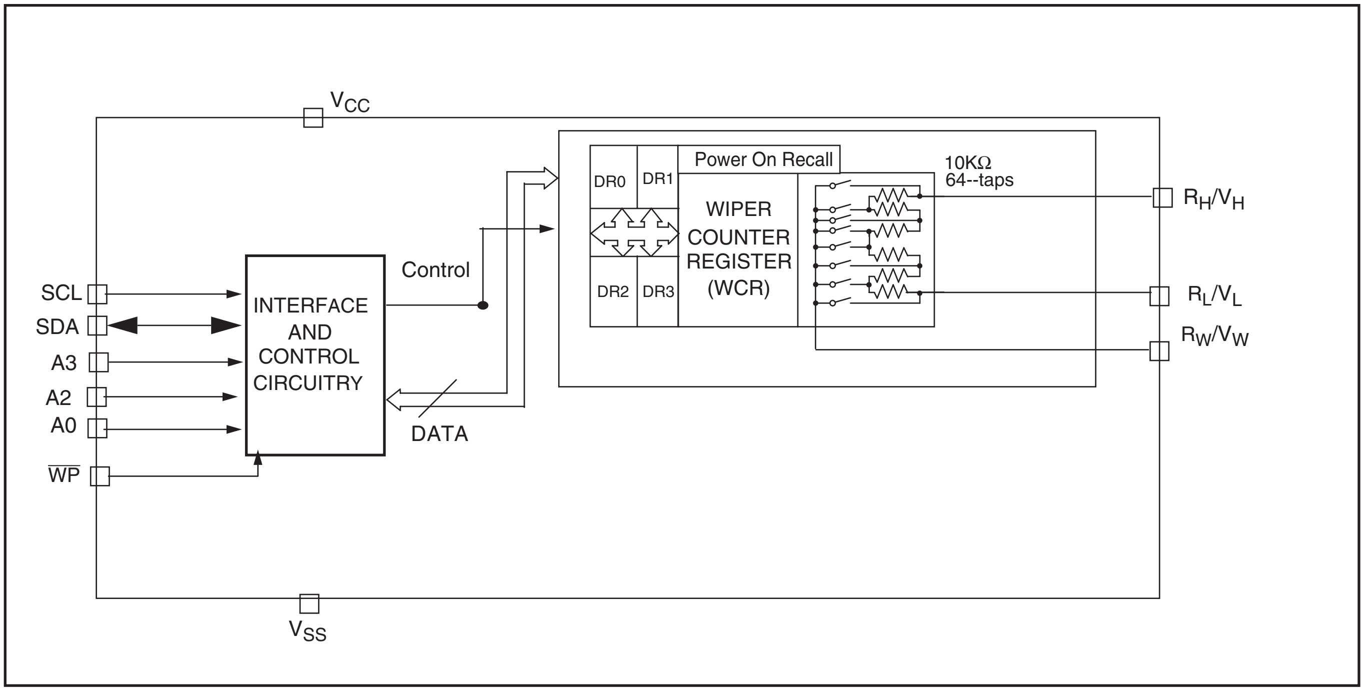
The digital controlled potentiometer is implemented using 63 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-wire bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and a four non-volatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array though the switches. Powerup recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

BLOCK DIAGRAM



DETAILED FUNCTIONAL DIAGRAM



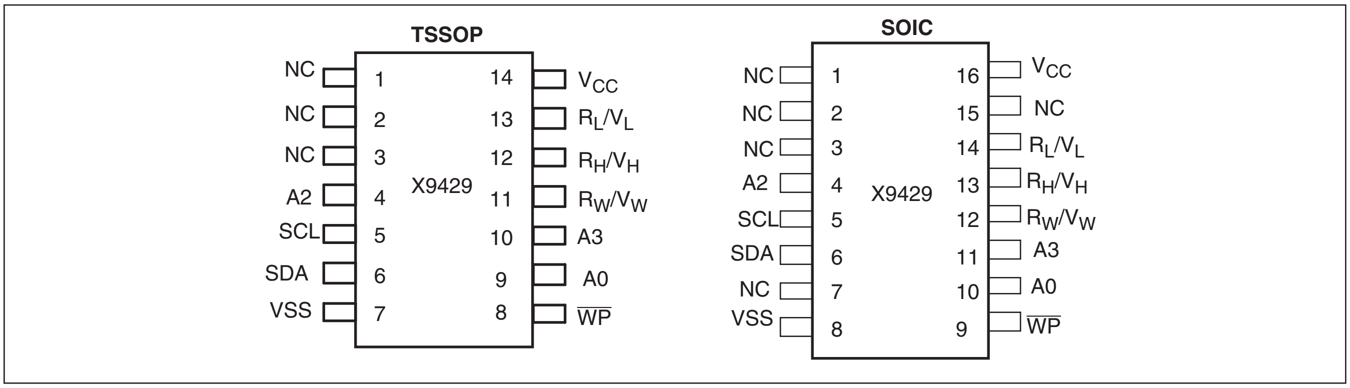
CIRCUIT LEVEL APPLICATIONS

- Vary the gain of a voltage amplifier
- Provide programmable dc reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the dc biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

SYSTEM LEVEL APPLICATIONS

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

PIN CONFIGURATION



PIN ASSIGNMENTS

TSSOP pin	SOIC pin	Symbol	Brief Description
1	1	NC	No Connect
2	2	NC	No Connect
3	3	NC	No Connect
4	4	A2	Device Address for 2-wire bus.
5	5	SCL	Serial Clock for 2-wire bus.
6	6	SDA	Serial Data Input/Output for 2-wire bus.
7	8	V_{SS}	System Ground
8	9	$\overline{WP}$	Hardware Write Protect
9	10	A0	Device Address for 2-wire bus.
10	11	A3	Device Address for 2-wire bus.
11	12	R_W / V_W	Wiper Terminal of the Potentiometer.
12	13	R_H / V_H	High Terminal of the Potentiometer.
13	14	R_L / V_L	Low Terminal of the Potentiometer.
14	16	V_{CC}	System Supply Voltage
	15	NC	No Connect
	7	NC	No Connect

PIN DESCRIPTIONS

Host Interface Pins

Serial Clock (SCL)

The SCL input is used to clock data into and out of the X9429.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

Device Address (A_0, A_2, A_3)

The Address inputs are used to set the least significant 3 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9429. A maximum of 8 devices may occupy the 2-wire serial bus.

Potentiometer Pins

R_H/V_H, R_L/V_L

The R_H/V_H and R_L/V_L inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

R_W/V_W

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

Hardware Write Protect Input $\overline{WP}$

The $\overline{WP}$ pin when low prevents nonvolatile writes to the Data Registers.

PRINCIPLES OF OPERATION

The X9429 is a highly integrated microcircuit incorporating a resistor array and its associated registers and counters and the serial interface logic providing direct communication between the host and the XDCP potentiometers.

Serial Interface

The X9429 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9429 will be considered a slave device in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods (t_{LOW}). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

Start Condition

All commands to the X9429 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH (t_{HIGH}). The X9429 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9429 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9429 will respond with a final acknowledge.

Array Description

The X9429 is comprised of a resistor array. The array contains 63 discrete resistive segments that are connected in series. The physical ends of the array are equivalent to the fixed terminals of a mechanical potentiometer (V_H/R_H and V_L/R_L inputs).

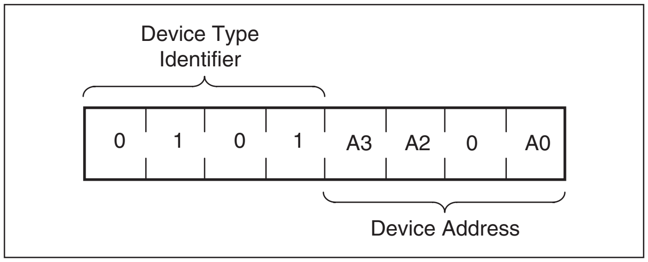
At both ends of the array and between each resistor segment is a CMOS switch connected to the wiper (V_W/R_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The six bits of the WCR are decoded to select, and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated Data Registers into the WCR. These Data Registers and the WCR can be read and written by the host system.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (refer to Figure 1). For the X9429 this is fixed as 0101[B].

Figure 1. Slave Address



The next four bits of the slave address are the device address. The physical device address is defined by the state of the A_0, A_2, and A_3 inputs. The X9429 compares the serial data stream with the address input state; a successful compare of all three address bits is required for the X9429 to respond with an acknowledge. The A_0, A_2, and A_3 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

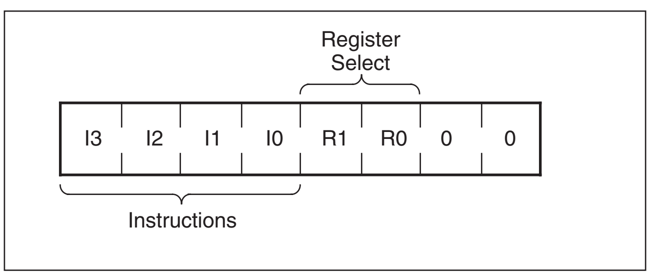
Acknowledge Polling

The disabling of the inputs, during the internal nonvolatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9429 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9429 is still busy with the write operation no ACK will be returned. If the X9429 has completed the write operation an ACK will be returned, and the master can then proceed with the next operation.

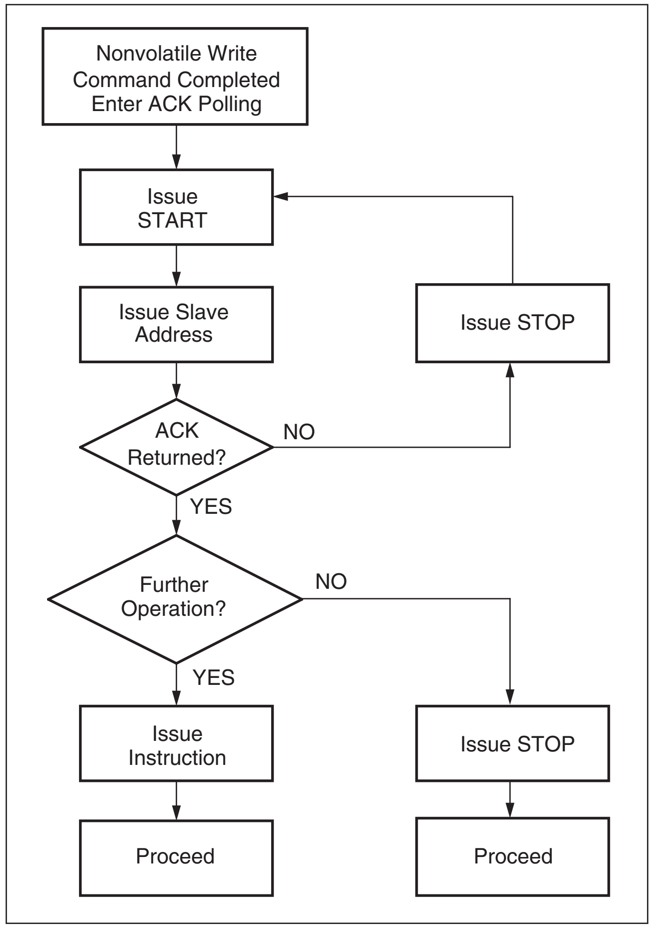
Instruction Structure

The next byte sent to the X9429 contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of four associated registers. The format is shown below in Figure 2.

Figure 2. Instruction Byte Format



Flow 1. ACK Polling Sequence

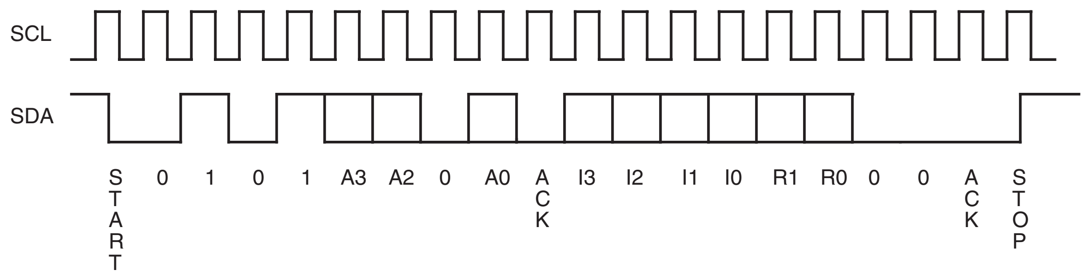


The four high order bits define the instruction. The next two bits (R1 and R0) select one of the four registers that is to be acted upon when a register oriented instruction is issued. Bits 0 and 1 are defined to be 0.

Four of the seven instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the Wiper Counter Register and one of the Data Registers. A transfer from a Data Register to a Wiper Counter Register is essentially a write to a static RAM. The response of the wiper to this action will be delayed t_{WRL}. A transfer from the Wiper Counter Register (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete.

Four instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9429; either between the host and one of the Data Registers or directly between the host and the Wiper Counter Register. These instructions are:

Figure 3. Two-Byte Instruction Sequence



Read Wiper Counter Register (read the current wiper position of the selected pot), write Wiper Counter Register (change current wiper position of the selected pot), read Data Register (read the contents of the selected nonvolatile register) and write Data Register (write a new value to the selected Data Register). The sequence of operations is shown in Figure 4.

The Increment/Decrement command is different from the other commands. Once the command is issued and the X9429 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the V_H/R_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the V_L/R_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figures 5 and 6 respectively.

Table 1. Instruction Set

Instruction	Instruction Set								Operation
	I_3	I_2	I_1	I_0	R_1	R_0	X_1	X_0	
Read Wiper Counter Register	1	0	0	1	0	0	0	0	Read the contents of the Wiper Counter Register
Write Wiper Counter Register	1	0	1	0	0	0	0	0	Write new value to the Wiper Counter Register
Read Data Register	1	0	1	1	1/0	1/0	0	0	Read the contents of the Data Register pointed to by R_1–R_0
Write Data Register	1	1	0	0	1/0	1/0	0	0	Write new value to the Data Register pointed to by R_1–R_0
XFR Data Register to Wiper Counter Register	1	1	0	1	1/0	1/0	0	0	Transfer the contents of the Data Register pointed to by R_1–R_0 to its Wiper Counter Register
XFR Wiper Counter Register to Data Register	1	1	1	0	1/0	1/0	0	0	Transfer the contents of the Wiper Counter Register to the Data Register pointed to by R_1–R_0
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	0	0	Enable Increment/decrement of the Wiper Counter Register

Note: (1) 1/0 = data is one or zero

Figure 4. Three-Byte Instruction Sequence

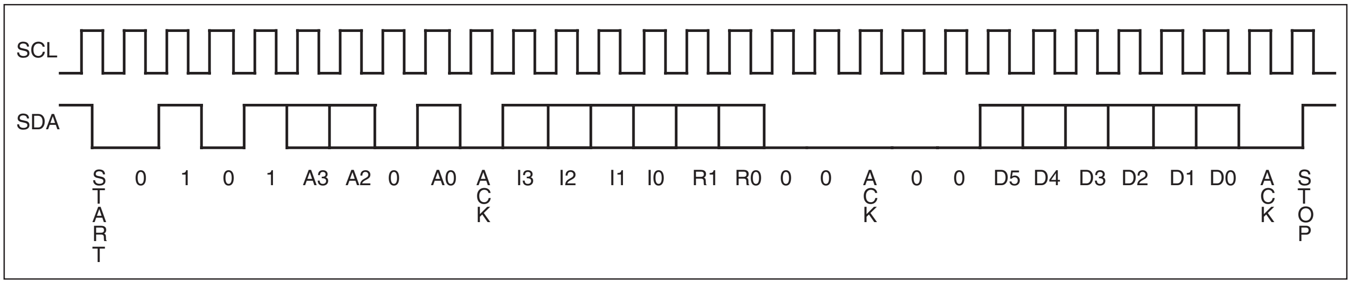


Figure 5. Increment/Decrement Instruction Sequence

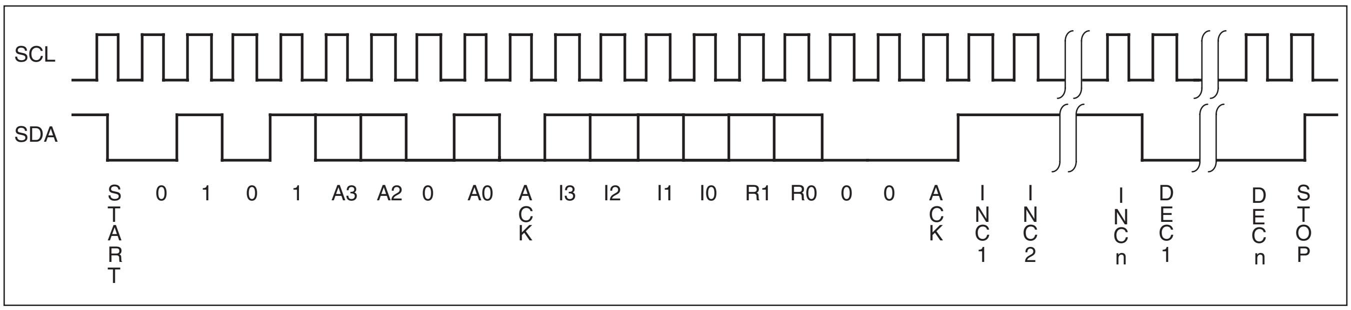


Figure 6. Increment/Decrement Timing Limits

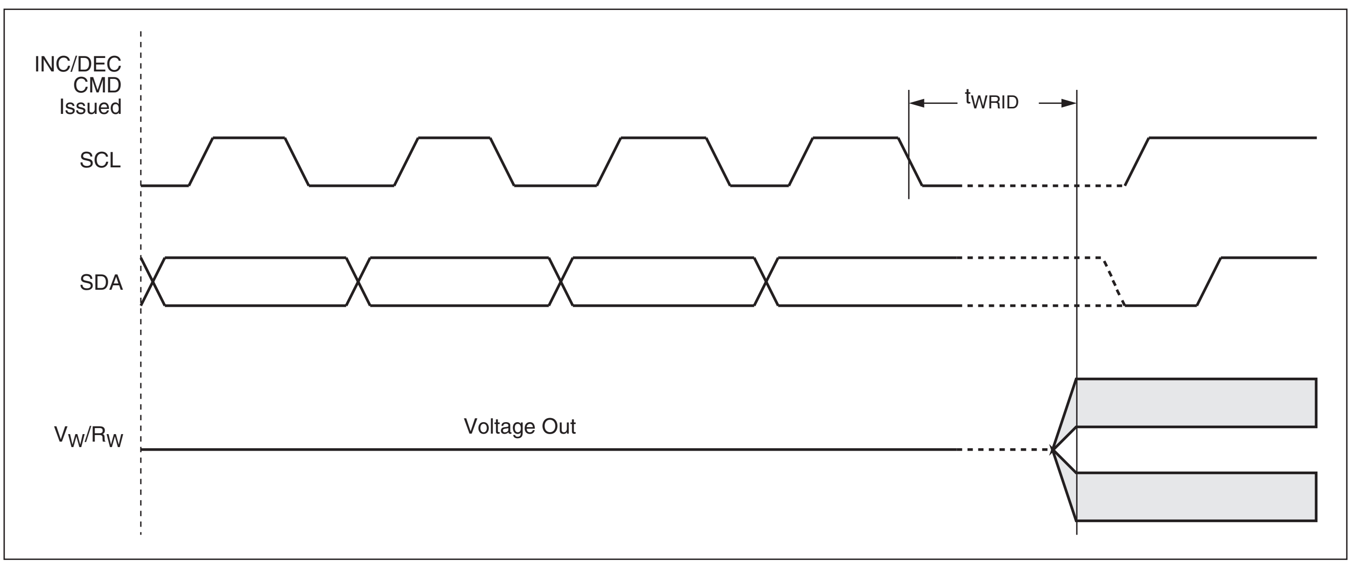


Figure 7. Acknowledge Response from Receiver

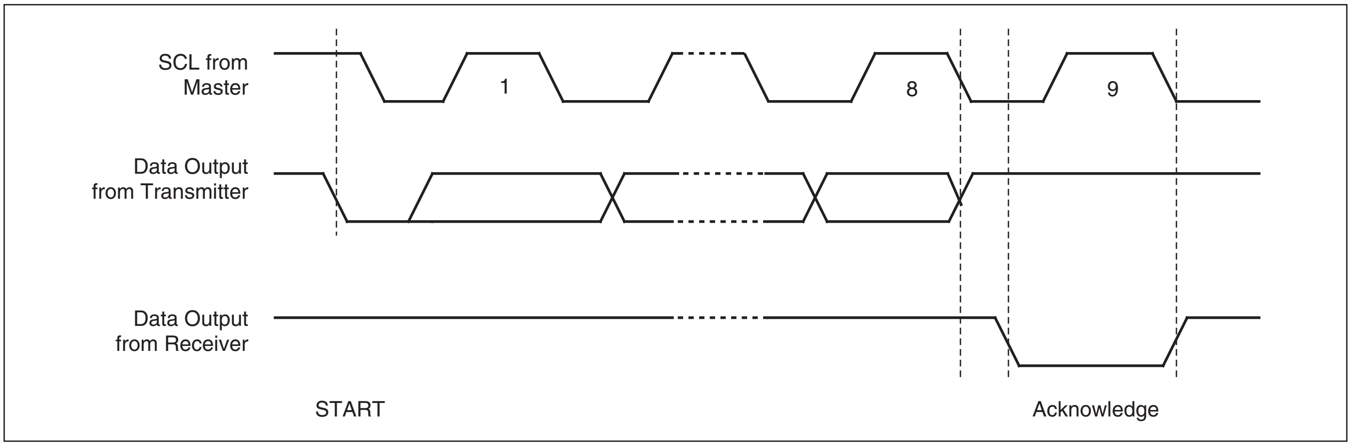
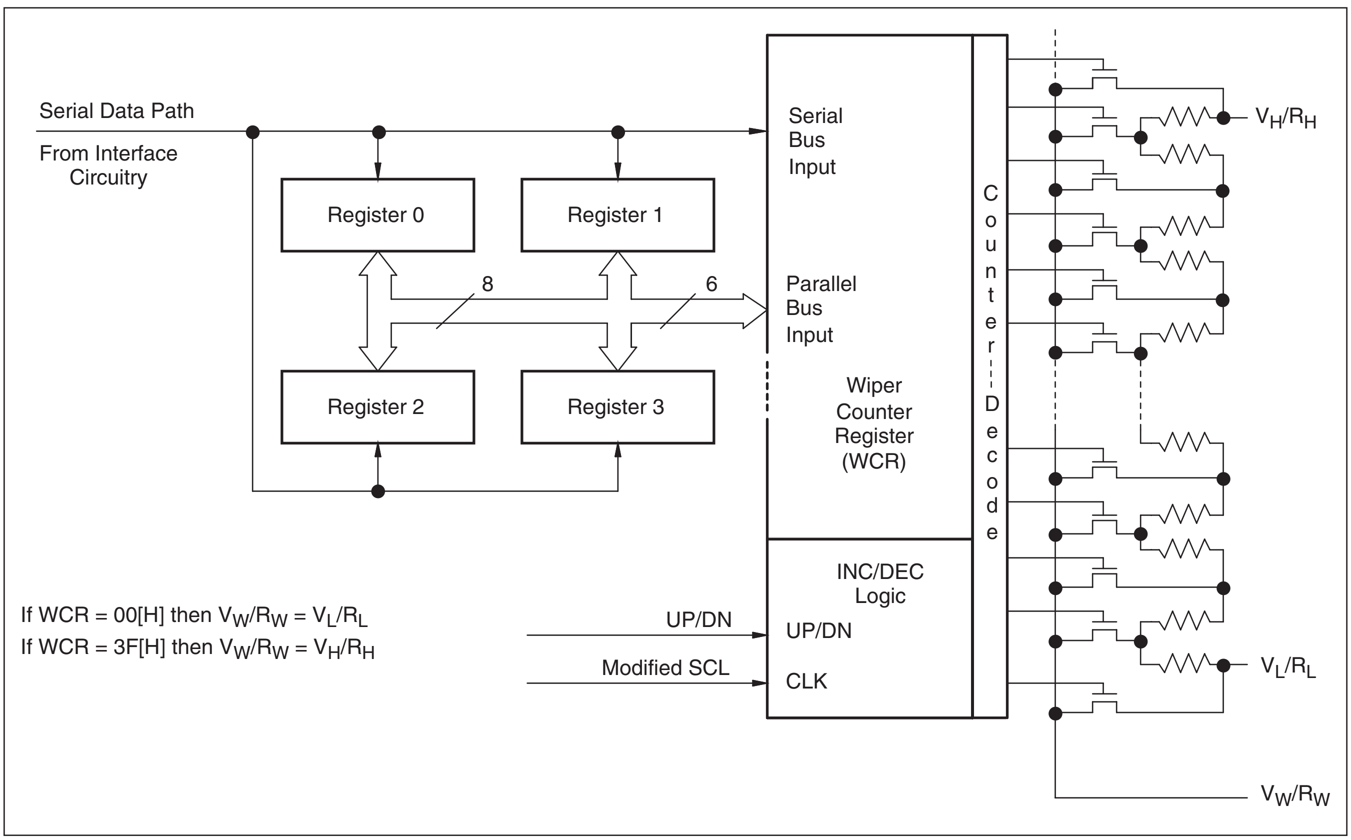


Figure 8. Detailed Potentiometer Block Diagram



DETAILED OPERATION

The potentiometer has a Wiper Counter Register and four Data Registers. A detailed discussion of the register organization and array operation follows.

Wiper Counter Register

The X9429 contains a Wiper Counter Register. The Wiper Counter Register can be envisioned as a 6-bit parallel and serial load counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated Data Registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction. Finally, it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The WCR is a volatile register; that is, its contents are lost when the X9429 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, it should be noted this may be different from the value present at power-down.

Data Registers

The potentiometer has four nonvolatile Data Registers. These can be read or written directly by the host and data can be transferred between any of the four Data Registers and the Wiper Counter Register. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could possibly store system parameters or user preference data.

Register Descriptions

Data Registers, (6-Bit), Nonvolatile

D5	D4	D3	D2	D1	D0
NV	NV	NV	NV	NV	NV
(MSB)					(LSB)

Four 6-bit Data Registers for each XDCP.

– {D5~D0}: These bits are for general purpose not volatile data storage or for storage of up to four different wiper values. The contents of Data Register 0 are automatically moved to the Wiper Counter Register on power-up.

Wiper Counter Register, (6-Bit), Volatile

WP5	WP4	WP3	WP2	WP1	WP0
V	V	V	V	V	V
(MSB)					(LSB)

One 6-bit wiper counter register for each XDCP.

– {D5~D0}: These bits specify the wiper position of the respective XDCP. The Wiper Counter Register is loaded on power-up by the value in Data Register 0. The contents of the WCR can be loaded from any of the other Data Register or directly. The contents of the WCR can be saved in a DR.

Instruction Format

Notes: (1) "MACK"/"SACK": stands for the acknowledge sent by the master/slave.
(2) "A3 ~ A0": stands for the device addresses sent by the master.
(3) "X": indicates that it is a "0" for testing purpose but physically it is a "don't care" condition.
(4) "I": stands for the increment operation, SDA held high during active SCL phase (high).
(5) "D": stands for the decrement operation, SDA held low during active SCL phase (high).

Read Wiper Counter Register (WCR)

START	device type identifier				device addresses				SACK	instruction opcode								SACK	wiper position (sent by slave on SDA)								MACK	STOP
	0	1	0	1	A3	A2	0	A0		1	0	0	1	0	0	0	0		0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Write Wiper Counter Register (WCR)

START	device type identifier				device addresses				SACK	instruction opcode								SACK	wiper position (sent by master on SDA)								SACK	STOP
	0	1	0	1	A3	A2	0	A0		1	0	1	0	0	0	0	0		0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Read Data Register (DR)

START	device type identifier				device addresses				SACK	instruction opcode				register addresses				SACK	wiper position/data (sent by slave on SDA)								MACK	STOP
	0	1	0	1	A3	A2	0	A0		1	0	1	1	R1	R0	0	0		0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Write Data Register (DR)

START	device type identifier				device addresses				SACK	instruction opcode				register addresses				SACK	wiper position/data (sent by master on SDA)								SACK	STOP	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A3	A2	0	A0		1	1	0	0	R1	R0	0	0		0	0	WP5	WP4	WP3	WP2	WP1	WP0			

XFR Data Register (DR) to Wiper Counter Register (WCR)

START	device type identifier				device addresses				SACK	instruction opcode				register addresses				SACK	STOP
	0	1	0	1	A3	A2	0	A0		1	1	0	1	R1	R0	0	0		

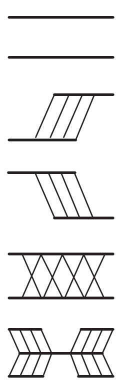
XFR Wiper Counter Register (WCR) to Data Register (DR)

START	device type identifier				device addresses				SACK	instruction opcode				register addresses				SACK	STOP	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A3	A2	0	A0		1	1	1	0	R1	R0	0	0			

Increment/Decrement Wiper Counter Register (WCR)

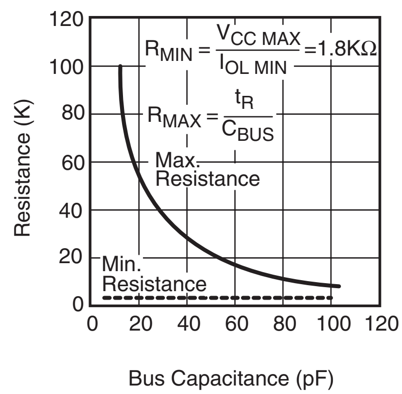
START	device type identifier				device addresses				SACK	instruction opcode								SACK	increment/decrement (sent by master on SDA)					STOP
	0	1	0	1	A3	A2	0	A0		0	0	1	0	0	0	0	0		I/D	I/D	. . . .	I/D	I/D	

SYMBOL TABLE



WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



ABSOLUTE MAXIMUM RATINGS

Temperature under bias : ....–65°C to +135°C
Storage temperature: ....–65°C to +150°C
Voltage on SCL, SDA any address input
with respect to V_{SS}: .... –1V to +7V
$\Delta V = | (V_H – V_L) |$..5V
Lead temperature (soldering, 10 seconds). ....300°C
I_W (10 seconds) .... ±6mA

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

Device	Supply Voltage (V_{CC}) Limits
X9429	5V ±10%
X9429-2.7	2.7V to 5.5V

ANALOG CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
	End to End Resistance Tolerance			±20	%	
	Power rating			50	mW	25°C, each pot
I_W	Wiper current			±3	mA	
R_W	Wiper resistance		150	250	Ω	Wiper current = ± 1mA, V_{CC} = 5V
			400	1000	Ω	Wiper current = ± 1mA, V_{CC} = 3V
V_{TERM}	Voltage on any V_H/R_H or V_L/R_L pin	V_{SS}		V_{CC}	V	V_{SS} = 0V
	Noise		-120		dBV	Ref: 1kHz
	Resolution (4)		1.6		%	
	Absolute Linearity (1)			±1	MI(3)	$V_{w(n)(actual)} — V_{w(n)(expected)}$
	Relative Linearity (2)			±0.2	MI(3)	$V_{w(n+1)} — [V_{w(n)+MI}]$
	Temperature Coefficient of R_{TOTAL}		±300		ppm/°C	
	Ratiometric Temperature Coefficient			±20	ppm/°C	
$C_H/C_L/C_W$	Potentiometer Capacitances		10/10/25		pF	See Circuit #3, Spice Macromodel

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
I_{CC1}	V_{CC} supply current (nonvolatile write)			1	mA	f_{SCL} = 400kHz, SDA = Open, Other Inputs = V_{SS}
I_{CC2}	V_{CC} supply current (move wiper, write, read)			100	µA	f_{SCL} = 400kHz, SDA = Open, Other Inputs = V_{SS}
I_{SB}	V_{CC} current (standby)			5	µA	SCL = SDA = V_{CC}, Addr. = V_{SS}
I_{LI}	Input leakage current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input HIGH voltage	V_{CC} x 0.7		V_{CC} x 0.5	V	
V_{IL}	Input LOW voltage	–0.5		V_{CC} x 0.1	V	
V_{OL}	Output LOW voltage			0.4	V	I_{OL} = 3mA

Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT/63 or (R_H—R_L)/63, single pot
(4) Typical = individual array resolutions.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Unit
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	Years

CAPACITANCE

Symbol	Test	Max.	Unit	Test Conditions
$C_{I/O}$(5)	Input/output capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(5)	Input capacitance (A0, A2,and A3 and SCL)	6	pF	V_{IN} = 0V

POWER-UP TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_RV_{CC}(6)	V_{CC} Power up ramp rate	0.2		50	V/msec

POWER-UP AND POWER-DOWN REQUIREMENTS

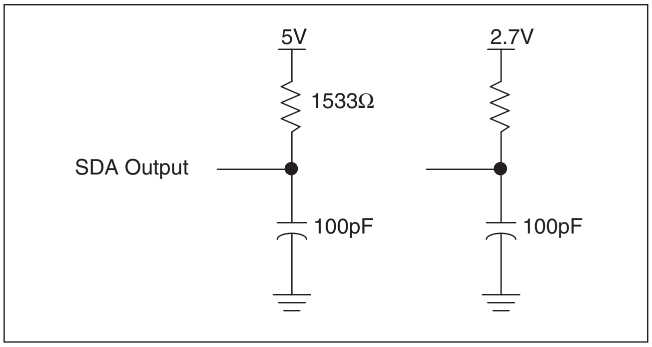
There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltage applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W, i.e., $V_{CC} \geq V_H, V_L, V_W$. The V_{CC} ramp rate spec is alway in effect.

Notes: (5) This parameter is periodically sampled and not 100% tested
(6) Sample tested only.

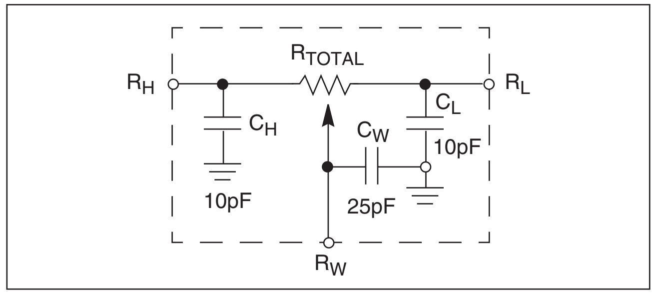
A.C. TEST CONDITIONS

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

EQUIVALENT A.C. LOAD CIRCUIT



Circuit #3 SPICE Macro Model



AC TIMING (Over recommended operating conditions)

Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	Clock frequency	100	400	kHz
t_{CYC}	Clock cycle time	2500		ns
t_{HIGH}	Clock high time	600		ns
t_{LOW}	Clock low time	1300		ns
$t_{SU:STA}$	Start setup time	600		ns
$t_{HD:STA}$	Start hold time	600		ns
$t_{SU:STO}$	Stop setup time	600		ns
$t_{SU:DAT}$	SDA data input setup time	100		ns
$t_{HD:DAT}$	SDA data input hold time	30		ns
t_R	SCL and SDA rise time		300	ns
t_F	SCL and SDA fall time		300	ns
t_{AA}	SCL low to SDA data output valid time		900	ns
t_{DH}	SDA data output hold time	50		ns
T_I	Noise suppression time constant at SCL and SDA inputs	50		ns
t_{BUF}	Bus free time (prior to any transmission)	1300		ns
$t_{SU:WPA}$	$\overline{WP}$, A0, A2, A3 setup time	0		ns
$t_{HD:WPA}$	$\overline{WP}$, A0, A2, A3 hold time	0		ns

HIGH-VOLTAGE WRITE CYCLE TIMING

Symbol	Parameter	Typ.	Max.	Unit
t_{WR}	High-voltage write cycle time (store instructions)	5	10	ms

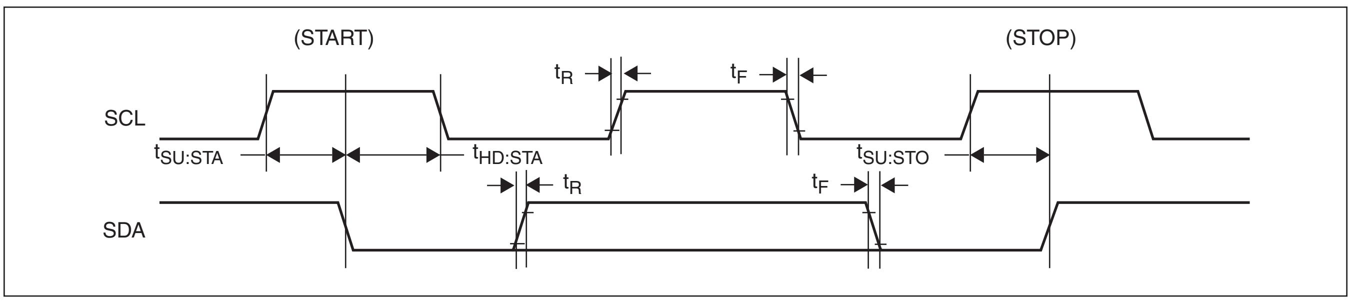
XDCP TIMING

Symbol	Parameter	Min.	Max.	Unit
t_{WRPO}	Wiper response time after the third (last) power supply is stable		10	µs
t_{WRL}	Wiper response time after instruction issued (all load instructions)		10	µs
t_{WRID}	Wiper response time from an active SCL/SCK edge (increment/decrement instruction)		10	µs

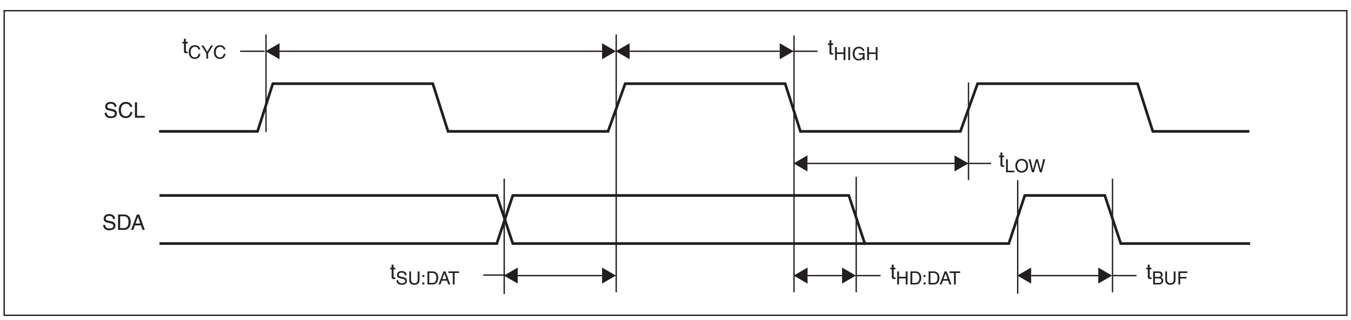
Note: (8) A device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

TIMING DIAGRAMS

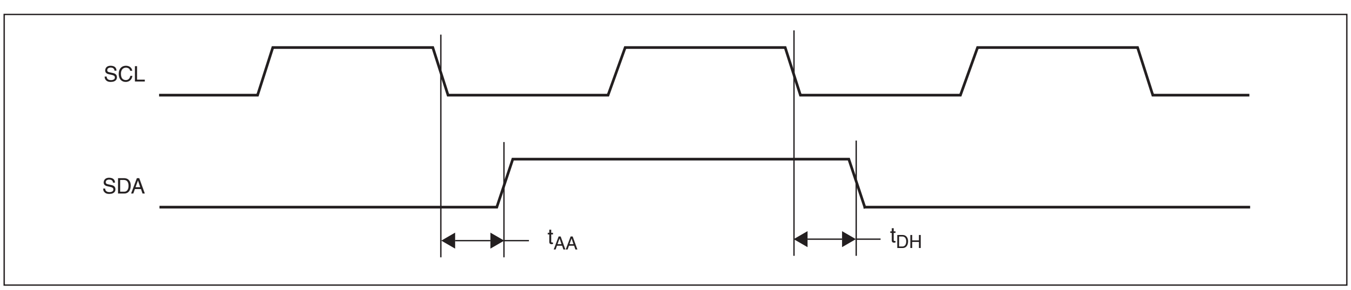
START and STOP Timing



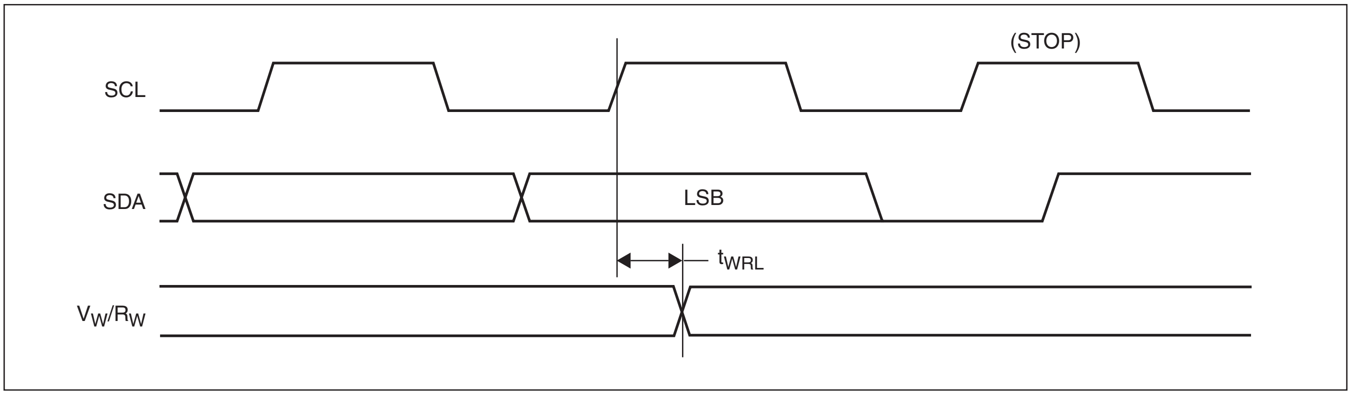
Input Timing



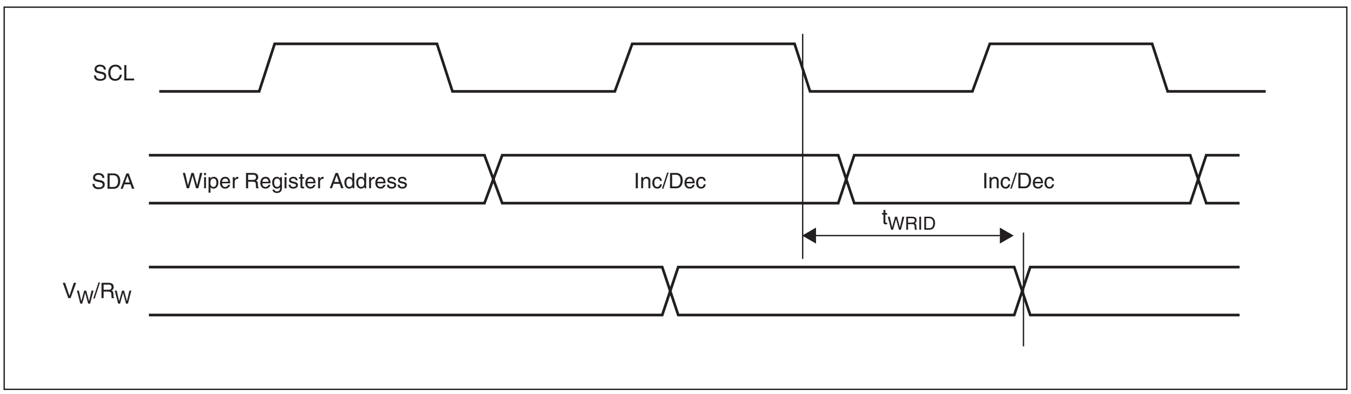
Output Timing



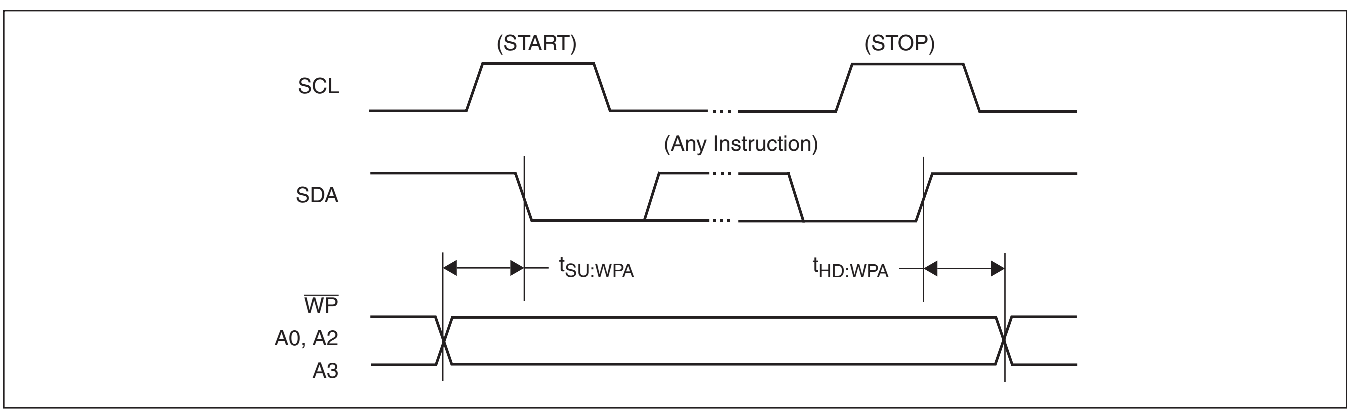
XDCP Timing (for All Load Instructions)



XDCP Timing (for Increment/Decrement Instruction)

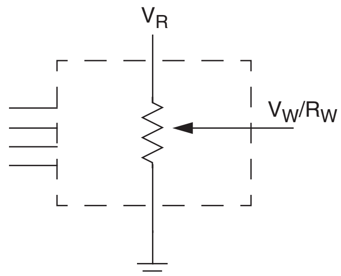


Write Protect and Device Address Pins Timing

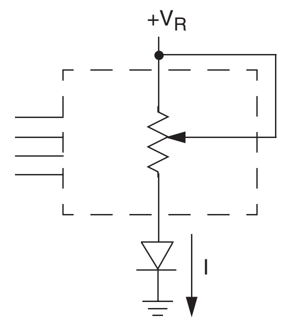


APPLICATIONS INFORMATION

Basic Configurations of Electronic Potentiometers



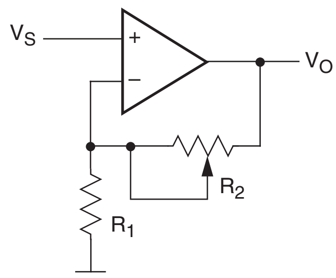
Three terminal Potentiometer;
Variable voltage divider



Two terminal Variable Resistor;
Variable current

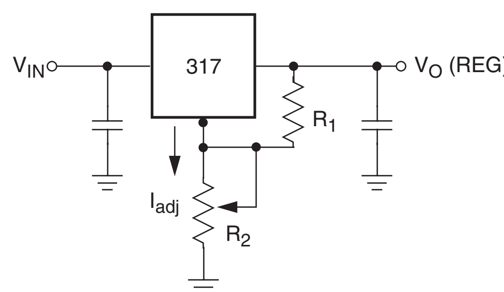
Application Circuits

Noninverting Amplifier



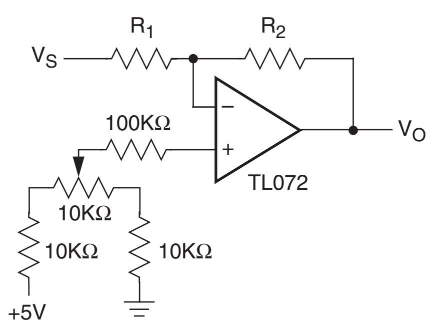
$V_O = (1+R_2/R_1)V_S$

Voltage Regulator

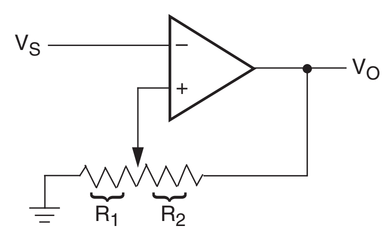


$V_O\ (REG) = 1.25V\ (1+R_2/R_1)+I_{adj}\ R_2$

Offset Voltage Adjustment



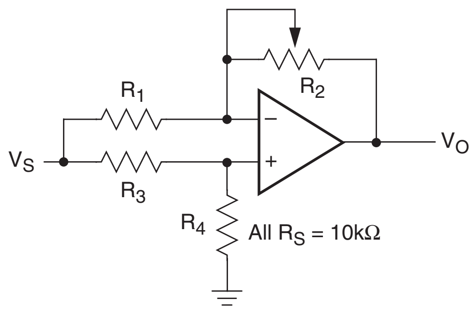
Comparator with Hysteresis



$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2)\}\ V_O(min)$

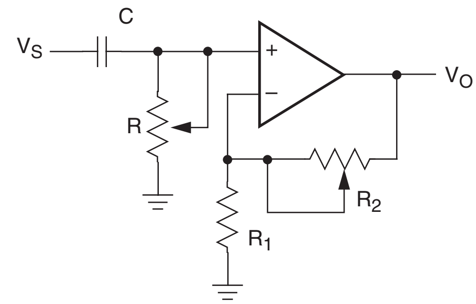
Application Circuits (continued)

Attenuator



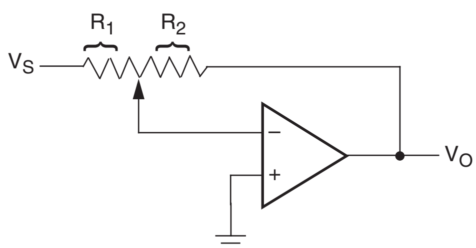
$V_O = G\ V_S$
$-1/2 \leq G \leq +1/2$

Filter



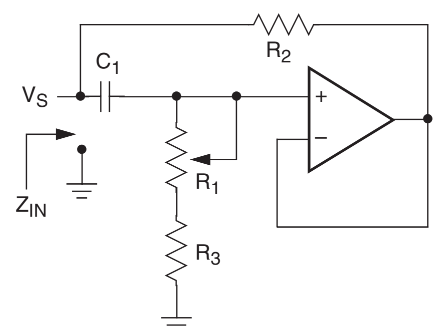
$G_O = 1 + R_2/R_1$
$fc = 1/(2pRC)$

Inverting Amplifier



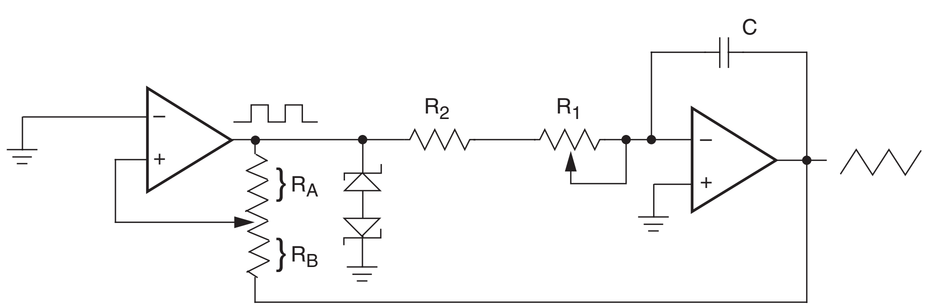
$V_O = G\ V_S$
$G = -R_2/R_1$

Equivalent L-R Circuit



$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

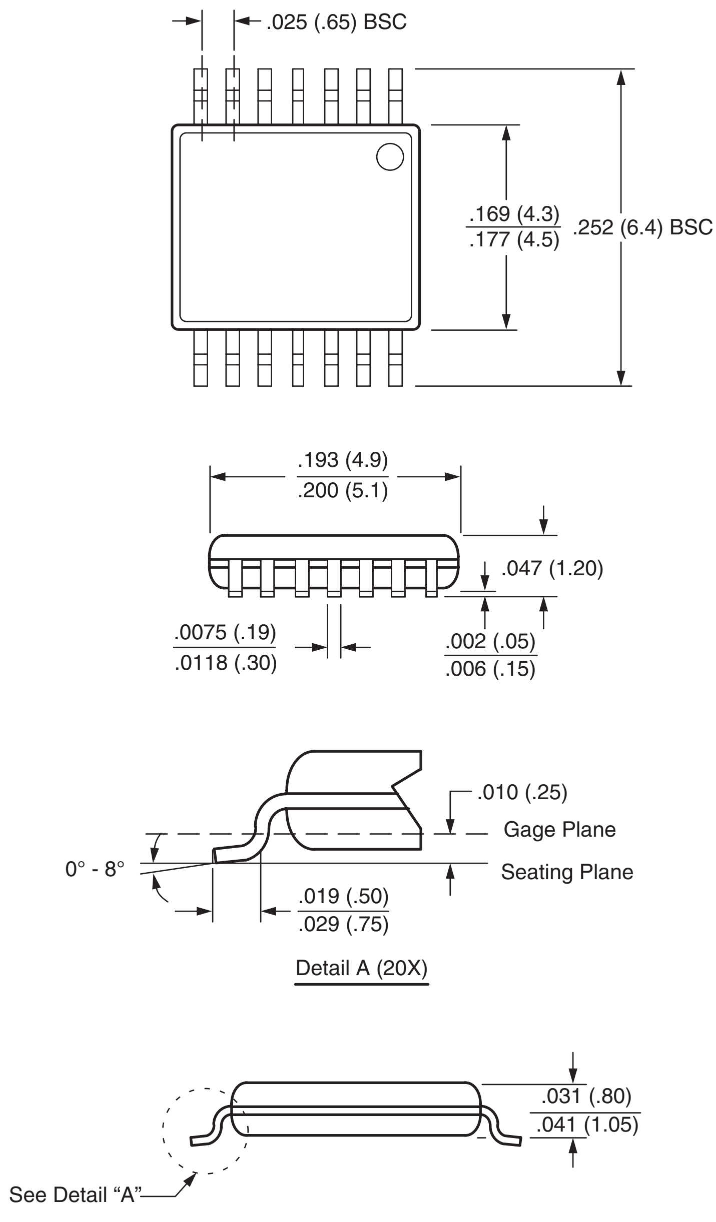
Function Generator



frequency $\propto R_1, R_2, C$
amplitude $\propto R_A, R_B$

PACKAGING INFORMATION

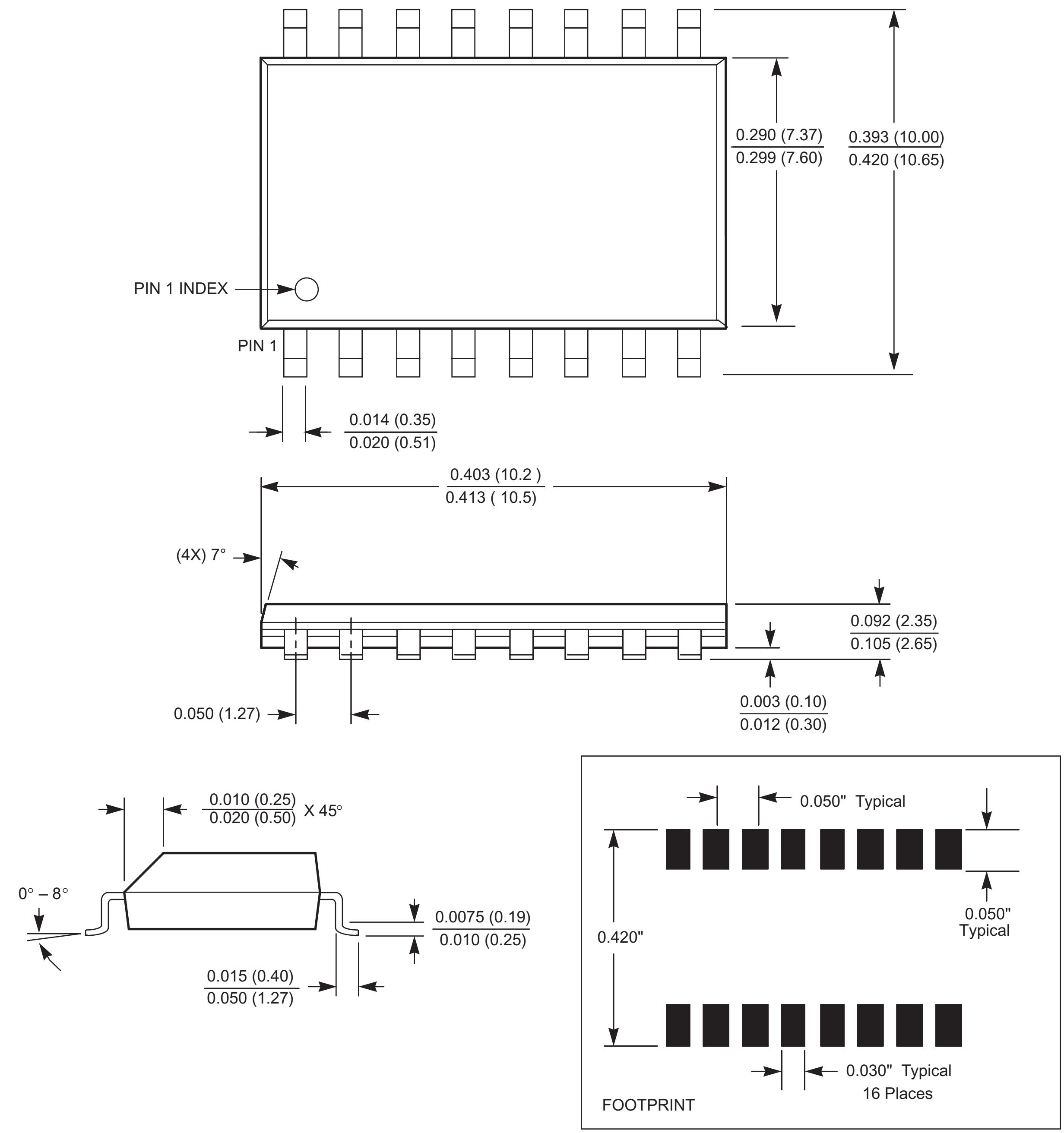
14-Lead Plastic, TSSOP, Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

16-Lead Plastic SOIC (300 Mil Body) Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information

X9429 Y P T V

Device — X9429

V_{CC} Limits (V)
Blank = 5V ±10%

Temperature Range (T)
Blank = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C

Package (P)
S = 16-Lead SOIC
V = 14-Lead TSSOP

Potentiometer Organization (Y)
W = 10KΩ
Y = 2.5KΩ

*Note: P package only available as X9429WP16I-2.7 for prototyping. Other resistor values not available in package.