CPU Supervisor with NOVRAM and Output Ports

FEATURES

- **4Kbit serial EEPROM**
  - **—400kHz serial interface speed**
  - **—16-byte page write mode**
- **One nibble NOVRAM**
  - **—120ns NOVRAM access speed**
  - **—AUTOSTORE**
  - **—Direct/bus access of NOVRAM bits**
- **Four output ports**
- **Operates at 3.3V ± 10%**
- **Low voltage reset when V_{CC} < 3V**
  - **—3% accurate thresholds available**
  - **—Output signal shows low voltage condition**
  - **—Activates NOVRAM AUTOSTORE**
  - **—Internal block on EEPROM operation**
- **Max EEPROM/NOVRAM nonvolatile write cycle: 5ms**
- **High reliability**
  - **—1,000,000 endurance cycles**
  - **—Guaranteed data retention: 100 years**
- **20-lead TSSOP package**

DESCRIPTION

The low voltage X4C105 combines several functions into one device. The first is a 2-wire, 4Kbit serial EEPROM memory with write protection. A Write Protect (WP) pin provides hardware protection for the upper half of this memory against inadvertent writes.

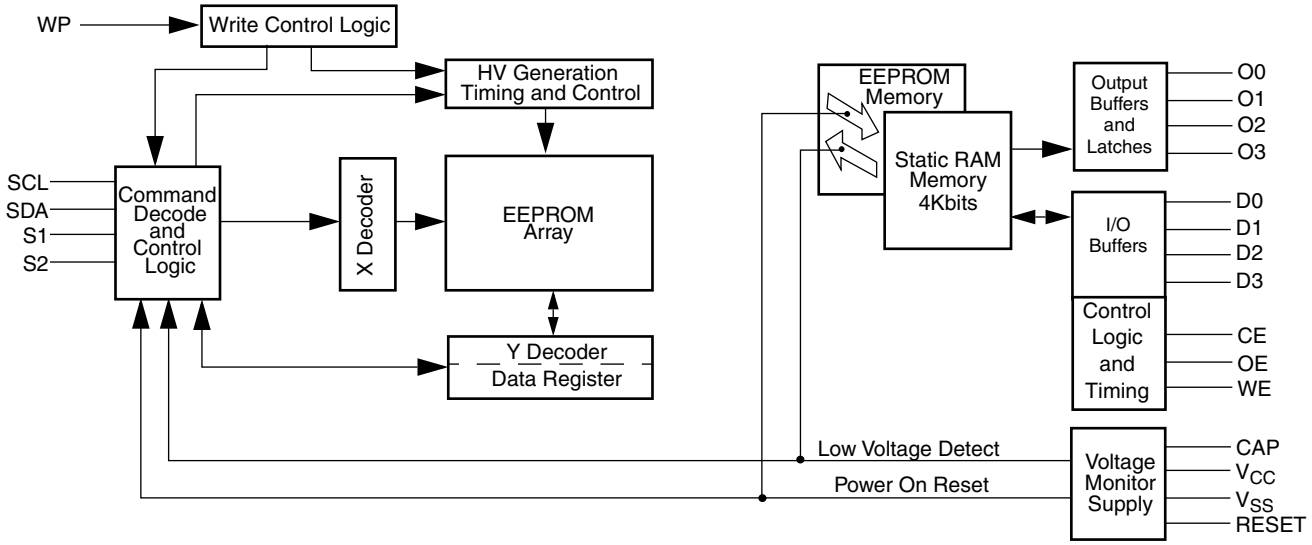
A one nibble NOVRAM is provided and occupies a single location. This allows access of 4-bits in a single 150ns cycle. This is useful for tracking system operation or process status. The NOVRAM memory is completely isolated from the serial memory section.

A low voltage detect circuit activates a $\overline{\text{RESET}}$ pin when V_{CC} drops below 3V. This signal also blocks new read or write operations and initiates a NOVRAM AUTOSTORE. The AUTOSTORE operation is powered by an external capacitor to ensure that the value in the NOVRAM is always maintained in the event of a power failure.

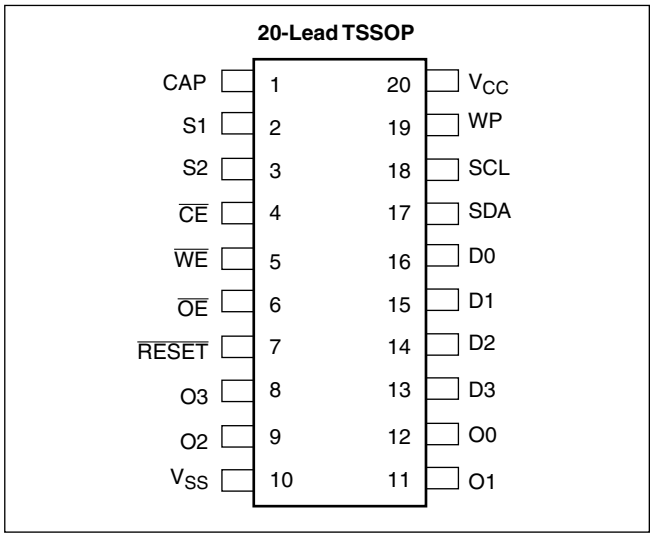
The four NOVRAM bits also appear on four separate output pins to allow continuous control of external circuitry, such as ASICs.

Xicor EEPROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

BLOCK DIAGRAM



PACKAGE/PINOUTS



Pin Names

Pin	Description
V_{SS}	Ground
SDA	Serial Data
V_{CC}	Power
SCL	Serial Clock
WP	Write Protect
S1, S2	Device Select Inputs
CAP	External AUTOSTORE Capacitor
D0–D3	NOVRAM I/Os
RESET	Low Voltage Detect Output
CE	NOVRAM Chip Enable
OE	NOVRAM Read Signal
WE	NOVRAM Write signal
O0-O3	NOVRAM Outputs

DEVICE DESCRIPTION

Serial Memory Section

The device contains a 4Kbit EEPROM memory array with an internal address counter that allows it to be read sequentially, through its entire address space after receiving only 1 full address. The serial interface includes a current address read that requires no input address, but allows reading of the entire array starting from the address plus one of the last read or write. The address counter is also used for the write operation where the user may enter up to a page of data (16 bytes) after supplying only 1 full address.

A WP pin provides hardware write protection. The WP pin active (HIGH) prevents writes to the top half of the memory.

This section is a 4K-bit version of an industry standard 24C04 device.

NOVRAM Section

The X4C105 also contains a single nibble of NOVRAM, with parallel access. This memory is completely isolated from the serial memory section. The NOVRAM is intended to connect to the system memory bus and uses standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ pins to control access.

A NOVRAM (or nonvolatile RAM) consists of an SRAM part and an EEPROM part. The SRAM is saved to EEPROM only when power fails and the EEPROM is recalled to SRAM only on power up.

Output Ports

The X4C105 has four output only ports. These are active whenever power is applied to the device. The state of the output pin reflects the value in the respective SRAM bit. As such, these port pins provide a nonvolatile state. The conditions on the pins are restored when power is re-applied to the device. This can be valuable as a DIP switch replacement for controlling the conditions of an ASIC or other system logic.

Low Voltage Detection

When the internal low voltage detect circuitry senses that V_{CC} is low, several things happen:

– The $\overline{RESET}$ pin goes active.

– The contents of the SRAM are automatically saved to the “shadow” EEPROM.

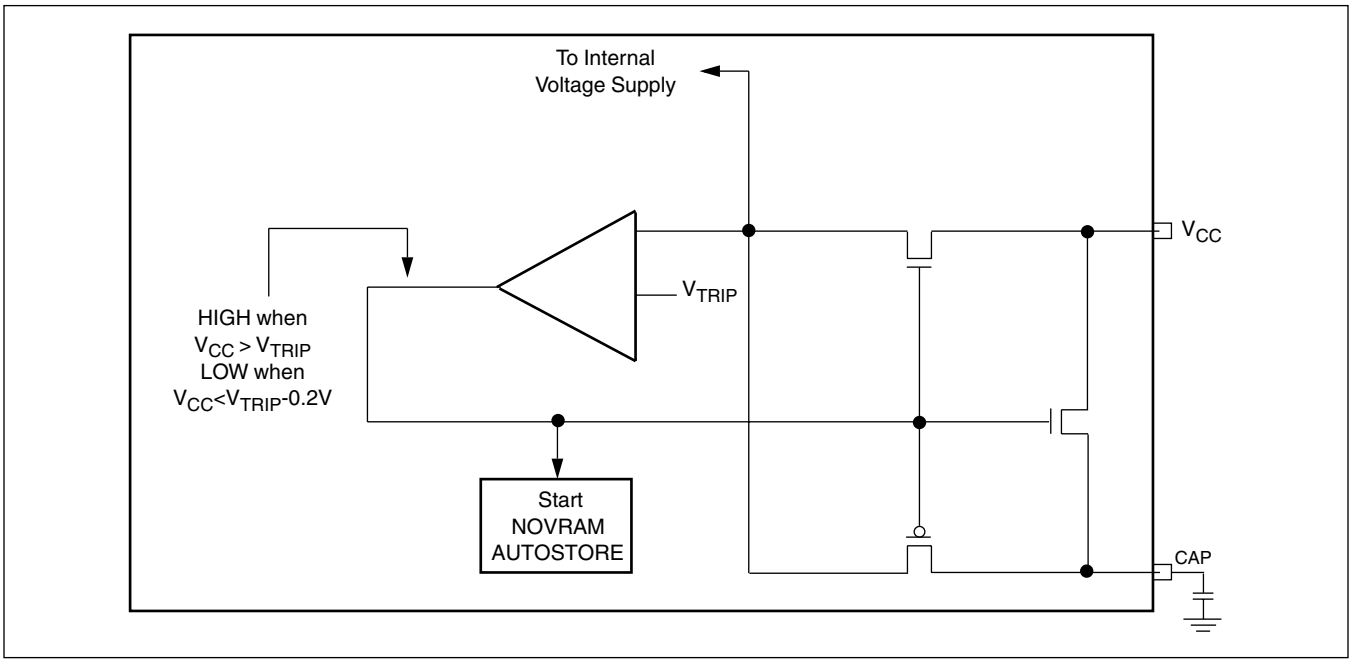
– Internal circuitry switches to provide power for the AUTOSTORE operation from the CAP pin so the store operation can complete even in the event of a catastrophic power failure. To insure this, it is recommended that a 47µF capacitor be used on the CAP pin. The capacitor is continuously charged during normal operation to provide the necessary charge to complete the store operation. Other internal circuits are turned off to minimize current consumption during the store operations.

— Communication to the device is interrupted and any command is aborted. If a serial nonvolatile store is in progress when power fails, the operation is completed and is followed by a NOVRAM AUTOSTORE cycle.

Capacitor Backup Circuit

The diagram in Figure1 shows a representation of the capacitor backup circuit.

Figure 1.



SERIAL INTERFACE

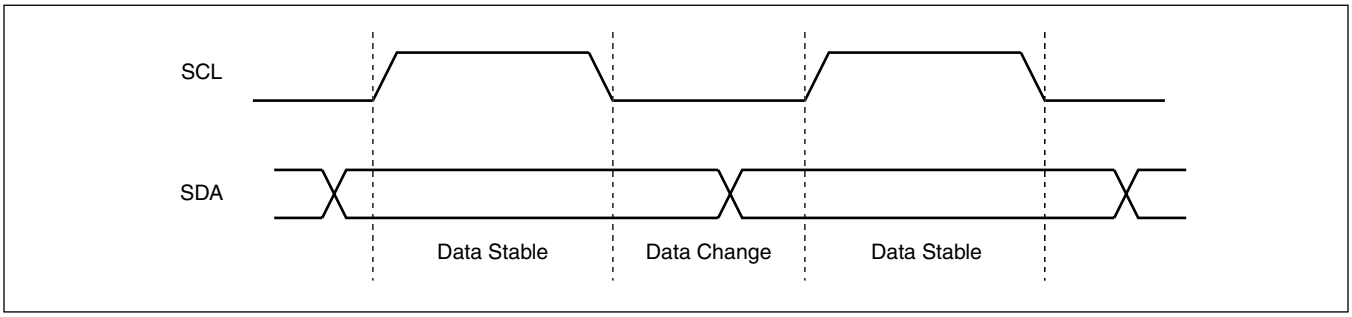
Serial Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

Serial Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 2.

Figure 2. Valid Data Changes on the SDA Bus



Serial Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 3.

Serial Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Figure 2.

Serial Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 4.

The device will respond with an acknowledge after recognition of a start condition and if the correct device identifier and select bits are contained in the slave address byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for the slave address byte when the device identifier and/or select bits are incorrect or when the device is busy, such as during a nonvolatile write.

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to standby mode and place the device into a known state.

Figure 3. Valid Start and Stop Conditions

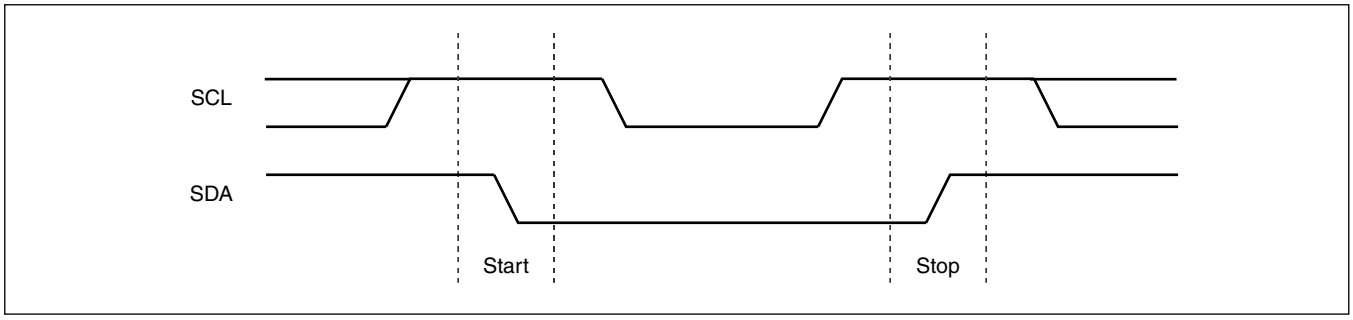
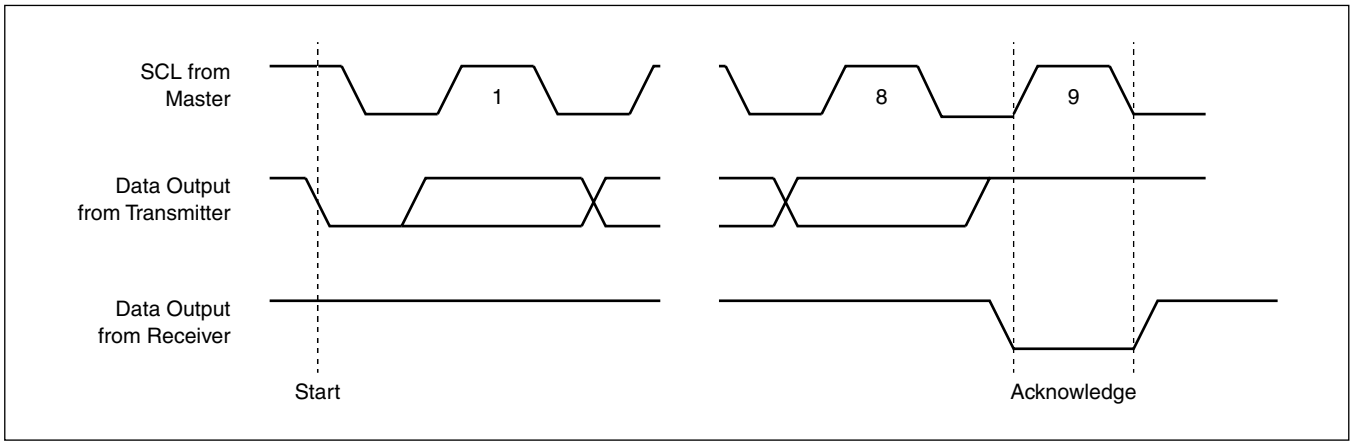


Figure 4. Acknowledge Response From Receiver



SERIAL WRITE OPERATIONS

Byte Write

For a write operation, the device requires the slave address byte and a word address byte. This gives the master access to any one of the words in the array. After receipt of the word address byte, the device responds with an acknowledge, and awaits the next eight bits of data. After receiving the 8 bits of the data byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. During this internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 5.

An attempted write to a protected block of memory will suppress the acknowledge bit and the operation will terminate.

Page Write

The device is capable of a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit an unlimited number of 8-bit bytes. After the receipt of each byte, the device will respond with an acknowledge, and the address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it “rolls over” and goes back to ‘0’ on the same page. This means that the master can write 16 bytes to the page starting at any location on that page. If the master begins writing at location 10, and loads 12 bytes, then the first 5 bytes are written to locations 10 through 15, and the last 7 bytes are written to locations 0 through 6. Afterwards, the address counter would point to location 7 of the page that was just written. See Figure 6. If the master supplies more than 16 bytes of data, then new data over-writes the previous data, one byte at a time.

Figure 5. Byte Write Sequence

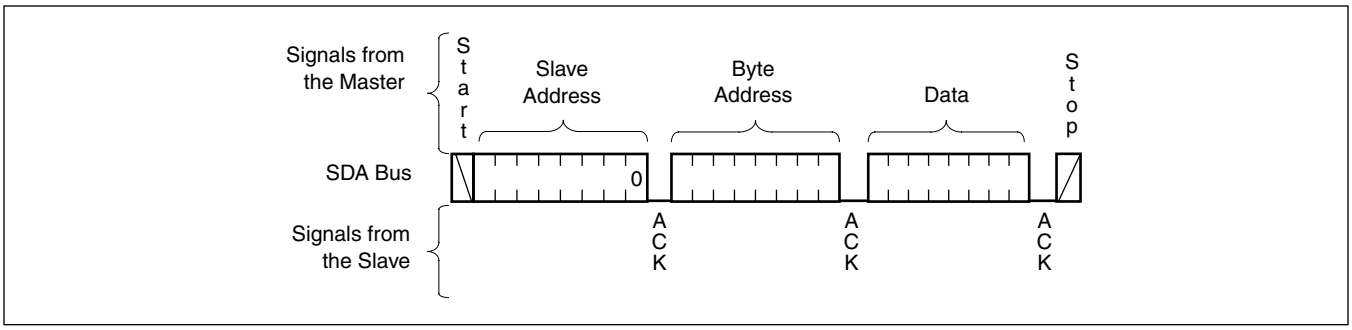
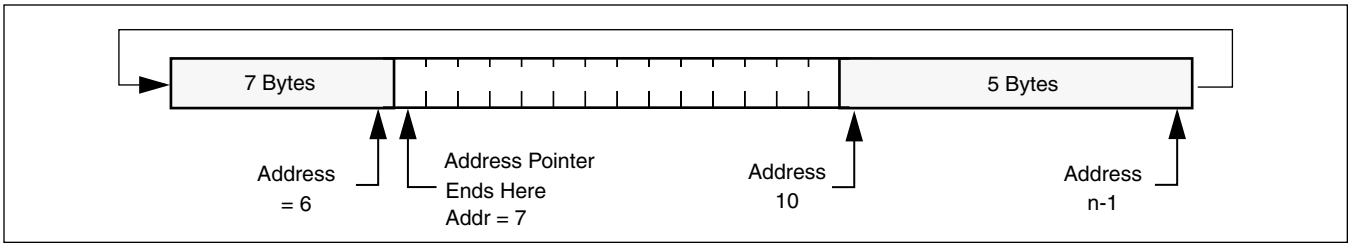


Figure 6. Writing 12 bytes to a 16-byte page starting at location 10.

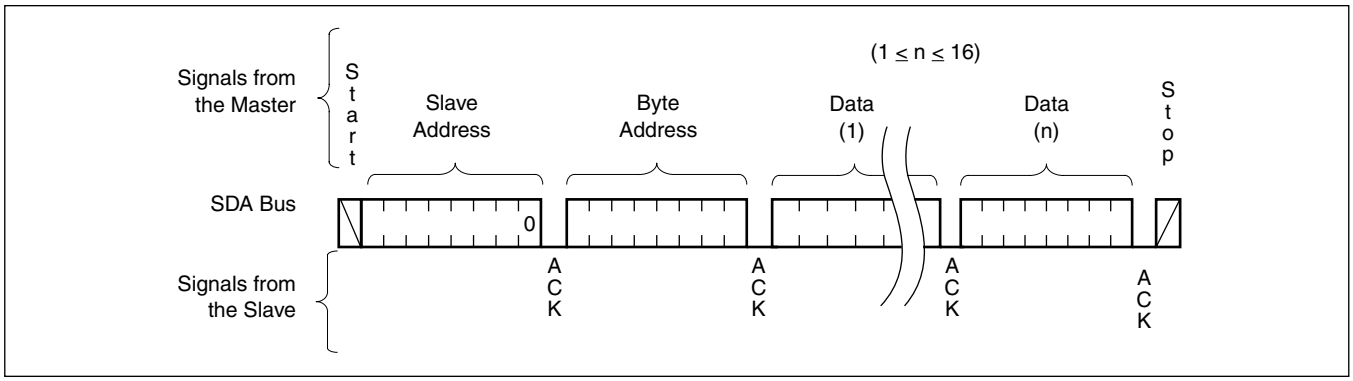


The master terminates the data byte loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 7 for the address, acknowledge, and data transfer sequence.

Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte plus the subsequent ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte plus its associated ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be affected.

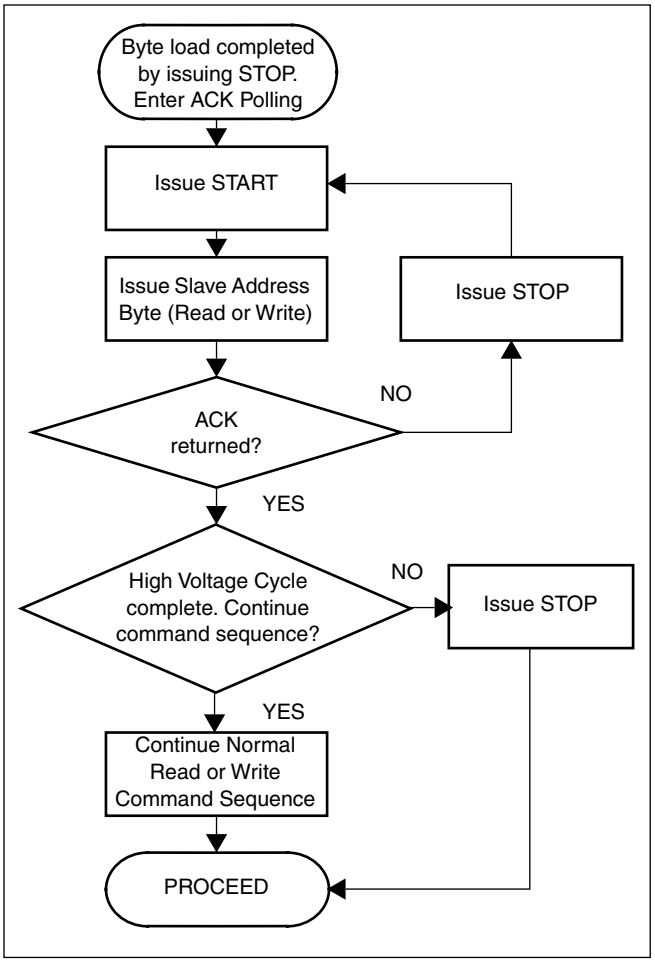
Figure 7. Page Write Operation



Acknowledge Polling

The disabling of the inputs during high voltage cycles can be used to take advantage of the typical 5ms write cycle time. Once the stop condition is issued to indicate the end of the master's byte load operation, the device initiates the internal non volatile write cycle. Acknowledge polling can be initiated immediately. To do this, the master issues a start condition followed by the slave address byte for a write or read operation. If the device is still busy with the high voltage cycle then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to the flow chart in Figure 8.

Figure 8. Acknowledge Polling Sequence



Serial Read Operations

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address byte is set to one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power up, the address of the address counter is undefined, requiring a read or write operation for initialization.

Upon receipt of the slave address byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the data byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. Refer to Figure 9 for the address, acknowledge, and data transfer sequence.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Random Read

A random read operation allows the master to access any memory location in the array. Prior to issuing the slave address byte with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition and the slave address byte, receives an acknowledge, then issues the word address byte. After acknowledging receipts of the word address byte, the master immediately issues another start condition and the slave address byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 10 for the address, acknowledge, and data transfer sequence.

Figure 9. Current Address Read Sequence

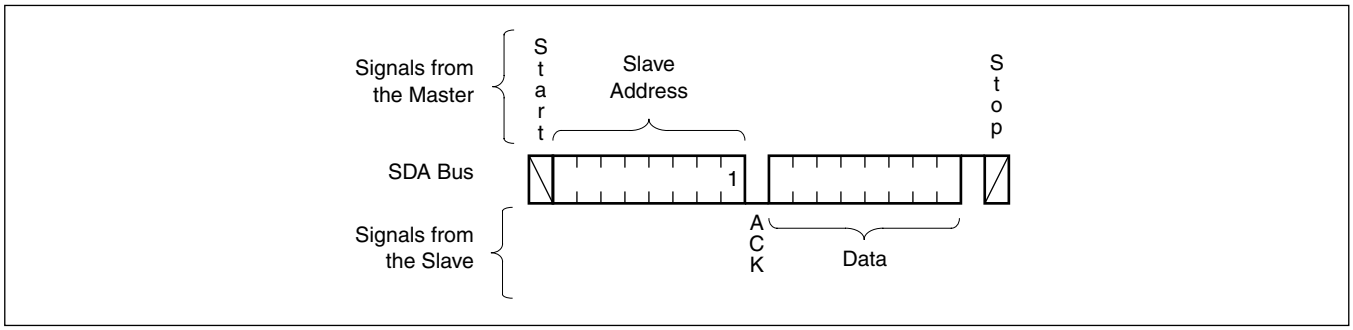
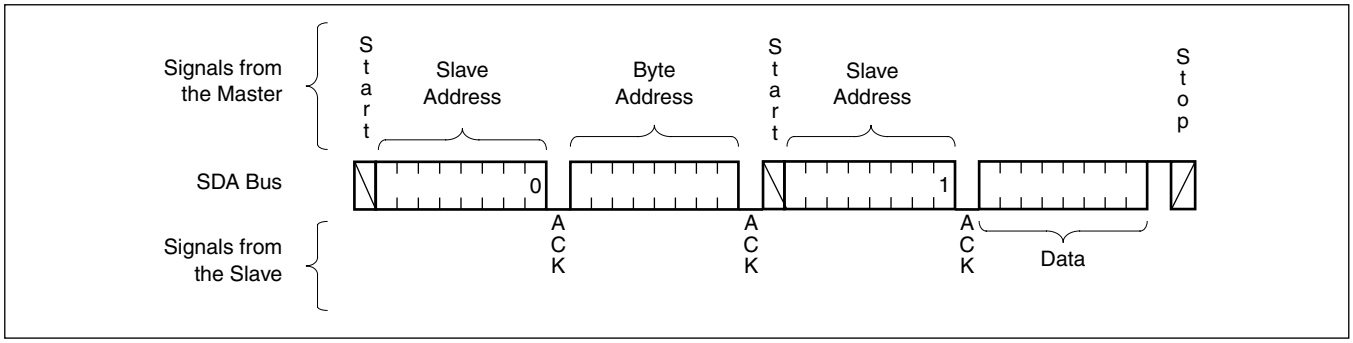


Figure 10. Random Address Read Sequence



The device offers a similar operation, called "Set Current Address," where the device ends the transmission and issues a stop instead of the second start, shown in Figure 10. The device goes into standby mode after the stop and all bus activity will be ignored until a start is detected. This operation loads the new address into the address counter. The next current address read operation will then read from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first data byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter "rolls over" to address 0000_H and the device continues to output data for each acknowledge received. Refer to Figure 11 for the acknowledge and data transfer sequence.

SERIAL DEVICE ADDRESSING

Slave Address Byte

Following a start condition, the master must output a slave address byte. This byte consists of several parts:

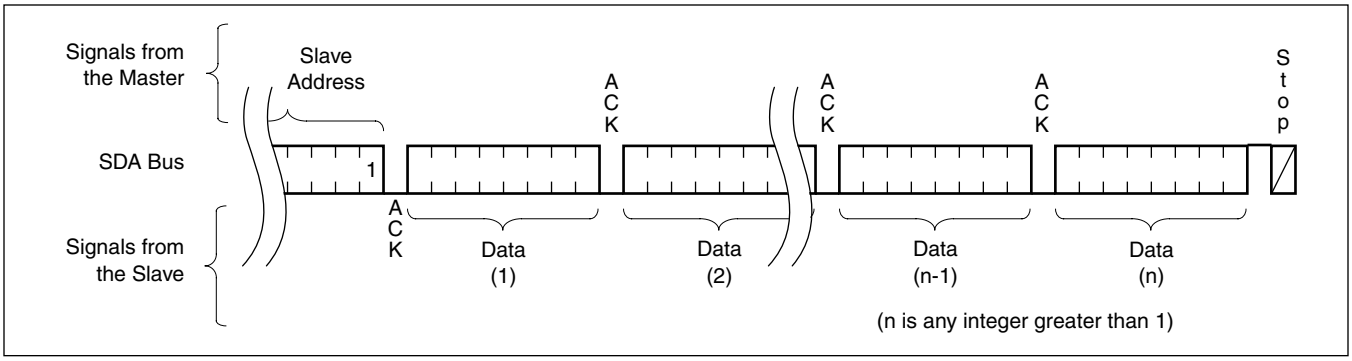
– a device type identifier that is always '1010'.

– two bits that provide the device select bits.

– one bit that becomes the MSB of the address.

– one bit of the slave command byte is a R/$\overline{W}$ bit. The R/$\overline{W}$ bit of the slave address byte defines the operation to be performed. When the R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation. Refer to Figure 12.

Figure 11. Sequential Read Sequence



After loading the entire slave address byte from the SDA bus, the device compares the device select bits with the status of the device select pins. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Slave Byte

1	0	1	0	S2	S1	A8	R/W

Word Address

The word address is either supplied by the master or obtained from an internal counter. The internal counter is undefined on a power up condition.

Write Protect Operations

The WP pin provides write protection. The WP pin protects the upper half of the array.

Table 1. Write Protected Areas

WP Pin	Serial Memory Write Protection
LOW	Writes possible to all locations
HIGH	No writes to 100H-1FFH, writes possible to 000H to 0FFH

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with
respect to ground .....-1.0V to 7.0V
DC output current..... 5 mA
Lead temperature (soldering, 10 seconds).....300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS V_{CC} = 3.0 to 3.6V at -40°C to +85°C unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{CC1}(1)	Active supply current serial read or serial write (does not include the nonvolatile store operation)		2.0	mA	$V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9, f_{SCL} = 400kHz, SDA = Read/Write Operation, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, D0–D3 = V_{IH}; O0–O3, $\overline{RESET}$ = Open CAP is tied to V_{CC}; $V_{CC} > V_{TRIP}$
I_{CC2}(1)	Average active supply current during serial non-volatile store operation		3.0	mA	$V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9, SCL, SDA = V_{IH}; WP, S1, S2 = V_{IL}, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, D0–D3 = V_{IH}; O0–O3, $\overline{RESET}$ = Open CAP is tied to V_{CC}. Test during the N.V. write cycle.
I_{CC3}(1)	Active supply current volatile NOVRAM read		3.0	mA	$V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9, SCL, SDA = V_{IH}; WP, S1, S2 = V_{IL}, $\overline{WE}$ = V_{IH}; $\overline{CE}$, $\overline{OE}$ = V_{IL}, D0–D3, O0–O3, $\overline{RESET}$ = Open CAP is tied to V_{CC}; $V_{CC} > V_{TRIP}$
I_{CC4}(1)	Active supply current volatile NOVRAM write		3.0	mA	$V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9, SCL, SDA = V_{IH}; WP, S1, S2 =V_{IL}, $\overline{OE}$ = V_{IH}; $\overline{CE}$, $\overline{WE}$ = V_{IL}, D0-D3 = V_{IL} or V_{IH}, O0-O3, $\overline{RESET}$ = Open CAP is tied to V_{CC}; $V_{CC} > V_{TRIP}$
I_{CC5}(1)	Average active supply current over NOVRAM store, or active current during recall		3.0	mA	$V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9, SCL, SDA, V_{IH}; WP, S1, S2 = V_{IL}, $\overline{WE}$, $\overline{CE}$, $\overline{OE}$ = V_{IH}; D0–D3, O0–O3, $\overline{RESET}$ = Open CAP is tied to V_{CC}, $V_{CC} < V_{TRIP}$ for Store; $V_{CC} > V_{TRIP}$ for Recall
I_{SB1}(1)	Standby current		50	µA	$V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9, SCL, SDA, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, D0–D3, = V_{IH}, WP = V_{IL}, O0–O3, $\overline{RESET}$ = Open; CAP is tied to V_{CC}
I_{LI}	Input leakage current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output leakage current		10	µA	V_{SDA} = GND to V_{CC}; Device is in Standby(2)
V_{IL}(3)	Input LOW voltage	-0.5	V_{CC} x 0.3	V	
V_{IH}(3	Input HIGH voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{HYS}	Schmitt trigger input hysteresis	.05 x V_{CC}		V	
V_{OL}	Output LOW voltage		0.4	V	I_{OL} = 2.0mA, V_{CC} = 3.3V
V_{OH}	Output HIGH voltage	V_{CC} – 0.4		V	I_{OH} = -1mA, V_{CC} = 3.3V

Notes: (1) The device enters the active state after any start, and remains active until: 9 clock cycles later if the device select bits in the slave address byte are incorrect; 200ns after a stop ending a read operation; or t_{WC} after a stop ending a write operation.
(2) The device goes into standby: 200ns after any stop, except those that initiate a high voltage write cycle; t_{WC} after a stop that initiates a high voltage cycle; or 9 clock cycles after any start that is not followed by the correct device select bits in the slave address byte.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 3.0-3.6V

Symbol	Parameter	Max.	Unit	Test Conditions
$C_{I/O}$[4]	Input/output capacitance (SDA, D0-D3, O0-O3)	8	pF	$V_{I/O}$ = 0V
C_{IN}[4]	Input capacitance (SCL, WP, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, S1, S2)	6	pF	V_{IN} = 0V

Note: (4) This parameter is periodically sampled and not 100% tested.

SERIAL NONVOLATILE WRITE CYCLE TIMING

Symbol	Parameter	Min.	Typ.[5]	Max.	Unit
t_{WC}[5]	Write cycle time		3	5	ms

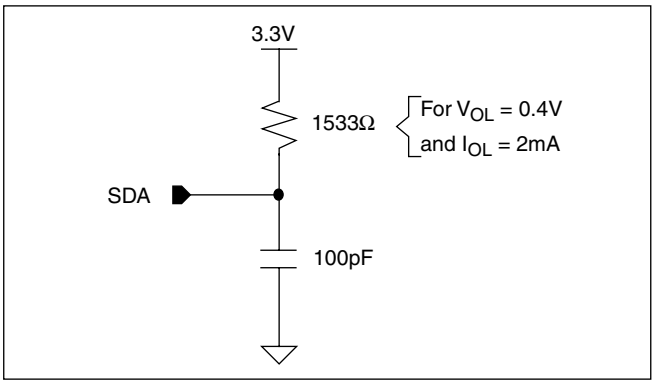
Note: (5) t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless acknowledge polling is used.

SERIAL MEMORY AC CHARACTERISTICS

Serial AC Test Conditions

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing levels	V_{CC} x 0.5
Output load	Standard output load

Equivalent AC Output Load Circuit for V_{CC} = 3.0–3.6V



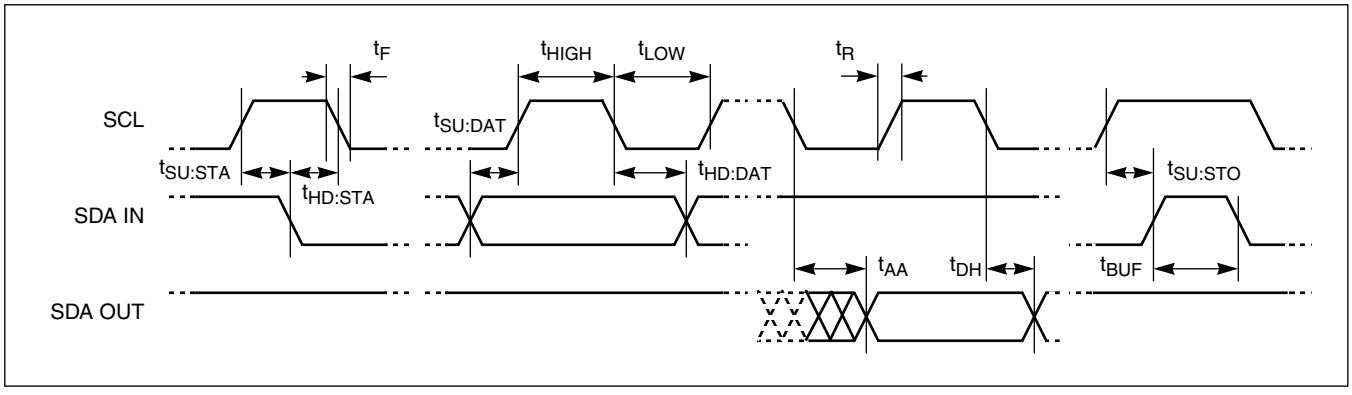
SERIAL AC SPECIFICATIONS T_A = -40°C to +85°C, V_{CC} = +3.0V to +3.6V, unless otherwise specified.

Symbol	Parameter	400kHz Option		Unit
		Min.	Max.	
f_{SCL}	SCL clock frequency	0	400	kHz
t_{IN}	Pulse width of spikes to be suppressed by the input filter	0	50	ns
t_{AA}	SCL LOW to SDA data out valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		µs
t_{LOW}	Clock LOW time	1.3		µs
t_{HIGH}	Clock HIGH time	0.6		µs
$t_{SU:STA}$	Start condition setup time	0.6		µs
$t_{HD:STA}$	Start condition hold time	0.6		µs
$t_{SU:DAT}$	Data in setup time	100		ns
$t_{HD:DAT}$	Data in hold time	0		µs
$t_{SU:STO}$	Stop condition setup time	0.6		µs
t_{DH}	Data output hold time	50		ns
t_R	SDA and SCL rise time	20 +.1Cb(8)	300	ns
t_F	SDA and SCL fall time	20 +.1Cb(8)	300	ns
$t_{SU:\ S1,\ S2,WP}$	S1, S2, and $\overline{WP}$ setup time	0.4		ms
$t_{HD:\ S1,\ S2,WP}$	S1, S2, and $\overline{WP}$ hold time	0.4		ms
Cb	Capacitive load for each bus line		400	pF

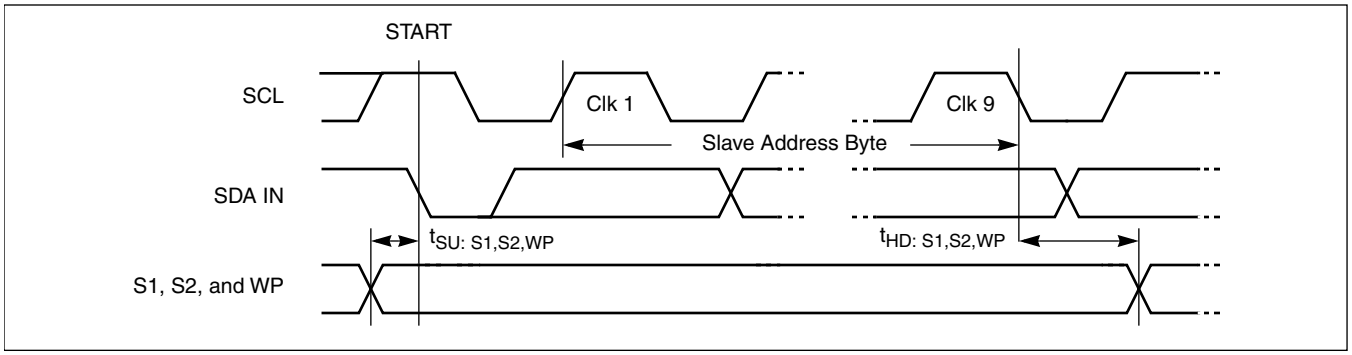
Notes: (7) This parameter is periodically sampled and not 100% tested.
(8) Cb = total capacitance of one bus line in pF.

SERIAL TIMING DIAGRAMS

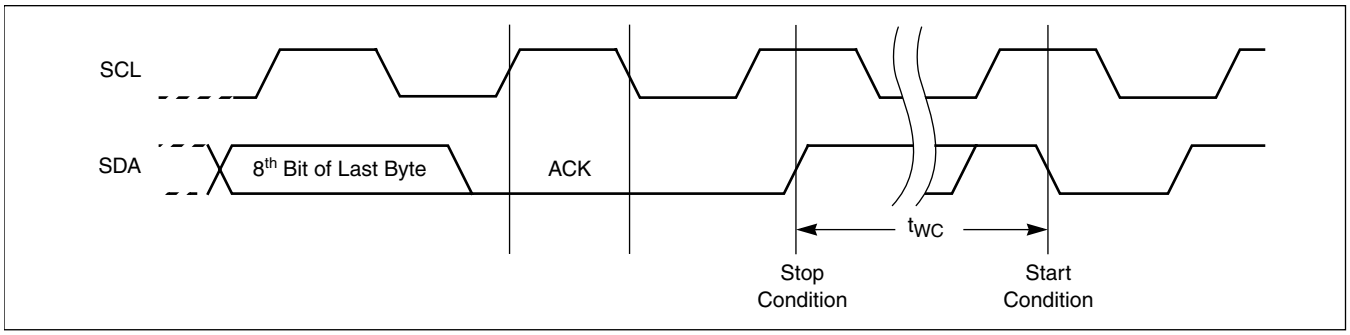
Bus Timing



S1, S2, and WP Pin Timing



Write Cycle Timing

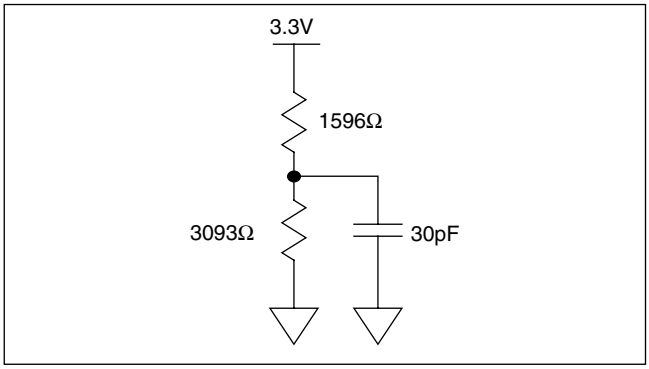


NOVRAM AC CHARACTERISTICS

NOVRAM AC Conditions of Test

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing levels	V_{CC} x 0.5

NOVRAM Equivalent A.C Load Circuits



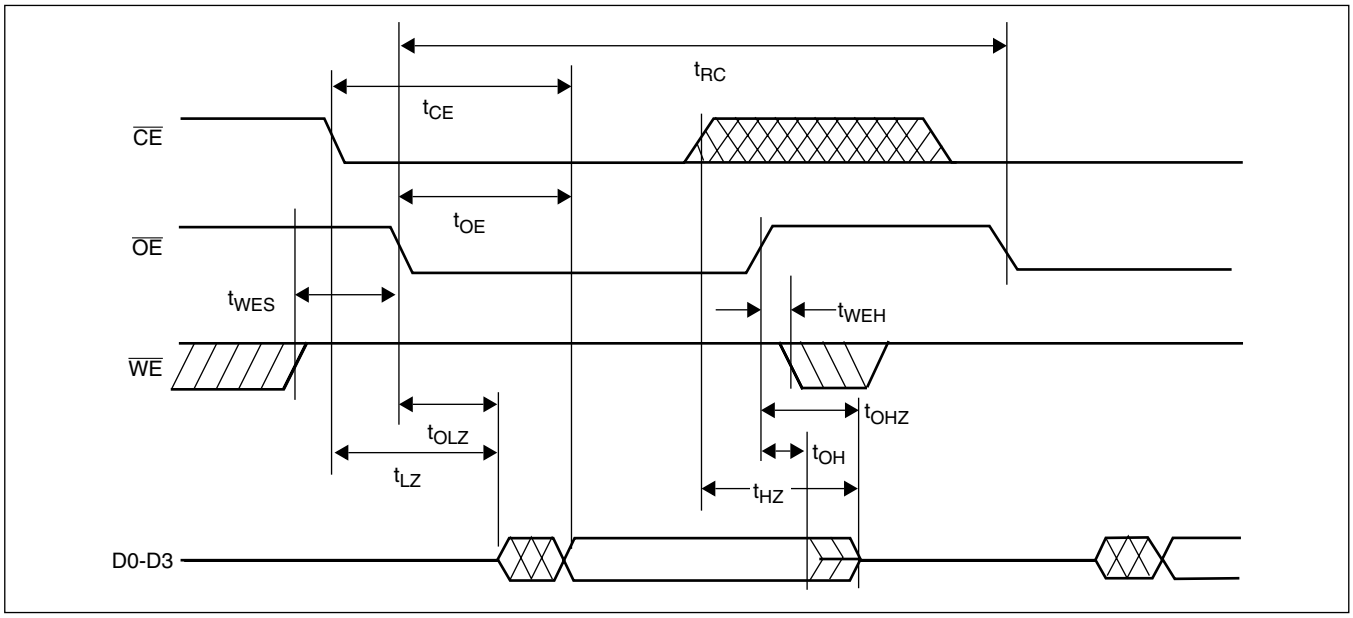
NOVRAM READ CYCLE SPECIFICATIONS

Table 2. NOVRAM Read Cycle Limits

Symbol	Parameter	V_{CC} = 3.0V-3.6V -40°C to +85°C		Unit
		Min.	Max.	
t_{RC}	Read cycle time		120	ns
t_{CE}	Chip enable access time		50	ns
t_{OE}	Output enable access time		50	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$ HIGH	0		ns
t_{WES}	Write enable HIGH setups time	25		ns
t_{WEH}	Write enable HIGH hold time	25		ns
t_{LZ}(9)	Chip enable to output in low Z	0		ns
t_{OLZ}(9)	Output enable to output in low Z	0		ns
t_{HZ}(9)	Chip disable to output in high Z	0	50	ns
t_{OHZ}(9)	Output disable to output in high Z	0	50	ns
t_{SOE}(9)	$\overline{OE}$ setup prior to operation in 2-wire mode	100		ms
t_{HOE}(9)	$\overline{OE}$ hold following operation in 2-wire mode	100		ms

Note: (9) t_{LZ} and t_{OLZ} min.; t_{SOE} and t_{HOE} min; and t_{HZ} and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with CL = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

NOVRAM Read Cycle

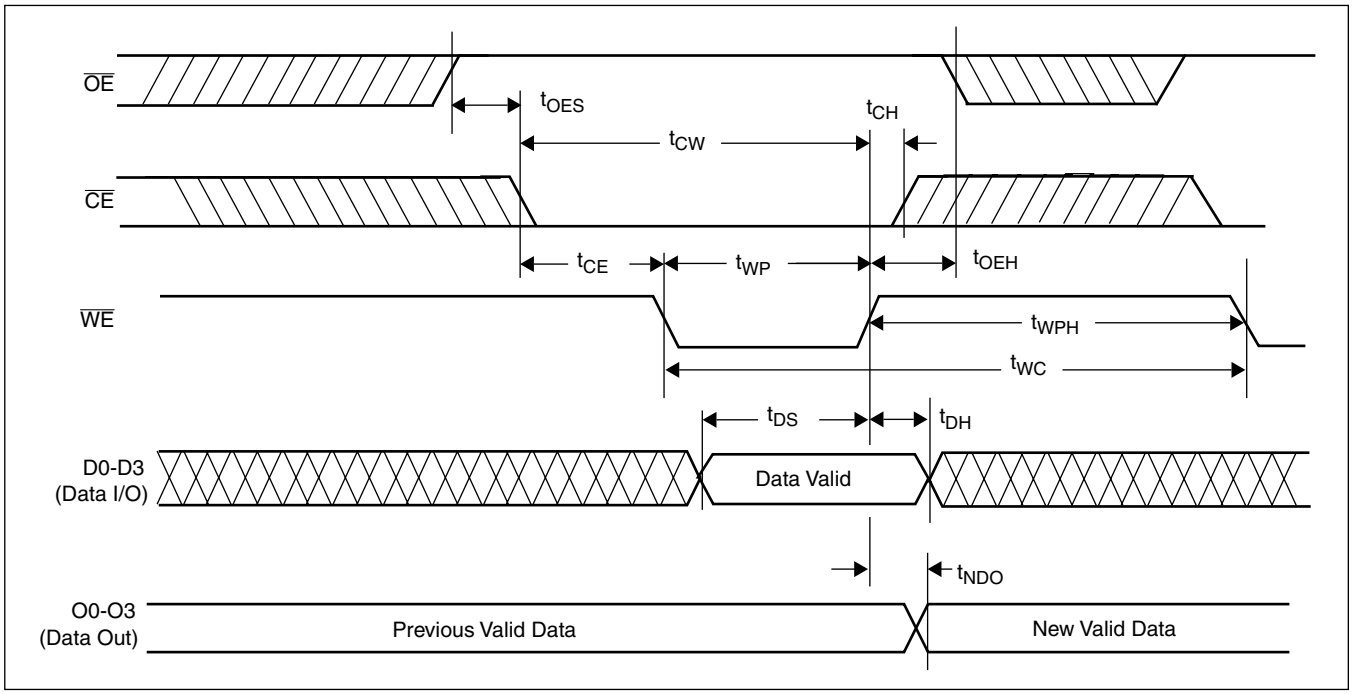


NOVRAM WRITE CYCLE SPECIFICATIONS NOVRAM Write Cycle Limits V_{CC} = 3.0V-3.6V, T_A = -40°C to +85°C

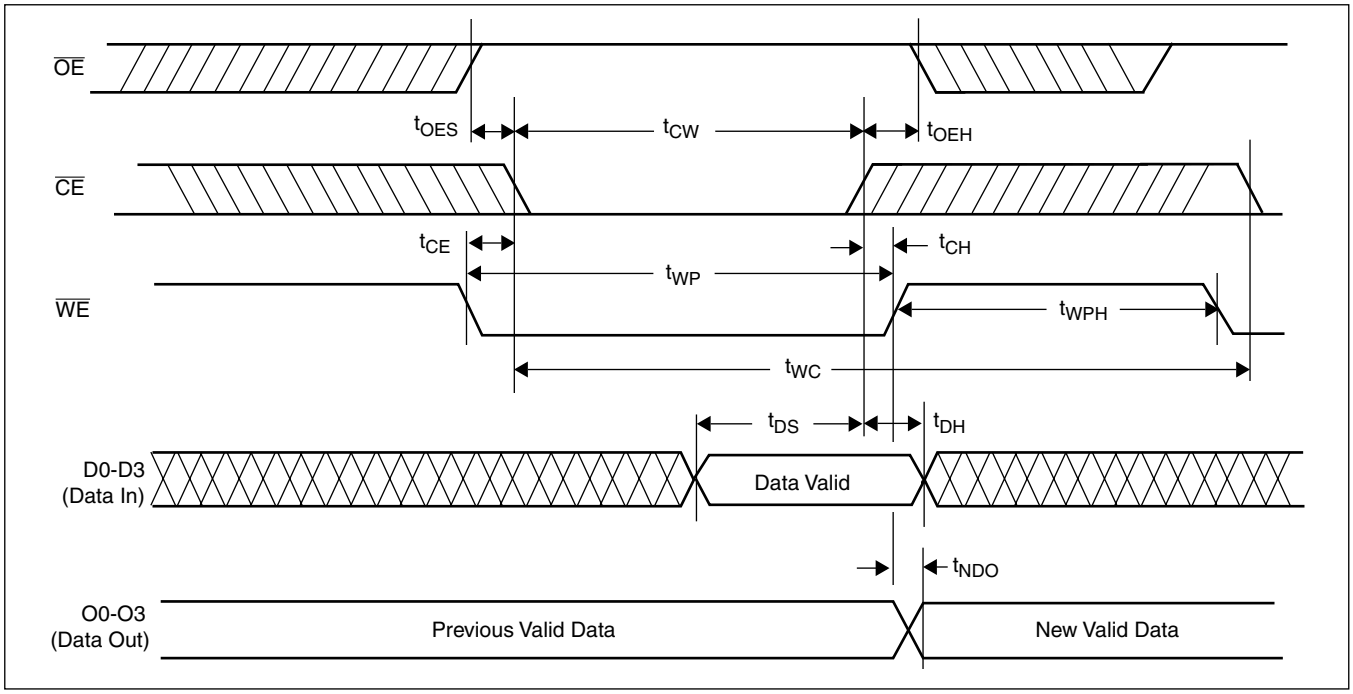
Symbol	Parameter	Min.	Max.	Unit
t_{WC}	Write cycle time	120		ns
t_{WC1}	Write cycle time	170		ns
t_{OES}	Output enable HIGH setup time	50		ns
t_{OEH}	Output enable HIGH hold time	50		ns
t_{CW}	Chip enable to end of write input	50		ns
t_{CE}	Write setup time	0		ns
t_{CH}	Write hold time	0		ns
t_{WP}	Write pulse width	50		ns
t_{WP1}	Write pulse width	100		ns
t_{WPH}	Write pulse HIGH recovery time	50		ns
t_{DS}	Data setup to end of write	40		ns
t_{DH}	Data hold time	0		ns
t_{NDO}	New data output		50	ns
t_{SOE}(10)	$\overline{OE}$ setup prior to operation in 2-wire mode	100		ms
t_{HOE}(10)	$\overline{OE}$ hold following operation in 2-wire mode	100		ms
t_{WZ}	Write enable to output in HIGH-Z		50	ns
t_{OW}	Output active from end of write	0		ns
t_{CHZ}(10)	Chip disable to output in high Z	0	50	ns
t_{OHZ}(10)	Output disable to output in high Z	0	50	ns

Note: (10)t_{LZ} and t_{OLZ} min.; t_{SOE} and t_{HOE} min; and t_{HZ} and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with CL = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

NOVRAM $\overline{WE}$ Controlled Write Cycle



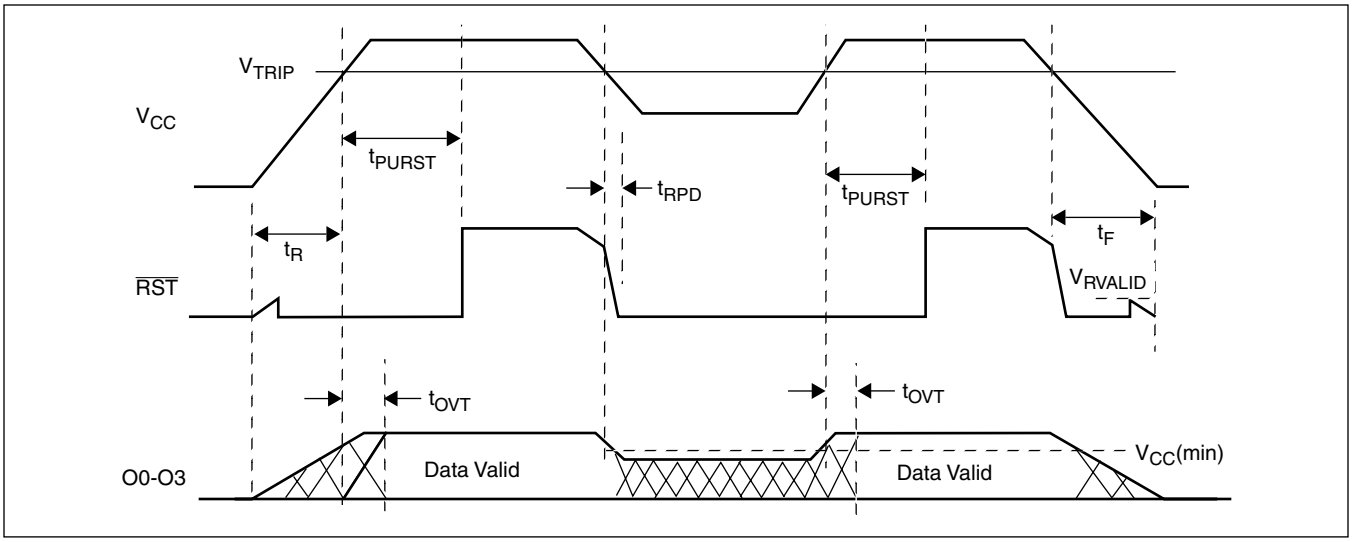
NOVRAM $\overline{CE}$ Controlled Write Cycle



LOW VOLTAGE DETECT/POWER CYCLE PARAMETERS

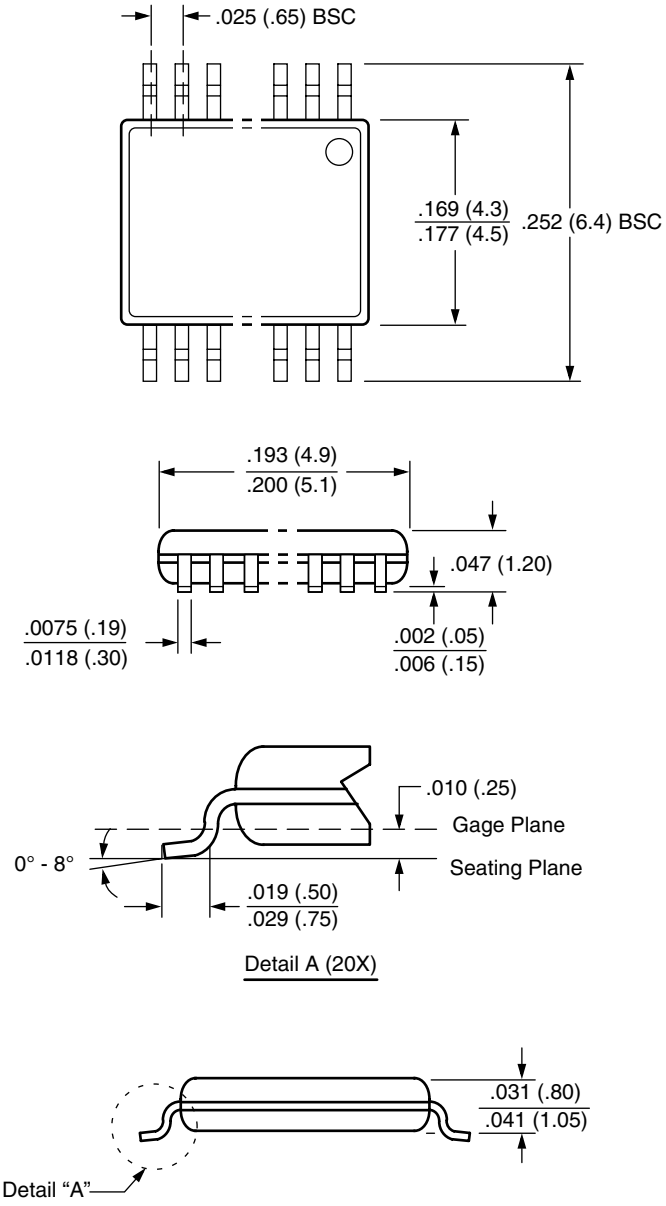
Symbols	Parameters	Min.	Typ.	Max.	Unit
V_{TRIP}	Reset trip voltage—blank	2.80	2.875	2.95	V
t_{RPD}	V_{CC} detect to reset active			500	ns
t_{PURST}	Power up reset time out delay (t_{PURST} Option 1)—default	100	200	400	ms
t_F	V_{CC} fall time from V_{CC} = 3V to V_{CC} = 2.5V	100			µs
t_R	V_{CC} rise time from V_{CC} = 2.5V to V_{CC} = 3V	100			µs
t_{OVT}	Output pins valid after V_{CC} exceeds V_{TRIP}			200	ns
V_{RVALID}	Reset valid V_{CC}	1			V

Low Voltage Detect and Output Pin Recall



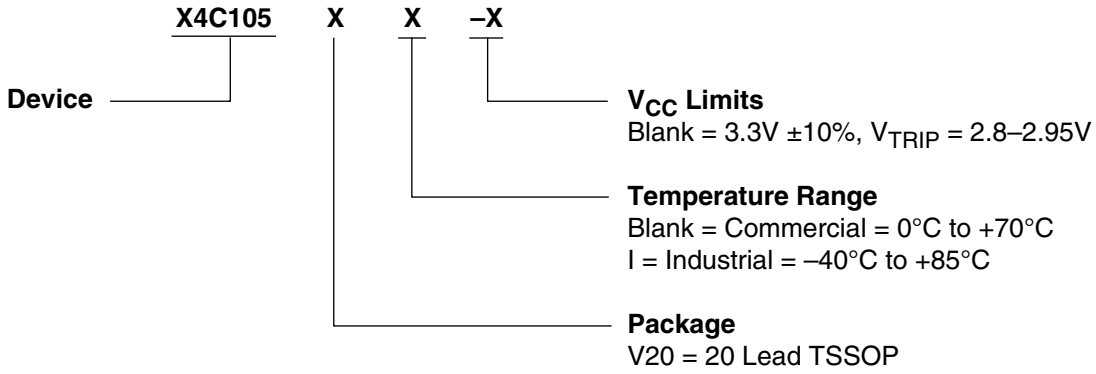
PACKAGING INFORMATION

20-Lead Plastic, TSSOP, Package Type V



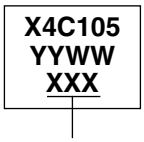
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information



Part Mark Convention

20-Lead TSSOP



Blank = 3.3V ±10%, 0 to +70°C, V_{TRIP} = 2.8–2.95V
I = 3.3 ±10%, -40 to +85°C, V_{TRIP} = 2.8–2.95V