# 64K XM20C64 8K x 8

## High Speed AUTOSTORE™ NOVRAM

### FEATURES

- **High Speed: $t_{AA}$ = 55ns**
- **NO Batteries!!**
- **Low Power CMOS**
- **AUTOSTORE™ NOVRAM**
  - **—Automatically Stores RAM data to E²PROM upon Power-fail Detection**
- **Open Drain AUTOSTORE Output Pin**
  - **—Provides Interrupt or Status Information**
  - **—Linkable to System Reset Circuitry**
- **Auto Recall**
  - **—Automatically Recalls E²PROM Data During Power-on**
- **Fully Decoded Module**
- **Full Military Temperature Range**
  - **— –55°C to +125°C**
- **High Reliability**
  - **—Endurance: 1,000,000 Nonvolatile Store Cycles**
  - **—Data Retention: 100 Years**
- **ESD Protection**
  - **—≥2KV All Pins**
- **Also Available in 66 Pin PUMA Package**

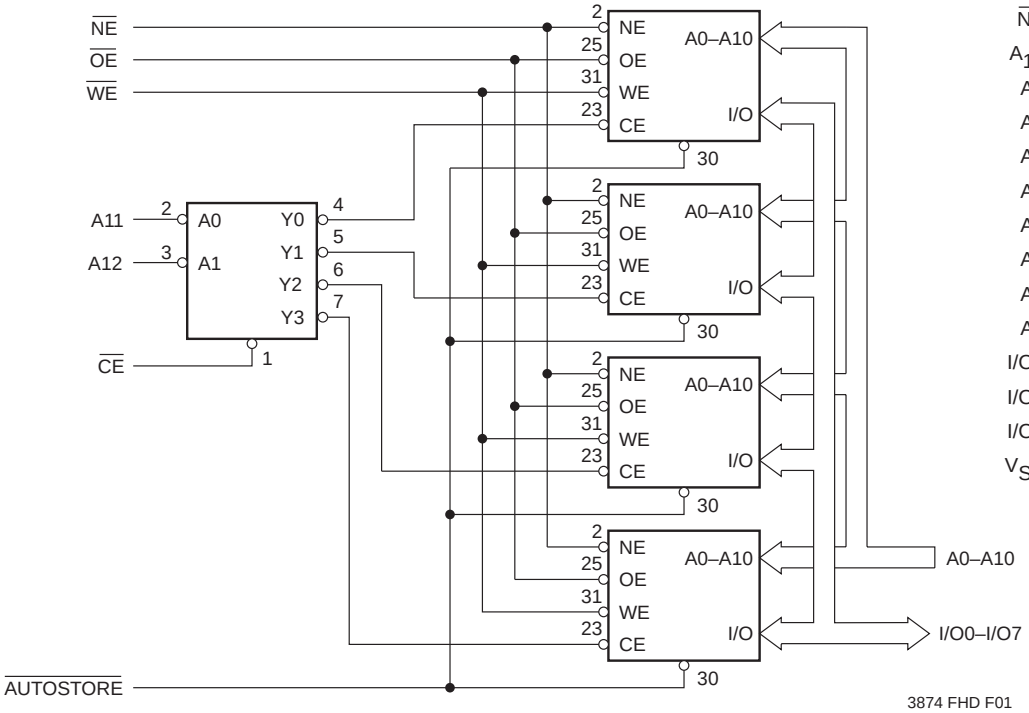
### DESCRIPTION

The XM20C64 is a high speed nonvolatile RAM Module. It is comprised of four Xicor X20C16 high speed NOVRAMs, a high speed decoder and decoupling capacitors mounted on a co-fired multilayered Ceramic substrate. The XM20C64 is configured 8K x 8 and is fully decoded. The module is a 28-lead DIP conforming to the industry standard pinout for SRAMs.

The XM20C64 fully supports the AUTOSTORE feature, providing hands-off automatic storing of RAM data into E²PROM when $V_{CC}$ falls below the AUTOSTORE threshold.

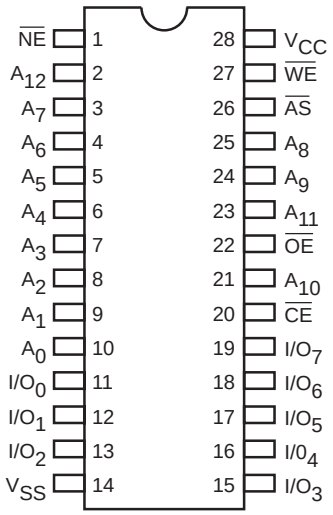
The XM20C64 is a highly reliable memory component, supporting unlimited writes to RAM, a minimum 1,000,000 store cycles and a minimum 100 year data retention.

### FUNCTIONAL DIAGRAM




3874 FHD F01

### PIN CONFIGURATION

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## PIN DESCRIPTIONS

### Addresses ($A_0$-$A_{12}$)

The address inputs select an 8-bit memory location during read and write operations.

### Chip Enable ($\overline{CE}$)

The chip enable input must be LOW to enable all read, write and user requested nonvolatile operations.

### Output Enable ($\overline{OE}$)

During normal RAM operations $\overline{OE}$ controls the data output buffers. If a hardware nonvolatile operation is selected ($\overline{NE}$ = $\overline{CE}$ = LOW) and $\overline{OE}$ strobes LOW, a recall operation will be initiated.

$\overline{OE}$ LOW will always disable a STORE operation regardless of the state of $\overline{NE}$, $\overline{WE}$, and $\overline{CE}$ so long as the internal transfer has not commenced.

### Write Enable ($\overline{WE}$)

During normal RAM operations $\overline{WE}$ = $\overline{CE}$ = LOW will cause data to be written to the RAM address pointed to by the $A_0$-$A_{12}$ inputs.

### Nonvolatile Enable ($\overline{NE}$)

The nonvolatile input controls the transfer of data from the $E^2$PROM array to the RAM array, when strobed LOW in conjunction with $\overline{CE}$ = $\overline{OE}$ = LOW.

### Data In/Data Out ($I/O_0$-$I/O_7$)

Data is written to or read from the X20C64 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

### AUTOSTORE Output ($\overline{AS}$)

$\overline{AS}$ is an open-drain output. When it is asserted (driving LOW) it indicates $V_{CC}$ has fallen below the AUTOSTORE threshold and an internal store operation has been initiated. Because $\overline{AS}$ is an open drain output it may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microprocessor.

## DEVICE OPERATION

NOVRAM operations are identical to those of a standard SRAM. When $\overline{OE}$ and $\overline{CE}$ are asserted data is presented at the I/Os from the address location pointed to by the $A_0$–$A_{12}$ inputs.

RAM write operations are initiated and the address input is latched by the HIGH to LOW transition of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

An array recall, $E^2$PROM data transferred to RAM, is initiated whenever $\overline{OE}$ = $\overline{NE}$ = $\overline{CE}$ = LOW. A recall is also performed automatically upon power-up.

### Command Sequence Operations

The X20C64 employs a version of the industry standard Software Data Protection (SDP). The end user can select various options for transferring data from RAM into the $E^2$PROM array.

All command sequences are comprised of three specific data/address write operations performed with $\overline{NE}$ LOW. A Store operation can be directly selected by issuing a Store command. The user may also enable and disable the AUTOSTORE function through the software data protection sequence. Refer to Table 1 below for a complete description of the command sequence.

### Operational Notes

The X20C64 should be viewed as a subsystem when writing software for the various store operations. The module contains four discrete components each needing to be set to the required state individually. The two high order address bits ($A_{11}$ and $A_{12}$) select only one of the four components.

**TABLE 1**

| Step | Operation | $A_0$–$A_{10}$* | Data Pattern |
|---|---|---|---|
| 1 | Write | 555 | AA |
| 2 | Write | 2AA | 55 |
| 3 | Write | 555 | Command |

3874 PGM T11

* It should be noted, the high order addresses should remain stable during the operations. It should also be noted that these commands are not global, that is only one device on the module will be affected by each command operation.

**TABLE 2**

| Command | Function |
|---|---|
| CC[H] | Enable Autostore |
| CD[H] | Disable Autostore |
| 33[H] | Store Operation |

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### Command Sequence Timing Limits

| Symbol | Parameter | Limits | | Units |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{STO}$ | Store Time | | 5 | ms |
| $t_{SP}$ | Command Write Pulse Width | 50 | | ns |
| $t_{SPH}$ | Inter Command Delay | 55 | | ns |

**Note:** All Write Command Sequence timings must conform to the standard write timing requirements.

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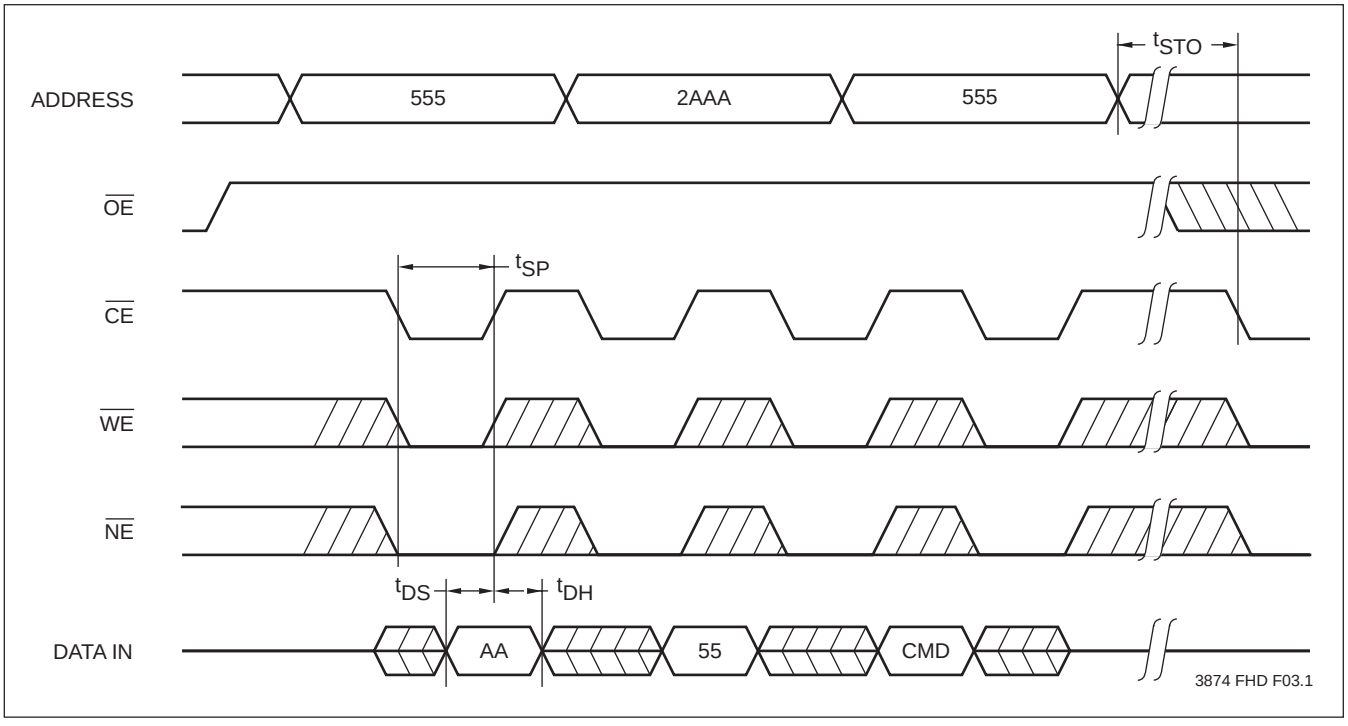
### Command Sequence

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**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias ..... –65°C to +125°C
Storage Temperature ..... –65°C to +125°C
Voltage on any Pin with
Respect to $V_{SS}$ ..... –1V to +7V
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the module. This is a stress rating only and the functional operation of the module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect module reliability.

**RECOMMENDED OPERATING CONDITIONS**

| Temperature | Min. | Max. |
|---|---|---|
| Military | –55°C | +125°C |

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| Supply Voltage | Limits |
|---|---|
| XM20C64 | 5V ±10% |

3874 PGM T07

**D.C. OPERATING CHARACTERISTICS** (Over recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Limits | | | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | Units | |
| $I_{CC1}$ | $V_{CC}$ Active Current | | 100 | mA | $\overline{NE}$ = $\overline{WE}$ + $V_{IH}$, $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, Address Inputs = TTL Inputs @ f = 20MHz All I/Os = Open |
| $I_{CC2}$ | $V_{CC}$ Active Current (AUTOSTORE) | | 10 | mA | All Inputs = $V_{IH}$, All I/Os = Open |
| $I_{SB}$ | $V_{CC}$ Standby Current | | 1.5 | mA | All Inputs = $V_{CC}$–0.3V All I/Os = Open |
| $I_{LI}$ | Input Leakage Current | | 10 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | 10 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$, $\overline{CE}$ = $V_{IH}$ |
| $V_{IL}$(1) | Input LOW Voltage | –0.5 | 0.8 | V | |
| $V_{IH}$(1) | Input HIGH Voltage | 2 | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output LOW Voltage | | 0.4 | V | $I_{OL}$ = 5mA |
| $V_{OLAS}$ | AUTOSTORE Output Voltage | | 0.4 | V | $I_{OLAS}$ = 1mA |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | V | $I_{OH}$ = –4mA |

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**POWER-UP TIMING**

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $t_{PUR}$ | Power-Up ($V_{CC}$ Min.) to RAM Operation | 500 | µs |
| $t_{PUST}$ | Power-Up ($V_{CC}$ Min.) to Store Operation | 5 | ms |

3874 PGM T09

**CAPACITANCE** $T_A$ = +25°C, f = 1MHz, $V_{CC}$ = 5V.

| Symbol | Test | Max. | Units | Conditions |
|---|---|---|---|---|
| $C_{I/O}$(2) | Input/Output Capacitance | 40 | pF | $V_{I/O}$ = 0V |
| $C_{IN}$(2) | Input Capacitance | 24 | pF | $V_{IN}$ = 0V |

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**Notes:** (1) $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

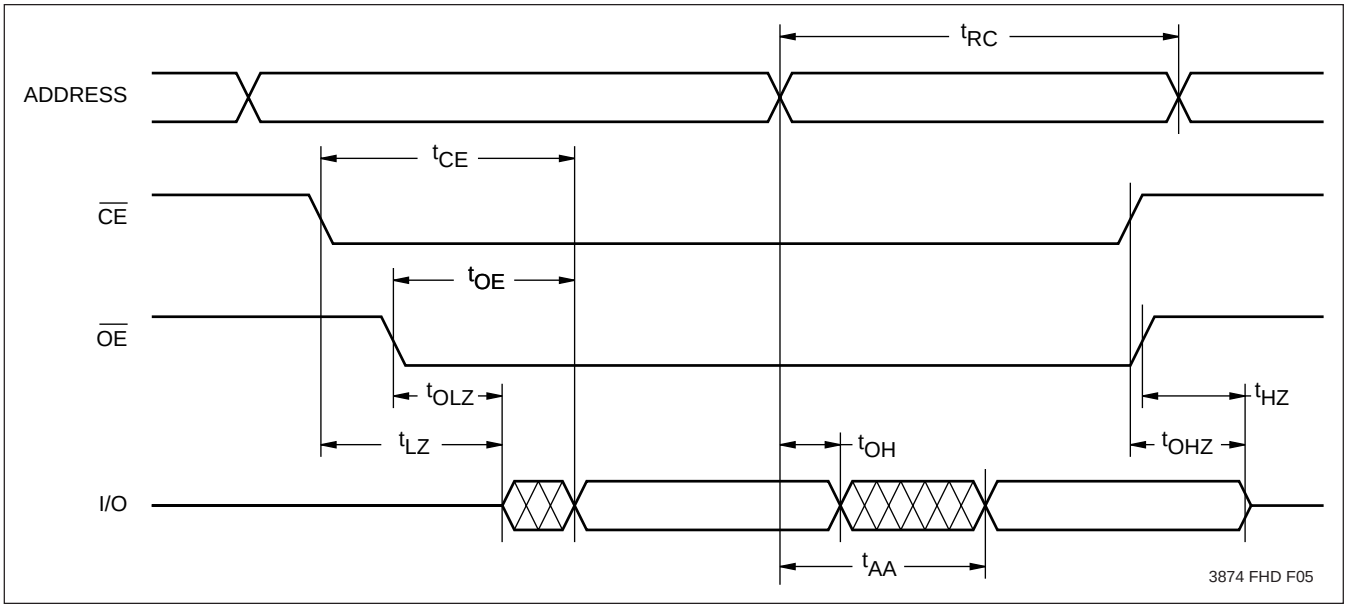
**A.C. CHARACTERISTICS** (Over the recommended operating conditions unless otherwise specified)

**Read Cycle Limits**

| Symbol | Parameter | Limits | | Units |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 55 | | ns |
| $t_{CE}$ | Chip Enable Access Time | | 55 | ns |
| $t_{AA}$ | Address Access Time | | 55 | ns |
| $t_{OE}$ | Output Enable Access Time | | 30 | ns |
| $t_{LZ}$(3) | $\overline{CE}$ Low to Output in Low Z | 0 | | ns |
| $t_{OLZ}$(3) | $\overline{OE}$ Low to Output in Low Z | 0 | | ns |
| $t_{HZ}$(3) | $\overline{CE}$ High to Output in Low Z | 0 | 25 | ns |
| $t_{OHZ}$(3) | $\overline{OE}$ High to Output in Low Z | 0 | 25 | ns |
| $t_{OH}$ | Output Hold | 0 | | ns |

3874 PGM T03

**Read Cycle Timing Diagram**




**Note:** (3) $t_{LZ}$ min., $t_{HZ}$ min., $t_{OLZ}$ min., and $t_{OHZ}$ min. are periodically sampled and not 100% tested. $t_{HZ}$ max. and $t_{OHZ}$ max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

**MODE SELECTION**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{NE}$ | $\overline{OE}$ | Mode | I/O State | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | Module Not Selected | High Z | Standby |
| L | H | H | L | Read RAM Active | Data Output | Active |
| L | L | H | X | Write RAM | Data Input | Active |
| L | L | L | H | Issue Software Command | Data Input | Active |
| L | H | H | H | Output Disabled | High Z | Active |
| L | H | L | L | Hardware Array Recall | High Z | Active |
| L | H | L | H | No Operation | High Z | Active |
| L | L | L | L | Not Allowed | High Z | Active |

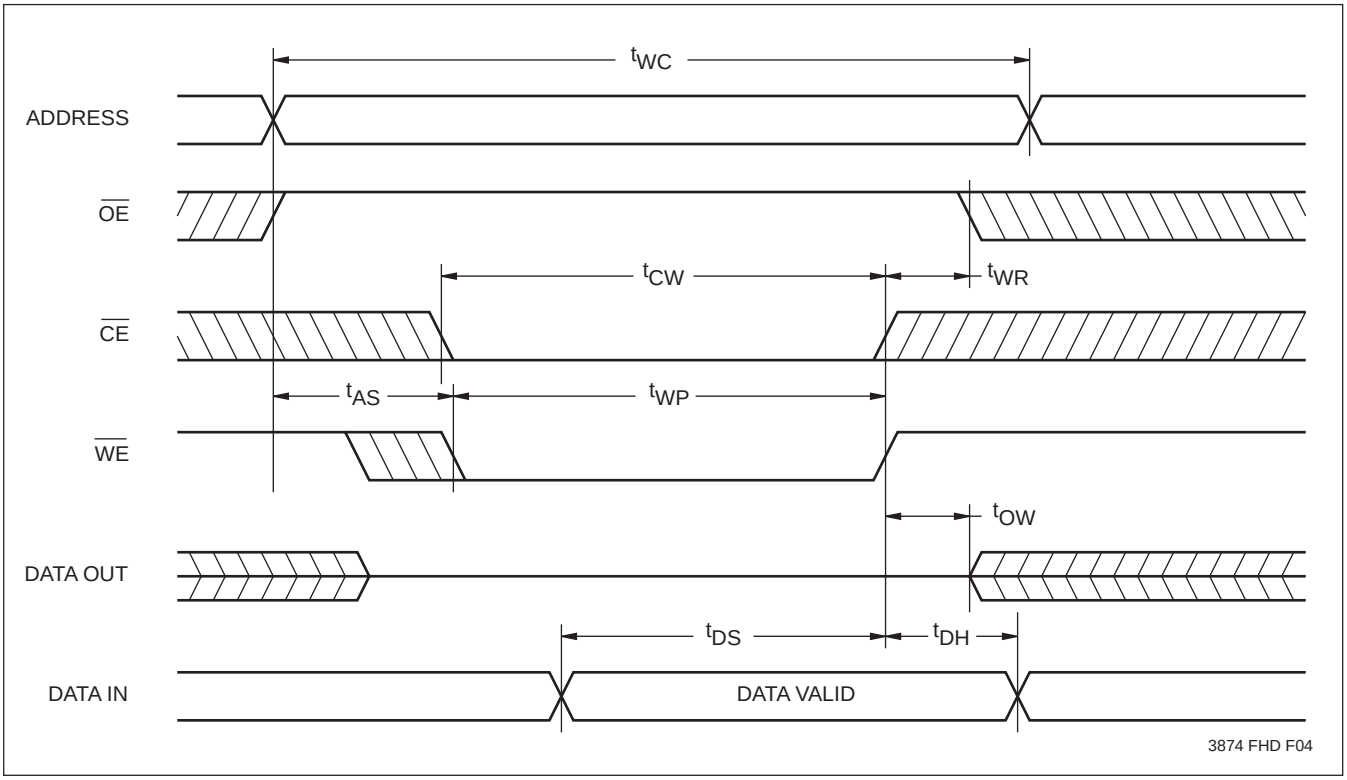
3874 PGM T04.1

### Write Cycle Limits

| Symbol | Parameter | Limits | | Units |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{WC}$ | Write Cycle time | 55 | | ns |
| $t_{WP}$ | $\overline{WE}$ Pulse Width | 40 | | ns |
| $t_{CW}$ | $\overline{CE}$ Pulse Width | 40 | | ns |
| $t_{AS}$ | Address Setup | 0 | | ns |
| $t_{DS}$ | Data Setup | 25 | | ns |
| $t_{DH}$ | Data Hold | 0 | | ns |
| $t_{OW}$ | Output Active from End of Write | | 5 | ns |
| $t_{WR}$ | End of Write to Read | 0 | | ns |

3874 PGM T02

### Write Cycle Timing Diagram




3874 FHD F04

### Array Recall Timing

| Symbol | Parameter | Limits | | Units |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{RCC}$ | Array Recall Time | | 10 | µs |
| $t_{RCP}$ | Recall Strobe Pulse Width | 50 | | ns |
| $t_{RWE}$ | Delay From $\overline{WE}$ HIGH to Recall | 0 | | ns |

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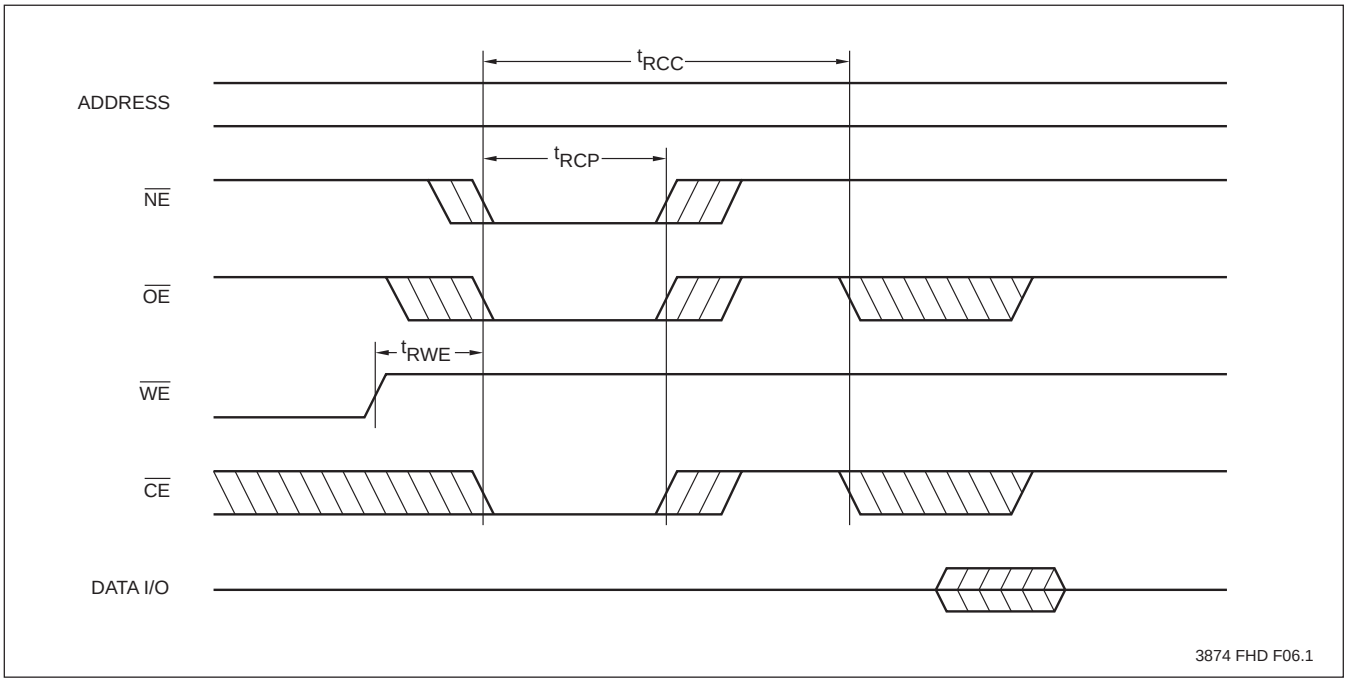
**Note:** The recall sequence must be repeated for each memory component individually. This is accomplished by sequencing through the Array Recall Cycle with all four combinations of $A_{11}$, and $A_{12}$.

### Array Recall Cycle

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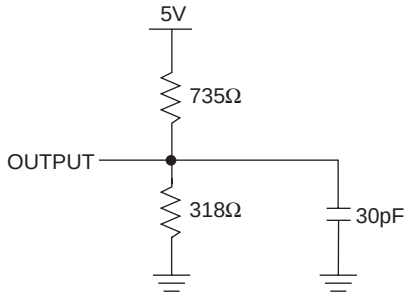
### EQUIVALENT TEST LOAD CIRCUIT

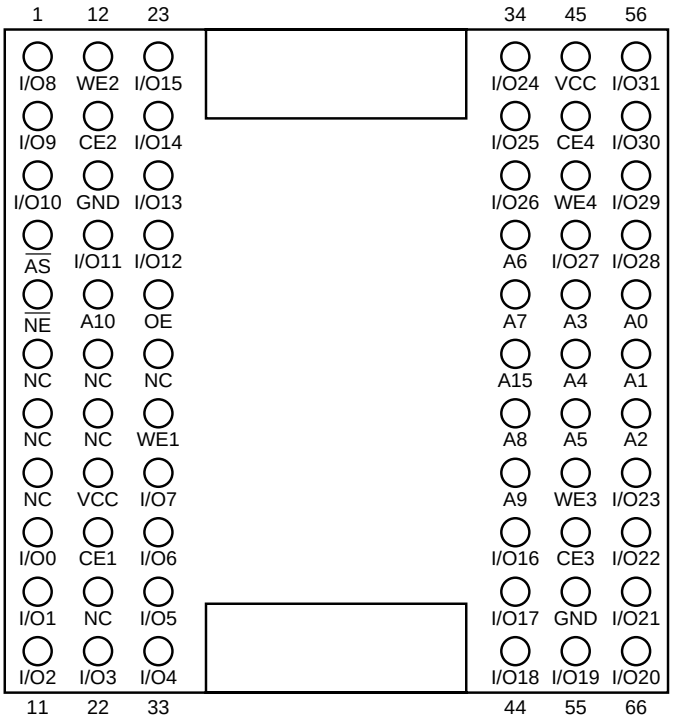



3874 FHD F07.2

### SYMBOL TABLE

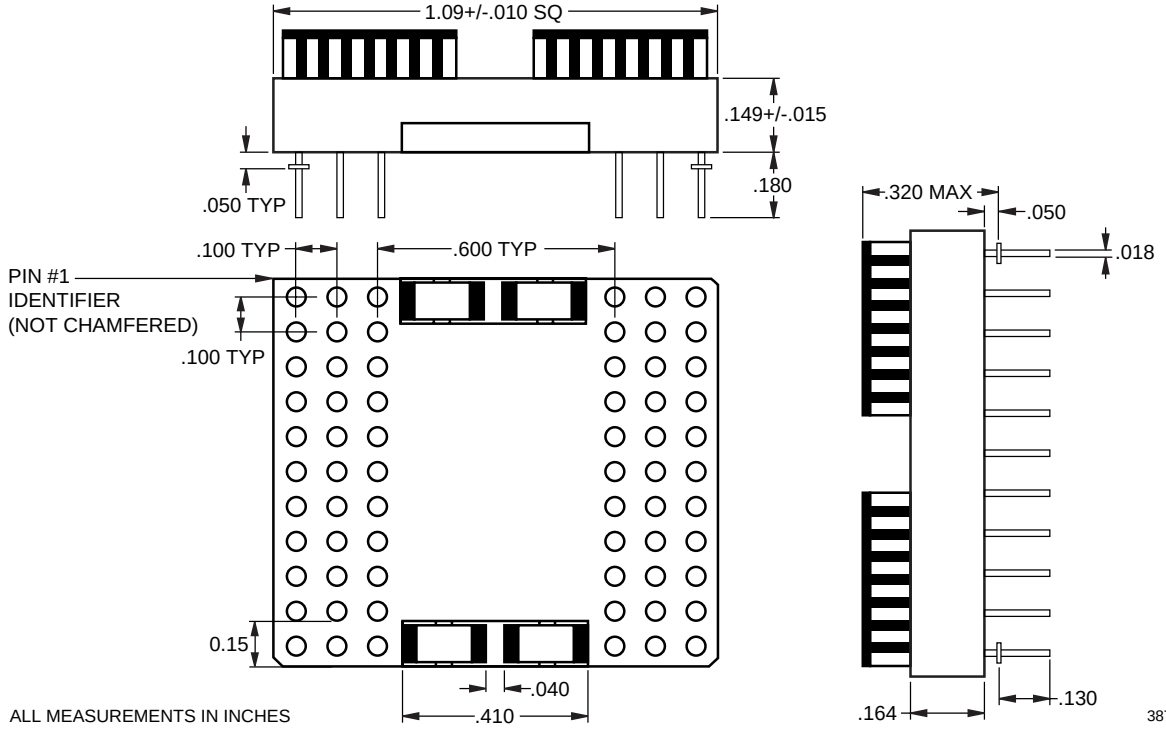
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from LOW to HIGH | Will change from LOW to HIGH |
| | May change from HIGH to LOW | Will change from HIGH to LOW |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

## PIN CONFIGURATION




3874 ILL F10

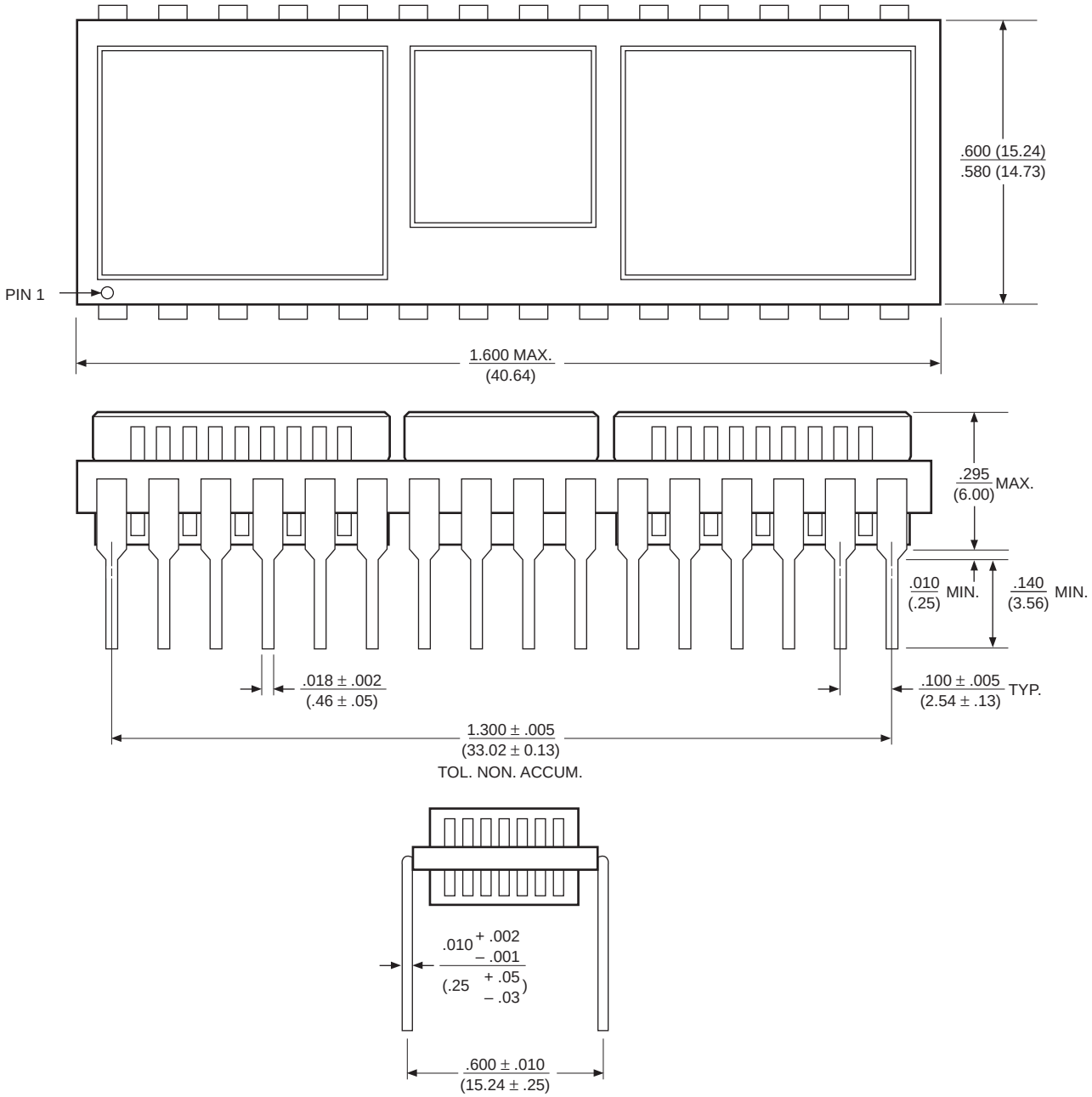
## PACKAGING INFORMATION




3874 ILL F11

## PACKAGING INFORMATION

### 28-PIN DUAL-IN-LINE PACKAGE CERAMIC LEADLESS CHIP CARRIERS ON CERAMIC SIDEBRAZED CERAMIC SUBSTRATE




**NOTES:**
**1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
**2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY**

3926 FHD F40

## ORDERING INFORMATION
**XM20C64: 2K X 8 CMOS NOVRAM Memory Module**