68XX Microcontroller Family Compatible

256K X68257 32,768 x 8 Bit

E^2 Micro-Peripheral

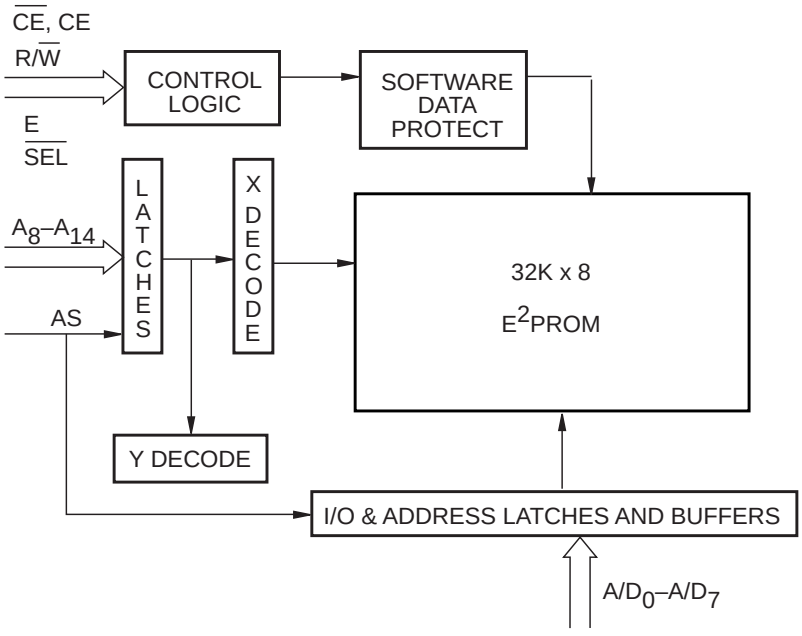
FEATURES

- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular 68HC11 Family**
- **High Performance CMOS**
  - **—Fast Access Time, 120ns**
  - **—Low Power**
    - **—60mA Active Maximum**
    - **—500μA Standby Maximum**
- **Software Data Protection**
- **Toggle Bit Polling**
  - **—Early End of Write Detection**
- **Page Mode Write**
  - **—Allows up to 128 Bytes to be Written in One Write Cycle**
- **High Reliability**
  - **—Endurance: 10,000 Write Cycle**
  - **—Data Retention: 100 Years**
- **28-Lead PDIP Package**
- **28-Lead SOIC Package**
- **32-Lead PLCC Package**

DESCRIPTION

The X68257 is an 32K x 8 E^2PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X68257 features a multiplexed address and data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

FUNCTIONAL DIAGRAM



6539 ILL F02.2

PIN DESCRIPTIONS

Address/Data (A/D_0–A/D_7)

Multiplexed low-order addresses and data. The addresses flow into the device while AS is HIGH. After AS transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on R/$\overline{W}$, $\overline{SEL}$, and CE.

Addresses (A_8–A_{14})

High order addresses flow into the device when AS = V_{IH} and are latched when AS goes LOW.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, AS is LOW, and CE is LOW, the X68257 is placed in the low power standby mode.

Chip Enable (CE)

Chip Enable is active HIGH. When CE is used to select the device, the CE must be tied HIGH.

Program Store Enable ($\overline{SEL}$)

When the X68257 is to be used in a 68XX-based system, $\overline{SEL}$ is tied to V_{SS}.

Read/Write (R/$\overline{W}$)

When the X68257 is to be used in a 68XX-based system, R/$\overline{W}$ is tied directly to the microcontroller's R/$\overline{W}$ output.

Address Strobe (AS)

Addresses flow through the latches to address decoders when AS is HIGH and are latched when AS transitions from a HIGH to LOW.

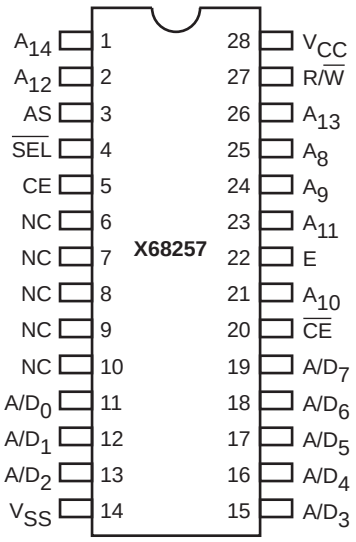
PIN NAMES

Symbol	Description
AS	Address Strobe
A/D_0–A/D_7	Address Inputs/Data I/O
A_8–A_{14}	Address Inputs
E	Enable Input
R/$\overline{W}$	Read/Write Input
CE, $\overline{CE}$	Chip Enable
$\overline{SEL}$	Device Select—Connect to V_{SS}
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

6539 PGM T01.2

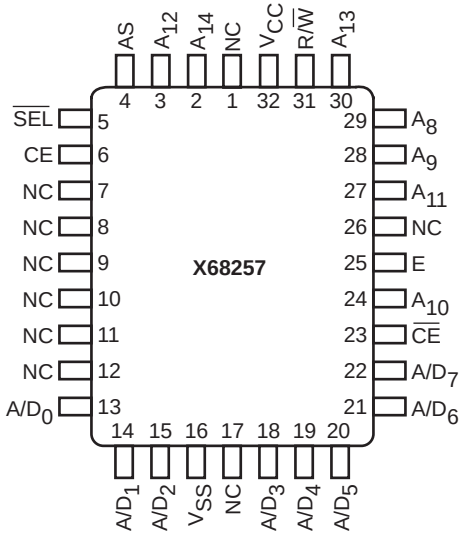
PIN CONFIGURATION

PDIP
SOIC



6539 FHD F01.3

PLCC



6539 FHD F01A.5

PRINCIPLES OF OPERATION

The X68257 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X68257 provides 32K-bytes of 5V E^{2}PROM which can be used either for program storage, data storage, or a combination of both, in systems based upon Von Neumann (68XX) architectures. The X68257 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the address/data bus to provide a “seamless” interface.

The interface inputs on the X68257 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller.

The X68257 features the industry standard 5V E^{2}PROM characteristics such as byte or page mode write and Toggle Bit Polling.

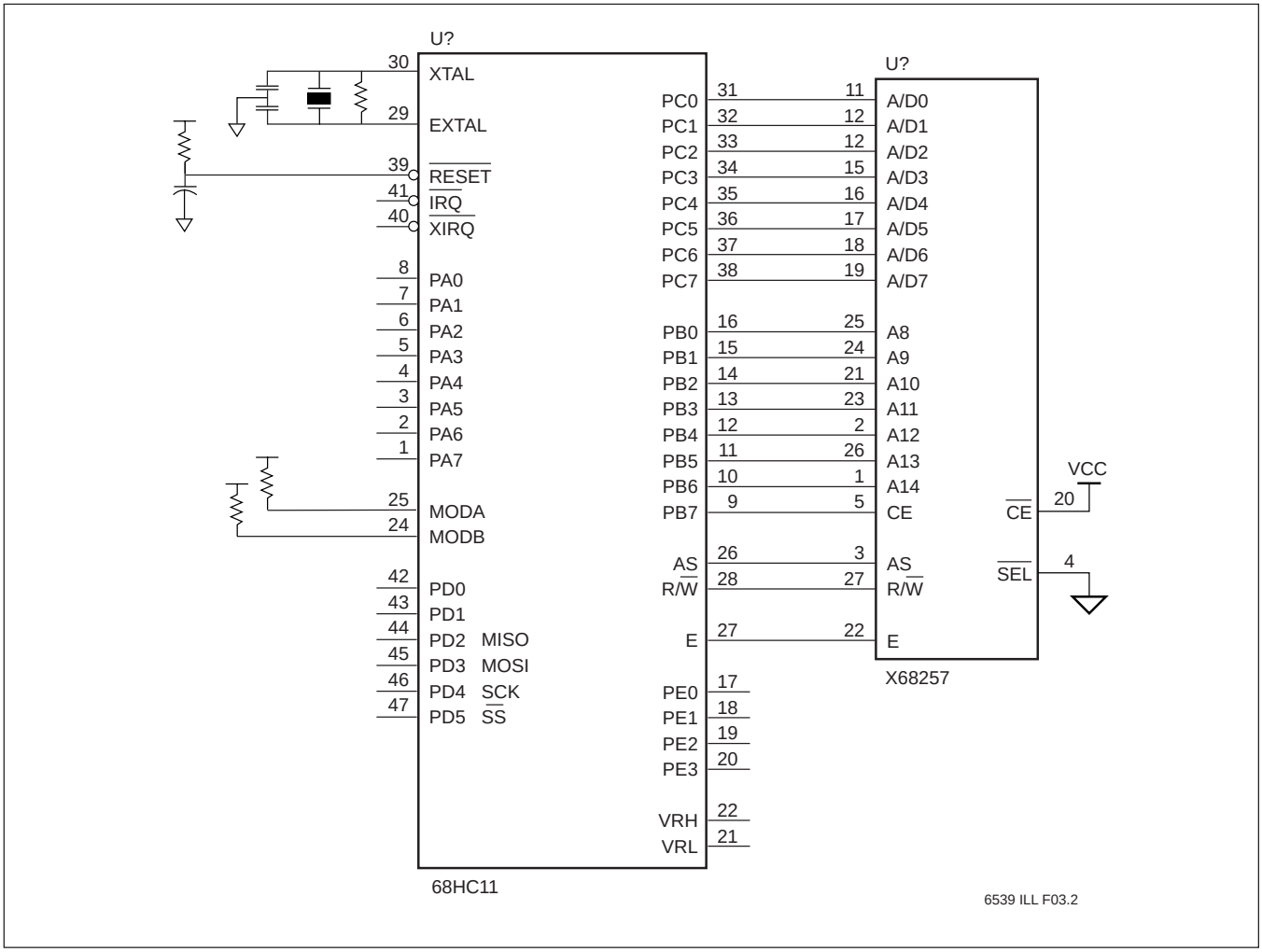
DEVICE OPERATION

Motorola 68XX operation requires the microcontroller AS, E, and R/$\overline{W}$ outputs to be tied to the X68257 AS, E, and R/$\overline{W}$ inputs respectively.

The falling edge of AS will latch the addresses for both a read and write operation. The state of the R/$\overline{W}$ output determines the operation to be performed, with the E signal acting as a data strobe.

If R/$\overline{W}$ is HIGH and CE is HIGH (read operation) data will be output on A/D_0–A/D_7 after E transitions HIGH. If R/$\overline{W}$ is LOW and CE is HIGH (write operation) data present at A/D_0–A/D_7 will be strobed into the X68257 on the HIGH to LOW transition of E.

Typical Application



MODE SELECTION

CE	E	R/$\overline{W}$	Mode	I/O	Power
V_{SS}	X	X	Standby	High Z	Standby (CMOS)
LOW	X	X	Standby	High Z	Standby (TTL)
HIGH	HIGH	HIGH	Read	D_{OUT}	Active
HIGH	↘	LOW	Write	D_{IN}	Active

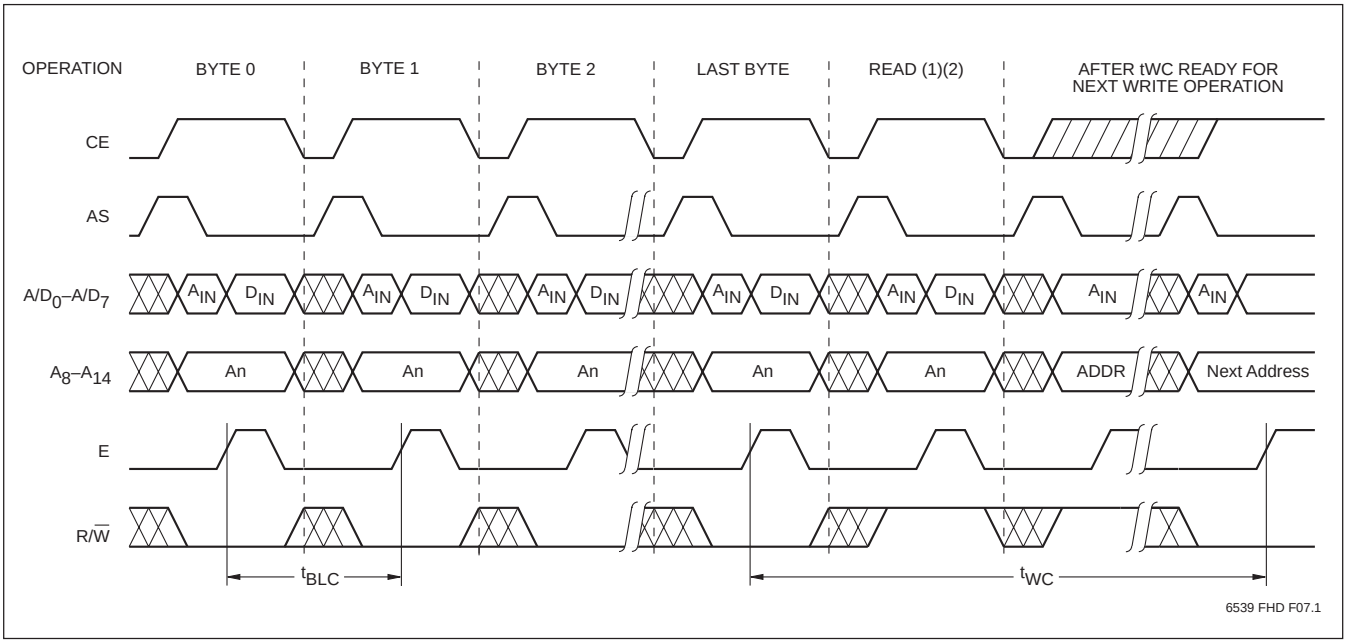
6539 PGM T02.2

PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X68257 supports page mode write operations. This allows the microcontroller to write from 1 to 128 bytes of data to the X68257. Each individual write within a page write operation must conform to the byte write timing requirements.

The rising edge of E starts a timer delaying the internal programming cycle 100µs. Therefore, each successive write operation must begin within 100µs of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for E Controlled Operation

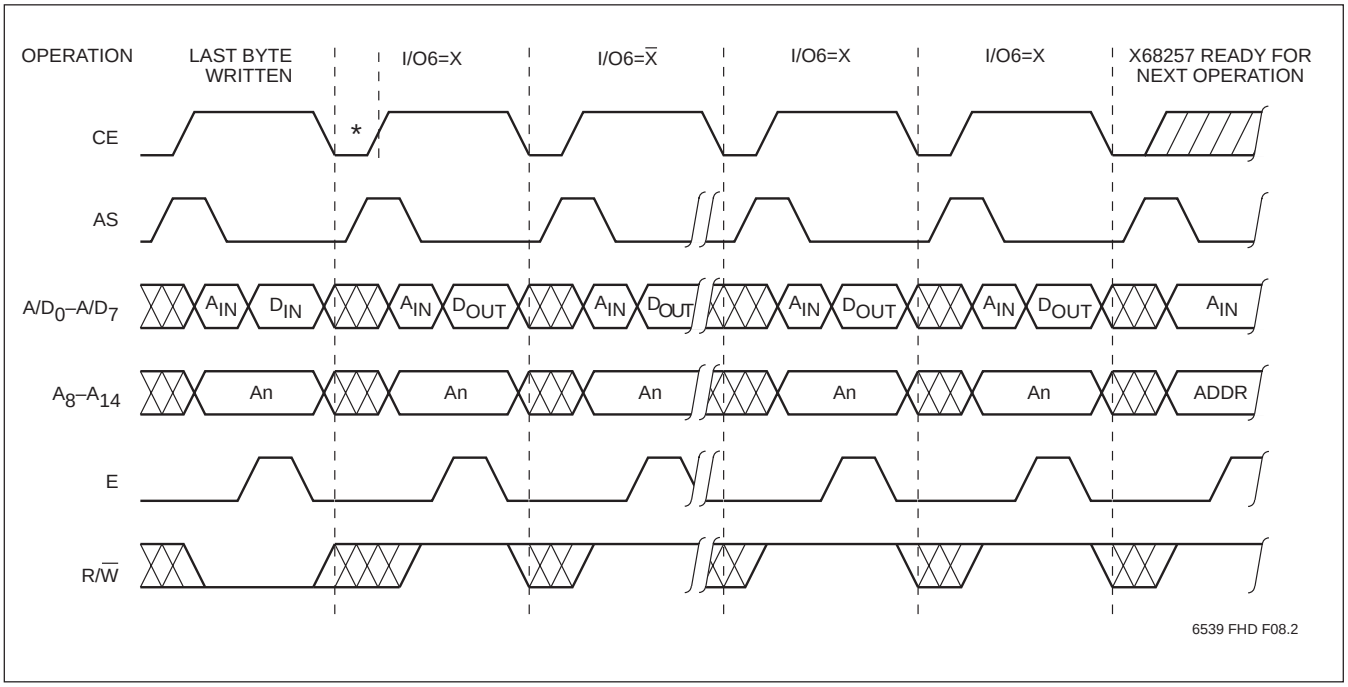


Note: (1) For each successive write within a page write cycle A_7–A_{14} must be the same.

Toggle Bit Polling

Because the typical write timing is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early end of write. During the internal programming cycle I/O_6 will toggle from “1” to “0” and “0” to “1” on subsequent attempts to read the device. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations.

Toggle Bit Polling E Control



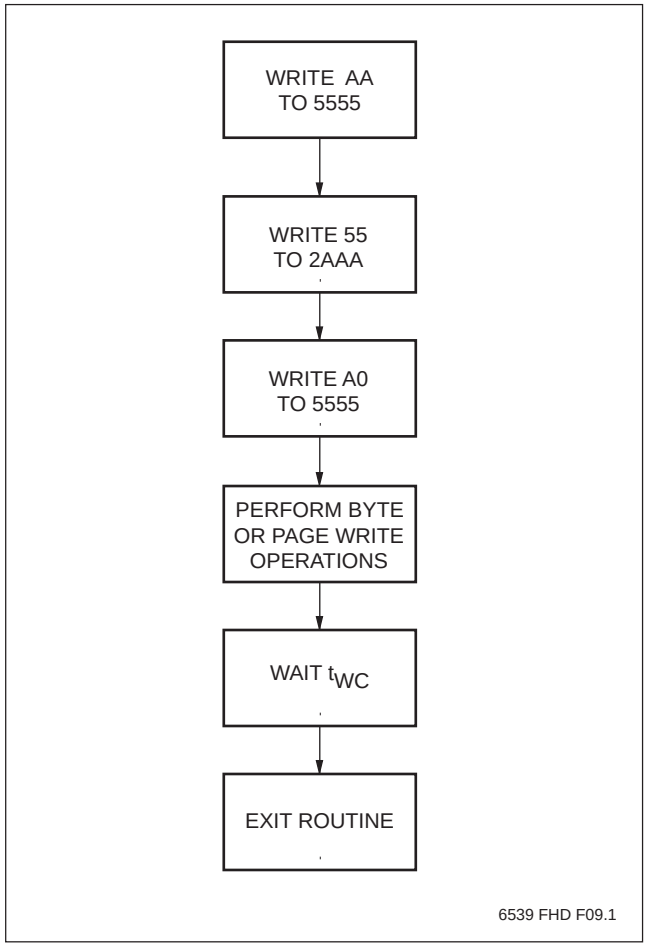
* Minumum time delay of 200 µs is required between the last byte write and start of the toggle bit polling sequence.

Software Data Protection

Software Data Protection (SDP) is employed to protect the entire array against inadvertent writes. To write to the X68257, a three-byte command sequence must precede the byte(s) being written.

All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

Writing with SDP



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

6539 PGM T03.1

Supply Voltage	Limits
X68257	5V ±10%

6539 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	CE = V_{IL}, All I/O's = Open, Other Inputs = V_{CC}, AS = V_{IH}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		500	µA	CE = V_{SS}, All I/O's = Open,Other Inputs = V_{CC} – 0.3V, AS = V_{SS}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		6	mA	CE = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, AS = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, E = V_{IL}
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

6539 PGM T05.1

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

6539 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to Read	1	ms
t_{PUW}(2)	Power-Up to Write	5	ms

6539 PGM T07

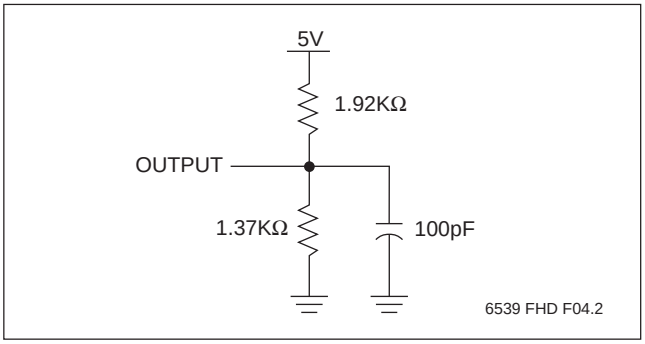
Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

6539 PGM T08.1

TEST CIRCUIT



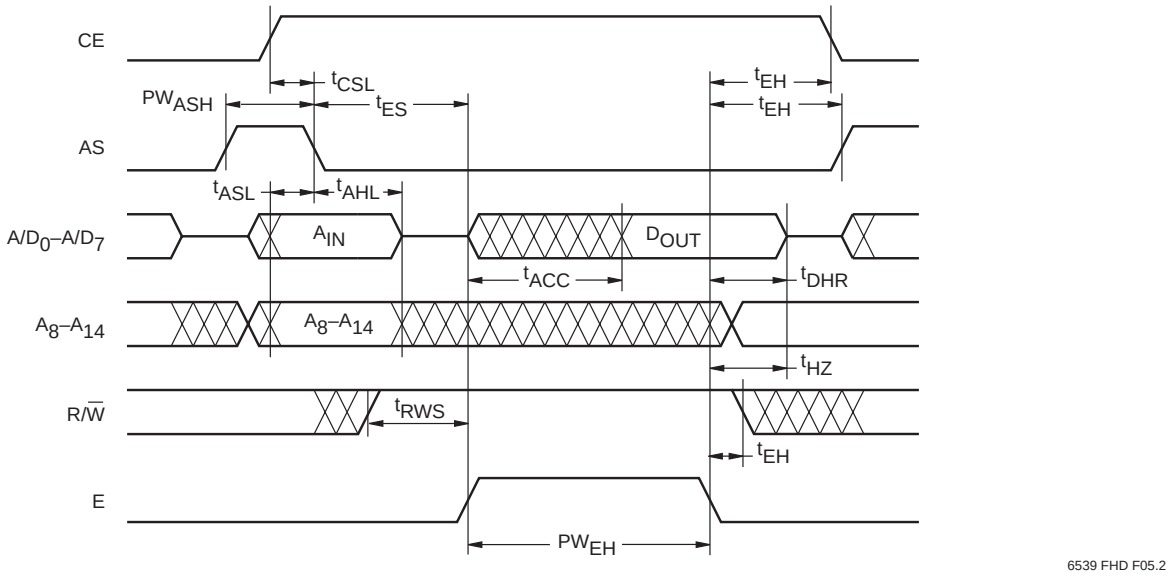
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

E Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
PW_{ASH}	Address Strobe Pulse Width	80		ns
t_{ASL}	Address Setup Time	20		ns
t_{AHL}	Address Hold Time	30		ns
t_{ACC}	Data Access Time		120	ns
t_{DHR}	Data Hold Time	0		ns
t_{CSL}	CE Setup Time	7		ns
PW_{EH}	E Pulse Width	150		ns
t_{ES}	Enable Setup Time	30		ns
t_{EH}	E Hold Time	20		ns
t_{RWS}	R/$\overline{W}$ Setup Time	20		ns
t_{HZ}(3)	E LOW to High Z Output		50	ns
t_{LZ}(3)	E HIGH to Low Z Output	0		ns

6539 PGM T09.1

E Controlled Read Cycle



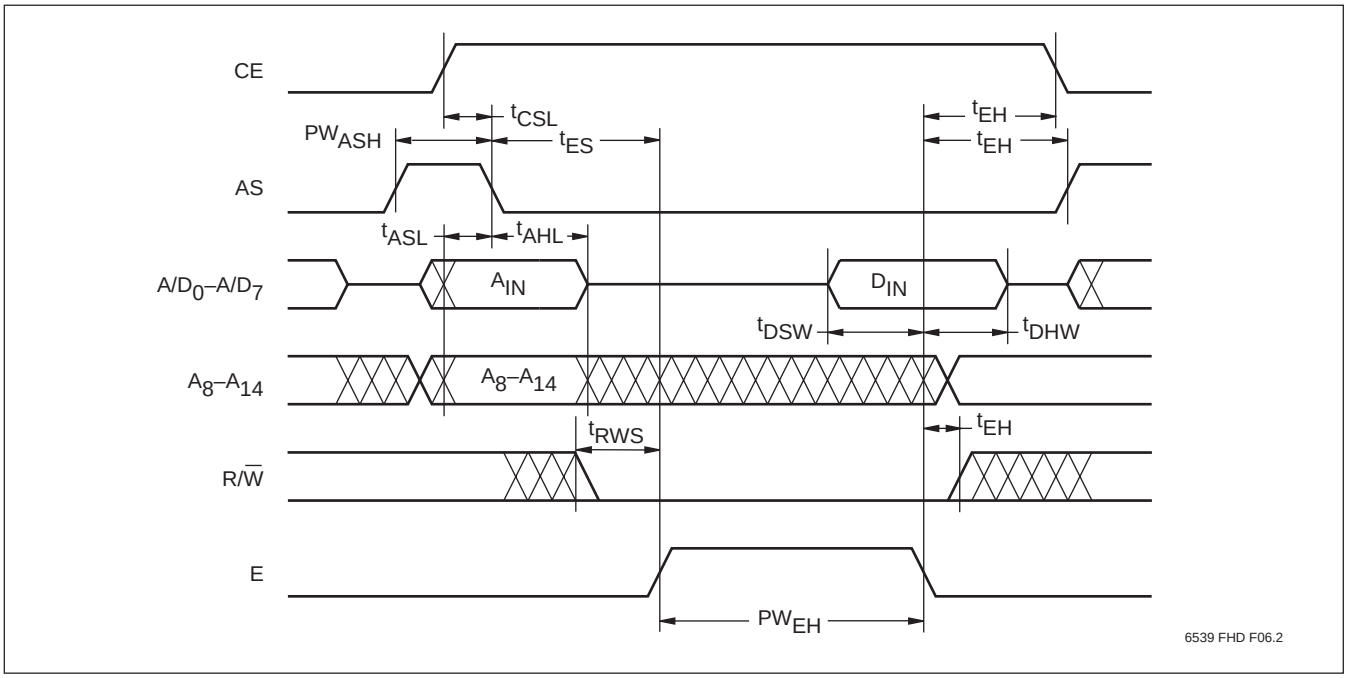
Note: (3) This parameter is periodically sampled and not 100% tested.

E Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
PW_{ASH}	Address Strobe Pulse Width	80		ns
t_{ASL}	Address Setup Time	20		ns
t_{AHL}	Address Hold Time	30		ns
t_{DSW}	Data Setup Time	50		ns
t_{DHW}	Data Hold Time	30		ns
t_{CSL}	CE Setup Time	7		ns
PW_{EH}	E Pulse Width	120		ns
t_{WC}	Write Cycle Time		5	ms
t_{ES}	Enable Setup Time	30		ns
t_{RWS}	R/$\overline{W}$ Setup Time	20		ns
t_{EH} 6539 FHD F05.2	E Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs

6539 PGM T10

E Controlled Write Cycle



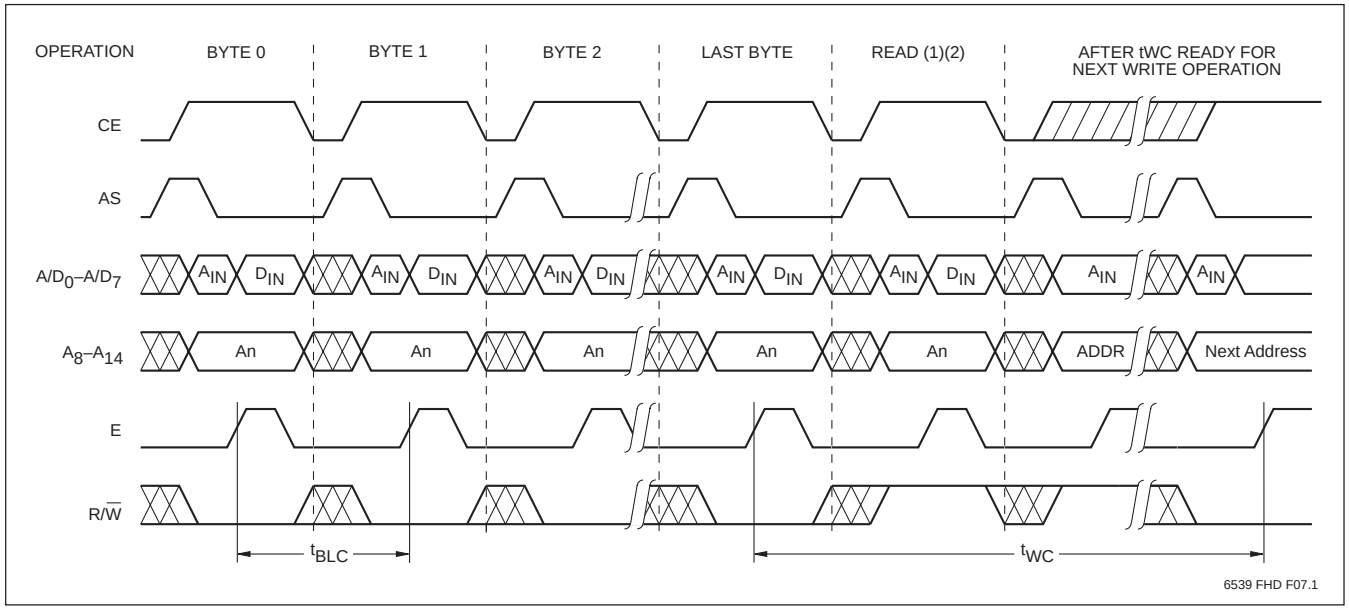
Note: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{DVWH}	Data Setup Time	50		ns
t_{WHDX}	Data Hold Time	30		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
t_{WRS}	$\overline{WR}$ Setup Time	30		ns
t_{WRH}	$\overline{WR}$ Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs
t_{WC} (7)	Write Cycle Time		5	ms

6539 PGM T11

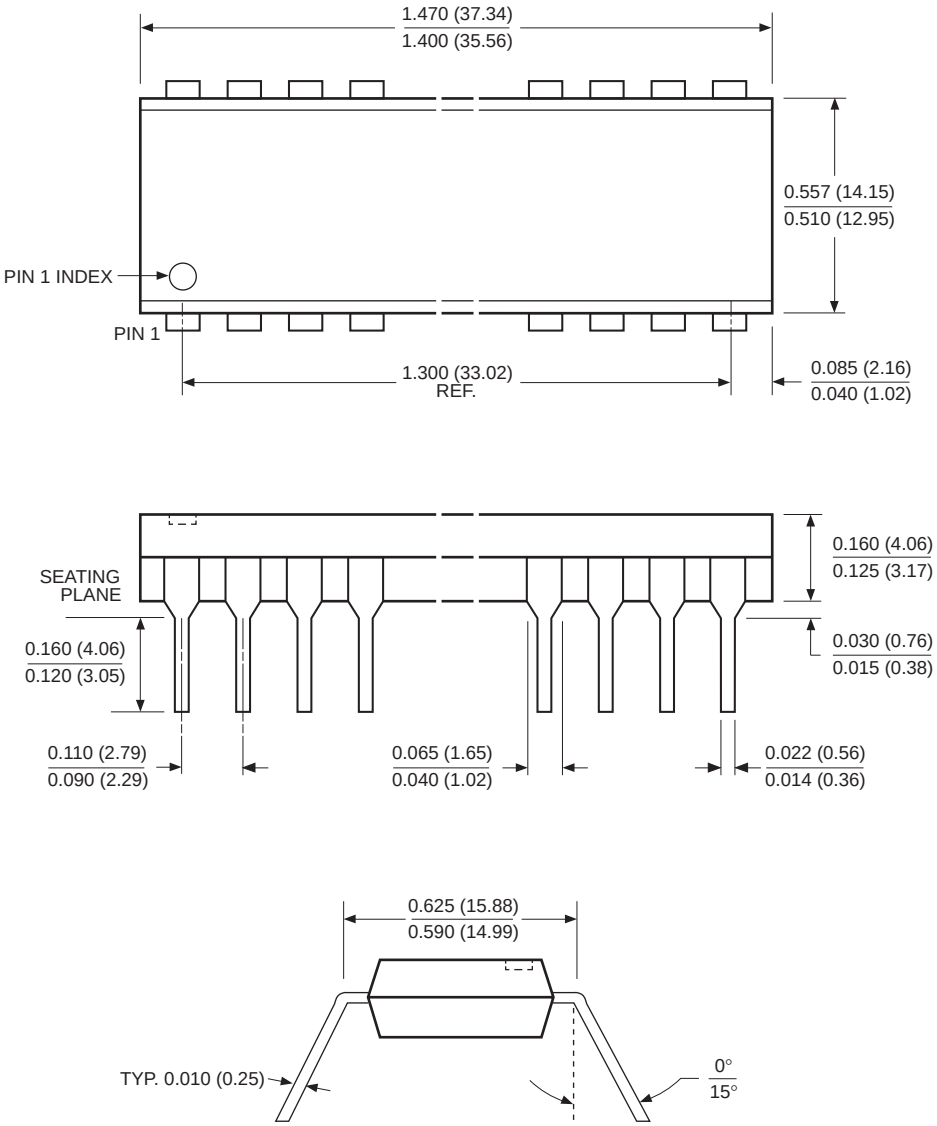
$\overline{WR}$ Controlled Write Timing Diagram



Note: (7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

PACKAGING INFORMATION

28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



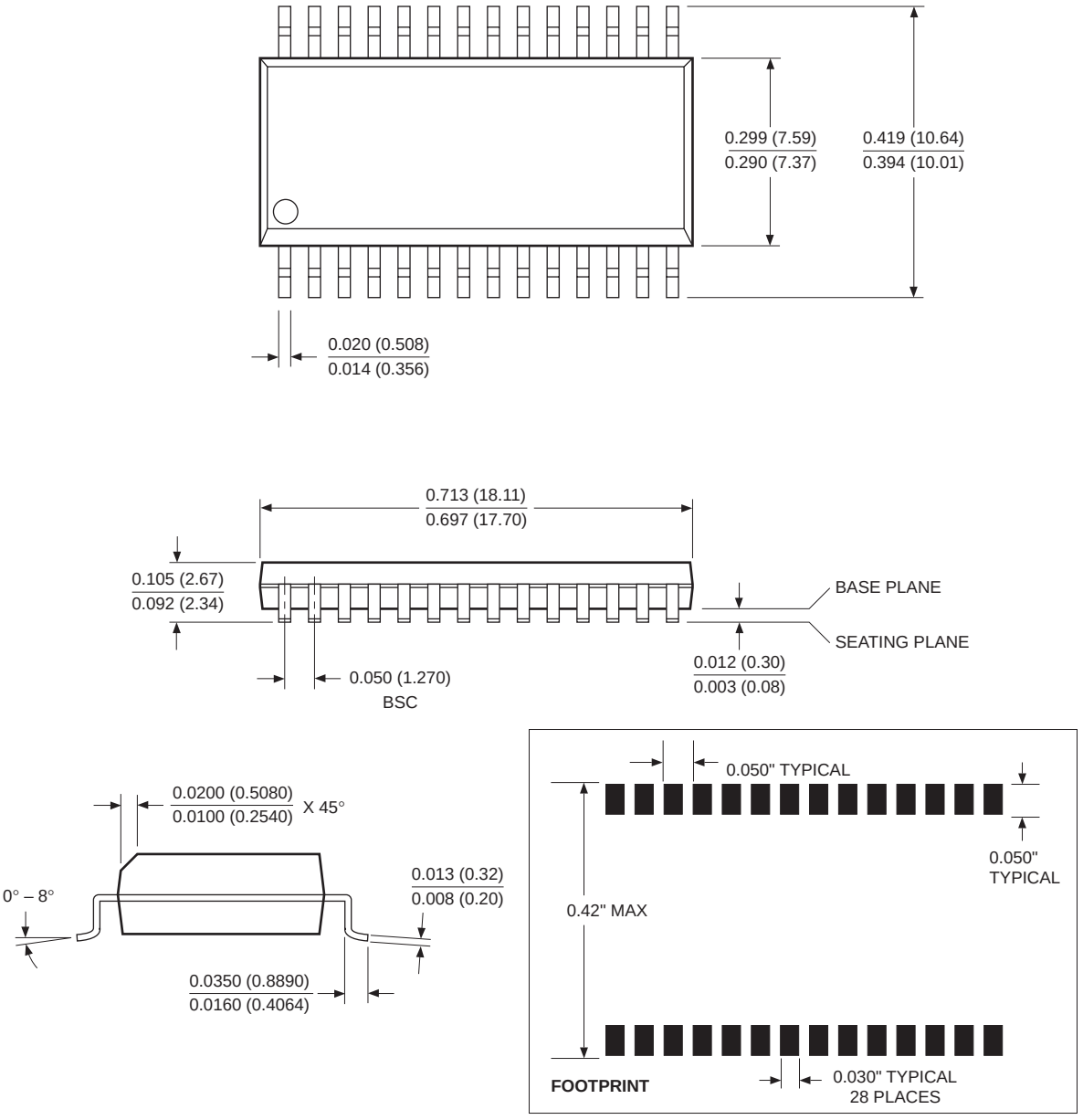
NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F04

PACKAGING INFORMATION

28-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTES:

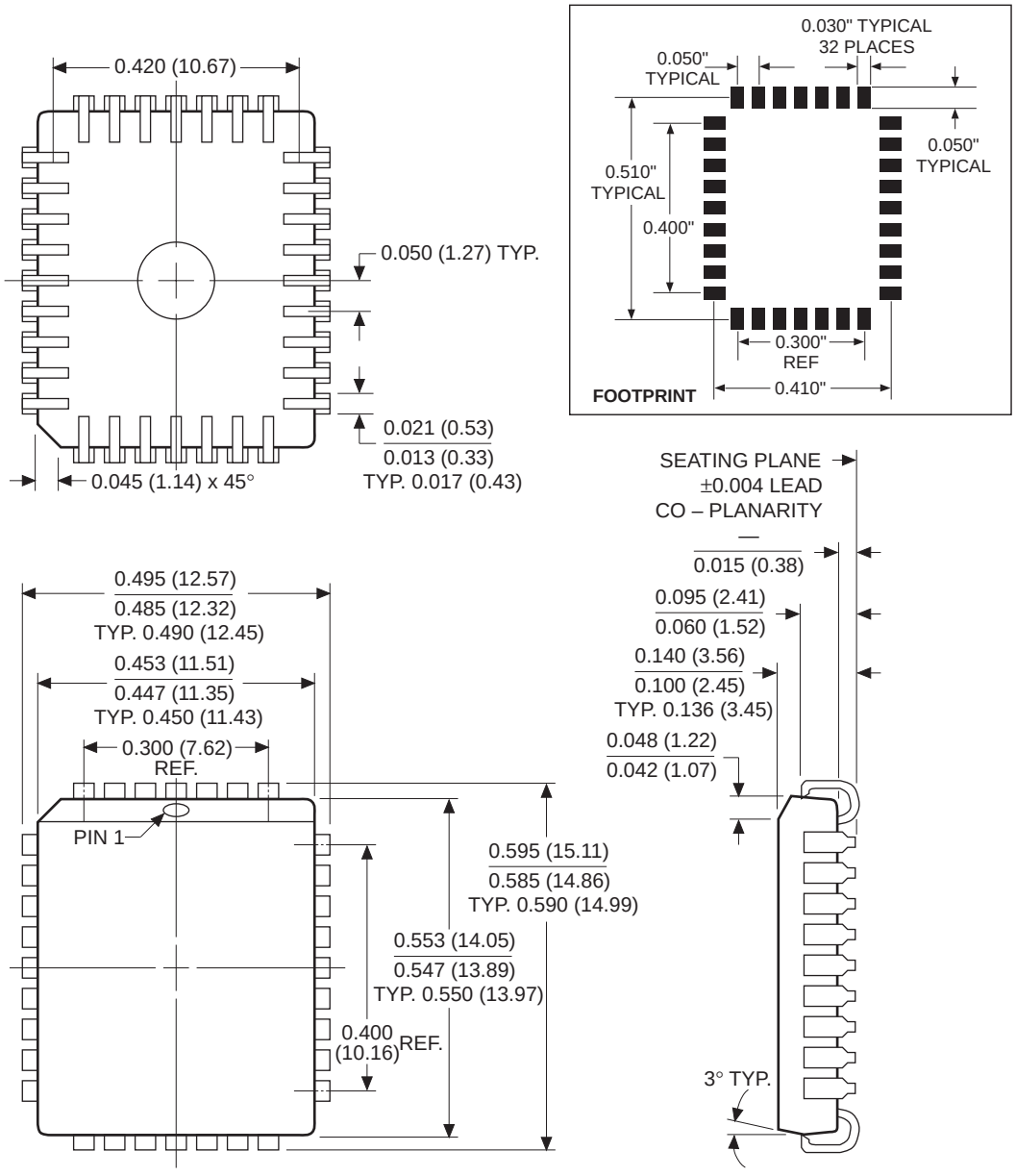
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

3926 FHD F17

PACKAGING INFORMATION

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

3926 FHD F13

ORDERING INFORMATION