64K X55060

Dual Voltage Monitor with Integrated System Battery Switch and EEPROM

FEATURES

- **Dual voltage monitoring**
- **System battery switch-over circuitry**
- **Early warning low V_{CC} fail indicator**
- **Active high and active low reset outputs**
- **Selectable watchdog timer**
  - **—(0.15s, 0.4s, 0.8s, off)**
- **Low V_{CC} (V1MON) and V2MON detection and reset assertion**
  - **—Four standard reset threshold voltages**
  - **—Re-program $V1_{TRIP}$ and $V2_{TRIP}$ reset threshold voltage using special programming sequence**
  - **—Reset signal valid to V_{CC} = 1V**
- **Long battery life with low power consumption**
  - **—<50µA max standby current, watchdog on**
  - **—<30µA max standby current, watchdog off**
  - **—<1.5mA max active current during read**
- **64Kbits of EEPROM**
- **Built-in inadvertent write protection**
  - **—Power-up/power-down protection circuitry**
  - **—In circuit programmable ROM mode**
- **10MHz SPI interface modes (0,0 & 1,1)**
- **Minimize EEPROM programming time**
  - **—64-byte page write mode**
  - **—Self-timed write cycle**
  - **—5ms write cycle time (typical)**
- **2.7V to 5.5V power supply operation**
- **Available packages**
  - **—20-lead TSSOP**

DESCRIPTION

This device combines power-on reset control, battery switch circuit, watchdog timer, supply voltage supervision, secondary voltage supervision, and 64Kbit serial EEPROM in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

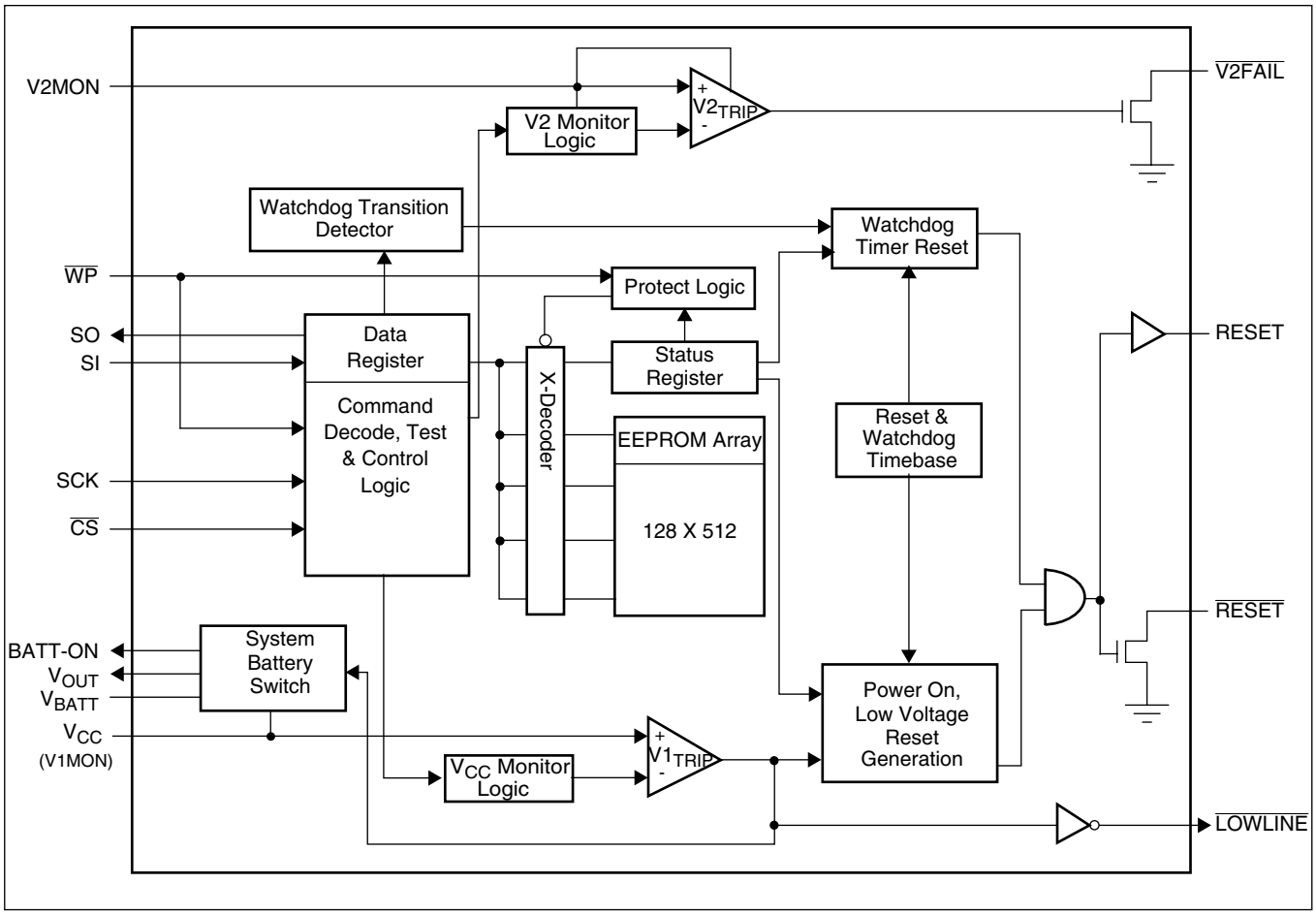
Applying power to the device activates the power on reset circuit which holds $\overline{\text{RESET}}$/RESET active for a period of time. This allows the power supply and oscillator to stabilize before the processor can execute code.

A system battery switch circuit compares V_{CC} (V1MON) with V_{BATT} input and connects V_{OUT} to whichever is higher. This provides voltage to external SRAM or other circuits in the event of main power failure. The X55060 can drive 50mA from V_{CC} and 250µA from V_{BATT}. The device switches to V_{BATT} when V_{CC} drops below the low V_{CC} voltage threshold and V_{BATT}.

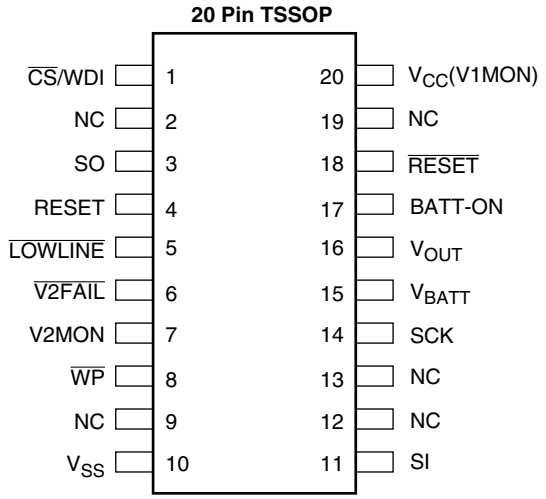
The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{\text{RESET}}$/RESET signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The device's low V_{CC} detection circuitry protects the user's system from low voltage conditions, resetting the system when V_{CC} (V1MON) falls below the minimum V_{CC} trip point ($V1_{TRIP}$). $\overline{\text{RESET}}$/RESET is asserted until V_{CC} returns to proper operating level and stabilizes. A second voltage monitor circuit tracks the unregulated supply or monitors a second power supply voltage to provide a power fail warning. Xicor's unique circuits allow the threshold for either voltage monitor to be reprogrammed to meet special needs or to fine-tune the threshold for applications requiring higher precision.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Function
1	$\overline{CS}$/WDI	**Chip Select Input.** $\overline{CS}$ HIGH, deselects the device and the SO output pin is at a high impedance state. Unless a nonvolatile write cycle is underway, the device will be in the standby power mode. $\overline{CS}$ LOW enables the device, placing it in the active power mode. Prior to the start of any operation after power up, a HIGH to LOW transition on $\overline{CS}$ is required. **Watchdog Input.** A HIGH to LOW transition on the WDI pin restarts the Watchdog timer. The absence of a HIGH to LOW transition within the watchdog time out period results in $\overline{RESET}$/RESET going active.
2	NC	No internal connections
3	SO	**Serial Output.** SO is a push/pull serial data output pin. A read cycle shifts data out on this pin. The falling edge of the serial clock (SCK) clocks the data out.
4	RESET	**Reset Output**. RESET is an active HIGH, CMOS output which is the inverse of the $\overline{RESET}$ output.
5	$\overline{LOWLINE}$	**Early Low V_{CC} Detect**. This CMOS output signal goes LOW when $V_{CC} < V1_{TRIP}$ and returns HIGH when $V_{CC} > V1_{TRIP}$. This pin goes LOW 250ns before $\overline{RESET}$ pin.
6	$\overline{V2FAIL}$	**V2 Voltage Fail Output.** This open drain output goes LOW when V2MON is less than $V2_{TRIP}$ and goes HIGH when V2MON exceeds $V2_{TRIP}$. There is no power up reset delay circuitry on this pin. This circuit works independently from the Low V_{CC} reset and battery switch circuits.
7	V2MON	**V2 Voltage Monitor Input.** When the V2MON input is less than the $V2_{TRIP}$ voltage, $\overline{V2FAIL}$ goes LOW. This input can monitor an unregulated power supply with an external resistor divider or can monitor a second power supply with no external components. Connect V2MON to V_{SS} or V_{CC} when not used.
8	$\overline{WP}$	**Write Protect.** The $\overline{WP}$ pin works in conjunction with a nonvolatile WPEN bit to “lock” the setting of the Watchdog Timer control and the memory write protect bits. This pin is also used as the test mode enable pin where the high voltage will be applied. Thus the layout for the input is different to allow for higher punch thru.
9	NC	No internal connections
10	V_{SS}	Ground

PIN DESCRIPTION (CONTINUED)

Pin	Name	Function
11	SI	**Serial Input.** SI is a serial data input pin. Input all opcodes, byte addresses, and memory data on this pin. The rising edge of the serial clock (SCK) latches the input data. Send all opcodes (Table 1), addresses and data MSB first.
12	NC	No internal connections
13	NC	No internal connections
14	SCK	**Serial Clock.** The Serial Clock controls the serial bus timing for data input and output. The rising edge of SCK latches in the opcode, address, or data bits present on the SI pin. The falling edge of SCK changes the data output on the SO pin.
15	V_{BATT}	**Battery Supply Voltage.** This input provides a backup supply in the event of a failure of the primary V_{CC} voltage. The V_{BATT} voltage typically provides the supply voltage necessary to maintain the contents of SRAM and also powers the internal logic to “stay awake.”
16	V_{OUT}	**Output Voltage.** $V_{OUT} = V_{CC}$ if $V_{CC} > V1_{TRIP}$. IF $V_{CC} < V1_{TRIP}$, then $V_{OUT} = V_{CC}$ if $V_{CC} > V_{BATT} + 0.03$, or $V_{OUT} = V_{BATT}$ if $V_{CC} < V_{BATT} – 0.03$. **Note:** There is hysteresis around $V_{BATT} \pm 0.03V$ point to avoid oscillation at or near the switchover voltage. A capacitance of 0.1µF must be connected to Vout to ensure stability.
17	BATT-ON	**Battery On.** This CMOS output goes HIGH when the V_{OUT} switches to V_{BATT} and goes LOW when V_{OUT} switches to V_{CC}. It is used to drive an external PNP pass transistor when $V_{CC} = V_{OUT}$ and current requirements are greater than 50mA. The purpose of this output is to drive an external transistor to get higher operating currents when the V_{CC} supply is fully functional. In the event of a V_{CC} failure, the battery voltage is applied to the V_{OUT} pin and the external transistor is turned off. In this “backup condition,” the battery only needs to supply enough voltage and current to keep SRAM devices from losing their data-there is no communication at this time.
18	$\overline{\text{RESET}}$	**$\overline{\text{RESET}}$ Output**. This is an active LOW, open drain output which goes active whenever V_{CC} falls below the minimum V_{CC} sense level. Then communication to the device is interrupted. It will remain active until V_{CC} rises above the minimum V_{CC} sense level for 150ms. $\overline{\text{RESET}}$ goes active if the Watchdog Timer is enabled and $\overline{\text{CS}}$ remains either HIGH or LOW longer than the selectable Watchdog time out period. $\overline{\text{RESET}}$ also goes active on power up and remains active for 150ms after the power supply stabilizes.
19	NC	No internal connections
20	V_{CC} (V1MON)	Supply Voltage **V1 Voltage Monitor Input.** When the V1MON input is less than the $V1_{TRIP}$ voltage, $\overline{\text{RESET}}$ and RESET goes ACTIVE.

PRINCIPLES OF OPERATION

Power On Reset

Application of power to the X55060 activates a Power On Reset Circuit. This circuit goes active at about 1V and pulls the $\overline{RESET}$/RESET pin active. This signal prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator. When Vcc exceeds the device $V1_{TRIP}$ value for 150ms (nominal) the circuit releases $\overline{RESET}$/RESET, allowing the processor to begin executing code.

Low V_{CC} (V1MON) Voltage Monitoring

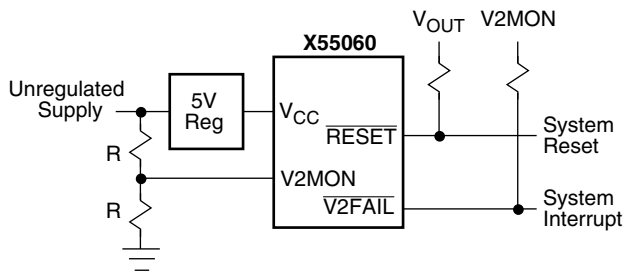
During operation, the X55060 monitors the V_{CC} level and asserts $\overline{RESET}$/RESET if supply voltage falls below a preset minimum $V1_{TRIP}$. During this time the communication to the device is interrupted. The $\overline{RESET}$/RESET signal also prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{RESET}$ signal remains active until the voltage drops below 1V. These also remain active until V_{CC} returns and exceeds $V1_{TRIP}$ for 150ms.

Low V2MON Voltage Monitoring

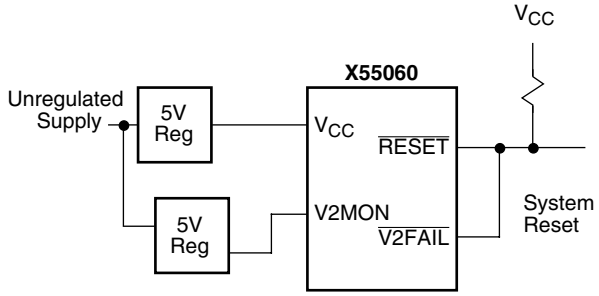
The X55060 also monitors a second voltage level and asserts $\overline{V2FAIL}$ if the voltage falls below a preset minimum $V2_{TRIP}$. The $\overline{V2FAIL}$ signal is either ORed with $\overline{RESET}$ to prevent the microprocessor from operating in a power fail or brownout condition or used to interrupt the microprocessor with notification of an impending power failure. The $\overline{V2FAIL}$ signal remains active until the V2MON drops below 1V (V2MON falling). It also remains active until V2MON returns and exceeds $V2_{TRIP}$ by 0.03V.

The V2MON voltage sensor is completely separate from the operation of the low V_{CC} sense, and is independent of V_{CC} supply.

Figure 1. Two Uses of Dual Voltage Monitoring



Resistors selected so 3V appears on V2MON when Unregulated supply reaches 6V.



Notice: No external components required to monitor two voltages.

Watchdog Timer

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the $\overline{CS}$ pin. The microprocessor must toggle the $\overline{CS}$ pin HIGH to LOW periodically prior to the expiration of the watchdog time out period to prevent a $\overline{RESET}$ and RESET signal going active. The state of two nonvolatile control bits in the Status Register determines the watchdog timer period. The microprocessor can change these watchdog bits by writing to the status register.

The Watchdog Timer oscillator stops when in battery backup mode. It re-starts when V_{CC} returns.

System Battery Switch

As long as V_{CC} exceeds the low voltage detect threshold V_{TRIP}, V_{OUT} is connected to V_{CC} through a 5 Ohm (typical) switch. When the V_{CC} has fallen below $V1_{TRIP}$, then V_{CC} is applied to V_{OUT} if V_{CC} is or equal to or greater than V_{BATT} – 0.03V. When V_{CC} drops to less than V_{BATT} – 0.03V, then V_{OUT} is connected to V_{BATT} through an 80 Ohm (typical) switch. V_{OUT} typically supplies the system static RAM voltage, so the switchover circuit operates to protect the contents of the static RAM during a power failure. Typically, when V_{CC} has failed, the SRAMs go into a lower power state and draw much less current than in their active mode. When V_{CC} returns, V_{OUT} switches back to V_{CC} when V_{CC} exceeds V_{BATT} + 0.03V. There is a 60mV hysteresis around this battery switch threshold to prevent oscillations between supplies.

While V_{CC} is connected to V_{OUT} the BATT-ON pin is pulled LOW. The signal can drive an external PNP transistor to provide additional current to the external circuits during normal operation.

V_{CC} (V1MON), V2MON Threshold Reset Procedure

The X55060 is shipped with standard V_{CC} (V1MON) and V2MON threshold ($V1_{TRIP}$, $V2_{TRIP}$) voltages. These values will not change over normal operating and storage conditions. However, in applications where the standard thresholds are not exactly right, or if higher precision is needed in the threshold value, the X55060 trip points may be adjusted. The procedure is described below, and uses the application of a high voltage control signal.

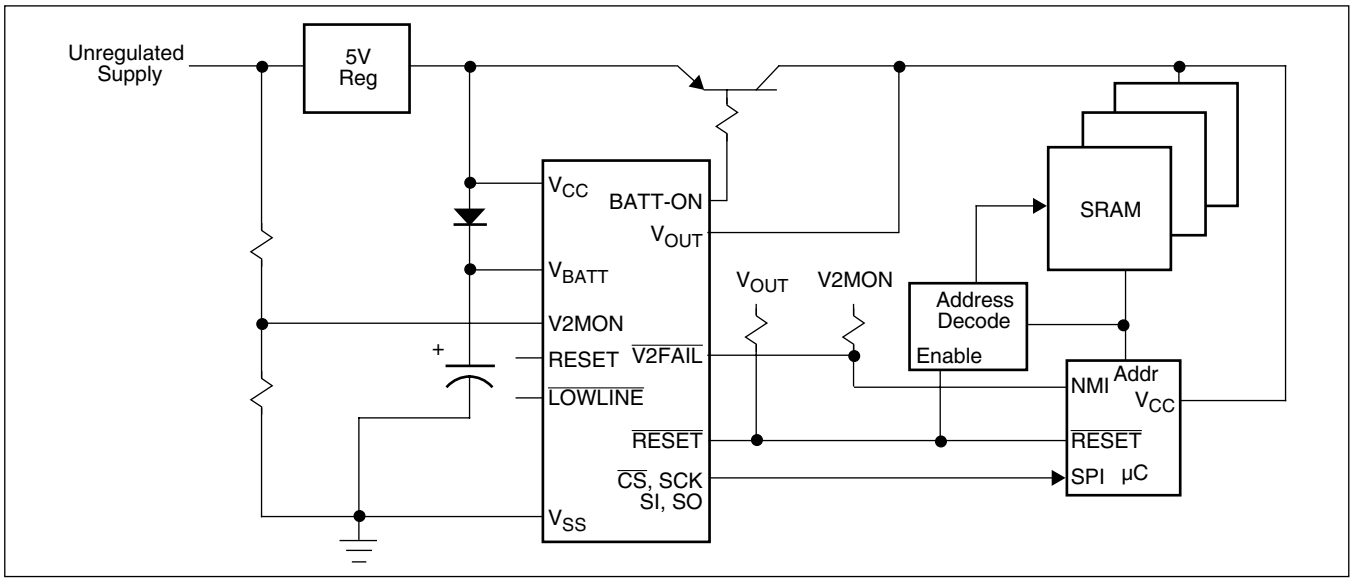
Setting the V_{TRIP} Voltage

This procedure is used to set the $V1_{TRIP}$ or $V2_{TRIP}$ to a lower or higher voltage value. It is necessary to reset the trip point before setting the new value.

To set the new voltage, apply the desired V_{TRIP} threshold voltage to the V_{CC} pin or the $V2_{TRIP}$ voltage to the V2MON pin, then tie the $\overline{WP}$ pin to the programming voltage V_P. Then, send the WREN command and write to address 01h or to address 0Bh to program $V1_{TRIP}$ or $V2_{TRIP}$, respectively (followed by data byte 00h). The $\overline{CS}$ going high after a valid write operation initiates the programming sequence. Bring $\overline{WP}$ LOW to complete the operation.

Note: This operation will not alter the contents of the EEPROM.

Figure 2. Example System Connection



Resetting the V_{TRIP} Voltage

This procedure is used to set the $V1_{TRIP}$ or the $V2_{TRIP}$ to a “native” voltage level. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} must be 4.0V, then the V_{TRIP} must be reset. When the threshold is reset, the new level is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the new $V1_{TRIP}$ or $V2_{TRIP}$ voltage, apply greater than 3V to V_{CC} or V2MON pin, respectively, and tie the $\overline{WP}$ pin to the programming voltage V_P. Then send the WREN command and write to address 03h or 0Dh to reset the $V1_{TRIP}$ or $V2_{TRIP}$ respectively (followed by data byte 00h). The $\overline{CS}$ going LOW to HIGH after a valid write operation initiates the programming sequence. Bring $\overline{WP}$ LOW to complete the operation.

Note: This operation does not change the contents of the EEPROM array.

Figure 3. Set V_{TRIP} Level Sequence (V_{CC} = desired V_{TRIP})

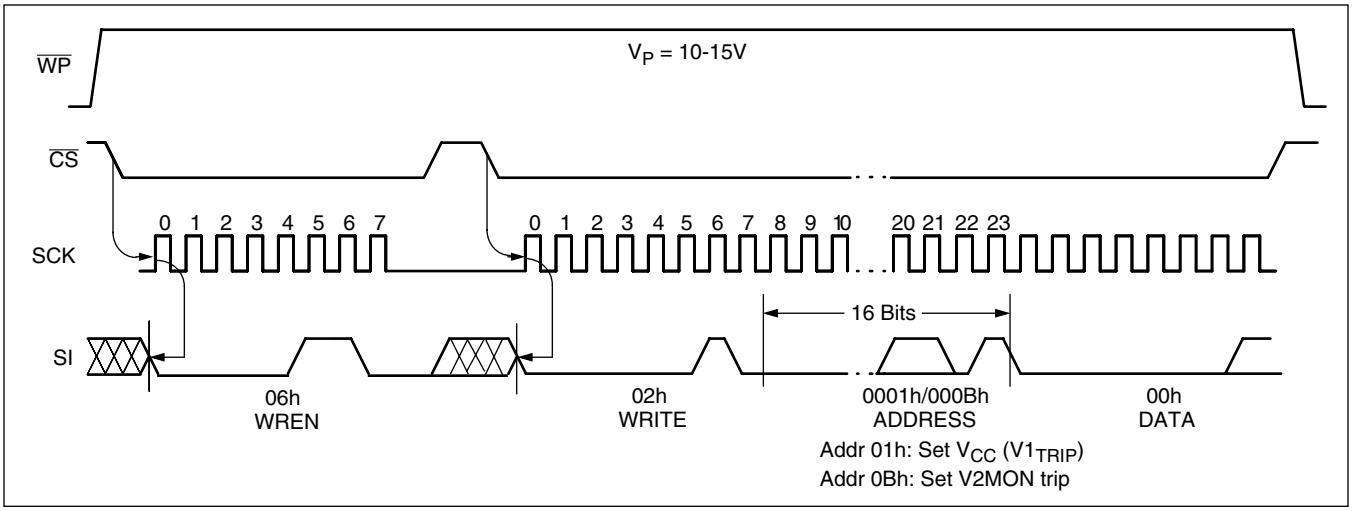


Figure 4. Reset V_{TRIP} Level Sequence (V_{CC} > 3V. $\overline{WP}$ = 10-15V)

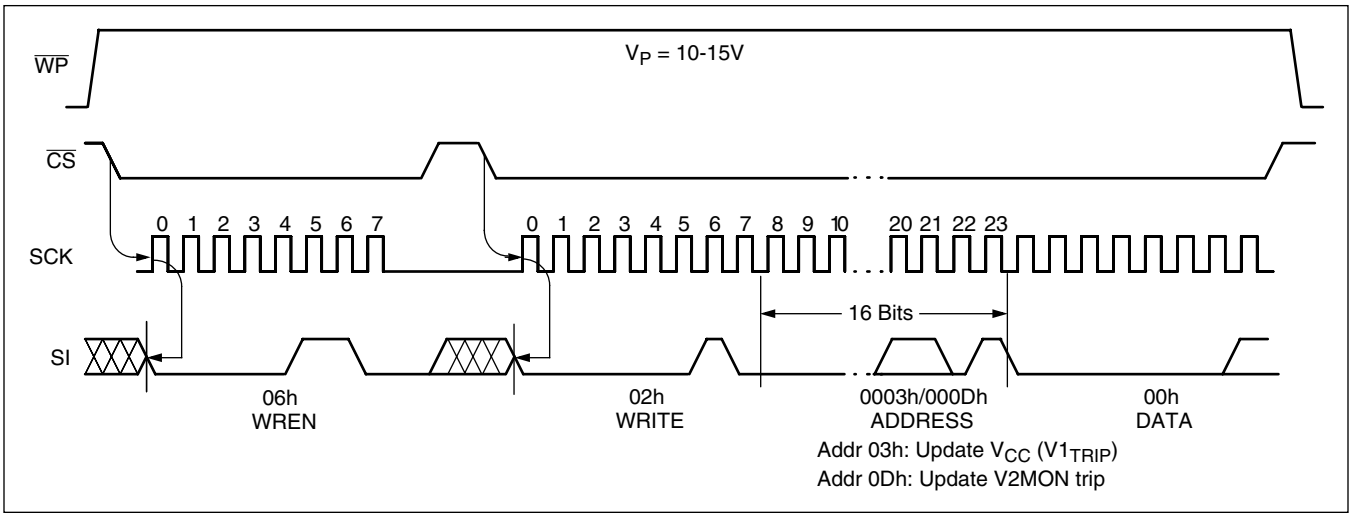


Figure 5. Sample V_{TRIP} Reset Circuit

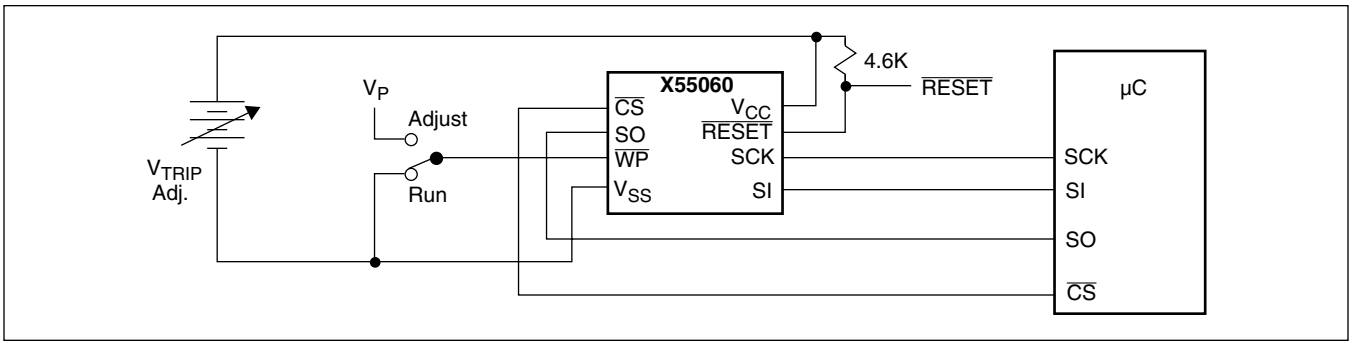
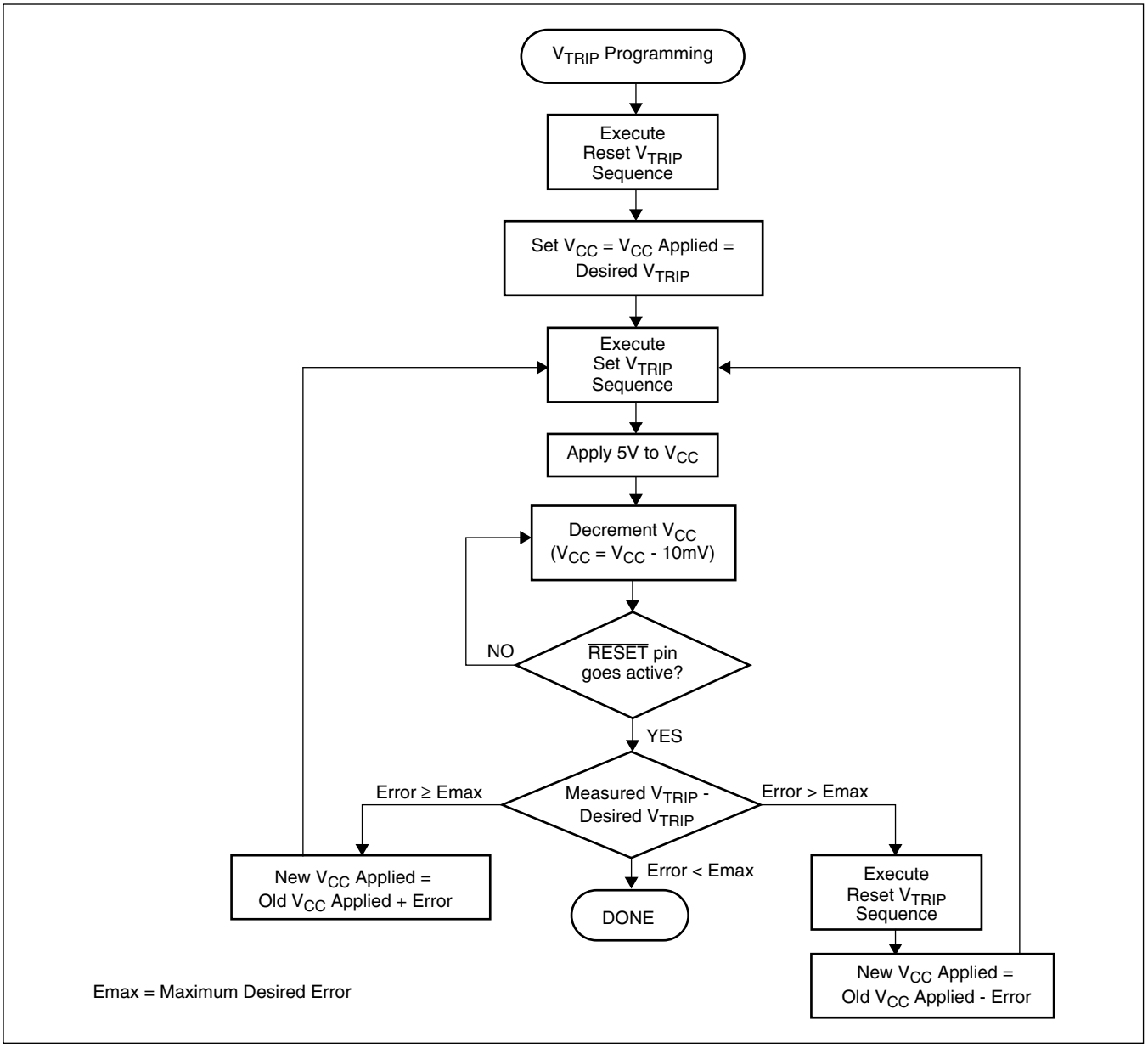


Figure 6. V_{TRIP} Programming Sequence Flow Chart



SPI SERIAL MEMORY

The memory portion of the device is a CMOS Serial EEPROM array. The array is internally organized as x 8. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 1,000,000 cycles and a minimum data retention of 100 years.

The device is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families. It contains an 8-bit instruction register that is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{CS}$ must be LOW during the entire operation.

All instructions (Table 1), addresses and data are transferred MSB first. Data input on the SI line is latched on the first rising edge of SCK after $\overline{CS}$ goes LOW. Data is output on the SO line by the falling edge of SCK. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

Write Enable Latch

The device contains a Write Enable Latch. This latch must be SET before a Write Operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 3). This latch is automatically reset upon a power-up condition and after the completion of a valid Write Cycle.

Status Register

The RDSR instruction provides access to the Status Register. The Status Register may be read at any time, even during a Write Cycle. The Status Register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	WD1	WD0	0	0	0	WEL	WIP

The Write-In-Progress (WIP) bit is a volatile, read only bit and indicates whether the device is busy with an internal nonvolatile write operation. The WIP bit is read using the RDSR instruction. When set to a "1", a nonvolatile write operation is in progress. When set to a "0", no write is in progress.

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch
RSDR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (Watchdog, Block Lock, WPEN)
READ	0000 0011	Read Data from Memory Array Beginning at Selected Address
WRITE	0000 0010	Write Data to Memory Array Beginning at Selected Address

Notes: *Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

The Write Enable Latch (WEL) bit indicates the Status of the Write Enable Latch. When WEL=1, the latch is set HIGH and when WEL=0 the latch is reset LOW. The WEL bit is a volatile, read only bit. It can be set by the WREN instruction and can be reset by the WRDS instruction.

The Watchdog Timer bits, WD0 and WD1, select the Watchdog Time Out Period. These nonvolatile bits are programmed with the WRSR instruction.

Status Register Bits		Watchdog Time Out (Typical)
WD1	WD0	
0	0	800 milliseconds
0	1	400 milliseconds
1	0	150 milliseconds
1	1	disabled

The nonvolatile WPEN bit is programmed using the WRSR instruction. This bit works in conjunction with the $\overline{WP}$ pin to provide an In-Circuit Programmable ROM function (Table 2). $\overline{WP}$ is LOW and WPEN bit programmed HIGH disables all Status Register Write Operations.

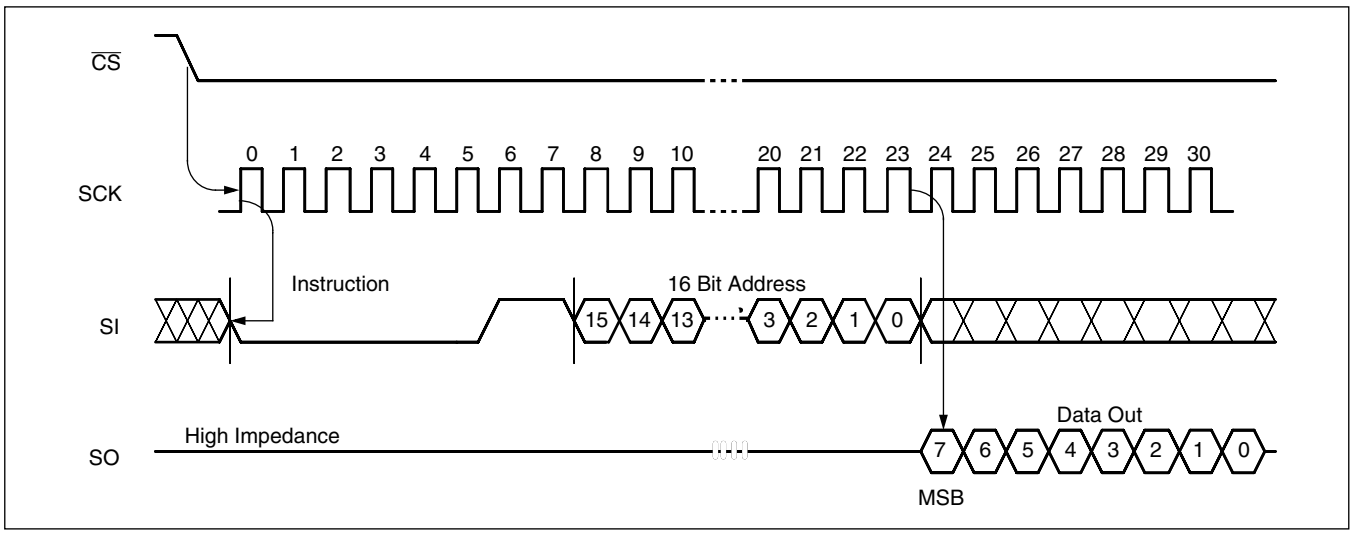
In Circuit Programmable ROM Mode

This mechanism protects the Watchdog bits from inadvertent corruption.

In the locked state (Programmable ROM Mode) the $\overline{WP}$ pin is LOW and the nonvolatile bit WPEN is “1”. This mode disables nonvolatile writes to the device’s Status Register.

Setting the $\overline{WP}$ pin LOW while WPEN is a “1” while an internal write cycle to the Status Register is in progress will not stop this write operation, but the operation disables subsequent write attempts to the Status Register.

Figure 7. Read EEPROM Array Sequence



When $\overline{WP}$ is HIGH, all functions, including nonvolatile writes to the Status Register operate normally. Setting the WPEN bit in the Status Register to “0” blocks the $\overline{WP}$ pin function, allowing writes to the Status Register when $\overline{WP}$ is HIGH or LOW. Setting the WPEN bit to “1” while the $\overline{WP}$ pin is LOW activates the Programmable ROM mode, thus requiring a change in the $\overline{WP}$ pin prior to subsequent Status Register changes. This allows manufacturing to install the device in a system with $\overline{WP}$ pin grounded and still be able to program the Status Register. Manufacturing can then load Configuration data, manufacturing time and other parameters into the EEPROM, then set the portion of memory to be protected by setting the block lock bits, and finally set the “OTP mode” by setting the WPEN bit. Data changes now require a hardware change.

Read Sequence

When reading from the EEPROM memory array, $\overline{CS}$ is first pulled low to select the device. The 8-bit READ instruction is transmitted to the device, followed by the 16-bit address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is

automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high. Refer to the Read EEPROM Array Sequence (Figure 1).

To read the Status Register, the $\overline{CS}$ line is first pulled low to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the Status Register are shifted out on the SO line. Refer to the Read Status Register Sequence (Figure 2).

Write Sequence

Prior to any attempt to write data into the device, the "Write Enable" Latch (WEL) must first be set by issuing the WREN instruction (Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the device. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the Write Operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the Write Operation will be ignored.

To write data to the EEPROM memory array, the user then issues the WRITE instruction followed by the 16 bit address and then the data to be written. Any unused address bits are specified to be "0's". The WRITE operation minimally takes 32 clocks. $\overline{CS}$ must go low and remain low for the duration of the operation. If the address counter reaches the end of a page and the clock continues, the counter will roll back to the first address of the page and overwrite any data that may have been previously written.

For the Page Write Operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed (Figure 4).

To write to the Status Register, the WRSR instruction is followed by the data to be written (Figure 5). Data bits 0 and 1 must be "0".

While the write is in progress following a Status Register or EEPROM Sequence, the Status Register may be read to check the WIP bit. During this time the WIP bit will be high.

OPERATIONAL NOTES

The device powers-up in the following state:

– The device is in the low power standby state.

– A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.

– SO pin is high impedance.

– The Write Enable Latch is reset.

– Reset Signal is active for t_{PURST}.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

– A WREN instruction must be issued to set the Write Enable Latch.

– $\overline{CS}$ must come HIGH at the proper clock count in order to start a nonvolatile write cycle.

Figure 8. Read Status Register Sequence

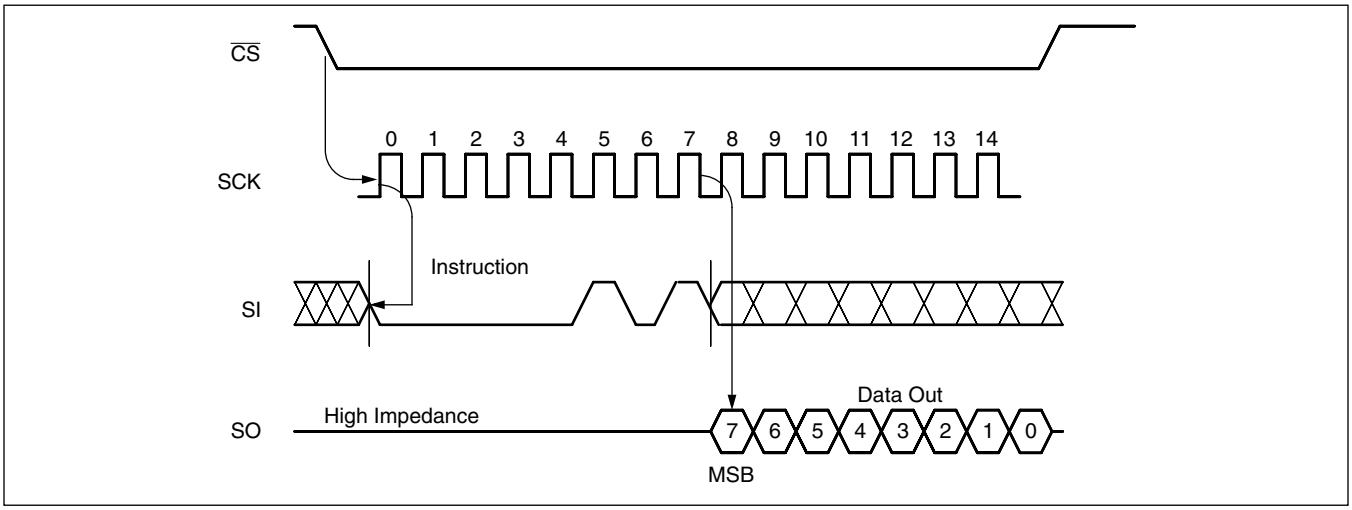


Figure 9. Write Enable Latch Sequence

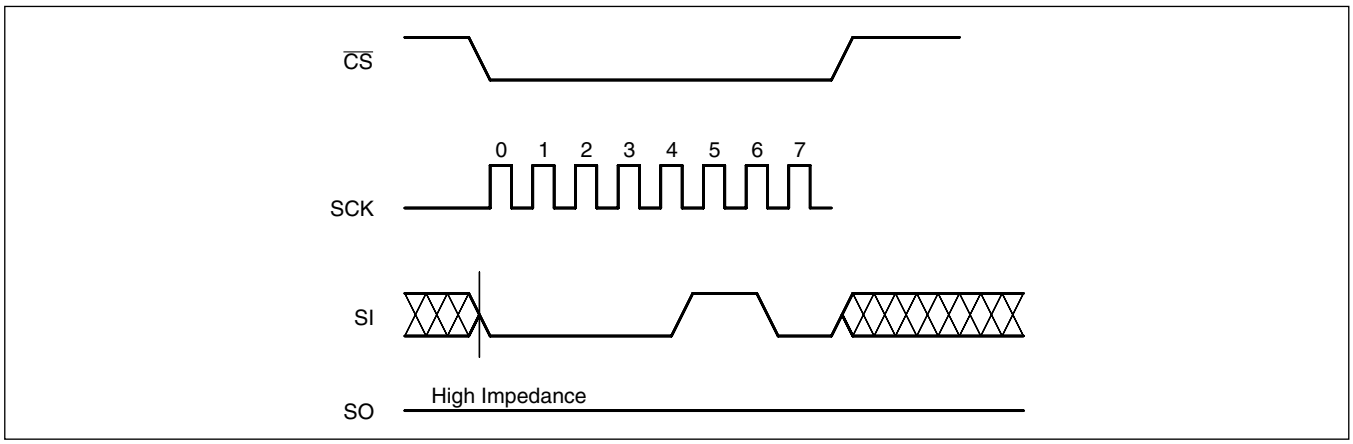


Figure 10. Write Sequence

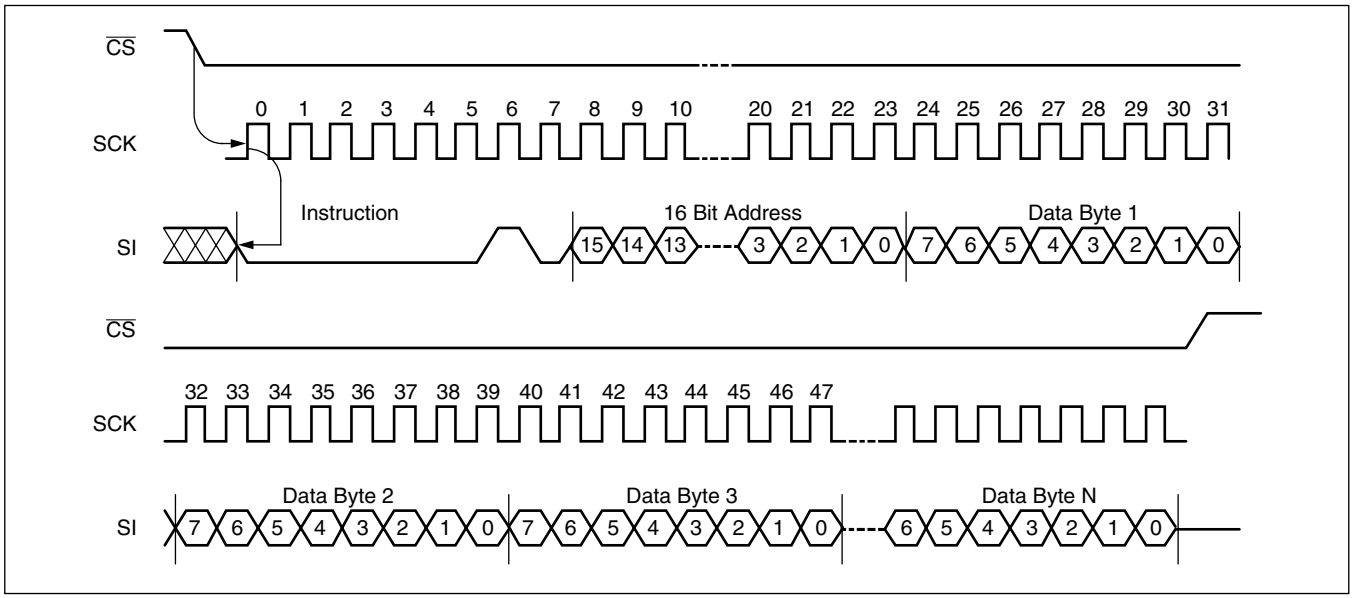
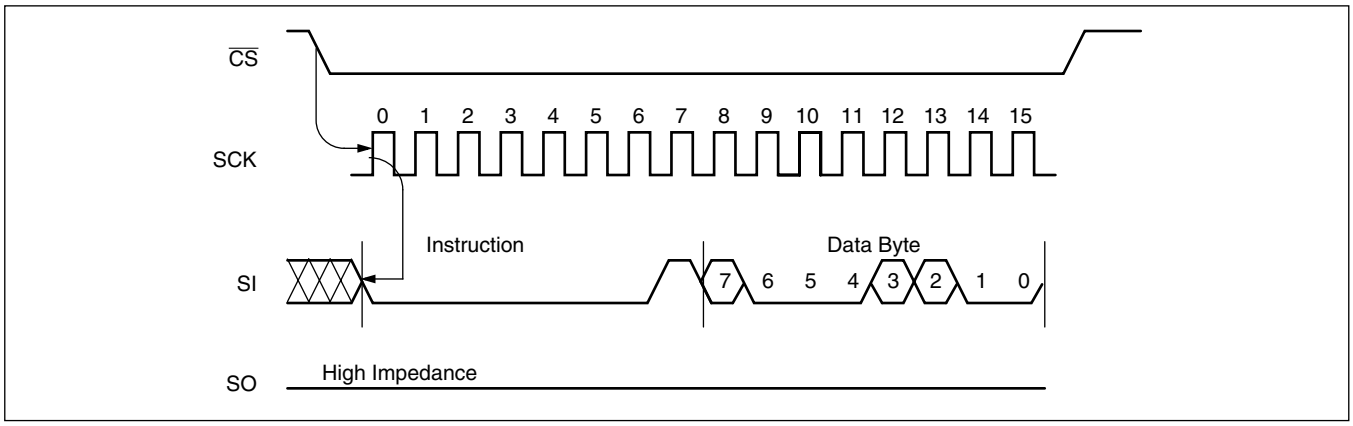
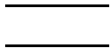
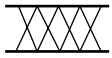
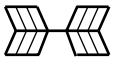


Figure 11. Status Register Write Sequence



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS

Temperature under bias .....–65°C to +135°C
Storage temperature .....–65°C to +150°C
Voltage on any pin with
respect to V_{SS}.....–1.0V to +7V
D.C. output current 5mA
Lead temperature (soldering, 10 seconds).....300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C

Device Option	Supply Voltage
-2.7A	2.7V-5.5V
Blank	4.5V-5.5V

D.C. OPERATING CHARACTERISTICS

(Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}[1]	V_{CC} Supply Current (Active) (Excludes I_{OUT}) Read Memory array (Excludes I_{OUT}) Write nonvolatile Memory			 1.5 3.0	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 10MHz, SO, V_{OUT}, RESET, $\overline{\text{LOWLINE}}$ = Open
I_{CC2}[2]	V_{CC} Supply Current (Passive) (Excludes I_{OUT}) WDT on, 5V (Excludes I_{OUT}) WDT on, 2.7V (Excludes I_{OUT}) WDT off, 5V		 50.0 40.0 30.0	 90.0 60.0 50.0	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{OUT}, RESET, $\overline{\text{LOWLINE}}$ = Open
I_{CC3}[1]	V_{CC} Current (Battery Backup Mode) (Excludes I_{OUT})			1	µA	V_{CC} = 0V, V_{BATT} = 2.8V, V_{OUT}, $\overline{\text{RESET}}$ = Open
I_{BATT1}[3]	V_{BATT} Current (Excludes I_{OUT})			1	µA	V_{OUT} = V_{CC}
I_{BATT2}	V_{BATT} Current (Excludes I_{OUT}) (Battery Backup Mode)		0.4	1.0	µA	V_{OUT} = V_{BATT}, V_{BATT} = 2.8V V_{OUT}, $\overline{\text{RESET}}$ = Open
V_{OUT1}	Output Voltage (V_{CC} > V_{BATT} + 0.03V or V_{CC} > V_{TRIP}	V_{CC} – 0.05 V_{CC} – 0.5		V_{CC} – 0.02 V_{CC} – 0.2	V V	I_{OUT} = -5mA I_{OUT} = -50mA
V_{OUT2}	Output Voltage (V_{CC} < V_{BATT} – 0.03V and V_{CC} < V_{TRIP}) {Battery Backup}	V_{BATT} – 0.2			V V	I_{OUT} = -250µA
V_{OLB}	Output (BATT-ON) LOW Voltage			0.4	V	I_{OL} = 3.0mA (5V) I_{OL} = 1.0mA (3V)
V_{OHB}	Output (BATT-ON) HIGH Voltage	V_{OUT} – 0.8			V	I_{OH} = -0.4mA (3V)
V_{BSH}	Battery Switch Hysteresis (V_{CC} < V_{TRIP})			50 -50	mV mV	Power Up Power Down

D.C. OPERATING CHARACTERISTICS (CONTINUED)
(Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
RESET/$\overline{\text{RESET}}$/$\overline{\text{LOWLINE}}$						
V_{TRIP}	V_{CC} Reset Trip Point Voltage	4.5	4.62	4.75	V	
V_{LVRH}	Low V_{CC} RESET Hysteresis			60	mV	
V_{OLR}	Output ($\overline{\text{RESET}}$, RESET, $\overline{\text{LOWLINE}}$) LOW Voltage			0.4	V	I_{OL} = 3.0mA (5V) I_{OL} = 1.0mA (3V)
V_{OHR}	Output (RESET, $\overline{\text{LOWLINE}}$) HIGH Voltage	V_{OUT} – 0.8			V	I_{OL} = -0.4mA (5V)
Second Supply Monitor						
I_{V2}	V2MON Current		15	30	µA	
$V2_{TRIP}$	V2MON Reset Trip Point Voltage	2.85	2.95	3.05	V	
V_{V2H}	V2MON Hysteresis			60	mV	
V_{OLx}	Output ($\overline{\text{V2FAIL}}$) LOW Voltage			0.4	V	I_{OL} = 3.0mA (5V) I_{OL} = 1.0mA (3V)
SPI Interface						
V_{ILx}(4)	Input ($\overline{\text{CS}}$, SI, SCK, $\overline{\text{WP}}$) LOW Voltage	-0.5		V_{CC} x 0.3	V	
V_{IHx}(4)	Input ($\overline{\text{CS}}$, SI, SCK, $\overline{\text{WP}}$) HIGH Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
I_{LIx}	Input Leakage Current ($\overline{\text{CS}}$, SI, SCK, $\overline{\text{WP}}$)			±10	µA	
V_{OLS}	Output (SO) LOW Voltage			0.4	V	I_{OL} = 3.0mA (5V) I_{OL} = 1.0mA (3V)
V_{OHS}	Output (SO) HIGH Voltage	V_{OUT} – 0.8			V	I_{OH} = -1.0mA (5V)

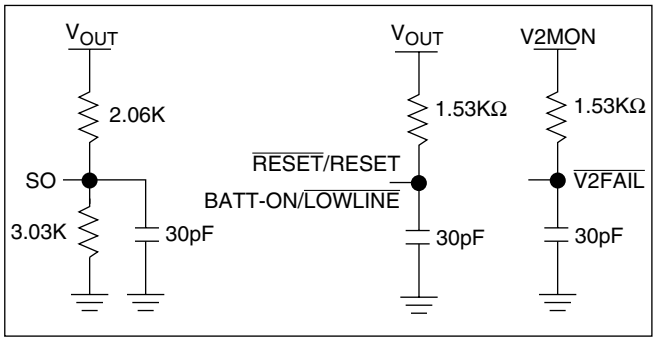
Notes: (1) The device enters the Active state after any start, and remains active until 9 clock cycles later if the Device Select Bits in the Slave Address Byte are incorrect; 200ns after a stop ending a read operation; or t_{WC} after a stop ending a write operation.
(2) The device goes into Standby: 200ns after any Stop, except those that initiate a high voltage write cycle; t_{WC} after a stop that initiates a high voltage cycle; or 9 clock cycles after any start that is not followed by the correct Device Select Bits in the Slave Address Byte.
(3) Negative number indicate charging current, Positive numbers indicate discharge current.
(4) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Unit	Conditions
C_{OUT}(1)	Output Capacitance (SO, $\overline{\text{RESET}}$, $\overline{\text{V2FAIL}}$, RESET, $\overline{\text{LOWLINE}}$, BATT-ON)	8	pF	V_{OUT} = 0V
C_{IN}(1)	Input Capacitance (SCK, SI, $\overline{\text{CS}}$, $\overline{\text{WP}}$)	6	pF	V_{IN} = 0V

Notes: (1) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

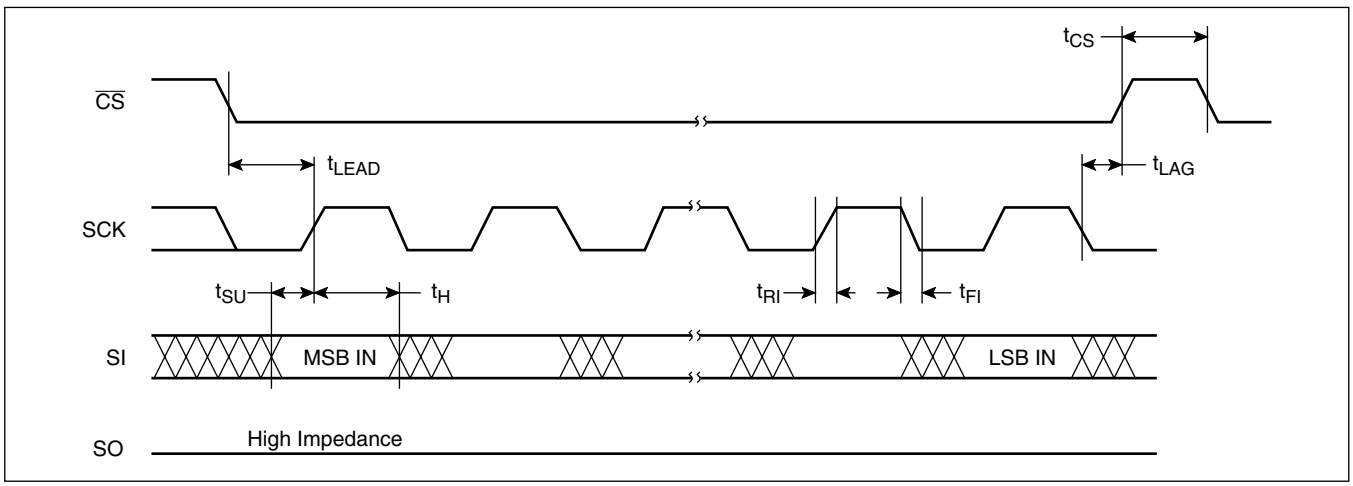
Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x0.5

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Serial Input Timing

Symbol	Parameter	2.7-5.5V		Unit
		Min.	Max.	
f_{SCK}	Clock Frequency	0	10	MHz
t_{CYC}	Cycle Time	100		ns
t_{LEAD}	$\overline{CS}$ Lead Time	50		ns
t_{LAG}	$\overline{CS}$ Lag Time	200		ns
t_{WH}	Clock HIGH Time	40		ns
t_{WL}	Clock LOW Time	40		ns
t_{SU}	Data Setup Time	10		ns
t_H	Data Hold Time	10		ns
t_{RI}(3)	Input Rise Time		20	ns
t_{FI}(3)	Input Fall Time		20	ns
t_{CS}	$\overline{CS}$ Deselect Time	50		ns
t_{WC}(4)	Write Cycle Time		10	ms

Serial Input Timing

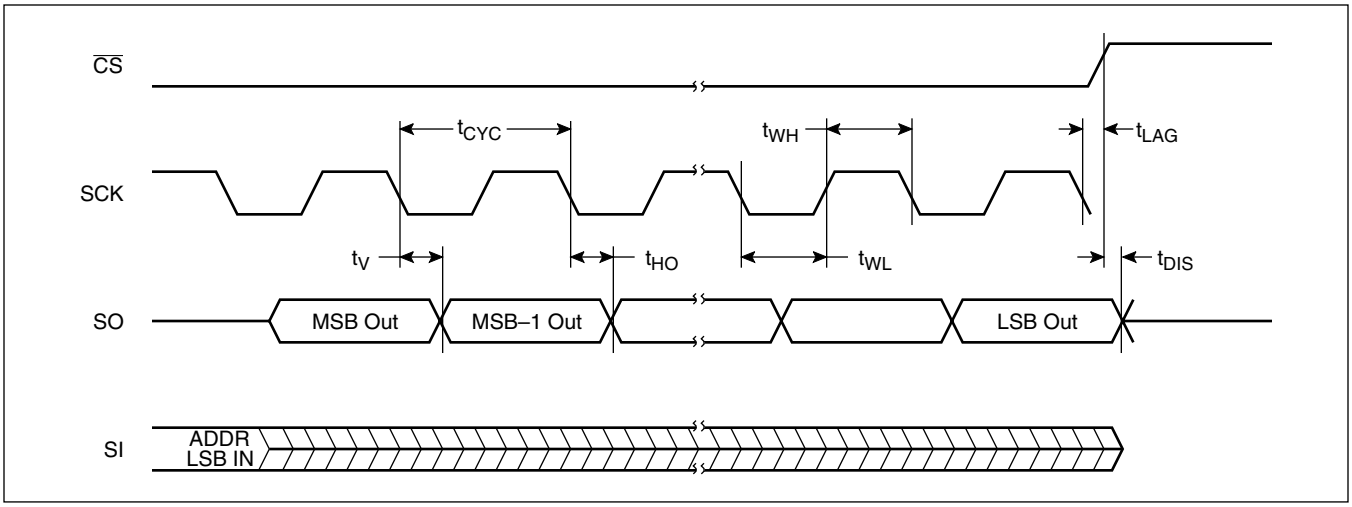


Serial Output Timing

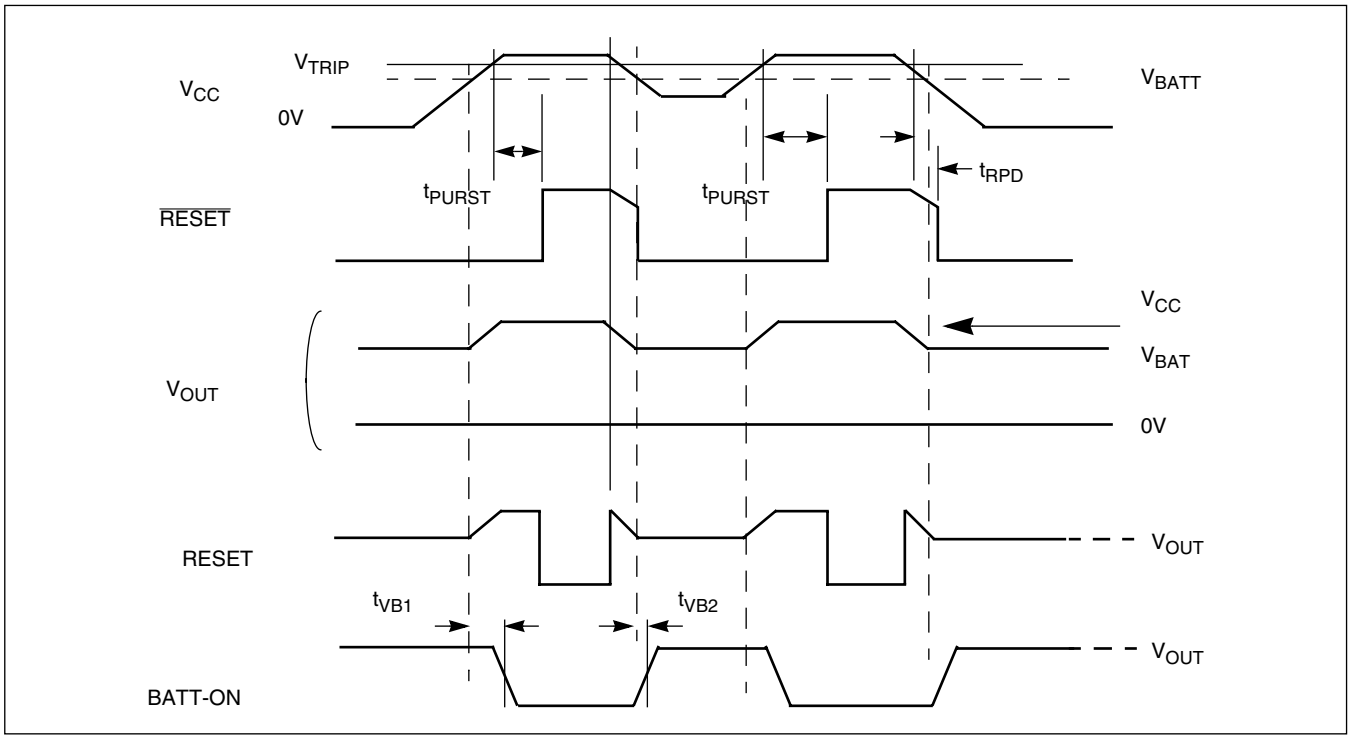
Symbol	Parameter	2.7-5.5V		Unit
		Min.	Max.	
f_{SCK}	Clock Frequency	0	10	MHz
t_{DIS}	Output Disable Time		50	ns
t_V	Output Valid from Clock Low		40	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(3)	Output Rise Time		25	ns
t_{FO}(3)	Output Fall Time		25	ns

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

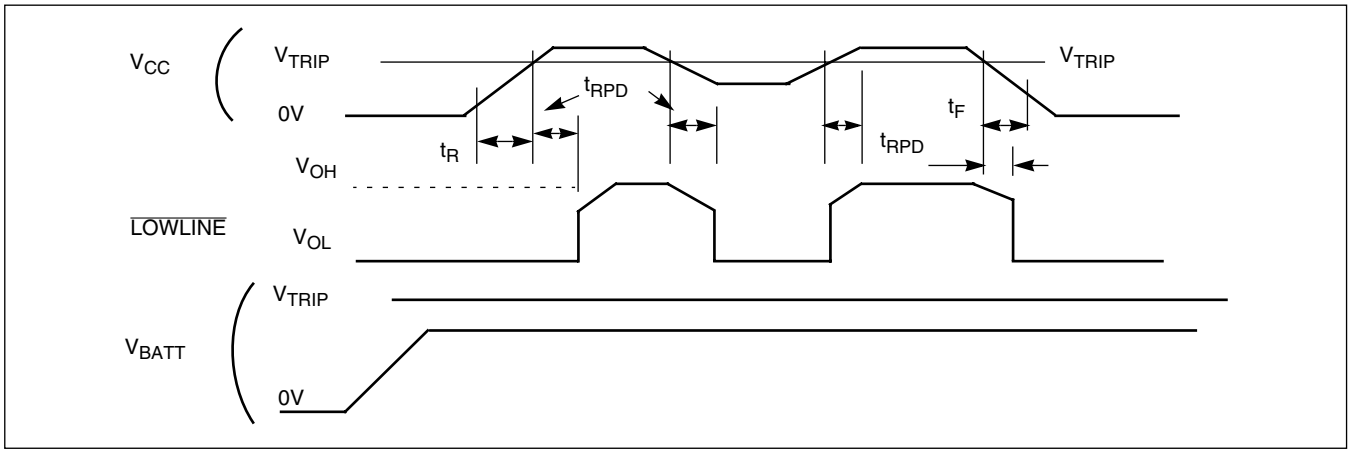
Serial Output Timing



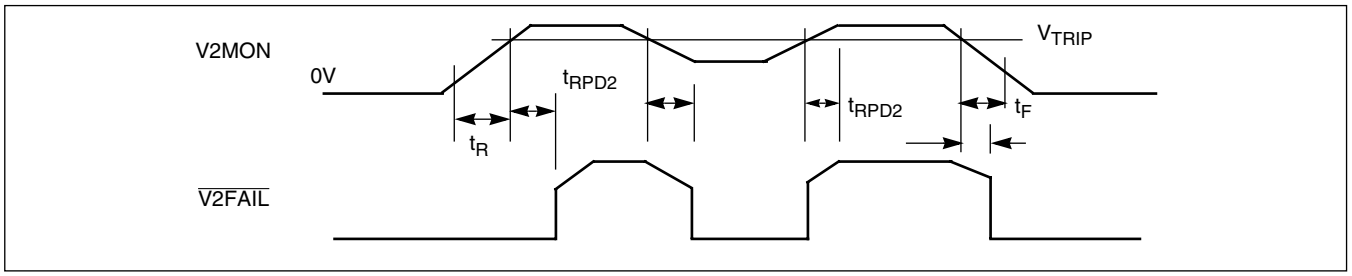
Power-Up and Power-Down Timing



V_{CC} to $\overline{\text{LOWLINE}}$ Timings



V2MON to $\overline{\text{V2FAIL}}$ Timings

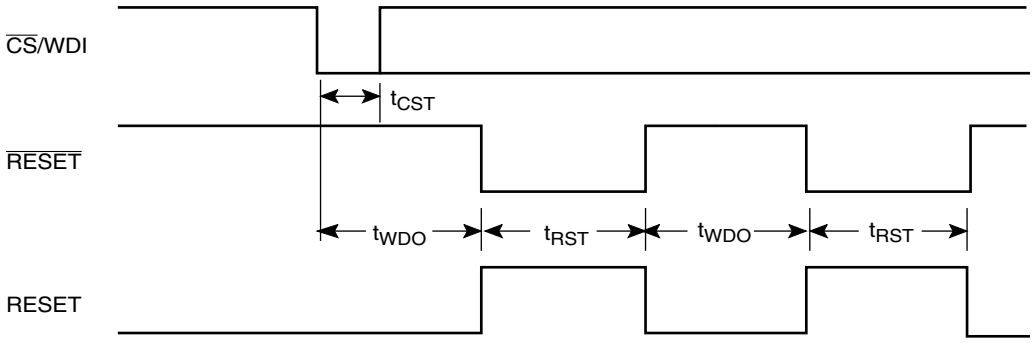


$\overline{\text{RESET}}$ Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PURST}	RESET/$\overline{\text{RESET}}$ Time Out Period	75	150	250	ms
t_{RPD}(5)	V_{TRIP} $\overline{\text{RESET}}$/RESET (Power down only) V_{TRIP} to $\overline{\text{LOWLINE}}$		10	20	µs
t_{RPD2}(5)	V_{TRIP} to $\overline{\text{V2FAIL}}$		10	20	µs
t_{LR}	$\overline{\text{LOWLINE}}$ to RESET/$\overline{\text{RESET}}$ delay (Power down only)	100	250	800	ns
t_F(6)	V_{CC}/V2MON Fall Time	1000			µs
t_R(6)	V_{CC}/V2MON Rise Time	1000			µs
V_{RVALID}	Reset Valid V_{CC}	1			V
t_{VB1}	V_{BATT} + 0.03 v to BATT-ON (logical 0)			20	µs
t_{VB2}	V_{BATT} – 0.03 v to BATT-ON (logical 1)			20	µs

Notes: (5) This parameter is not 100% tested.
(6) This measurement is from 10% to 90% of the supply voltage.

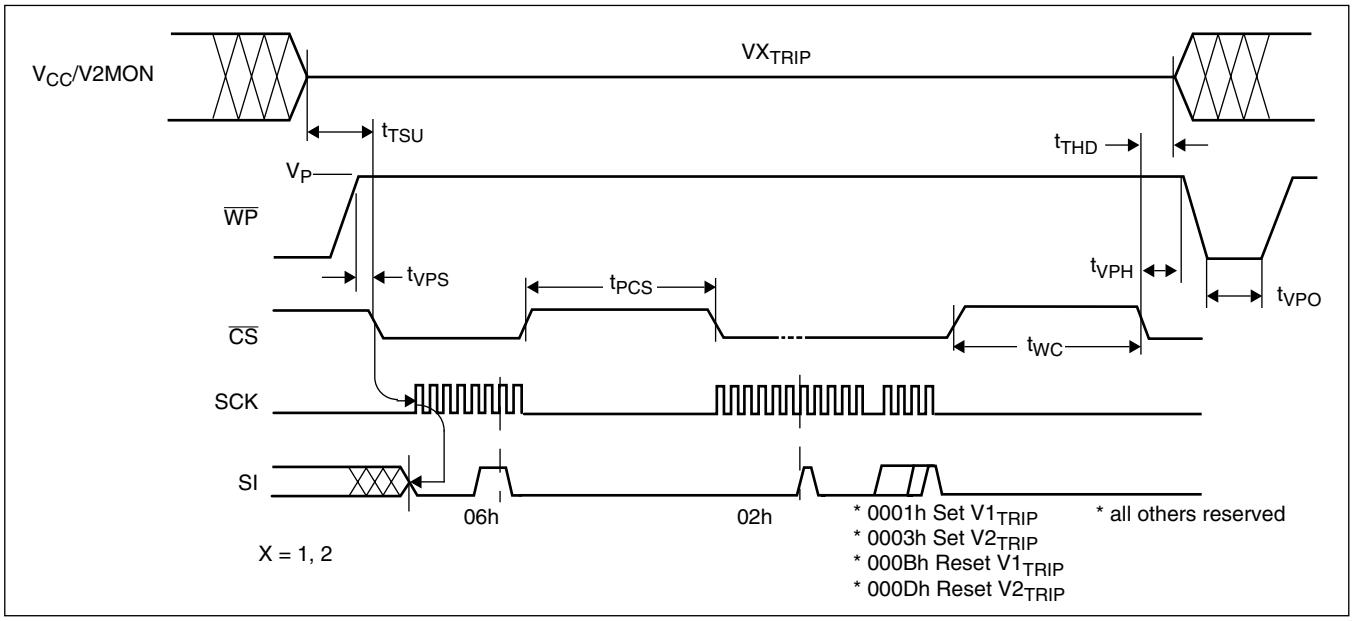
$\overline{\text{CS}}$/WDI vs. $\overline{\text{RESET}}$/RESET Timing



$\overline{\text{RESET}}$/RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WDO}	Watchdog Time Out Period, WD1 = 1, WD0 = 0 WD1 = 0, WD0 = 1 WD1 = 0, WD0 = 0	 75 200 500	 150 400 800	 250 600 1200	 ms ms ms
t_{CST}	$\overline{\text{CS}}$ Pulse Width to Reset the Watchdog	400			ns
t_{RST}	Reset Time Out	75	150	250	ms

V_{TRIP} Set/Reset Conditions



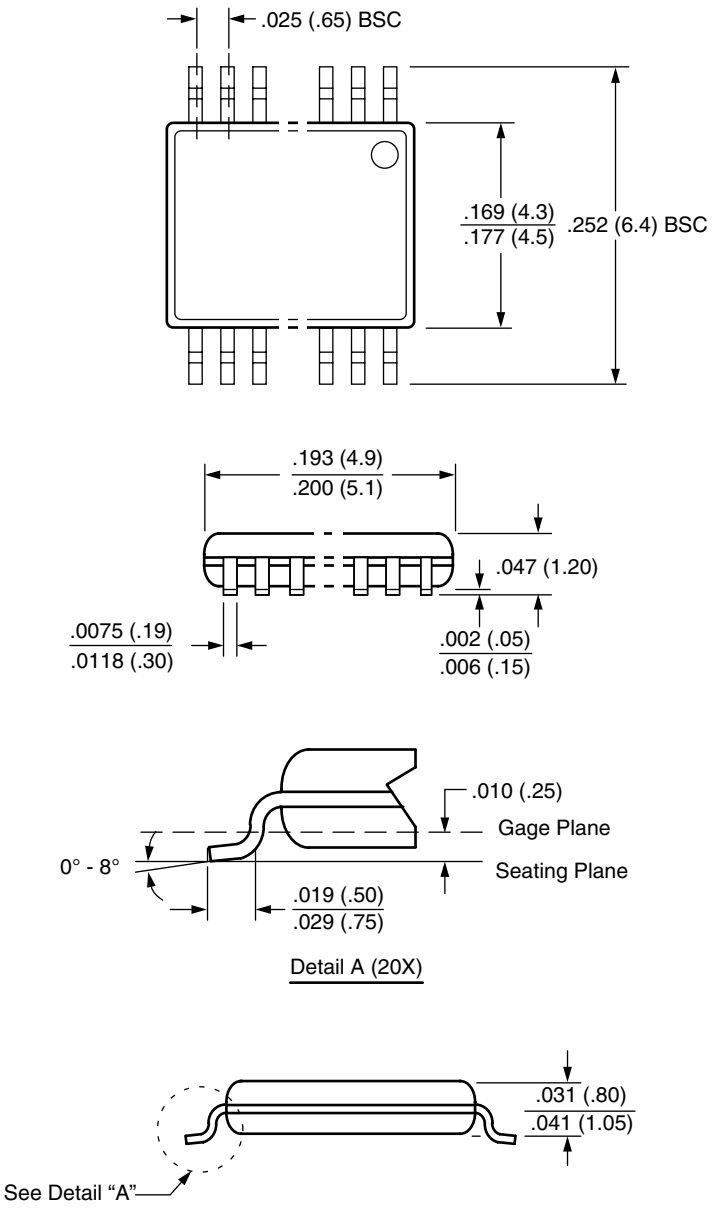
$V1_{TRIP}$, $V2_{TRIP}$ Programming Specifications V_{CC} = 2.7-5.5V; Temperature = 25°C

Parameter	Description	Min.	Max.	Unit
t_{VPS}	$\overline{WP}$ V_{TRIP} Program Voltage Setup time	10		µs
t_{VPH}	$\overline{WP}$ V_{TRIP} Program Voltage Hold time	10		µs
t_{TSU}	V_{TRIP} Level Setup time	10		µs
t_{THD}	V_{TRIP} Level Hold (stable) time	10		ms
t_{WC}	V_{TRIP} Write Cycle Time		10	ms
t_{VPO}	$\overline{WP}$ V_{TRIP} Program Voltage Off time before next cycle	1		ms
V_P	Programming Voltage	10	15	V
V_{TRAN}	V_{TRIP} Programed Voltage Range	2.5	5.0	V
V_{ta1}	Initial V_{TRIP} Program Voltage accuracy (V_{CC} applied—V_{TRIP}) (Programmed at 25°C.)	-0.2	+0.4	V
V_{ta2}	Subsequent V_{TRIP} Program Voltage accuracy [(V_{CC} applied—V_{ta1})—V_{TRIP}) (Programmed at 25°C.)	-25	+25	mV
V_{tr}	V_{TRIP} Program Voltage repeatability (Successive program operations.) (Programmed at 25°C.)	-25	+25	mV
V_{tv}	V_{TRIP} Program variation after programming (0–75°C). (Programmed at 25°C.)	-25	+25	mV

V_{TRIP} Programming parameters are periodically sampled and are not 100% tested.

PACKAGING INFORMATION

20-Lead Plastic, TSSOP, Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information

V_{CC} Range	$V1_{TRIP}$ Range	$V2_{TRIP}$ Range	Package	Operating Temperature Range	Part Number
4.5–5.5V	4.5–4.75V	2.55–2.7V	20L TSSOP	0°C–70°C	X55060V20-4.5A
				-40°C–85°C	X55060V20I-4.5A
4.5–5.5V	4.5–4.75V	2.85–3.0V	20L TSSOP	0°C–70°C	X55060V20
				-40°C–85°C	X55060V20I
2.7–5.5V	2.85–3.0V	4.5–4.75V	20L TSSOP	0°C–70°C	X55060V20-2.7A
				-40°C–85°C	X55060V20I-2.7A
2.7–5.5V	2.55–2.75V	4.5–4.75V	20L TSSOP	0°C–70°C	X55060V20-2.7
				-40°C–85°C	X55060V20I-2.7

Part Mark Information