WM8045

Advance Information
August 1997 Rev.2.1

Twisted Pair Transceiver for 100BASE-TX, TP-FDDI and ATM-155Mb/s

Description

WM8045 is a high performance monolithic transceiver circuit that operates between a physical layer controller and the analogue signals present on twisted pair cable (UTP-5 or STP). WM8045 operates with a 2 or 3 level data stream at rates of up to 160 Mb/s.

WM8045 receiver's adaptive equaliser will accurately compensate for cable losses in cable up to 100 metres in length. The equaliser uses external components allowing WM8045's operation over a range of user selectable data rates. Data dependent DC shifts in the incoming data stream are corrected by the baseline wander loop to minimise errors in the receipt of a transmitted frame. WM8045's transmitter input and receiver output signals are in PECL NRZI format. WM8045 can also convert, transmit and receive these signals in differential MLT3 format under control of the ENCSEL pin. Transmitter amplitude is controlled by a single external resistor.

The device has a high degree of flexibility, allowing it to be used in various standard applications and to enable performance tailoring for customer specific requirements. The device is fully compliant with ANSI X3T12 TP-PMD for TP-FDDI, IEEE 802.3u for Fast Ethernet 100Base-TX & ATM-UNI-PMD STS3c for 155 Mb/s specifications.

Features

- **Compliance with PMD standards IEEE, ANSI, ATM**
- **Baseline wander correction compliant**
- **Programmable adaptive equaliser**
- **Programmable MLT3/NRZI operation**
- **Programmable TX amplitude**
- **Supports 100m of Unshielded Twisted Pair category 5 (UTP-5) or Shielded Twisted Pair (STP) cable**
- **Independent RX and TX**

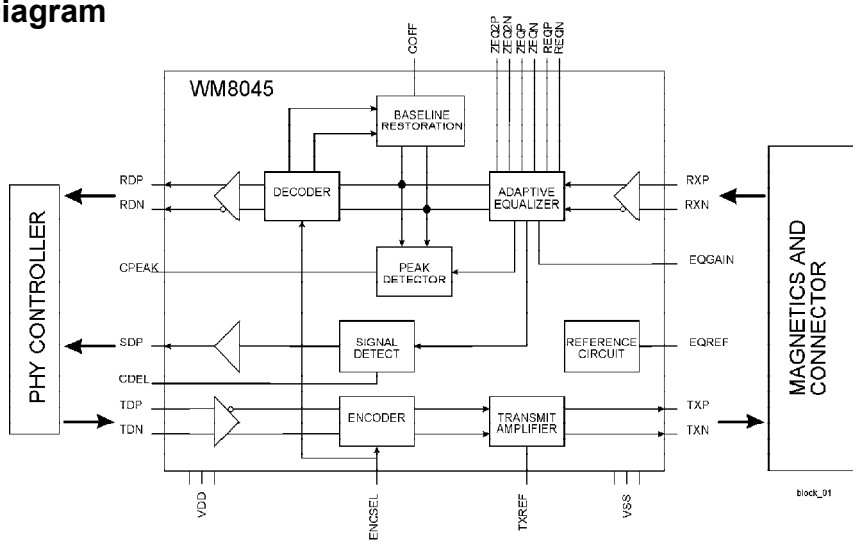
Key Specifications

- **Single 5V supply voltage**
- **Supply Current 166 mA typical**
- **20 mA typical TX balanced output current**
- **RX input voltage range: 2.6 Vp-p**

Applications

- **100 Base -TX Fast Ethernet**
- **155 Mb/s ATM over UTP-5 or STP cable**
- **100 Mb/s TP-FDDI over copper**
- **Direct replacement for MX98702 or PE95000**

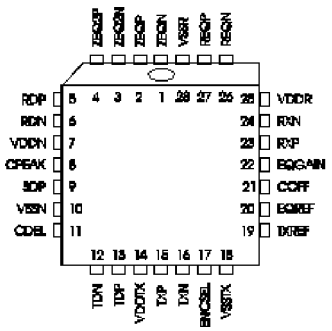
Block Diagram



Wolfson Microelectronics
Lutton Court, Bernard Terrace, Edinburgh EH8 9NX, UK
Tel: +44 (0) 131 667 9386 Fax: +44 (0) 131 667 5176
email: admin@wolfson.co.uk
www: http://www.wolfson.co.uk

Package Information

Top View
28 PLCC



Ordering Information

DEVICE	STANDARD	PACKAGE
XWM8045ECFN	100Base-TX	28 pin PLCC
XWM8045ACFN	ATM	28 pin PLCC

Absolute Maximum Ratings (note 1)

Supply Voltage (VDD - VGND) . . . . . +7V
Inputs . . . . . GND - 0.3 V, V_{DD} + 0.3 V

Operating temperature range, T_A . . . . 0°C to +70°C
Storage Temperature . . . . . -40°C to +85°C
Lead Temperature (soldering, 10 sec) . . . . . +260°C

Note 1: Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating range limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	V_{DD}	4.75	5	5.25	V
High level PECL digital input voltage	V_{IH}	V_{DD}-1.15		V_{DD}-0.72	V
Low level PECL digital input voltage	V_{IL}	V_{DD}-1.95		V_{DD}-1.46	V
High level PECL digital output voltage (note 2)	V_{OH}	V_{DD}-1.24		V_{DD}-0.72	V
Low level PECL digital output voltage (note 2)	V_{OL}	V_{DD}-1.95		V_{DD}-1.6	V
PECL output differential	V_{OH} - V_{OL}	0.70			V
High level CMOS input voltage	V_{ih}	0.8 * V_{DD}			V
Low level CMOS input voltage	V_{il}			0.2 * V_{DD}	V
Operating free air temperature	T_a	0	25	70	°C

Note 2: Without external load

DC Characteristics

VDD = 5V +/- 5%, GND = 0 V, Ta = 0°C to 70°C. Load Conditions unless otherwise stated :
50Ω resistor TXP to V_{DD} ,50Ω resistor TXN to V_{DD}, 100Ω resistor TXP to TXN, 12pF capacitor TXP to TXN, R(TXREF) and R(RXREF) = 1kΩ

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
High-level PECL Digital input current	I_{IH}			450	µA
Low-level PECL Digital input current	I_{IL}			60	µA
Supply Current (inc. transmit current)		129.4	166.64	201.9	mA

Transmitter Operating Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Iout max TXP,TXN (see note 1)	39.4		41.9	mA
Iout TXP,TXN in balanced condition	19.70		20.95	mA
ITXP/ITXN in balanced condition	0.98	1.0	1.02	ratio
Current gain ITXREF to IOUT TXP,TXN		16		ratio

Receiver Operating Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Comparator output current at EQGAIN wrt IEQREF	+/-0.03		+/-0.045	ratio
Diff. voltage gain REQP/REQN;ZEQP/ ZEQN; ZEQ2P/ ZEQ2N (1V input)	0.245	0.25	0.255	Vgain
Sink Current I_{REQP},I_{REQN},I_{ZEQP},I_{ZEQN},I_{ZEQ2P},I_{ZEQ2N}	-4.0	-6.0		mA
Source Current I_{REQP},I_{REQN},I_{ZEQP},I_{ZEQN},I_{ZEQ2P},I_{ZEQ2N}	4.0			mA
Nominal operating voltage on CPEAK		3.8		V
Common mode input voltage at RXP/N	3.0	3.5	4.0	V
Differential input impedence RXP/N	8	24	40	kΩ

Note 1: Iout max is defined as the maximum current that can be supplied by each pin. When Iout max flows from TXP then Iout TXN is zero and vice versa.

AC Characteristics

This section gives characteristics of the device functioning in a typical application. These parameters are not guaranteed by production testing. Refer to WM8045 application notes for specific configurations and results.

Transmitter characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Data clock frequency TDP, TDN		125	160	MHz
Differential rise/fall time TXP/TXN (note 1)			2	ns
Total Peak-to-Peak Jitter		0.5	1	ns
Current ITXP, ITXN change over 500 ns			1	%
Duty cycle distortion, DCD, 16ns pulse width (note 2)			+/-150	ps
Signal overshoot TXP,TXN			1.5	%
Common mode output on TXP, TXN wrt differential signal up to 125 MHz		-40		dB
Power supply rejection 100 mVp-p up to 200 kHz (note 3)		60		dB

Receiver Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Data Clock frequency		125	160	MHz
Rise Time at RDP/N (10%-90%)	0.3	0.7	1.2	ns
Fall Time at RDP/N (90%-10%)	0.3	0.7	1.2	ns
Total Peak-to-Peak Jitter Binary mode (note 4)		1.0	2.0	ns
Total Peak-to-Peak Jitter MLT3 mode (note 4)		1.5	2.5	ns
Common mode rejection of receiver upto 125MHz (note 5)	40			dB
Power supply rejection ratio 100mVp-p upto 200 kHz (note 5)		60		dB
Duty cycle distortion		+/- 0.3		ns

Signal Assert Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Assert Time (see Pin Descriptions note 6)			1000	µs
Deassert Time (see Pin Descriptions note 7)			350	µs

Notes:

1. Rise/fall time can be controlled by external capacitor.
2. Duty cycle distortion is measured as the time difference from an ideal signal with 16ns pulse width.
3. Measured by change in output current TXP,TXN max.
4. Includes jitter from the transmitter, cable and receiver.
5. Measured as differential signal at SDP,SDN using test mode.
6. CDEL: The capacitor at CDEL delays assertion of the SD signal to allow the equaliser to stabilise.
   Max assert time (µs)
   =C(EQGAIN)(nF)x40 + C(CDEL)(nF)x25.
7. EQGAIN: Indicates gain factor of equaliser. The capacitor at this pin determines the maximum SD de-assert time.
   Maximum de-assert time (µs) = C(EQGAIN)(nF)x20.

Pin Descriptions

PIN NAME	No.	I/O TYPE	DESCRIPTION
ZEQN	1	Voltage I/O	Equaliser impedance 1 negative (note 1)
ZEQP	2	Voltage I/O	Equaliser impedance 1 positive (note 1)
ZEQ2N	3	Voltage I/O	Equaliser impedance 2 negative (note 2)
ZEQ2P	4	Voltage I/O	Equaliser impedance 2 positive (note 2)
RDP	5	PECL Output	Receive data output positive
RDN	6	PECL Output	Receive data output negative
VDDN	7	Supply	Receive noisy VDD supply
CPEAK	8	Current output	Peak detector capacitor (note 3)
SDP	9	PECL Output	Signal detect output positive
VSSN	10	Supply	Receive noisy VSS supply
CDEL	11	Current output	Signal detect assert delay capacitor (note 4)
TDN	12	PECL Input	Transmit data input negative
TDP	13	PECL Input	Transmit data input positive
VDDTX	14	Supply	Transmit VDD supply
TXP	15	Current output	Transmit signal output positive
TXN	16	Current output	Transmit signal output negative
ENCSEL	17	CMOS , pull down	Select encoding/decoding (note 5)
VSSTX	18	Supply	Transmit VSS supply
TXREF	19	Current in	Transmit reference current (note 6)
EQREF	20	Current in	Equaliser reference current (note 7)
COFF	21	Current output	Offset correction capacitor (note 8)
EQGAIN	22	Current output	Equaliser gain control capacitor (note 9)
RXP	23	Voltage input	Receive signal input positive
RXN	24	Voltage input	Receive signal input negative
VDDR	25	Supply	Receive VDD supply
REQN	26	Voltage I/O	Equaliser gain resistor negative (note 10)
REQP	27	Voltage I/O	Equaliser gain resistor positive (note 10)
VSSR	28	Supply	Receive VSS supply

Notes:

1. ZEQP/N: The RC network between these pins sets a frequency dependent gain which is increased linearly from zero to maximum as the equalisation level increases from minimum to maximum.
2. ZEQ2P/N: The RC network between these pins sets a frequency dependent gain which is increased linearly from zero to maximum as the equalisation level increased from its mid-point to maximum. This provides gain boost for longer lengths of cable.
3. CPEAK: The RC network of CPEAK pin control the frequency response of the on chip peak detector.
4. CDEL: The capacitor at CDEL delays assertion of the SD signal to allow the equaliser to stabilise.
   Max assert time (µs)
   =C(EQGAIN)(nF)x40 + C(CDEL)(nF)x25.
5. ENCSEL: CMOS selection pin of encode/decode mode. High = Binary, Low = MLT3.
6. TXREF: Resistor controls the amplitude of the current outputs, which determines the transmit signal voltage amplitude. For the Chip + Transformer the resistor value can be determined as follows:
   R(TXREF) = (20 x Zcable) / Vpp where
   Vpp = pk-pk differential amplitude (line output,V)
   Zcable = Characteristic differential cable impedance.
7. EQREF: The resistor at EQREF pin sets internal reference currents for the receiver circuitry.
8. COFF: Capacitor determines time constant of BLW loop.
9. EQGAIN: Indicates gain factor of equaliser. The capacitor at this pin determines the maximum SD de-assert time.
   Maximum de-assert time (µs) = C(EQGAIN)(nF)x20.
10. REQP/N: The resistor at REQP/N sets the minimum signal gain through the equaliser.

Functional Description

The WM8045 acts as an interface between the digital data of the physical layer controller and the analog signals present on the twisted pair cable. (see Block Diagram, Page 1)

Transmit Channel

The transmitter consists of an encoder and a current driver. The transmitter input (TDP/TDN) receives a digital data bit stream at pseudo ECL levels from the physical layer controller. The signal is fed to an encoder which converts the NRZI input data to MLT3 format, or passes it through unencoded, depending on the setting of the ENCSEL pin. The signal is then fed to a current output driver whose maximum signal amplitude is controlled by an external resistor at TXREF. The current signal output TXP/TXN will drive a cable via a transformer/filter module.

Receiver Channel

The receiver channel consists of an adaptive equalizer, a decoder and a signal detect block. The receiver channel input (RXP/RXN) is isolated from the cable by a transformer/filter module. The adaptive equalization amplifier compensates for the attenuation of the cable for all cable lengths up to 100 metres, and the effects of the a.c. coupling of the transformers. These cable characteristics are defined by EIA/TIA 568 standard - fig. 1 shows typical UTP-5 cable attenuation curves which incorporate "real world" connector and punch-down block contributions, as well as typical equalizer response curve to compensate for these losses. The equalizer transfer function of WM8045 is fully controlled by external components resulting in a low cost and flexible architecture.

Application diagrams (figs 3-5) detail the filters required (at REQP/REQPN, ZEPQ/ZEQPN and ZEQP2/ZEQPN2 pins) for standard applications over standard twisted pair cable. The effect of the external filter networks on the signal is varied from zero to full compensation by a feedback loop which senses the incoming amplitude (with peak detector) and optimizes the applied equalization.

The equalised signal is fed to the decoding circuit which converts the analog signal to a digital PECL datastream, converting from MLT3 or NRZ waveforms as selected by the ENCSEL pin. The baseline restoration loop compensates for baseline wander i.e. DC drifts in incoming signal which may occur due to data pattern dependent DC shifts and the inherent low frequency bandwidth of the channel and AC coupling transformers. If not corrected this baseline wander effect can cause degradation in signal/noise ratio and furthermore result in data errors/link failure. The feedback loop compares the incoming equalised signal with a reconstructed reference. The difference is filtered and used to effect low frequency compensation in order to maintain the equalised signal at the reference level. The filter characteristic is determined by the external capacitor at COFF. The value of COFF has been chosen to remove disruptive high frequency components while allowing the circuit to track baseline changes limited by the time constant of the transformers. The receiver outputs are then driven out by PECL buffers to be connected to a physical layer controller.

The signal detect circuit monitors the gain control to give a reliable indication of the presence of a valid equalised signal in accordance with the TP-PMD specification. After processing this information, signal detect (SDP) is fed in pseudo ECL format to the physical layer controller.

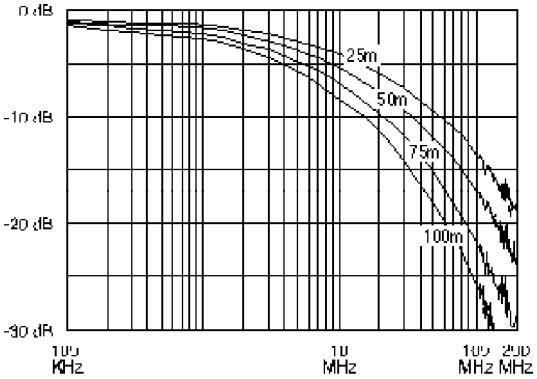
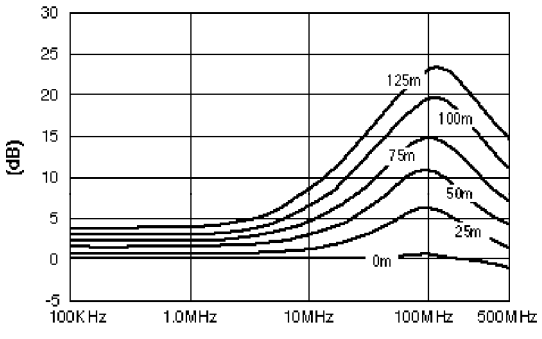


Fig 1: Typical UTP CAT5 Cable Loss Curves



Typical Equalizer Transfer Function

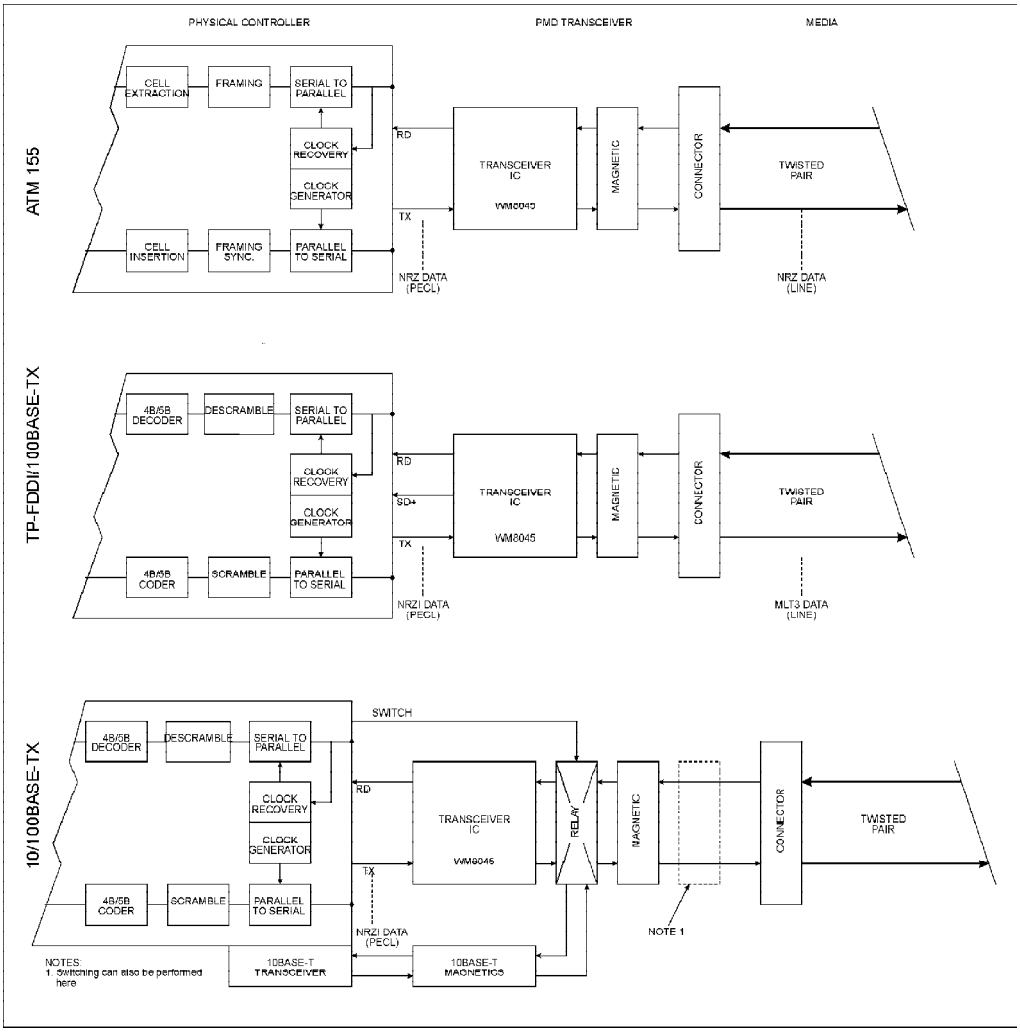
System Application

WM8045 enables implementation of the following architectures:

1. ATM 155
2. 100Base-TX only adapters & repeaters.
3. 10/100-TX adapters with separate 10/100 cable connectors.
4. 10/100-TX products which employ 10/100 switching (on primary or secondary of magnetics).
5. 10/100-TX products which employ a common magnetic module with inherent 10/100 mixing.

The 10/100 system diagram indicates a generic switching arrangement. Non-standard configurations are also possible.

Fig 2. System Application



System Application (continued)

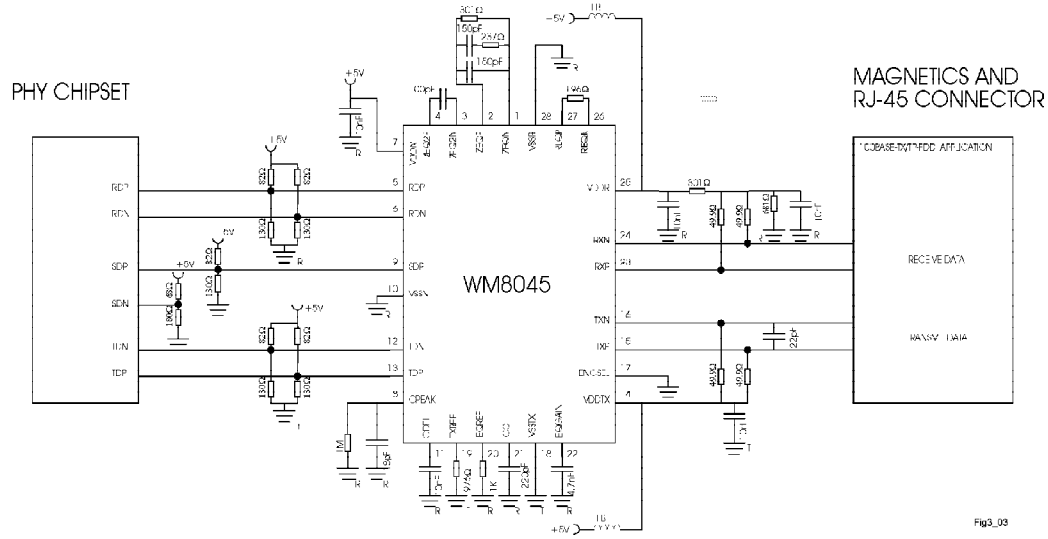


Fig. 3: Application Circuit TP-FDDI/100BASE-TX

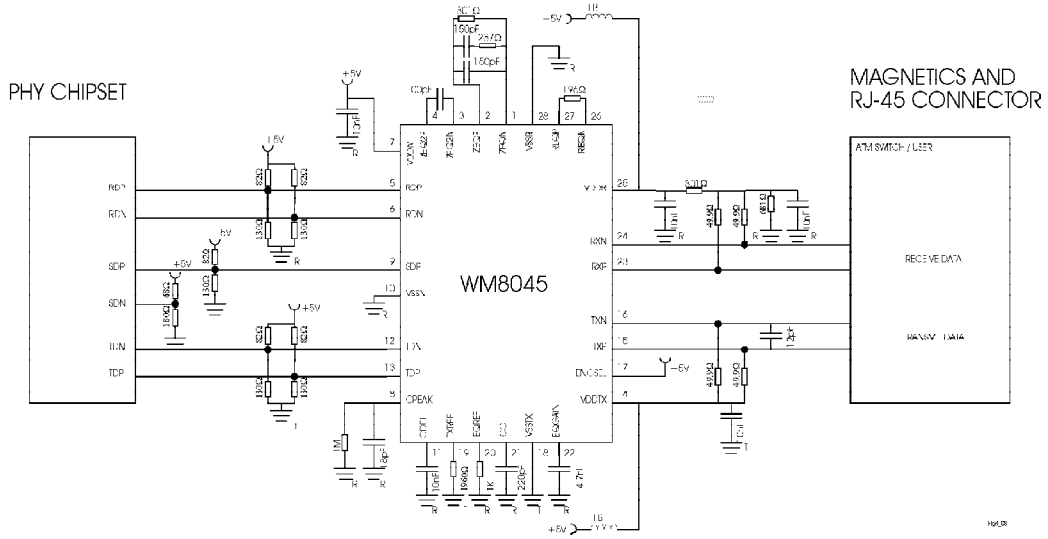


Fig. 4: Application Circuit ATM 155

System Application (continued)

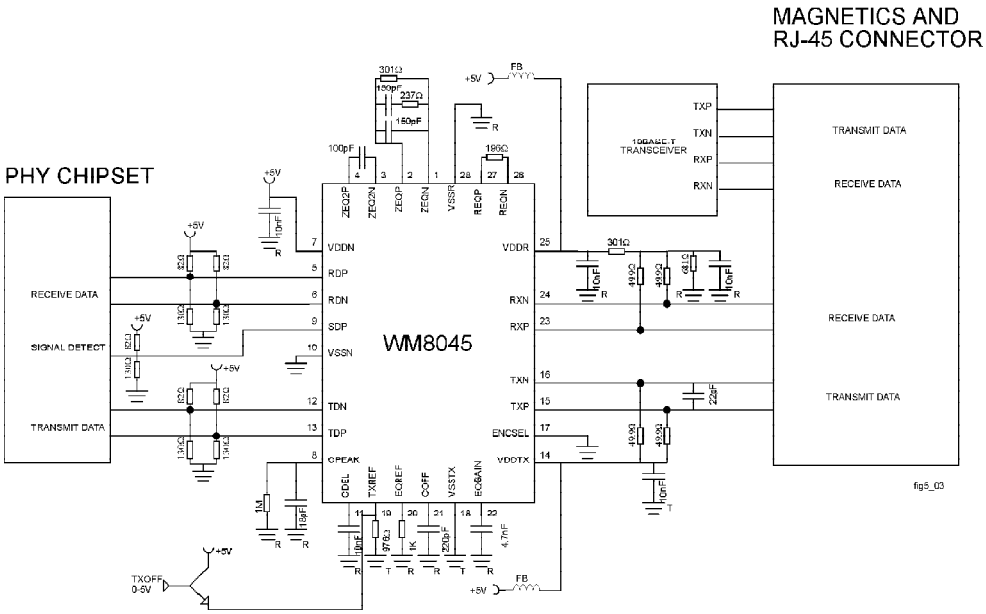


Fig. 5: Application Circuit 10/100BASE-TX

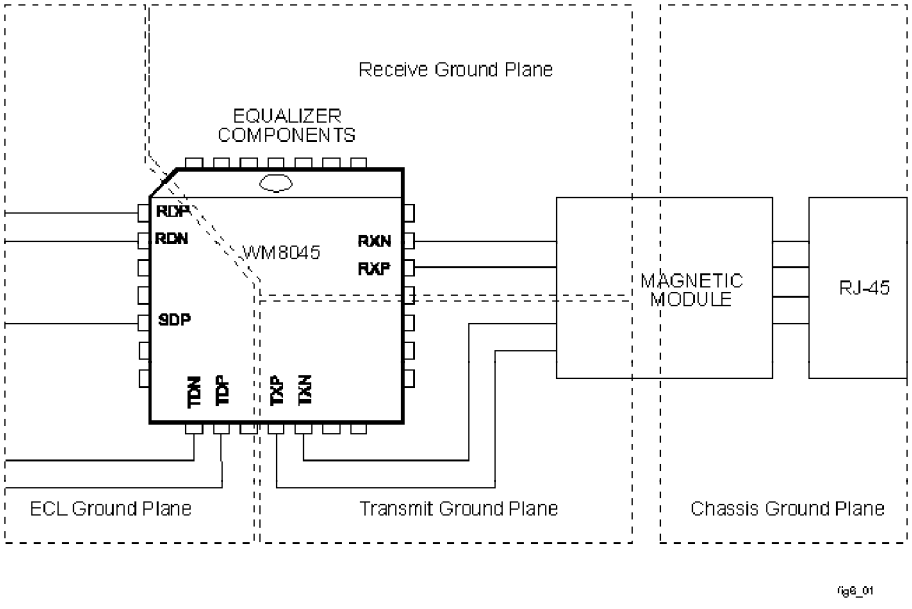


Fig. 6. Layout Guide

Application Notes

1 All resistors are 1% tolerance, capacitors 5% except for bypass capacitors.

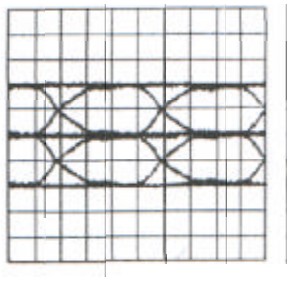
2. The equaliser components connected to REQP/N, ZEQP/N, ZEQ2P/N are sensitive and should be placed as close as possible to the pins to avoid coupling high frequency noise into the receiver signal path. Keep area in immediate vicinity of these signals as free as possible of other signal routing. Keep layout as symmetric as possible to avoid uneven parasitic loading.
3. PCB traces connecting external components to TXREF, EQREF, COFF and CPEAK pins should be likewise kept as short as possible.
4. The termination resistors on the receiver inputs must be connected to a common mode voltage of 3.15V. This is generated from the receiver 5V supply by the divider network shown in figures 3,4,5). Decoupling of this voltage is recommended for noise immunity.
5. The transmit signal rise-time can be adjusted by a shunt capacitor between signals TXP & TXN. The capacitor values shown result in Tr ~3.7ns for TP-FDDI/100Base-TX and Tr ~2.8ns for ATM155 to comply with the relevant standards.
6. The PECL termination networks shown (Thevenin 50 ohm) are typical. Signal traces should be effective 50Ω transmission lines. Other suitable termination schemes may be used.
7. Place termination networks near input data pins of Transceiver (TD) and PHY device (SD,RD) for optimum termination.
8. For controller chipsets with differential SD inputs, the unused SDN signal can be terminated with a divider network of 68Ω to Vdd/180Ω to ground.
9. Make all differential signal paths short and of same length to avoid unbalancing effects and unwanted loops.
10. Decouple VDD signals close to IC. Use series ferrite beads and ideally a 10µF tantalum may be placed in parallel with the 0.1µF low inductance ceramic bypass capacitor. Device ground pins should be directly connected to low impedance ground plane.
11. For TP-FDDI over STP (150Ω) applications, the following modifications are required:
    R(Txref) = 1.22K; R (REQP/REQN) = 205Ω;
    Receiver termination = 2x 75Ω;
    Transmit termination = 2x 75Ω.
    Pinout of DB9 connector is as follows -
    Transmit: TX+ = P5, TX- = P9;
    Receive: RX+ = P1, RX- = P6.
    There is no need to consider termination of unused pairs because of the inherent shielding of the cable.
12. For 10/100Base-TX there are a number of architecture choices, The circuit shown in fig. 5 utilises a single magnetic module which integrates the 10/100 transformer/choke and incorporates passive mixing of 10/100 transmit signals.
13. A switching transistor is shown connected to the TXREF pin which can be used to disable the 100Base-TX transmit output signal. Forcing the TXREF pin above its normal operating voltage (1.25V) disables the current to the TX output driver effectively disabling it. For this application, it is not essential to disable the 100TX outputs - it would also suffice to ensure that transmit lines from controller remain “quiet”.
14. For 10/100TX applications, one can also use switching (relay or solid-state) on primary or secondary of the magnetic module, as indicated in figure 2, 10/100Base-TX. This allows one to use standard 10Base-T transceiver/10Base-T filter module, with the switch typically controlled by the physical controller/MAC device.
15. It is important to implement a PCB layout which adheres to good analog layout rules for optimum network & EMC performance. An example of such a layout is as shown in the Layout Guide, fig. 6, which minimises the noise coupling through use of distinct power & ground partitions. Power islands should be connected by ferrite beads. Please refer to the EMC section for more EMC specific application guidelines.
16. Implementation of circuits as recommended will result in nominal Vpp = 2V for TP/FDDI, 100Base-TX and Vpp=1V for ATM 155 applications.

Performance

The following eye pattern measurements show the operation of the adaptive equaliser and the jitter performance on a design using an WM8045 solution. Figure A shows the MLT3 transmit output waveform at 0m cable. Fig B shows the waveform at receiver input after the attenuation & phase distortion effects of 100m UTP-5 cable. Fig. C shows the recovered NRZI data for same signal. Similar measurements are repeated in Figures D,E and F for ATM 155Mb/s NRZ signals.

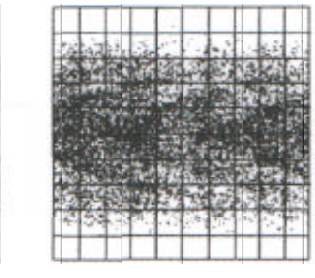
TP-FDDI/100Base-TX

MLT3 Transmit Output (TXP/N)



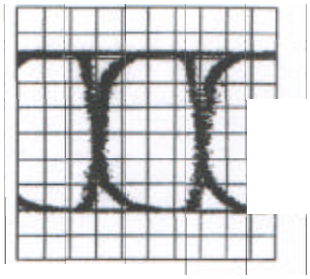
A
0m UTP-5 Cable
500mV/DIV, 2ns/DIV

Receiver Input (RXP/N)



B
100m UTP-5 Cable
200mV/DIV, 2ns/DIV

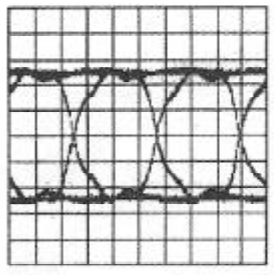
NRZI Receiver Output (RDP/N)



C
100m UTP-5 Cable
200mV/DIV, 2ns/DIV

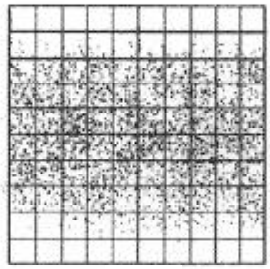
ATM-155

NRZ Transmit Output (TXP/N)



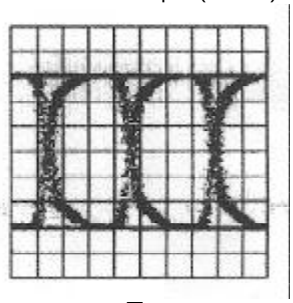
D
100m UTP-5 Cable
200mV/DIV, 2ns/DIV

Receiver Input (RXP/N)



E
100m UTP-5 Cable
200mV/DIV, 2ns/DIV

NRZI Receiver Output (RDP/N)



F
100m UTP-5 Cable
200mV/DIV, 2ns/DIV

All jitter measurements shown are peak values resulting from combination of transmit, receive and cable contributions. In MLT3 mode, the transmit eye pattern has a 3.5ns rise-time, overshoot <3% and transmit jitter <1ns. As a result of this, the receiver eye pattern has 2ns of jitter at 100m UTP-5 cable. In NRZ mode, the transmit eye pattern has a rise-time of 3ns, <5% overshoot and transmit jitter <1ns. As a result, the receiver jitter at 100m UTP-5 cable is 1.6ns.

There is a general performance trade-off involved here. A faster rise time will reduce jitter and result in lower Bit Error Rate (BER). However, a faster rise time can also result in excessive signal overshoot and EMI emissions when signal encounters impedance mismatches in cable or punch down blocks. The application circuits shown should result in optimum waveform parameters.

EMC Considerations

TP-FDDI/100Base-TX uses MLT3 line coding (fundamental frequency = 32.5 MHz) to shift 90% of spectral energy to below 40 MHz. ATM 155 (fundamental frequency = 77.5 MHz) uses NRZ coding with 1Vpp amplitude to reduce EMI emissions.

The WM8045 has been designed to minimise EMI emissions and noise susceptibility. The key measures which help to achieve this are as follows:

Edge-rate control on WM8045 signal transceiver output

Excellent CMRR and PSRR of transmit/receive amplifiers

It is crucial to employ good high speed PCB design rules in layout out the board.

1. Use multi-layer PCB with dedicated ground and power layers for best high frequency and EMC performance. At least four layers are recommended with outside layers for signal routing and inner layers for supply planes.
2. Use of ground plane partitions as indicated in the layout guide is recommended. The chassis ground is generally connected to backplate directly. The ground plan area under the magnetic module is left void for optimum noise separation.
3. Use of shielded RJ45 (UTP-5) or DB9 (STP) is recommended with galvanic contact to backplate for chassis ground continuity.
4. Terminations of unused cable pairs is recommended. The unused pairs are terminated in their common mode impedance (to chassis ground) to minimise cable reflections and common mode standing waves. The application circuits shown indicate one termination scheme but there are other options. Refer to the PMD standards for additional information.

It should however be noted that EMC performance is a system measurement and highly implementation specific.

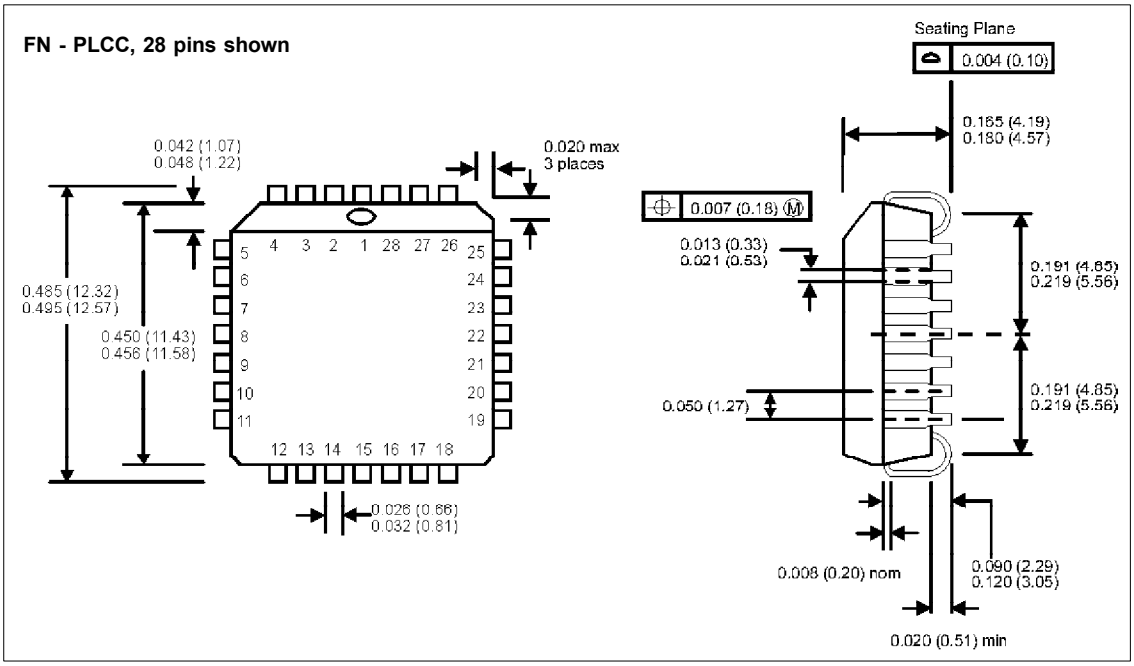
Appendix 1: Physical Controller Chipsets

Standard	Vendor	Device	Description
TP-FDD1/100TX	AMD	AM79565/AM566	Clock generation/recovery
TP-FDD1/100TX	ICS	ICS1887	Clock generation/recovery
TP-FDD1/100TX	Motorola	MC68836	Clock generation/recovery
100TX	Macronix	MX98704	Clock generation/recovery
100TX	DEC	21140	LAN controller for PCI
100TX	National Semiconductors	DP83840	10/100Mb/s Ethernet Physical Layer
ATM	PMC-Sierra	SUNI Series	Saturn user network interface

Appendix 2: Magnetics

Standard	Vendor	Device
TP-FDD1/100TX	Pulse Engineering	PE-68517
ATM	Pulse Engineering	PE-68517
10/100TX	Pulse Engineering	PE-69016
100TX	Valor	ST6114

Package Dimensions



Notes:

A. Dimensions in inches (mm).
B. Complies with Jedec standard MS-018.
C. This drawing is subject to change without notice.