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SEMICONDUCTOR TECHNICAL DATA

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DSP56301/D

DSP56301

Advance Information
24-BIT DIGITAL SIGNAL PROCESSOR

The DSP56301 is a member of the DSP56300 core family of programmable CMOS Digital Signal Processors (DSPs). This family uses a high performance, single-clock-cycle-per-instruction engine providing a twofold performance increase over Motorola's popular DSP56000 core family, while retaining code compatibility. Significant architectural enhancements in the DSP56300 core family include a barrel shifter, 24-bit addressing, instruction cache, and Direct Memory Access (DMA). The DSP56301 offers 66 / 80 / 100 MIPS using an internal 66 / 80 / 100 MHz clock at 3.0–3.6 volts. The DSP56300 core family offers a new level of performance in speed and power provided by its rich instruction set and low power dissipation, enabling a new generation of wireless, telecommunications, and multimedia products.

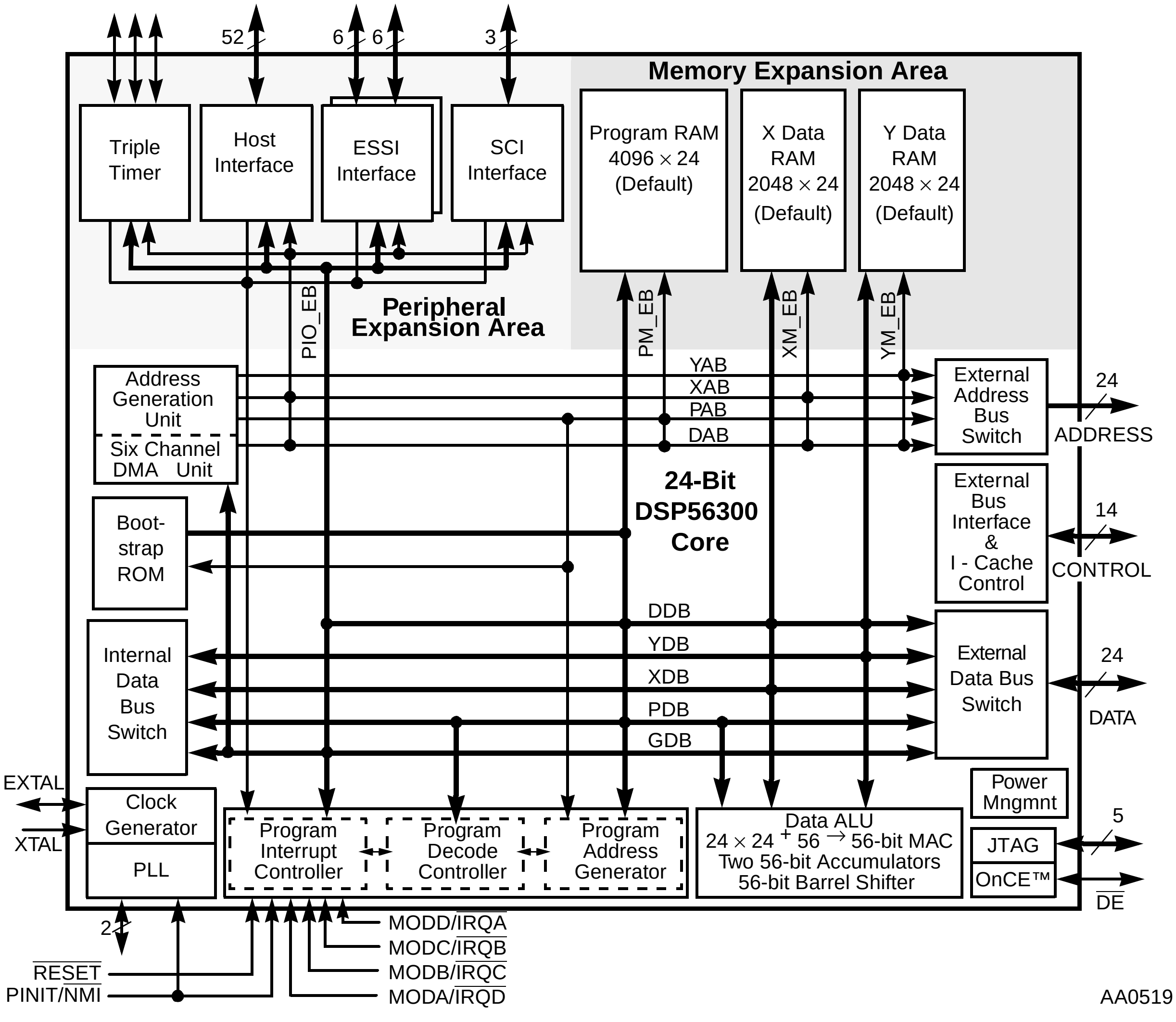

Figure 1 DSP56301 Block Diagram

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FOR TECHNICAL ASSISTANCE:

Telephone:	1-800-521-6274
Email:	dsphelp@dsp.sps.mot.com
Internet:	http://www.motorola-dsp.com

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL} / V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
PIN	True	Asserted	V_{IH} / V_{OH}
PIN	False	Deasserted	V_{IL} / V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

FEATURES

High Performance DSP56300 Core

- 66 / 80 / 100 Million Instructions Per Second (MIPS) with a 66 / 80 / 100 MHz clock at 3.0–3.6 V
- Object code compatible with the DSP56000 core
- Highly parallel instruction set
- Data Arithmetic Logic Unit (Data ALU)
  - Fully pipelined 24 x 24-bit parallel Multiplier-Accumulator (MAC)
  - 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing)
  - Conditional ALU instructions
  - 24-bit or 16-bit arithmetic support under software control
- Program Control Unit (PCU)
  - Position Independent Code (PIC) support
  - Addressing modes optimized for DSP applications (including immediate offsets)
  - On-chip instruction cache controller
  - On-chip memory-expandable hardware stack
  - Nested hardware DO loops
  - Fast auto-return interrupts
- Direct Memory Access (DMA)
  - Six DMA channels supporting internal and external accesses
  - One-, two-, and three- dimensional transfers (including circular buffering)
  - End-of-block-transfer interrupts
  - Triggering from interrupt lines and all peripherals
- Phase Lock Loop (PLL)
  - Allows change of low power Divide Factor (DF) without loss of lock
  - Output clock with skew elimination

- Hardware debugging support
  - On-Chip Emulation (OnCE™) module
  - Joint Action Test Group (JTAG) Test Access Port (TAP) port
  - Address Trace mode reflects internal Program RAM accesses at the external port

On-Chip Memories

- Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable:

Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size	Instruction Cache[1]	Switch Mode[2]
4096 × 24-bit	0	2048 × 24-bit	2048 × 24-bit	disabled (CE = 0)	disabled (MS = 0)
3072 × 24-bit	1024 × 24-bit	2048 × 24-bit	2048 × 24-bit	enabled (CE = 1)	disabled (MS = 0)
2048 × 24-bit	0	3072 × 24-bit	3072 × 24-bit	disabled (CE = 0)	enabled (MS = 1)
1024 × 24-bit	1024 × 24-bit	3072 × 24-bit	3072 × 24-bit	enabled (CE = 1)	enabled (MS = 1)

Note: 1. Controlled by the Cache Enable (CE) bit in the Status Register (SR)
2. Controlled by the Memory Select (MS) bit in the Operating Mode Register (OMR)

- 192 × 24-bit bootstrap ROM

Off-Chip Memory Expansion

- Data memory expansion to two 16 M × 24-bit word memory spaces in 24-Bit mode or two 64 K × 16-bit memory spaces in 16-Bit Compatibility mode
- Program memory expansion to one 16 M × 24-bit words memory space in 24-Bit mode or 64 K × 16-bit in 16-Bit Compatibility mode
- External memory expansion port
- Chip Select Logic for glueless interface to SRAMs
- On-chip DRAM Controller for glueless interface to DRAMs

On-Chip Peripherals

- 32-bit parallel PCI / Universal Host Interface (HI32), PCI Rev. 2.1 compliant with glueless interface to other DSP563xx buses
- ISA interface requires only 74LS45-style buffer
- Two Enhanced Synchronous Serial Interfaces (ESSI0 and ESSI1)
- Serial Communications Interface (SCI) with baud rate generator
- Triple timer module
- Up to forty-two programmable General Purpose Input / Output (GPIO) pins, depending on which peripherals are enabled

Reduced Power Dissipation

- Very low power CMOS design
- Wait and Stop low power standby modes
- Fully-static logic, operation frequency down to 0 Hz (DC)
- Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

TARGET APPLICATIONS

The DSP56301 is intended for general-purpose digital signal processing, particularly in multimedia and telecommunication applications, such as videoconferencing and cellular telephony.

PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

Table 1 DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM / AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM / AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301 / D

SECTION 1

SIGNAL/CONNECTION DESCRIPTIONS

SIGNAL GROUPINGS

The input and output signals of the DSP56301 are organized into functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**.

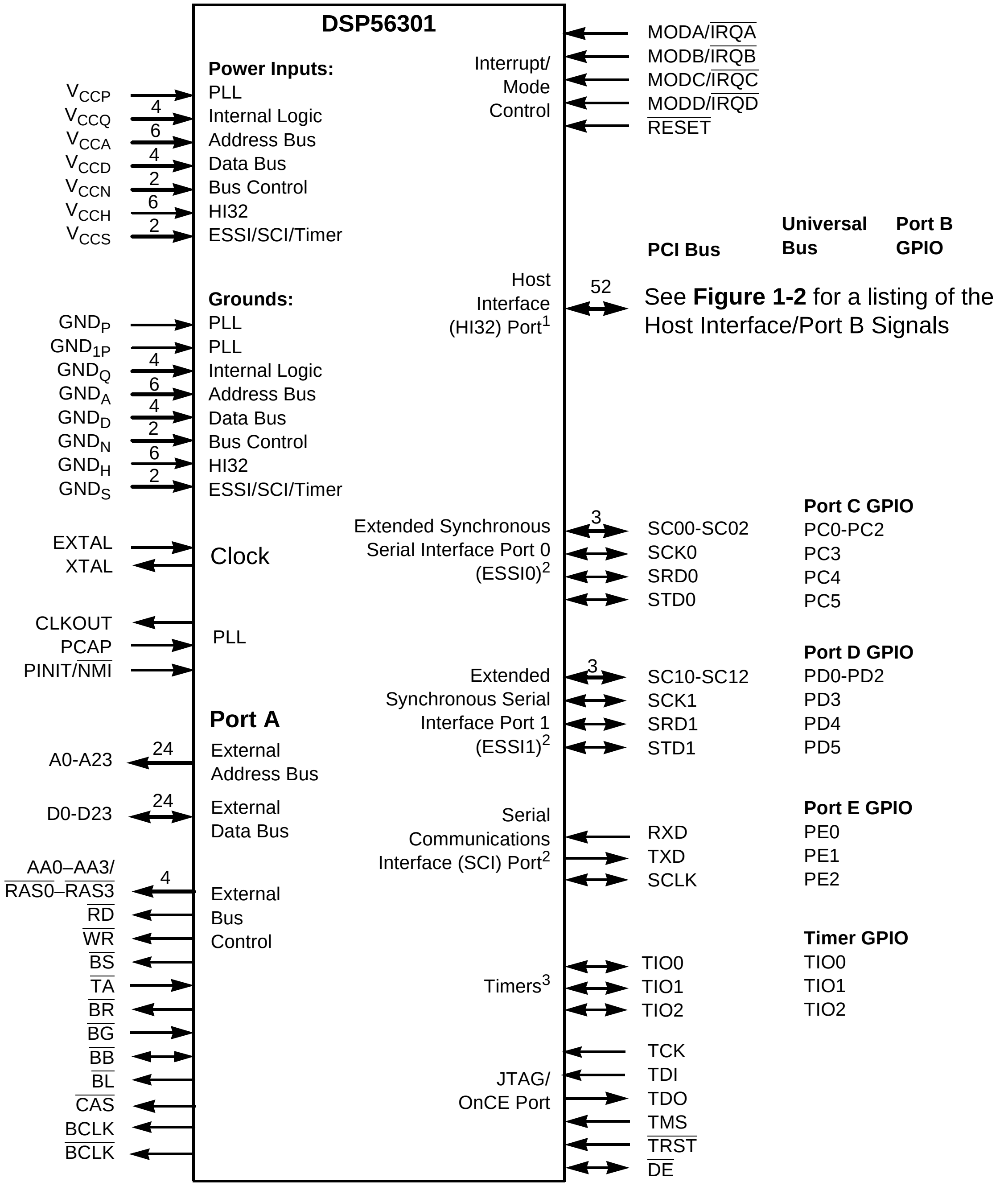
The DSP56301 is operated from a 3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 1-1 DSP56301 Functional Signal Groupings

Functional Group		**Number of Signals**	**Detailed Description**
Power (V_{CC})		25	**Table 1-2**
Ground (GND)		26	**Table 1-3**
Clock		2	**Table 1-4**
PLL		3	**Table 1-5**
Address Bus	Port A[1]	24	**Table 1-6**
Data Bus		24	**Table 1-7**
Bus Control		15	**Table 1-8**
Interrupt and Mode Control		5	**Table 1-9**
Host Interface (HI32)	Port B[2]	52	**Table 1-11**
Extended Synchronous Serial Interface (ESSI)	Ports C and D[3]	12	**Table 1-12** and **Table 1-13**
Serial Communication Interface (SCI)	Port E[4]	3	**Table 1-14**
Timer		3	**Table 1-15**
JTAG / OnCE Port		6	**Table 1-16**

Note:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI32 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.

Figure 1-1 is a diagram of DSP56301 signals by functional group.



Note:

1. The HI32 port supports PCI and non-PCI bus configurations. Twenty-four of these HI32 signals can also be configured alternately as GPIO signals (PB0–PB23).
2. The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC0–PC5), Port D GPIO signals (PD0–PD5), and Port E GPIO signals (PE0–PE2), respectively.
3. TIO0–TIO2 can be configured as GPIO signals.

Figure 1-1 Signals Identified by Functional Group

DSP56301	PCI Bus	Universal Bus	Port B GPIO	Host Port (HP) Reference
Host Interface (HI32)/ Port B Signals	HAD0	HA3	PB0	HP0
	HAD1	HA4	PB1	HP1
	HAD2	HA5	PB2	HP2
	HAD3	HA6	PB3	HP3
	HAD4	HA7	PB4	HP4
	HAD5	HA8	PB5	HP5
	HAD6	HA9	PB6	HP6
	HAD7	HA10	PB7	HP7
	HAD8	HD0	PB8	HP8
	HAD9	HD1	PB9	HP9
	HAD10	HD2	PB10	HP10
	HAD11	HD3	PB11	HP11
	HAD12	HD4	PB12	HP12
	HAD13	HD5	PB13	HP13
	HAD14	HD6	PB14	HP14
	HAD15	HD7	PB15	HP15
	HC0/$\overline{\text{HBE0}}$	HA0	PB16	HP16
	HC1/$\overline{\text{HBE1}}$	HA1	PB17	HP17
	HC2/$\overline{\text{HBE2}}$	HA2	PB18	HP18
	HC3/$\overline{\text{HBE3}}$	Tie to pull-up or V_{CC}	PB19	HP19
	$\overline{\text{HTRDY}}$	$\overline{\text{HDBEN}}$	PB20	HP20
	$\overline{\text{HIRDY}}$	$\overline{\text{HDBDR}}$	PB21	HP21
	$\overline{\text{HDEVSEL}}$	$\overline{\text{HSAK}}$	PB22	HP22
	$\overline{\text{HLOCK}}$	$\overline{\text{HBS}}$	PB23	HP23
	HPAR	$\overline{\text{HDAK}}$	Internal disconnect	HP24
	$\overline{\text{HPERR}}$	HDRQ	Internal disconnect	HP25
	$\overline{\text{HGNT}}$	HAEN	Internal disconnect	HP26
	$\overline{\text{HREQ}}$	HTA	Internal disconnect	HP27
	$\overline{\text{HSERR}}$	$\overline{\text{HIRQ}}$	Internal disconnect	HP28
	$\overline{\text{HSTOP}}$	$\overline{\text{HWR}}$/HRW	Internal disconnect	HP29
	HIDSEL	$\overline{\text{HRD}}$/$\overline{\text{HDS}}$	Internal disconnect	HP30
	$\overline{\text{HFRAME}}$	Tie to pull-up or V_{CC}	Internal disconnect	HP31
	HCLK	Tie to pull-up or V_{CC}	Internal disconnect	HP32
	HAD16	HD8	Internal disconnect	HP33
	HAD17	HD9	Internal disconnect	HP34
	HAD18	HD10	Internal disconnect	HP35
	HAD19	HD11	Internal disconnect	HP36
	HAD20	HD12	Internal disconnect	HP37
	HAD21	HD13	Internal disconnect	HP38
	HAD22	HD14	Internal disconnect	HP39
	HAD23	HD15	Internal disconnect	HP40
	HAD24	HD16	Internal disconnect	HP41
	HAD25	HD17	Internal disconnect	HP42
	HAD26	HD18	Internal disconnect	HP43
	HAD27	HD19	Internal disconnect	HP44
	HAD28	HD20	Internal disconnect	HP45
	HAD29	HD21	Internal disconnect	HP46
	HAD30	HD22	Internal disconnect	HP47
	HAD31	HD23	Internal disconnect	HP48
	$\overline{\text{HRST}}$	$\overline{\text{HRST}}$	Internal disconnect	HP49
	$\overline{\text{HINTA}}$	$\overline{\text{HINTA}}$	Internal disconnect	HP50
	PVCL	Leave unconnected	Leave unconnected	PVCL

Note: HPxx is a reference only and is not a signal name. GPIO references formerly designated as HIOxx have been renamed PBxx for consistency with other Motorola DSPs.

AA1070

Figure 1-2 Host Interface/Port B Detail Signal Diagram

POWER

Table 1-2 Power Inputs

Power Name	Description
V_{CCP}	**PLL Power**—V_{CCP} provides isolated power for the Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail. There is one V_{CCP} input.
V_{CCQ} (4)	**Quiet Power—**V_{CCQ} provides isolated power for the internal processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCQ} inputs.
V_{CCA} (6)	**Address Bus Power**—V_{CCA} provides isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are six V_{CCA} inputs.
V_{CCD} (4)	**Data Bus Power**—V_{CCD} provides isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCD} inputs.
V_{CCN} (2)	**Bus Control Power**—V_{CCN} provides isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCN} inputs.
V_{CCH} (6)	**Host Power**—V_{CCH} provides isolated power for the HI32 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one V_{CCH} input.
V_{CCS} (2)	**ESSI, SCI, and Timer Power**—V_{CCS} provides isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCS} inputs.
Note: These designations are package-dependent. Some packages connect all V_{CC} inputs except V_{CCP} to each other internally. On those packages, all power input, except V_{CCP}, are labeled V_{CC}. The numbers of connections indicated in this table are minimum values; the total V_{CC} connections are package-dependent.	

GROUND

Table 1-3 Grounds

Ground Name	Description
GND$_P$	**PLL Ground** —GND$_P$ is ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V$_{CCP}$ should be bypassed to GND$_P$ by a 0.47 µF capacitor located as close as possible to the chip package. There is one GND$_P$ connection.
GND$_{1P}$	**PLL Ground 1** —GND$_{1P}$ is ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. There is one GND$_{P1}$ connection.
GND$_Q$ (4)	**Quiet Ground** —GND$_Q$ provides isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND$_Q$ connections.
GND$_A$ (6)	**Address Bus Ground** —GND$_A$ provides isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND$_A$ connections.
GND$_D$ (4)	**Data Bus Ground** —GND$_D$ provides isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND$_D$ connections.
GND$_N$ (2)	**Bus Control Ground** —GND$_N$ provides isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND$_N$ connections.
GND$_H$ (6)	**Host Ground** —GND$_H$ provides isolated ground for the HI32 I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GND$_H$ connection.
GND$_S$ (2)	**ESSI, SCI, and Timer Ground** —GND$_S$ provides isolated ground for the ESSI, SCI, and timer I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND$_S$ connections.
Note:	These designations are package-dependent. Some packages connect all GND inputs except GND$_P$ and GND$_{1P}$ to each other internally. On those packages, all power input, except GND$_P$ and GND$_{1P}$, are labeled GND. The numbers of connections indicated in this table are minimum values; the total GND connections are package-dependent.

CLOCK

Table 1-4 Clock Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—EXTAL interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip Driven	**Crystal Output**—XTAL connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

PHASE LOCK LOOP (PLL)

Table 1-5 Phase Lock Loop Signals

Signal Name	Type	State During Reset	Signal Description
PCAP	Input	Input	**PLL Capacitor**—PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP may be tied to V_{CC}, GND, or left floating.
CLKOUT	Output	Chip-driven	**Clock Output**—CLKOUT provides an output clock synchronized to the internal core clock phase. If the PLL is enabled and both the multiplication and division factors equal one, then CLKOUT is also synchronized to EXTAL. If the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL.
PINIT/$\overline{\text{NMI}}$	Input	Input	**PLL Initial/Non-Maskable Interrupt**—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered Non-Maskable Interrupt (NMI) request internally synchronized to CLKOUT. PINIT/$\overline{\text{NMI}}$ can tolerate 5 V.

EXTERNAL MEMORY EXPANSION PORT (PORT A)

Note: When the DSP56301 enters a low-power standby mode (Stop or Wait), it releases bus mastership and tri-states the relevant Port A signals: A0–A23, D0–D23, AA0/$\overline{RAS0}$–AA3/$\overline{RAS3}$, $\overline{RD}$, $\overline{WR}$, $\overline{BB}$, $\overline{CAS}$, BCLK, and $\overline{BCLK}$. If hardware refresh of external DRAM is enabled, Port A exits the Wait mode to allow the refresh to occur and then returns to the Wait mode.

EXTERNAL ADDRESS BUS

Table 1-6 External Address Bus Signals

Signal Name	Type	State During Reset	Signal Description
A0–A23	Output	Tri-stated	**Address Bus** —When the DSP is the bus master, A0–A23 are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A0–A23 do not change state when external memory spaces are not being accessed.

EXTERNAL DATA BUS

Table 1-7 External Data Bus Signals

Signal Name	Type	State During Reset	Signal Description
D0–D23	Input/ Output	Tri-stated	**Data Bus** —When the DSP is the bus master, D0–D23 are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D0–D23 are tri-stated.

EXTERNAL BUS CONTROL

Table 1-8 External Bus Control Signals

Signal Name	Type	State During Reset	Signal Description
AA0–AA3/ $\overline{RAS0}$–$\overline{RAS3}$	Output	Tri-stated	**Address Attribute or Row Address Strobe** — When defined as AA, these signals can be used as chip selects or additional address lines. When defined as $\overline{RAS}$, these signals can be used as $\overline{RAS}$ for Dynamic Random Access Memory (DRAM) interface. These signals are tri-statable outputs with programmable polarity.
$\overline{RD}$	Output	Tri-stated	**Read Enable** —When the DSP is the bus master, $\overline{RD}$ is an active-low output that is asserted to read external memory on the data bus (D0 – D23). Otherwise, $\overline{RD}$ is tri-stated.

Table 1-8 External Bus Control Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{WR}$	Output	Tri-stated	**Write Enable** —When the DSP is the bus master, $\overline{WR}$ is an active-low output that is asserted to write external memory on the data bus (D0 – D23). Otherwise, the signals are tri-stated.
$\overline{BS}$	Output	Tri-stated	**Bus Strobe**—When the DSP is the bus master, $\overline{BS}$ is asserted for half a clock cycle at the start of a bus cycle to provide an “early bus start” signal for a bus controller. If the external bus is not used during an instruction cycle, $\overline{BS}$ remains deasserted until the next external bus cycle.
$\overline{TA}$t	Input	Ignored Input	**Transfer Acknowledge** —If the DSP56301 is the bus master and there is no external bus activity, or the DSP56301 is not the bus master, the $\overline{TA}$ input is ignored. The $\overline{TA}$ input is a Data Transfer Acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2,..., infinity) may be added to the wait states inserted by the BCR by keeping $\overline{TA}$ deasserted. In typical operation, $\overline{TA}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{TA}$ is asserted synchronous to CLKOUT. The number of wait states is determined by the $\overline{TA}$ input or by the Bus Control Register (BCR), whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. In order to use the $\overline{TA}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access can not be extended by $\overline{TA}$ deassertion, otherwise improper operation may result. $\overline{TA}$ can operate synchronously or asynchronously depending on the setting of the TAS bit in the Operating Mode Register (OMR). $\overline{TA}$ functionality may not be used while performing DRAM type accesses, otherwise improper operation may result.

Table 1-8 External Bus Control Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\mathrm{BR}}$	Output	Output (deasserted)	**Bus Request** —$\overline{\mathrm{BR}}$ is an active-low output, never tri-stated. $\overline{\mathrm{BR}}$ is asserted when the DSP requests bus mastership. $\overline{\mathrm{BR}}$ is deasserted when the DSP no longer needs the bus. $\overline{\mathrm{BR}}$ may be asserted or deasserted independent of whether the DSP56301 is a bus master or a bus slave. Bus “parking” allows $\overline{\mathrm{BR}}$ to be deasserted even though the DSP56301 is the bus master (see the description of bus “parking” in the $\overline{\mathrm{BB}}$ signal description). The Bus Request Hold (BRH) bit in the BCR allows $\overline{\mathrm{BR}}$ to be asserted under software control even though the DSP does not need the bus. $\overline{\mathrm{BR}}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{\mathrm{BR}}$ is only affected by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{\mathrm{BR}}$ is deasserted and the arbitration is reset to the bus slave state.
$\overline{\mathrm{BG}}$	Input	Ignored Input	**Bus Grant** —$\overline{\mathrm{BG}}$ is asserted by an external bus arbitration circuit when the DSP56301 becomes the next bus master. $\overline{\mathrm{BG}}$ must be asserted / deasserted synchronous to CLKOUT for proper operation. When $\overline{\mathrm{BG}}$ is asserted, the DSP56301 must wait until $\overline{\mathrm{BB}}$ is deasserted before taking bus mastership. When $\overline{\mathrm{BG}}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution.
$\overline{\mathrm{BB}}$	Input / Output	Input	**Bus Busy** —$\overline{\mathrm{BB}}$ indicates that the bus is active. $\overline{\mathrm{BB}}$ must be asserted and deasserted synchronous to CLKOUT. Only after $\overline{\mathrm{BB}}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep $\overline{\mathrm{BB}}$ asserted after ceasing bus activity regardless of whether $\overline{\mathrm{BR}}$ is asserted or deasserted. This is called “bus parking” and allows the current bus master to reuse the bus without re-arbitration until another device requires the bus. The deassertion of $\overline{\mathrm{BB}}$ is done by an “active pull-up” method (i.e., $\overline{\mathrm{BB}}$ is driven high and then released and held high by an external pull-up resistor). $\overline{\mathrm{BB}}$ requires an external pull-up resistor.

Table 1-8 External Bus Control Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{BL}}$	Output	Driven high	**Bus Lock**—$\overline{\text{BL}}$ is asserted at the start of an external divisible Read-Modify-Write (RMW) bus cycle, remains asserted between the read and write cycles, and is deasserted at the end of the write bus cycle. This provides an “early bus start” signal for the bus controller. BL may be used to “resource lock” an external multi-port memory for secure semaphore updates. Early deassertion provides an “early bus end” signal useful for external bus control. If the external bus is not used during an instruction cycle, BL remains deasserted until the next external indivisible RMW cycle. The only instructions that assert $\overline{\text{BL}}$ automatically are BSET, CLR, and BCHG when the access external memory. An operation can also assert $\overline{\text{BL}}$ by setting the BLH bit in the Bus Control Register.
$\overline{\text{CAS}}$	Output	Tri-stated	**Column Address Strobe** —When the DSP is the bus master, $\overline{\text{CAS}}$ is used by DRAM to strobe the column address. Otherwise, if the Bus Mastership Enable (BME) bit in the DRAM Control Register is cleared, the signal is tri-stated.
BCLK	Output	Tri-stated	**Bus Clock** —When the DSP is the bus master, BCLK is an active-high output that is active when the ATE bit in the OMR is set. When BCLK is active and synchronized to CLKOUT by the internal PLL, BCLK precedes CLKOUT by one-fourth of a clock cycle.
$\overline{\text{BCLK}}$	Output	Tri-stated	**Bus Clock Not**—When the DSP is the bus master, $\overline{\text{BCLK}}$ is an active-low output that is the inverse of the BCLK signal. Otherwise, the signal is tri-stated.

INTERRUPT AND MODE CONTROL

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is deasserted, these inputs are hardware interrupt request lines.

Table 1-9 Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{RESET}}$	Input	Input	**Reset—**$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. Deassertion of $\overline{\text{RESET}}$ is internally synchronized to the clock out (CLKOUT). When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. If $\overline{\text{RESET}}$ is deasserted synchronous to CLKOUT, exact start-up timing is guaranteed, allowing multiple processors to start synchronously and operate together in "lock-step." When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted after power up. This input is 5 V tolerant.
MODA	Input	Input	**Mode Select A—**MODA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input $\overline{\text{IRQA}}$ during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQA}}$	Input		**External Interrupt Request A—**$\overline{\text{IRQA}}$ is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. If $\overline{\text{IRQA}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQA}}$ to exit the Wait state. If the processor is in the Stop standby state and $\overline{\text{IRQA}}$ is asserted, the processor will exit the Stop state. These inputs are 5 V tolerant.

Table 1-9 Interrupt and Mode Control (Continued)

Signal Name	Type	State During Reset	Signal Description
MODB	Input	Input	**Mode Select B**—MODB selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input $\overline{\text{IRQB}}$ during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQB}}$	Input		**External Interrupt Request B**—$\overline{\text{IRQB}}$ is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. If $\overline{\text{IRQB}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQB}}$ to exit the Wait state. If the processor is in the Stop standby state and $\overline{\text{IRQC}}$ is asserted, the processor will exit the Stop state. These inputs are 5 V tolerant.
MODC	Input	Input	**Mode Select C**—MODC selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input $\overline{\text{IRQC}}$ during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQC}}$	Input		**External Interrupt Request C**—$\overline{\text{IRQC}}$ is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. If $\overline{\text{IRQC}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQC}}$ to exit the Wait state. If the processor is in the Stop standby state and $\overline{\text{IRQC}}$ is asserted, the processor will exit the Stop state. These inputs are 5 V tolerant.

Table 1-9 Interrupt and Mode Control (Continued)

Signal Name	Type	State During Reset	Signal Description
MODD	Input	Input	**Mode Select D—**MODD selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input $\overline{\text{IRQD}}$ during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQD}}$	Input		**External Interrupt Request D—**$\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. If $\overline{\text{IRQD}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQD}}$ to exit the Wait state. If the processor is in the Stop standby state and $\overline{\text{IRQD}}$ is asserted, the processor will exit the Stop state. These inputs are 5 V tolerant.

HOST INTERFACE (HI32)

The Host Interface (HI32) provides a fast parallel data to 32-bit port, which may be connected directly to the host bus.

The HI32 supports a variety of standard buses, and provides a glueless connection to a PCI bus and a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

Host Port Usage Considerations

Careful synchronization is required when reading multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in the following table:

Table 1-10 Host Port Usage Considerations

Action	Description
Asynchronous read of receive byte registers	When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), the host interface programmer should use interrupts or poll the Receive register Data Full (RXDF) flag which indicates that data is available. This assures that the data in the receive byte registers will be valid.
Asynchronous write to transmit byte registers	The host interface programmer should not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the Host Receive (HRX) register.
Asynchronous write to host vector	The host interface programmer should change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This will guarantee that the DSP interrupt control logic will receive a stable vector.

Host Port Configuration

The functions of the signals associated with the HI32 vary according to the programmed configuration of the interface as determined by the 24-bit DSP Control Register (DCTR). Refer to the *DSP56301 User's Manual* for detailed descriptions of this and the other configuration registers used with the HI32.

Table 1-11 Host Interface

Signal Name	**Type**	**State During Reset**	**Signal Description**
HAD0–HAD7	Input/ Output	Tri-stated	**Host Address/Data 0–7**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, these signals are lines 0–7 of the bidirectional, multiplexed Address/Data bus.
HA3–HA10	Input		**Host Address 3–10**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, these signals are lines 3–10 of the input Address bus.
PB0–PB7	Input or Output		**Port B 0–7**—When the HI32 is configured as GPIO through the DCTR, these signals are individually programmed as inputs or outputs through the HI32 Data Direction Register (DIRH). These inputs are 5 V tolerant.
HAD8–HAD15	Input/ Output	Tri-stated	**Host Address/Data 8–15**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, these signals are lines 8–15 of the bidirectional, multiplexed Address/Data bus.
HD0–HD7	Input/ Output		**Host Data 0–7**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, these signals are lines 0–7 of the bidirectional Data bus.
PB8–PB15	Input or Output		**Port B 8–15**—When the HI32 is configured as GPIO through the DCTR, these signals are individually programmed as inputs or outputs through the HI32 DIRH. These inputs are 5 V tolerant.

Table 1-11 Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
HC0–HC3/ $\overline{\mathrm{HBE0}}$–$\overline{\mathrm{HBE3}}$	Input/ Output	Tri-stated	**Command 0–3/Byte Enable 0–3**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, these signals are lines 0–7 of the bidirectional, multiplexed Address/Data bus.
HA0–HA2	Input		**Host Address 0–2**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, these signals are lines 0–2 of the input Address bus. Note: The fourth signal in this set should be connected to a pull-up resistor or directly to V_{CC} when using a non-PCI bus.
PB16–PB19	Input or Output		**Port B 16–19**—When the HI32 is configured as GPIO through the DCTR, these signals are individually programmed as inputs or outputs through the HI32 DIRH. These inputs are 5 V tolerant.
$\overline{\mathrm{HTRDY}}$	Input/ Output	Tri-stated	**Host Target Ready**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Target Ready signal.
$\overline{\mathrm{HDBEN}}$	Output		**Host Data Bus Enable**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host Data Bus Enable output.
PB20	Input or Output		**Port B 20**—When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed as an input or output through the HI32 DIRH. This input is 5 V tolerant.
$\overline{\mathrm{HIRDY}}$	Input/ Output	Tri-stated	**Host Initiator Ready**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Initiator Ready signal.
$\overline{\mathrm{HDBDR}}$	Output		**Host Data Bus Direction**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host Data Bus Direction output.
PB21	Input or Output		**Port B 21**—When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed as an input or output through the HI32 DIRH. This input is 5 V tolerant.

Table 1-11 Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{HDEVSEL}}$	Input/ Output	Tri-stated	**Host Device Select**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Device Select signal.
$\overline{\text{HSAK}}$	Output		**Host Select Acknowledge**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host Select Acknowledge output.
PB22	Input or Output		**Port B 22**—When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed as an input or output through the HI32 DIRH. This input is 5 V tolerant.
$\overline{\text{HLOCK}}$	Input/ Output	Tri-stated	**Host Lock**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Lock signal.
$\overline{\text{HBS}}$	Input		**Host Bus Strobe**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host Bus Strobe Schmitt-trigger input.
PB23	Input or Output		**Port B 23**—When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed as an input or output through the HI32 DIRH. This input is 5 V tolerant.
HPAR	Input/ Output	Tri-stated	**Host Parity**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Parity signal.
$\overline{\text{HDAK}}$	Input		**Host DMA Acknowledge**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host DMA Acknowledge Schmitt-trigger input. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.

Table 1-11 Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{HPERR}}$	Input/ Output	Tri-stated	**Host Parity Error**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Parity Error signal.
HDRQ	Output		**Host DMA Request**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host DMA Request output. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HGNT}}$	Input	Input	**Host Bus Grant**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Bus Grant signal.
HAEN	Input		**Host Address Enable**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host Address Enable output. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HREQ}}$	Output	Tri-stated	**Host Bus Request**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Bus Request signal.
HTA	Output		**Host Transfer Acknowledge**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host Data Bus Enable output. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.

Table 1-11 Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\mathrm{HSERR}}$	Output, open drain	Tri-stated	**Host System Error**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host System Error signal.
$\overline{\mathrm{HIRQ}}$	Output, open drain		**Host Interrupt Request**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host Interrupt Request output. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\mathrm{HSTOP}}$	Input/ Output	Tri-stated	**Host Stop**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Stop signal.
$\overline{\mathrm{HWR}}$/HRW	Input		**Host Write/Host Read-Write**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host Write / Host Read-Write Schmitt-trigger input. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HIDSEL	Input	Input	**Host Initialization Device Select**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Initialization Device Select signal.
$\overline{\mathrm{HRD}}$/$\overline{\mathrm{HDS}}$	Input		**Host Read/Host Data Strobe**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is Host Data Read / Host Data Strobe Schmitt-trigger input. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.

Table 1-11 Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{HFRAME}}$	Input/ Output	Tri-stated	**Host Frame**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host cycle Frame signal. **Non-PCI bus—**When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal must be connected to a pull-up resistor or directly to V_{CC}. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HCLK	Input	Input	**Host Clock**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Host Bus Clock input. **Non-PCI bus—**When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal must be connected to a pull-up resistor or directly to V_{CC}. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HAD16–HAD31 HD8–HD23	Input/ Output Input/ Output	Tri-stated	**Host Address/Data 16–31**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, these signals are lines 16–31 of the bidirectional, multiplexed Address/Data bus. **Host Data 8–23**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, these signals are lines 8–23 of the bidirectional Data bus. **Port B**—When the HI32 is configured as GPIO through the DCTR, these signals are internally disconnected. These inputs are 5 V tolerant.

Table 1-11 Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{HRST}}$	Input	Tri-stated	**Hardware Reset**—When the HI32 is programmed to interface a PCI bus and the HI function is selected, this is the Hardware Reset input.
HRST	Input		**Hardware Reset**—When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal is the Hardware Reset Schmitt-trigger input. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HINTA}}$	Output, open drain	Tri-stated	**Host Interrupt A**—When the HI function is selected, this signal is the Interrupt A open-drain output. **Port B**—When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
PVCL	Input	Input	**PCI Voltage Clamp—**When the HI32 is programmed to interface a PCI bus and the HI function is selected and the PCI bus uses a 3 V signal environment, connect this pin to V_{CC} (3.3 V) to enable the high voltage clamping required by the PCI specifications. In all other cases, including a 5 V PCI signal environment, leave the input unconnected.

ENHANCED SYNCHRONOUS SERIAL INTERFACE 0 (ESSI0)

There are two synchronous serial interfaces (ESSI0 and ESSI1) that provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals which implement the Motorola Serial Peripheral Interface (SPI).

Table 1-12 Enhanced Synchronous Serial Interface 0 (ESSI0)

Signal Name	Type	State During Reset	Signal Description
SC00	Input or Output	Input	**Serial Control 0** —The function of SC00 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal will be used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used either for Transmitter 1 output or for Serial I/O Flag 0.
PC0			**Port C 0**—The default configuration following reset is GPIO input PC0. When configured as PC0, signal direction is controlled through the Port Directions Register (PRR0). The signal can be configured as ESSI signal SC00 through the Port Control Register (PCR0). This input is 5 V tolerant.
SC01	Input/Output	Input	**Serial Control 1** —The function of this signal is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is the receiver frame sync I/O. For Synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1.
PC1	Input or Output		**Port C 1**—The default configuration following reset is GPIO input PC1. When configured as PC1, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SC01 through PCR0. This input is 5 V tolerant.

Table 1-12 Enhanced Synchronous Serial Interface 0 (ESSI0) (Continued)

Signal Name	Type	State During Reset	Signal Description
SC02	Input/Output	Input	**Serial Control Signal 2** —SC02 is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in Synchronous mode, and for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PC2	Input or Output		**Port C 2**—The default configuration following reset is GPIO input PC2. When configured as PC2, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SC02 through PCR0. This input is 5 V tolerant.
SCK0	Input/Output	Input	**Serial Clock** —SCK0 is a bidirectional Schmitt-trigger input signal providing the serial bit rate clock for the ESSI interface. The SCK0 is a clock input or output used by both the transmitter and receiver in Synchronous modes, or by the transmitter in Asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6 T (i.e., the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PC3	Input or Output		**Port C 3**—The default configuration following reset is GPIO input PC3. When configured as PC3, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SCK0 through PCR0. This input is 5 V tolerant.

Table 1-12 Enhanced Synchronous Serial Interface 0 (ESSI0) (Continued)

Signal Name	Type	State During Reset	Signal Description
SRD0 PC4	Input/Output Input or Output	Input	**Serial Receive Data** —SRD0 receives serial data and transfers the data to the ESSI receive shift register. SRD0 is an input when data is being received. **Port C 4**—The default configuration following reset is GPIO input PC4. When configured as PC4, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SRD0 through PCR0. This input is 5 V tolerant.
STD0 PC5	Input/Output Input or Output	Input	**Serial Transmit Data** —STD0 is used for transmitting data from the serial transmit shift register. STD0 is an output when data is being transmitted. **Port C 5**—The default configuration following reset is GPIO input PC5. When configured as PC5, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal STD0 through PCR0. This input is 5 V tolerant.

ENHANCED SYNCHRONOUS SERIAL INTERFACE 1 (ESSI1)

Table 1-13 Enhanced Synchronous Serial Interface 1 (ESSI1)

Signal Name	Type	State During Reset	Signal Description
SC10	Input or Output	Input	**Serial Control 0** —The function of SC10 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal will be used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used either for Transmitter 1 output or for Serial I/O Flag 0.
PD0			**Port D 0**—The default configuration following reset is GPIO input PD0. When configured as PD0, signal direction is controlled through the Port Directions Register (PRR1). The signal can be configured as an ESSI signal SC10 through the Port Control Register (PCR1). This input is 5 V tolerant.
SC11	Input/Output	Input	**Serial Control 1** —The function of this signal is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is the receiver frame sync I/O. For Synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1.
PD1	Input or Output		**Port D 1**—The default configuration following reset is GPIO input PD1. When configured as PD1, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SC11 through PCR1. This input is 5 V tolerant.

Table 1-13 Enhanced Synchronous Serial Interface 1 (ESSI1) (Continued)

Signal Name	Type	State During Reset	Signal Description
SC12	Input/Output	Input	**Serial Control Signal 2** —SC12 is used for frame sync I/O. SC12 is the frame sync for both the transmitter and receiver in Synchronous mode, and for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in Synchronous operation).
PD2	Input or Output		**Port D 2**—The default configuration following reset is GPIO input PD2. When configured as PD2, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SC12 through PCR1. This input is 5 V tolerant.
SCK1	Input/Output	Input	**Serial Clock** —SCK1 is a bidirectional Schmitt-trigger input signal providing the serial bit rate clock for the ESSI interface. The SCK1 is a clock input or output used by both the transmitter and receiver in Synchronous modes, or by the transmitter in Asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6 T (i.e., the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SCK1 through PCR1. This input is 5 V tolerant.

Table 1-13 Enhanced Synchronous Serial Interface 1 (ESSI1) (Continued)

Signal Name	Type	State During Reset	Signal Description
SRD1	Input/Output	Input	**Serial Receive Data** —SRD1 receives serial data and transfers the data to the ESSI receive shift register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SRD1 through PCR1. This input is 5 V tolerant.
STD1	Input/Output	Input	**Serial Transmit Data** —STD1 is used for transmitting data from the serial transmit shift register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal STD1 through PCR1. This input is 5 V tolerant.

SERIAL COMMUNICATION INTERFACE (SCI)

The Serial Communication interface (SCI) provides a full duplex port for serial communication to other DSPs, microprocessors, or peripherals such as modems.

Table 1-14 Serial Communication Interface (SCI)

Signal Name	Type	State During Reset	Signal Description
RXD	Input	Input	**Serial Receive Data** —This input receives byte oriented serial data and transfers it to the SCI receive shift register.
PE0	Input or Output		**Port E 0**—The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the SCI Port Directions Register (PRR). The signal can be configured as an SCI signal RXD through the SCI Port Control Register (PCR). This input is 5 V tolerant.
TXD	Output	Input	**Serial Transmit Data** —This signal transmits data from SCI transmit data register.
PE1	Input or Output		**Port E 1**—The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal TXD through the SCI PCR. This input is 5 V tolerant.
SCLK	Input/Output	Input	**Serial Clock** —This is the bidirectional Schmitt-trigger input signal providing the input or output clock used by the transmitter and/or the receiver.
PE2	Input or Output		**Port E 2**—The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal SCLK through the SCI PCR. This input is 5 V tolerant.

TIMERS

Three identical and independent timers are implemented in the DSP56301. Each timer can use internal or external clocking, and can interrupt the DSP56301 after a specified number of events (clocks), or can signal an external device after counting a specific number of internal events.

Table 1-15 Triple Timer Signals

Signal Name	Type	State During Reset	Signal Description
TIO0	Input or Output	Input	**Timer 0 Schmitt-Trigger Input/Output** —When Timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When Timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input / Output through the Timer 0 Control / Status Register (TCSR0). This input is 5 V tolerant.
TIO1	Input or Output	Input	**Timer 1 Schmitt-Trigger Input/Output** —When Timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When Timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input / Output through the Timer 1 Control / Status Register (TCSR1). This input is 5 V tolerant.
TIO2	Input or Output	Input	**Timer 2 Schmitt-Trigger Input/Output** —When Timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When Timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input / Output through the Timer 2 Control / Status Register (TCSR2). This input is 5 V tolerant.

JTAG/ONCE INTERFACE

Table 1-16 JTAG / OnCE Interface

Signal Name	Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock** —TCK is a test clock input signal used to synchronize the JTAG test logic. This input is 5 V tolerant.
TDI	Input	Input	**Test Data Input** —TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 5 V tolerant.
TDO	Output	Tri-stated	**Test Data Output** —TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select** —TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 5 V tolerant.
$\overline{\text{TRST}}$	Input	Input	**Test Reset** —$\overline{\text{TRST}}$ is an active-low Schmitt-trigger input signal used to asynchronously initialize the test controller. $\overline{\text{TRST}}$ has an internal pull-up resistor. $\overline{\text{TRST}}$ must be asserted after power up. This input is 5 V tolerant.

Table 1-16 JTAG / OnCE Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\mathrm{DE}}$	Input/Output	Input	**Debug Event** —$\overline{\mathrm{DE}}$ is an open-drain bidirectional active-low signal providing, as an input, a means of entering the Debug mode of operation from an external command controller, and, as an output, a means of acknowledging that the chip has entered the Debug mode. This signal, when asserted as an input, causes the DSP56300 core to finish the current instruction being executed, save the instruction pipeline information, enter the Debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters the Debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{\mathrm{DE}}$ has an internal pull-up resistor. This is not a standard part of the JTAG Test Access Port (TAP) Controller. The signal connects directly to the OnCE module to initiate Debug mode directly or to provide a direct external indication that the chip has entered the Debug mode. All other interface with the OnCE module must occur through the JTAG port. This input is 5 V tolerant.

SECTION 2

SPECIFICATIONS

INTRODUCTION

The DSP56301 is fabricated in high density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs. The DSP56301 specifications are preliminary and are from design simulations, and may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after full characterization and device qualifications are complete.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CC}	–0.3 to +4.0	V
All input voltages excluding “5 V tolerant” inputs[3]	V_{IN}	GND – 0.3 to V_{CC} + 0.3	V
All “5 V tolerant” input voltages[3]	V_{IN5}	GND – 0.3 to V_{CC} + 3.95	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_J	–40 to +100	°C
Storage temperature	T_{STG}	–55 to +150	°C

Notes:
1. GND = 0 V, V_{CC} = 3.3 V ± 0.3 V, T_J = –40°C to +100°C, CL = 50 pF + 2 TTL Loads
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. **CAUTION**: All “5 V Tolerant” input voltages cannot be more than 3.95 V greater than the supply voltage; this restriction applies to “power on”, as well as during normal operation. In any case, the input voltages can not be more than 5.75 V. “5 V Tolerant” inputs are inputs that tolerate 5 V.

THERMAL CHARACTERISTICS

Table 2-2 Thermal Characteristics

Characteristic	Symbol	TQFP Value	PBGA[3] Value	PBGA[4] Value	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	49.5	48.4	25.2	°C / W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	7.2	9	—	°C / W
Thermal characterization parameter	Ψ_{JT}	4.7	5	—	°C / W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111)
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are simulated values. Test board has 2-ounce copper traces routed to the outer row of balls.
4. These are simulated values. The test board has two, 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.

DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics[6]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage • D(0:23), $\overline{\text{BG}}$, $\overline{\text{BB}}$, $\overline{\text{TA}}$, $\overline{\text{BL}}$ • MOD[1] / $\overline{\text{IRQ}}$[1], $\overline{\text{RESET}}$, PINIT / $\overline{\text{NMI}}$ and all JTAG / ESSI / SCI / Timer / HI08 pins • EXTAL[8]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 $0.8 \times V_{CC}$	 — — —	 V_{CC} $V_{CC} + 3.95$ V_{CC}	 V V V
Input low voltage • D(0:23), $\overline{\text{BG}}$, $\overline{\text{BB}}$, $\overline{\text{TA}}$, $\overline{\text{BL}}$, MOD[1] / $\overline{\text{IRQ}}$[1], $\overline{\text{RESET}}$, PINIT • All JTAG / ESSI / SCI / Timer / HI08 pins • EXTAL[8]	 V_{IL} V_{ILP} V_{ILX}	 – 0.3 – 0.3 – 0.3	 — — —	 0.8 0.8 $0.2 \times V_{CC}$	 V V V
Input leakage current	I_{IN}	– 10	—	10	μA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	– 10	—	10	μA
Output high voltage • TTL ($I_{OH} = -0.4$ mA)[5,7] • CMOS ($I_{OH} = -10$ μA)[5]	V_{OH}	 $V_{CC} - 0.4$ $V_{CC} - 0.01$	 — —	 — —	 V V
Output low voltage • TTL ($I_{OL} = 3.0$ mA, open-drain pins $I_{OL} = 6.7$ mA)[5,7] • CMOS ($I_{OL} = 10$ μA)[5]	V_{OL}	 — —	 — —	 0.4 0.01	 V V
Internal supply current[2]: • In Normal mode	I_{CCI}	—	**66 MHz**: 84 **80 MHz**: 102 **100 MHz:** 127	**66 MHz**: 120 **80 MHz**: 145 **100 MHz:** 181	mA mA mA
• In Wait mode[3]	I_{CCW}	—	**66 MHz**: 5 **80 MHz**: 6 **100 MHz: 7.5**	**66 MHz**: 7 **80 MHz**: 9 **100 MHz**: 11	mA mA mA
• In Stop mode[4]	I_{CCS}	—	**66 MHz**: 100 **80 MHz**: 100 **100 MHz:** 100	**66 MHz**: 150 **80 MHz**: 150 **100 MHz:** 150	μA μA μA

Table 2-3 DC Electrical Characteristics[6] (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
PLL supply current		—	1	2.5	mA
Input capacitance[5]	C_{IN}	—	—	10	pF

Notes:
1. Refers to MODA / $\overline{\text{IRQA}}$, MODB / $\overline{\text{IRQB}}$, MODC / $\overline{\text{IRQC}}$, and MODD / $\overline{\text{IRQD}}$ pins
2. **Power Consumption Considerations** on page 4-4 provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with $V_{CC} = 3.0$ V at $T_J = 100°C$. Maximum internal supply current is measured with $V_{CC} = 3.6$ V at $T_J = 100°C$.
3. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). PLL and XTAL signals are disabled during Stop state.
4. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).
5. Periodically sampled and not 100% tested
6. $V_{CC} = 3.3$ V ± 0.3 V; $T_J = –40°C$ to +100 °C, $C_L = 50$ pF + 2 TTL Loads
7. This characteristic does not apply to XTAL and PCAP.
8. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than $0.9 \times V_{CC}$ and the maximum V_{ILX} should be no higher than $0.1 \times V_{CC}$.

AC ELECTRICAL CHARACTERISTICS

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in **Note 6** of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56301 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.

INTERNAL CLOCKS

Table 2-4 Internal Clocks, CLKOUT

Characteristics	**Symbol**	**Expression[1, 2]**		
		Min	**Typ**	**Max**
Internal operation frequency and CLKOUT with PLL enabled	f	—	(Ef × MF) / (PDF × DF)	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef / 2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	— $0.49 \times ET_C \times PDF \times DF / MF$ $0.47 \times ET_C \times PDF \times DF / MF$	ET_C — —	— $0.51 \times ET_C \times PDF \times DF / MF$ $0.53 \times ET_C \times PDF \times DF / MF$
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	— $0.49 \times ET_C \times PDF \times DF / MF$ $0.47 \times ET_C \times PDF \times DF / MF$	ET_C — —	— $0.51 \times ET_C \times PDF \times DF / MF$ $0.53 \times ET_C \times PDF \times DF / MF$
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	$ET_C \times PDF \times DF / MF$	—
Internal clock and CLKOUT cycle time with PLL disabled	T_C	—	$2 \times ET_C$	—
Instruction cycle time	I_{CYC}	—	T_C	—

Notes: 1. DF = Division Factor
Ef = External frequency
ET_C = External clock cycle
MF = Multiplication Factor
PDF = Predivision Factor
T_C = internal clock cycle
2. See the **PLL and Clock Generation** section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

EXTERNAL CLOCK OPERATION

The DSP56301 system clock may be derived from the on–chip crystal oscillator, as shown in **Figure 1** on the cover page, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, leaving XTAL physically not connected to the board or socket.

Fundamental Frequency Fork Crystal Oscillator

Fundamental Frequency Crystal Oscillator

Suggested Component Values:

f_{OSC} = 32.768 kHz
R1 = 3.9 MΩ ± 10%
C = 22 pF ± 20%
R2 = 200 kΩ ± 10%

Calculations were done for a 32.768 kHz crystal with the following parameters:
a load capacitance (C_L) of 12.5 pF,
a shunt capacitance (C_0) of 1.8 pF,
a series resistance of 40 kΩ, and
a drive level of 1 µW.

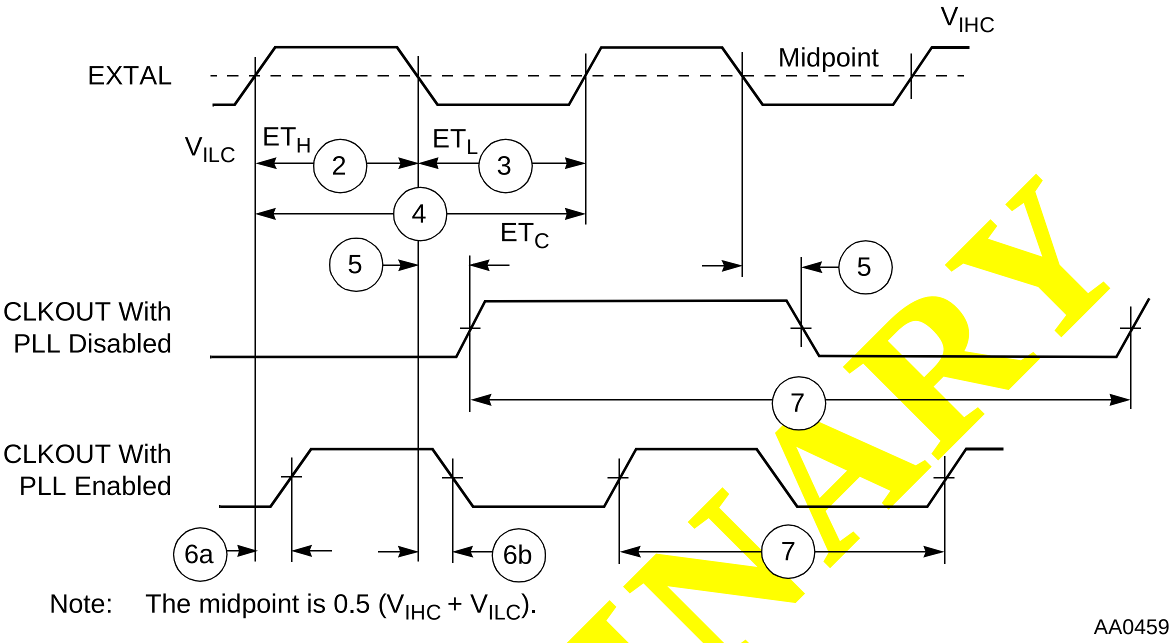
Suggested Component Values:

f_{OSC} = 4 MHz	f_{OSC} = 20 MHz
R = 680 kΩ ± 10%	R = 680 kΩ ± 10%
C = 56 pF ± 20%	C = 22 pF ± 20%

Calculations were done for a 4/20 MHz crystal with the following parameters:
a $C_L$of 30/20 pF,
a C_0 of 7/6 pF,
a series resistance of 100/20 Ω, and
a drive level of 2 mW.

AA1071

Figure 2-1 Crystal Oscillator Circuits



Note: The midpoint is 0.5 ($V_{IHC} + V_{ILC}$).

Figure 2-2 External Clock Timing

Table 2-5 Clock Operation

No.	Characteristics	Symbol	66 MHz		80 MHz		100 MHz	
			Min	**Max**	**Min**	**Max**	**Min**	**Max**
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	66.0	0	80.0	0	100.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_H	7.08 ns 6.44 ns	∞ 157.0 µs	5.84 ns 5.31 ns	∞ 157.0 µs	4.67 ns 4.25 ns	∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_L	7.08 ns 6.44 ns	∞ 157.0 µs	5.84 ns 5.31 ns	∞ 157.0 µs	4.67 ns 4.25 ns	∞ 157.0 µs

Table 2-5 Clock Operation (Continued)

No.	Characteristics	Symbol	66 MHz		80 MHz		100 MHz	
			Min	**Max**	**Min**	**Max**	**Min**	**Max**
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	15.15 ns 15.15 ns	∞ 273.1 µs	12.50 ns 12.50 ns	∞ 273.1 µs	10.00 ns 10.00 ns	∞ 273.1 µs
5	CLKOUT change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns	4.3 ns	11.0 ns	4.3 ns	11.0 ns
6	CLKOUT rising edge from EXTAL rising edge with PLL enabled (MF = 1, PDF = 1, Ef > 15 MHz)[3,5]		0.0 ns	1.8 ns	0.0 ns	1.8 ns	0.0 ns	1.8 ns
	CLKOUT falling edge from EXTAL rising edge with PLL enabled (MF = 2 or 4, PDF = 1, Ef > 15 MHz)[3,5]		0.0 ns	1.8 ns	0.0 ns	1.8 ns	0.0 ns	1.8 ns
	CLKOUT falling edge from EXTAL falling edge with PLL enabled (MF ≤ 4, PDF ≠ 1, Ef / PDF > 15 MHz)[3,5]		0.0 ns	1.8 ns	0.0 ns	1.8 ns	0.0 ns	1.8 ns
7	Instruction cycle time = $I_{CYC} = T_C$[4] (See **Table 2-4**.) (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	30.3 ns 15.15 ns	∞ 8.53 µs	25.0 ns 12.50 ns	∞ 8.53 µs	20.0 ns 10.00 ns	∞ 8.53 µs

Notes:
1. Measured at 50% of the input transition
2. The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.
3. Periodically sampled and not 100% tested
4. The maximum value for PLL enabled is given for minimum V_{CO} and maximum DF.
5. The skew is not guaranteed for any other MF value.
6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

PHASE LOCK LOOP (PLL) CHARACTERISTICS

Table 2-6 PLL Characteristics

Characteristics	66 MHz		80 MHz		100 MHz		Unit
	Min	Max	Min	Max	Min	Max	
V_{CO} frequency when PLL enabled ($MF \times E_f \times 2 / PDF$)	30	132	30	160	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1])							
• @ $MF \leq 4$	$(MF \times 425) - 125$	$(MF \times 590) - 175$	$(MF \times 425) - 125$	$(MF \times 590) - 175$	$(MF \times 425) - 125$	$(MF \times 590) - 175$	pF
• @ $MF > 4$	$MF \times 520$	$MF \times 920$	$MF \times 520$	$MF \times 920$	$MF \times 520$	$MF \times 920$	pF

Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:

$(500 \times MF) - 150$, for $MF \leq 4$, or

$690 \times MF$, for $MF > 4$.

RESET, STOP, MODE SELECT, ND INTERRUPT TIMING

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6]

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26.0	—	26.0	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[4]								
	• Power on, external clock generator, PLL disabled	50 × ET_C	760.0	—	625.0	—	500.0	—	ns
	• Power on, external clock generator, PLL enabled	1000 × ET_C	15.2	—	12.5	—	10.0	—	µs
	• Power on, internal oscillator	75000 × ET_C	1.14	—	1.0	—	0.75	—	ms
	• During STOP, XTAL disabled (PCTL Bit 16 = 0)	75000 × ET_C	1.14	—	1.0	—	0.75	—	ms
	• During STOP, XTAL enabled (PCTL Bit 16 = 1)	2.5 × T_C	38.0	—	31.3	—	25.0	—	ns
	• During normal operation	2.5 × T_C	38.0	—	31.3	—	25.0	—	ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5]								
	• Minimum	**66 MHz**: 3.25 × T_C + 2.0	51.0	—	—	—	—	—	ns
		80 MHz: 3.25 × T_C + 2.0	—	—	42.6	—	—	—	ns
		100 MHz: 3.25 × T_C + 2.0	—	—	—	—	34.5	—	ns
	• Maximum	**66 MHz**: 20.25 T_C + 11.0	—	318.0	—	—	—	—	ns
		80 MHz: 20.25 T_C + 9.95	—	—	—	263.1	—	—	ns
		100 MHz: 20.25 T_C + 7.50	—	—	—	—	—	211.5	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
11	Synchronous reset setup time from $\overline{\text{RESET}}$ deassertion to CLKOUT Transition 1 • Minimum • Maximum	T_C	9.0 —	— 15.2	7.4 —	— 12.5	5.9 —	— 10.0	ns ns
12	Synchronous reset deasserted, delay time from the CLKOUT Transition 1 to the first external address output • Minimum • Maximum	$3.25 \times T_C + 1.0$ $20.25\ T_C + 5.0$	50.0 —	— 312.0	41.6 —	— 258.1	33.5 —	— 207.5	ns ns
13	Mode select setup time		30.0	—	30.0	—	30.0	—	ns
14	Mode select hold time		0.0	—	0.0	—	0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		10.0	—	8.25	—	6.6	—	ns
16	Minimum edge-triggered interrupt request deassertion width		10.0	—	8.25	—	6.6	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, NMI assertion to external memory access address out valid • Caused by first interrupt instruction fetch • Caused by first interrupt instruction execution	$4.25 \times T_C + 2.0$ $7.25 \times T_C + 2.0$	66.0 112.0	— —	55.1 92.6	— —	44.5 74.5	— —	ns ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, NMI assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	157.0	—	130.0	—	105.0	—	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1]	**66 MHz[8]**: $3.75 \times T_C + WS \times T_C - 14$ **80 MHz[8]**: $3.75 \times T_C + WS \times T_C - 12.4$ **100 MHz[8]**: $3.75 \times T_C + WS \times T_C - 10.94$	—		—		—		ns ns ns
20	Delay from $\overline{RD}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1]	**66 MHz[8]**: $3.25 \times T_C + WS \times T_C - 14$ **80 MHz[8]**: $3.25 \times T_C + WS \times T_C - 12.4$ **100 MHz[8]**: $3.25 \times T_C + WS \times T_C - 10.94$	—		—		—		ns ns ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
21	Delay from $\overline{\text{WR}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1] • DRAM for all WS	**66 MHz**[8]: $(WS + 3.5) \times T_C - 14$	—						ns
		80 MHz[8]: $(WS + 3.5) \times T_C - 12.4$			—				ns
		100 MHz[8]: $(WS + 3.5) \times T_C - 10.94$					—		ns
	• SRAM WS = 1	**66 MHz**[8]: $(WS + 3.5) \times T_C - 14$	—						ns
		80 MHz[8]: $(WS + 3.5) \times T_C - 12.4$			—				ns
		100 MHz[8]: $(WS + 3.5) \times T_C - 10.94$					—		ns
	• SRAM WS = 2, 3	**66 MHz**[8]: $(WS + 3) \times T_C - 14$	—						ns
		80 MHz[8]: $(WS + 3) \times T_C - 12.4$			—				ns
		100 MHz[8]: $(WS + 3) \times T_C - 10.94$					—		ns
	• SRAM WS ≥ 4	**66 MHz**[8]: $(WS + 2.5) \times T_C - 14$	—						ns
		80 MHz[8]: $(WS + 2.5) \times T_C - 12.4$			—				ns
		100 MHz[8]: $(WS + 2.5) \times T_C - 10.94$					—		ns
22	Synchronous interrupt setup time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to the CLKOUT Transition 2		9.0	T_C	7.4	T_C	5.9	T_C	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
23	Synchronous interrupt delay time from the CLKOUT Transition 2 to the first external address output valid caused by the first instruction fetch after coming out of Wait Processing state • Minimum • Maximum	 $9.25 \times T_C + 1.0$ $24.75 \times T_C + 5.0$	 141.0 —	 — 380.0	 116.6 —	 — 314.4	 93.5 —	 — 252.5	 ns ns
24	Duration for $\overline{\text{IRQA}}$ assertion to recover from Stop state		9.0	—	7.4	—	5.9	—	ns
25	Delay from $\overline{\text{IRQA}}$ assertion to fetch of first instruction (when exiting Stop)[2, 3]								
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128\ K - PLC/2) \times T_C$	2.0	64.1	1.6	17.0	1.3	13.6	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$	352.3 ns	62.1 ms	290.6 ns	15.4 ms	232.5 ns	12.3 ms	
	• PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)	$(8.25 \pm 0.5) \times T_C$	117.4	132.6	96.9	109.4	77.5	87.5	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
26	Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[2, 3]								
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$	64.1	—	17.0	—	13.6	—	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$	62.1	—	15.4	—	12.3	—	ms
	• PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay)	$5.5 \times T_C$	83.4	—	68.8	—	55.0	—	ns
27	Interrupt Requests Rate								
	• HI08, ESSI, SCI, Timer	$12T_C$	—	181.8	—	150.0	—	120.0	ns
	• DMA	$8T_C$	—	121.2	—	100.0	—	80.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$8T_C$	—	121.2	—	100.0	—	80.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (level trigger)	$12T_C$	—	181.8	—	150.0	—	120.0	ns
28	DMA Requests Rate								
	• Data read from HI08, ESSI, SCI	$6T_C$	—	90.9	—	75.0	—	60.0	ns
	• Data write to HI08, ESSI, SCI	$7T_C$	—	106.1	—	87.5	—	70.0	ns
	• Timer	$2T_C$	—	30.3	—	25.0	—	20.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$3T_C$	—	45.5	—	37.5	—	30.0	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing^6 (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
29	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory (DMA source) access address out valid	$4.25 \times T_C + 2.0$	66.0	—	55.1	—	44.0	—	ns

Notes:

1. When using fast interrupts and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. This timing depends on several settings:

   For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure the oscillator is stable before executing programs. In that case, resetting the Stop delay (OMR Bit 6 = 0) will provide the proper delay. While it is possible to set OMR Bit 6 = 1, it is not recommended and these specifications do not guarantee timings for that case.

   For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery time will be minimal (OMR Bit 6 setting is ignored).

   For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the PCTL Bit 17 and OMR Bit 6 settings.

   For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery will end when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.

   PLC value for PLL disable is 0.

   The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (i.e., for 66 MHz it is 4096 / 66 MHz = 62 µs). During the stabilization period, T_C, T_H, and T_L will not be constant, and their width may vary, so timing may vary as well.
3. Periodically sampled and not 100% tested

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	

4. For an external clock generator, $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.

   For internal oscillator, $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.

   When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
5. If PLL does not lose lock
6. $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = –40°C$ to $+100°C$, $C_L = 50\ pF$ + 2 TTL Loads
7. WS = number of wait states (measured in clock cycles, number of T_C)
8. Use expression to compute maximum value.

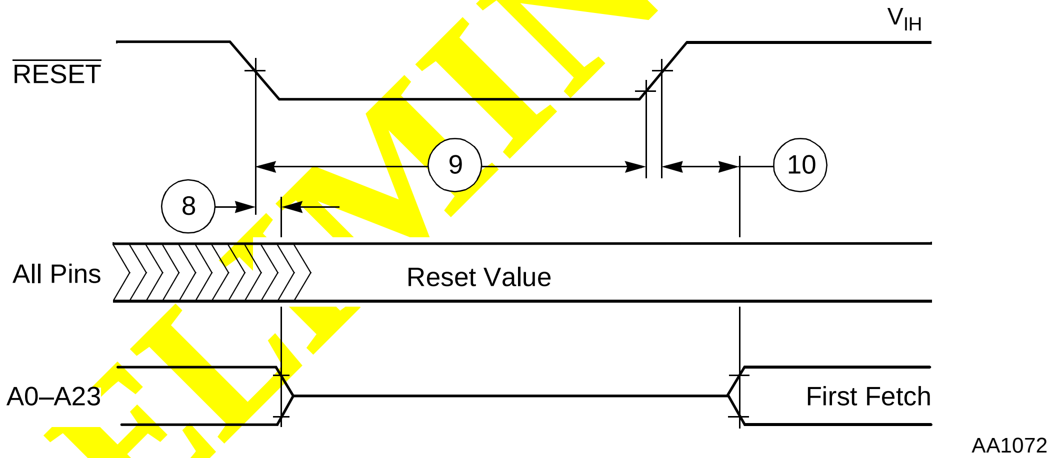


Figure 2-3 Reset Timing

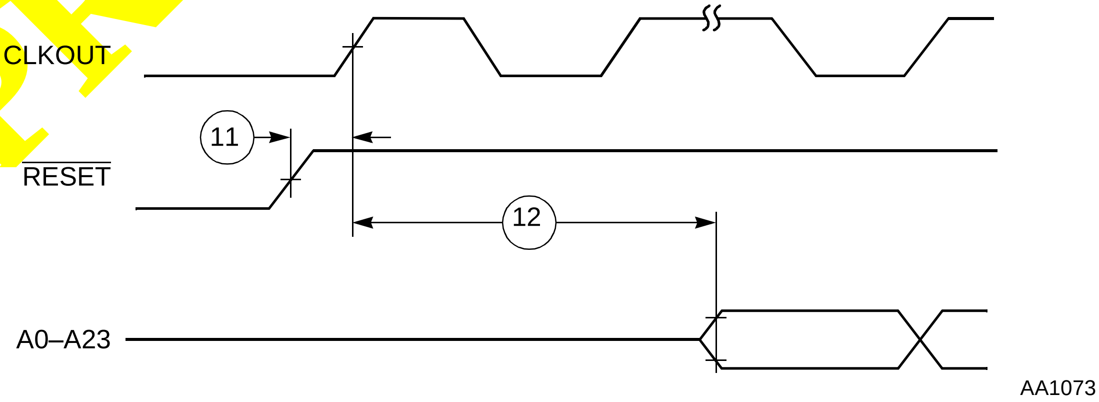
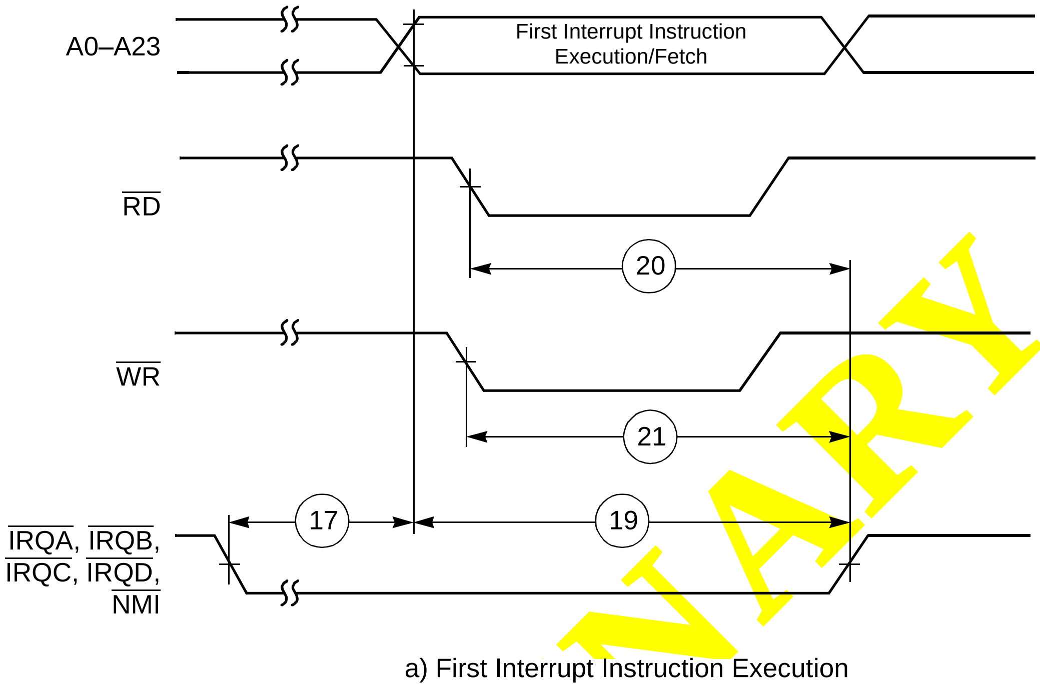
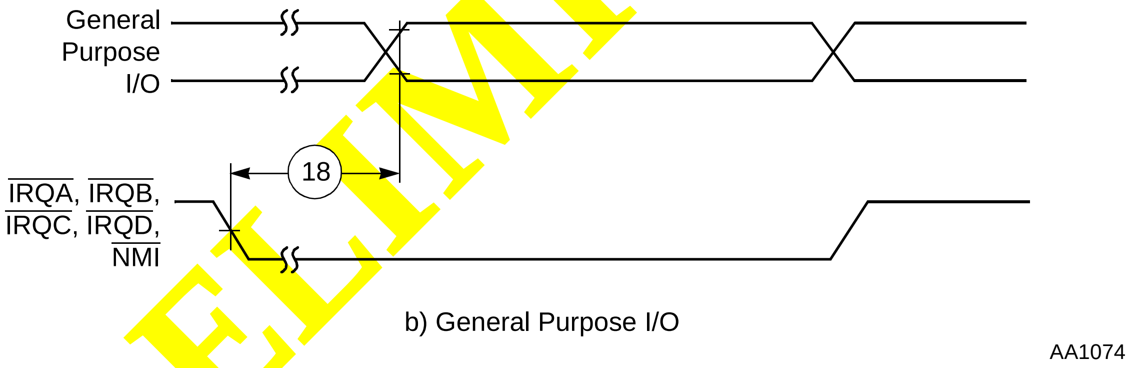


Figure 2-4 Synchronous Reset Timing



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 2-5 External Fast Interrupt Timing

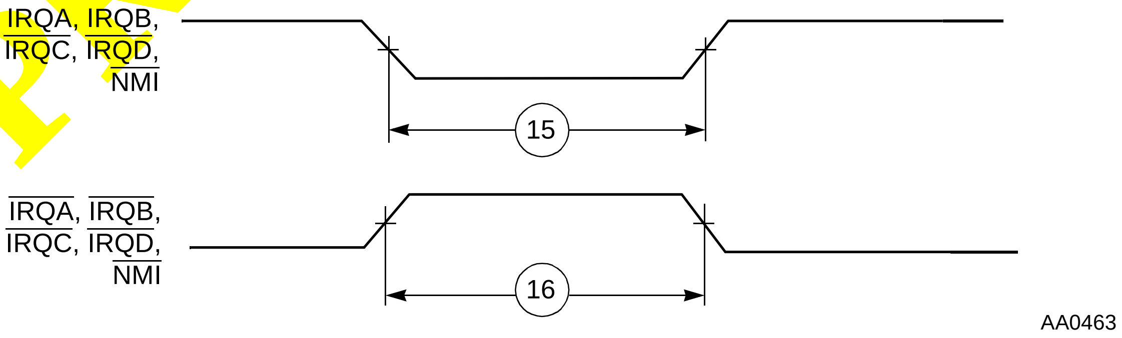


Figure 2-6 External Interrupt Timing (Negative Edge-Triggered)

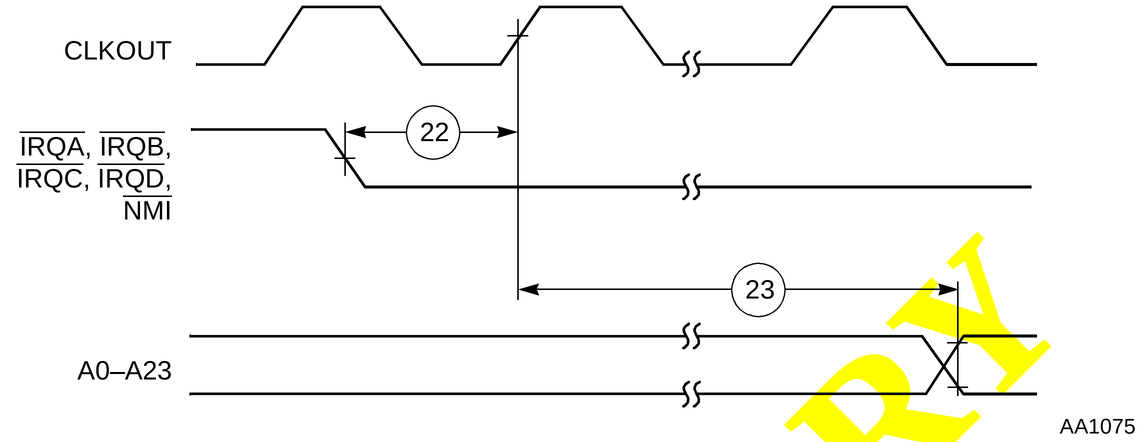


Figure 2-7 Synchronous Interrupt from Wait State Timing

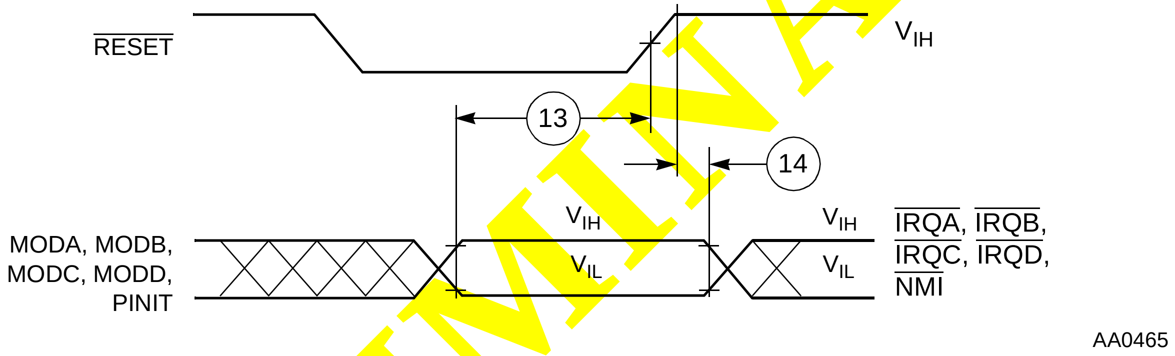


Figure 2-8 Operating Mode Select Timing

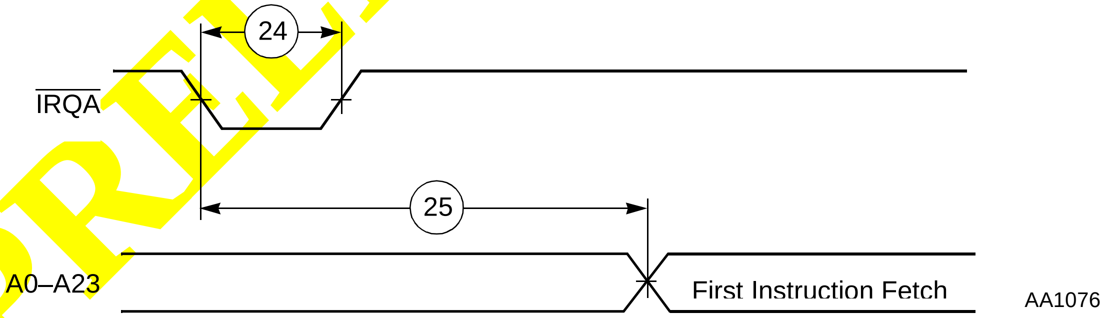


Figure 2-9 Recovery from Stop State Using $\overline{\text{IRQA}}$

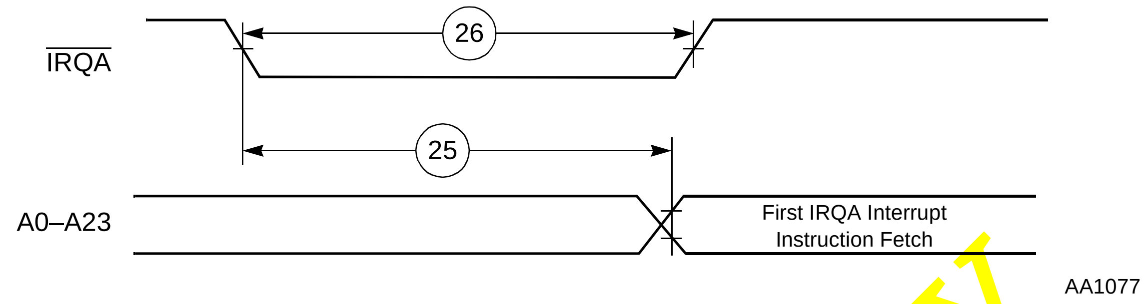


Figure 2-10 Recovery from Stop State Using IRQA Interrupt Service

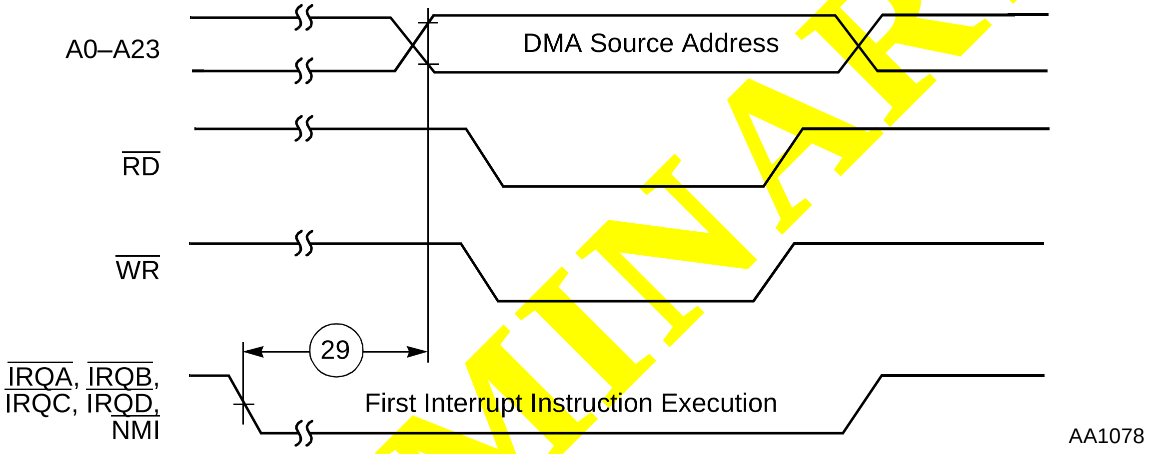


Figure 2-11 External Memory Access (DMA Source) Timing

EXTERNAL MEMORY EXPANSION PORT (PORT A)

SRAM Timing

Table 2-8 SRAM Read and Write Accesses

No.	Characteristics	Symbol	Expression[1]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
100	Address valid and AA assertion pulse width	t_{RC}, t_{WC}	$(WS + 1) \times T_C - 4.0$ $[1 \le WS \le 3]$	26.3	—	21.0	—	16.0	—	ns
			$(WS + 2) \times T_C - 4.0$ $[4 \le WS \le 7]$	86.9	—	71.0	—	56.0	—	ns
			$(WS + 3) \times T_C - 4.0$ $[WS \ge 8]$	162.7	—	133.5	—	106.0	—	ns
101	Address and AA valid to $\overline{\text{WR}}$ assertion	t_{AS}	**66 MHz:** $0.25 \times T_C - 3.7$ $[WS = 1]$	0.1	—	—	—	—	—	ns
			80 MHz: $0.25 \times T_C - 3.0$ $[WS = 1]$	—	—	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$ $[WS = 1]$	—	—	—	—	0.1	—	ns
			All frequencies: $0.75 \times T_C - 4.0$ $[2 \le WS \le 3]$	7.4	—	5.4	—	3.5	—	ns
			$1.25 \times T_C - 4.0$ $[WS \ge 4]$	14.9	—	11.6	—	8.5	—	ns
102	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.5$ $[WS = 1]$	18.2	—	14.3	—	10.5	—	ns
			$WS \times T_C - 4.0$ $[2 \le WS \le 3]$	26.3	—	21.0	—	16.0	—	ns
			$(WS - 0.5) \times T_C - 4.0$ $[WS \ge 4]$	49.0	—	39.8	—	31.0	—	ns

Table 2-8 SRAM Read and Write Accesses (Continued)

No.	Characteristics	Symbol	Expression[1]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	**66 MHz:** $0.25 \times T_C - 3.8$ $[1 \le WS \le 3]$	0.1	—	—	—	—	—	ns
			80 MHz: $0.25 \times T_C - 3.0$ $[1 \le WS \le 3]$	—	—	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$ $[1 \le WS \le 3]$	—	—	—	—	0.1	—	ns
			All frequencies: $1.25 \times T_C - 4.0$ $[4 \le WS \le 7]$	14.9	—	11.6	—	8.5	—	ns
			$2.25 \times T_C - 4.0$ $[WS \ge 8]$	30.1	—	24.1	—	18.5	—	ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	**66 MHz:** $(WS + 0.75) \times T_C - 11.0$ $[WS \ge 1]$	—	15.5	—	—	—	—	ns
			80 MHz: $(WS + 0.75) \times T_C - 9.5$ $[WS \ge 1]$	—	—	—	12.4	—	—	ns
			100 MHz: $(WS + 0.75) \times T_C - 8.0$ $[WS \ge 1]$	—	—	—	—	—	9.5	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	**66 MHz:** $(WS + 0.25) \times T_C - 11.0$ $[WS \ge 1]$	—	7.9	—	—	—	—	ns
			80 MHz: $(WS + 0.25) \times T_C - 9.5$ $[WS \ge 1]$	—	—	—	6.1	—	—	ns
			100 MHz: $(WS + 0.25) \times T_C - 8.0$ $[WS \ge 1]$	—	—	—	—	—	4.5	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	0.0	—	0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion	t_{AW}	$(WS + 0.75) \times T_C - 4.0$ $[WS \ge 1]$	22.5	—	17.9	—	13.5	—	ns

Table 2-8 SRAM Read and Write Accesses (Continued)

No.	Characteristics	Symbol	Expression[1]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
108	Data valid to $\overline{\text{WR}}$ deassertion (data setup time)	t_{DS} (t_{DW})	**66 MHz:** $(WS - 0.25) \times T_C - 3.9$ $[WS \geq 1]$	7.5	—	—	—	—	—	ns
			80 MHz: $(WS - 0.25) \times T_C - 3.3$ $[WS \geq 1]$	—	—	6.1	—	—	—	ns
			100 MHz: $(WS - 0.25) \times T_C - 2.75$ $[WS \geq 1]$	—	—	—	—	4.8	—	ns
109	Data hold time from $\overline{\text{WR}}$ deassertion	t_{DH}	**66 MHz:** $0.25 \times T_C - 3.7$ $[1 \leq WS \leq 3]$	0.1	—	—	—	—	—	ns
			80 MHz: $0.25 \times T_C - 3.0$ $[1 \leq WS \leq 3]$	—	—	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$ $[1 \leq WS \leq 3]$	—	—	—	—	0.1	—	ns
			All frequencies: $1.25 \times T_C - 3.8$ $[4 \leq WS \leq 7]$	15.2	—	11.8	—	8.7	—	ns
			$2.25 \times T_C - 3.8$ $[WS \geq 8]$	30.4	—	24.3	—	18.7	—	ns
110	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 3.7$ $[WS = 1]$	7.7	—	5.7	—	3.8	—	ns
			$0.25 \times T_C - 3.7$ $[2 \leq WS \leq 3]$	0.1	—	–0.6	—	–1.2	—	ns
			$-0.25 \times T_C - 3.7$ $[WS \geq 4]$	–7.5	—	–6.8	—	–6.2	—	ns
111	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C + 0.2$ $[1 \leq WS \leq 3]$	—	4.0	—	3.3	—	2.7	ns
			$1.25 \times T_C + 0.2$ $[4 \leq WS \leq 7]$	—	19.1	—	15.8	—	12.7	ns
			$2.25 \times T_C + 0.2$ $[WS \geq 8]$	—	34.3	—	28.3	—	22.7	ns
112	Previous $\overline{\text{RD}}$ deassertion to data active (write)		$1.25 \times T_C - 4.0$ $[1 \leq WS \leq 3]$	14.9	—	11.6	—	8.5	—	ns
			$2.25 \times T_C - 4.0$ $[4 \leq WS \leq 7]$	30.1	—	24.1	—	18.5	—	ns
			$3.25 \times T_C - 4.0$ $[WS \geq 8]$	45.2	—	36.6	—	28.5	—	ns

Table 2-8 SRAM Read and Write Accesses (Continued)

No.	Characteristics	Symbol	Expression[1]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
113	$\overline{\text{RD}}$ deassertion time		$0.75 \times T_C - 4.0$ [1 ≤ WS ≤ 3]	7.4	—	5.4	—	3.5	—	ns
			$1.75 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	22.5	—	17.9	—	13.5	—	ns
			$2.75 \times T_C - 4.0$ [WS ≥ 8]	37.7	—	30.4	—	23.5	—	ns
114	$\overline{\text{WR}}$ deassertion time		$0.5 \times T_C - 3.5$ [WS = 1]	4.1	—	2.8	—	1.5	—	ns
			$T_C - 3.5$ [2 ≤ WS ≤ 3]	11.7	—	9.0	—	6.5	—	ns
			$2.5 \times T_C - 3.5$ [4 ≤ WS ≤ 7]	34.4	—	27.8	—	21.5	—	ns
			$3.5 \times T_C - 3.5$ [WS ≥ 8]	49.5	—	40.3	—	31.5	—	ns
115	Address valid to $\overline{\text{RD}}$ assertion		$0.5 \times T_C - 4$	3.5	—	2.3	—	1.0	—	ns
116	$\overline{\text{RD}}$ assertion pulse width		$(WS + 0.25) \times T_C - 3.8$	15.1	—	11.8	—	8.7	—	ns
117	$\overline{\text{RD}}$ deassertion to address not valid		$0.25 \times T_C - 3.0$ [1 ≤ WS ≤ 3]	0.7	—	0.1	—	0.0	—	ns
			$1.25 \times T_C - 3.0$ [4 ≤ WS ≤ 7]	15.9	—	12.6	—	9.5	—	ns
			$2.25 \times T_C - 3.0$ [WS ≥ 8]	31.0	—	25.1	—	19.5	—	ns

Notes:
1. WS is the number of wait states specified in the BCR.
2. $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF + 2$ TTL Loads

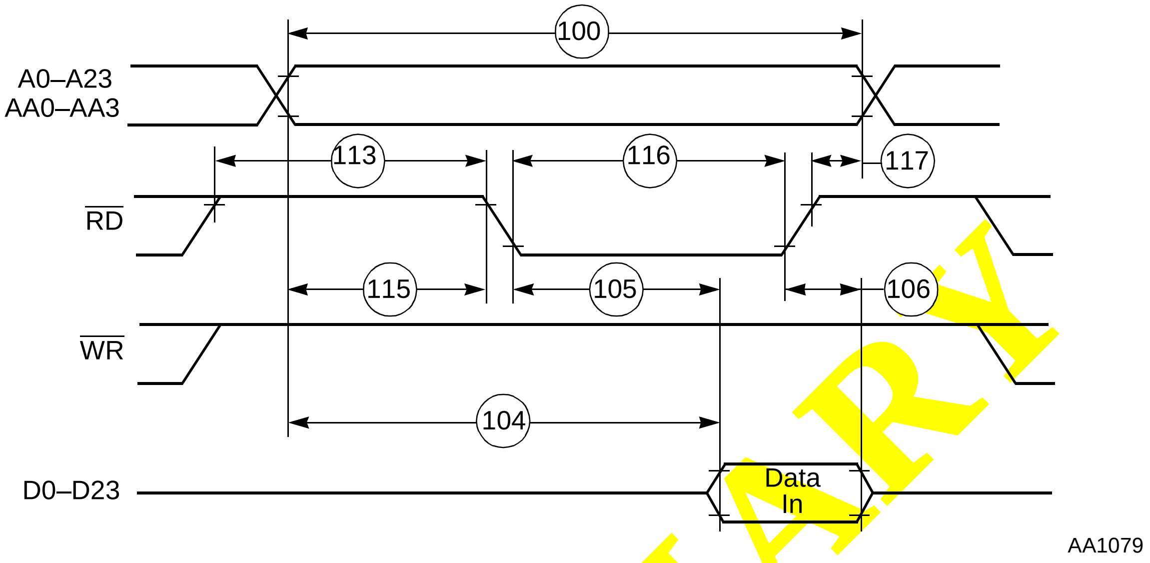


Figure 2-12 SRAM Read Access

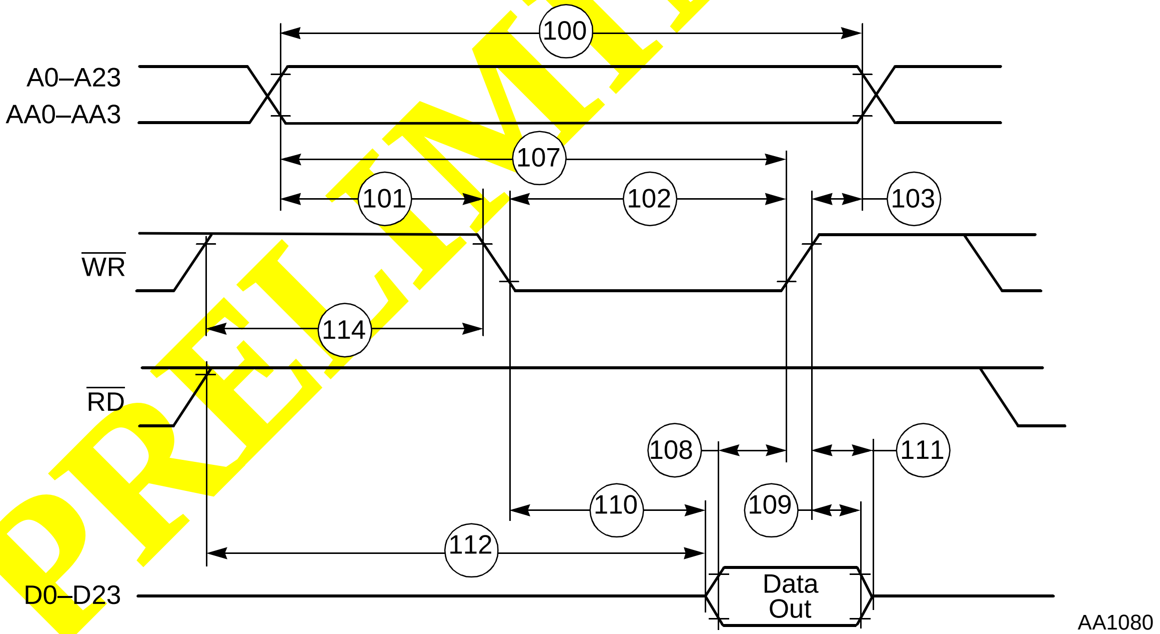
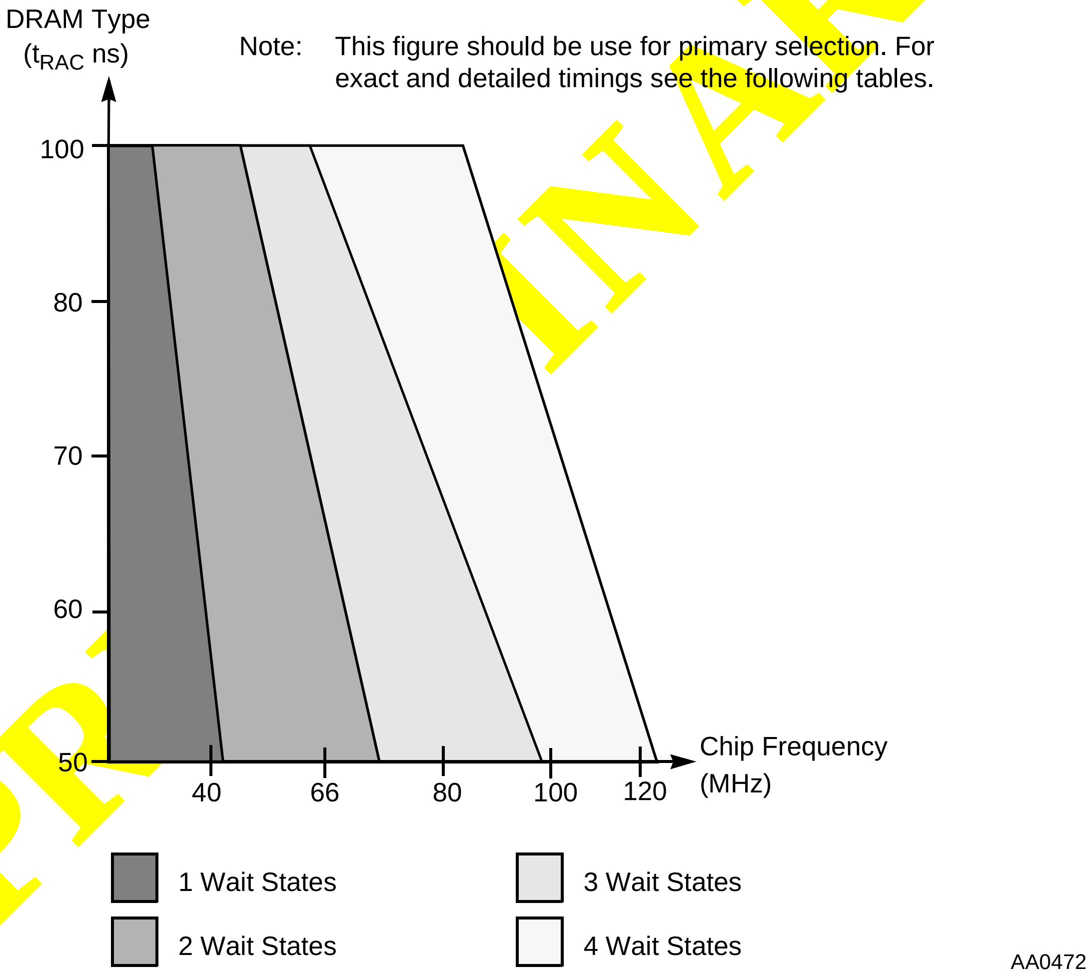


Figure 2-13 SRAM Write Access

DRAM Timing

The selection guides provided in **Figure 2-14** and **Figure 2-17** on page 2-37 should be used for primary selection only. Final selection should be based on the timing provided in the following tables. As an example, the selection guide suggests that 4 wait states must be used for 100 MHz operation when using Page Mode DRAM. However, by using the information in the appropriate table, a designer may choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (e.g., 95 MHz), using faster DRAM (if it becomes available), and control factors such as capacitive and resistive load to improve overall system performance.



Note: This figure should be use for primary selection. For exact and detailed timings see the following tables.

Figure 2-14 DRAM Page Mode Wait States Selection Guide

Table 2-9 DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

No.	Characteristics	Symbol	Expression	20 MHz[6]		30 MHz[6]		Unit
				Min	Max	Min	Max	
131	Page mode cycle time	t_{PC}	$1.25 \times T_C$	62.5	—	41.7	—	ns
132	$\overline{\text{CAS}}$ assertion to data valid (read)	t_{CAC}	$T_C - 7.5$	—	42.5	—	25.8	ns
133	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
134	$\overline{\text{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
136	Previous $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion	t_{RHCP}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
137	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
138	Last $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion[4]	t_{CRP}						
	• BRW[1:0] = 00		$1.75 \times T_C - 6.0$	81.5	—	52.3	—	ns
	• BRW[1:0] = 01		$3.25 \times T_C - 6.0$	156.5	—	102.2	—	ns
	• BRW[1:0] = 10		$4.25 \times T_C - 6.0$	206.5	—	135.5	—	ns
	• BRW[1:0] = 11		$6.25 \times T_C - 6.0$	306.5	—	202.1	—	ns
139	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
140	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
141	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
142	Last column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
143	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$0.75 \times T_C - 3.8$	33.7	—	21.2	—	ns
144	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RCH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns
145	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$0.5 \times T_C - 4.2$	20.8	—	12.5	—	ns
146	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.5$	70.5	—	45.5	—	ns
147	Last $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns

Table 2-9 DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

No.	Characteristics	Symbol	Expression	20 MHz[6]		30 MHz[6]		Unit
				Min	Max	Min	Max	
148	$\overline{\mathrm{WR}}$ assertion to $\overline{\mathrm{CAS}}$ deassertion	t_{CWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns
149	Data valid to $\overline{\mathrm{CAS}}$ assertion (Write)	t_{DS}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
150	$\overline{\mathrm{CAS}}$ assertion to data not valid (write)	t_{DH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
151	$\overline{\mathrm{WR}}$ assertion to $\overline{\mathrm{CAS}}$ assertion	t_{WCS}	$T_C - 4.3$	45.7	—	29.0	—	ns
152	Last $\overline{\mathrm{RD}}$ assertion to $\overline{\mathrm{RAS}}$ deassertion	t_{ROH}	$1.5 \times T_C - 4.0$	71.0	—	46.0	—	ns
153	$\overline{\mathrm{RD}}$ assertion to data valid	t_{GA}	$T_C - 7.5$	—	42.5	—	25.8	ns
154	$\overline{\mathrm{RD}}$ deassertion to data not valid [5]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{\mathrm{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
156	$\overline{\mathrm{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	12.5	—	8.3	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $2 \times T_C$ for read-after-read or write-after-write sequences).
4. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
5. $\overline{\mathrm{RD}}$ deassertion will always occur after $\overline{\mathrm{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
6. Reduced DSP clock speed allows use of Page Mode DRAM with one Wait state (See **Figure 2-14**.).

Table 2-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 7]

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		Unit
				Min	**Max**	**Min**	**Max**	
131	Page mode cycle time	t_{PC}	2.75 × T_C	41.7	—	34.4	—	ns
132	$\overline{\text{CAS}}$ assertion to data valid (read)	t_{CAC}	**66 MHz**: 1.5 × T_C – 7.5 **80 MHz**: 1.5 × T_C – 6.5	— —	15.2 —	— —	— 12.3	ns ns
133	Column address valid to data valid (read)	t_{AA}	**66 MHz**: 2.5 × T_C – 7.5 **80 MHz**: 2.5 × T_C – 6.5	— —	30.4 —	— —	— 24.8	ns
134	$\overline{\text{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	1.75 × T_C – 4.0	22.5	—	17.9	—	ns
136	Previous $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion	t_{RHCP}	3.25 × T_C – 4.0	45.2	—	36.6	—	ns
137	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	1.5 × T_C – 4.0	18.7	—	14.8	—	ns
138	Last $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion[5] • BRW[1:0] = 00 • BRW[1:0] = 01 • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	2.0 × T_C – 6.0 3.5 × T_C – 6.0 4.5 × T_C – 6.0 6.5 × T_C – 6.0	24.4 47.2 62.4 92.8	— — — —	19.0 37.8 50.3 75.3	— — — —	ns ns ns ns
139	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	1.25 × T_C – 4.0	14.9	—	11.6	—	ns
140	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	T_C – 4.0	11.2	—	8.5	—	ns
141	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	1.75 × T_C – 4.0	22.5	—	17.9	—	ns
142	Last column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	3 × T_C – 4.0	41.5	—	33.5	—	ns
143	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	1.25 × T_C – 3.8	15.1	—	11.8	—	ns
144	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RCH}	0.5 × T_C – 3.7	3.9	—	2.6	—	ns
145	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	1.5 × T_C – 4.2	18.5	—	14.6	—	ns
146	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	2.5 × T_C – 4.5	33.4	—	26.8	—	ns

Table 2-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 7] (Continued)

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
147	Last $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$2.75 \times T_C - 4.3$	37.4	—	30.1	—	ns
148	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	$2.5 \times T_C - 4.3$	33.6	—	27.0	—	ns
149	Data valid to $\overline{\text{CAS}}$ assertion (write)	t_{DS}	**66 MHz**: $0.25 \times T_C - 3.7$ **80 MHz**: $0.25 \times T_C - 3.0$	0.1 —	— —	— 0.1	— —	ns ns
150	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
151	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$T_C - 4.3$	10.9	—	8.2	—	ns
152	Last $\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	ns
153	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	**66 MHz**: $1.75 \times T_C - 7.5$ **80 MHz**: $1.75 \times T_C - 6.5$	— —	19.0 —	— —	— 15.4	ns ns
154	$\overline{\text{RD}}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	ns
156	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56301.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM Control Register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
7. There are no DRAMs fast enough to fit to two wait states Page mode @ 100MHz (See **Figure 2-14**.)

Table 2-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
131	Page mode cycle time	t_{PC}	$3.5 \times T_C$	53.0	—	43.8	—	35.0	—	ns
132	$\overline{\text{CAS}}$ assertion to data valid (read)	t_{CAC}	**66 MHz**: $2 \times T_C - 7.5$ **80 MHz**: $2 \times T_C - 6.5$ **100 MHz**: $2 \times T_C - 5.7$	— — —	22.8 — —	— — —	— 18.5 —	— — —	— — 14.3	ns ns ns
133	Column address valid to data valid (read)	t_{AA}	**66 MHz**: $3 \times T_C - 7.5$ **80 MHz**: $3 \times T_C - 6.5$ **100 MHz**: $3 \times T_C - 5.7$	— — —	37.9 — —	— — —	— 31.0 —	— — —	— — 24.3	ns ns ns
134	$\overline{\text{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	0.0	—	ns
135	Last $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	21.0	—	ns
136	Previous $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	64.2	—	52.3	—	41.0	—	ns
137	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	26.3	—	21.0	—	16.0	—	ns
138	Last $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion[5] • BRW[1:0] = 00 • BRW[1:0] = 01 • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	$2.25 \times T_C - 6.0$ $3.75 \times T_C - 6.0$ $4.75 \times T_C - 6.0$ $6.75 \times T_C - 6.0$	28.2 51.0 66.2 96.6	— — — —	22.2 40.9 53.4 78.4	— — — —	16.5 31.5 41.5 61.5	— — — —	ns ns ns ns
139	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	11.0	—	ns
140	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$T_C - 4.0$	11.2	—	8.5	—	6.0	—	ns
141	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	21.0	—	ns
142	Last column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	56.6	—	46.0	—	36.0	—	ns
143	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	15.1	—	11.8	—	8.7	—	ns
144	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	7.7	—	5.7	—	3.8	—	ns

Table 2-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3] (Continued)

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
145	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	29.9	—	23.9	—	18.3	—	ns
146	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	48.5	—	39.3	—	30.5	—	ns
147	Last $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	52.5	—	42.6	—	33.2	—	ns
148	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	44.9	—	36.3	—	28.2	—	ns
149	Data valid to $\overline{\text{CAS}}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	3.6	—	2.3	—	1.0	—	ns
150	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	21.0	—	ns
151	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	14.6	—	11.3	—	8.2	—	ns
152	Last $\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	49.0	—	39.8	—	31.0	—	ns
153	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	**66 MHz**: $2.5 \times T_C - 7.5$ **80 MHz**: $2.5 \times T_C - 6.5$ **100 MHz**: $2.5 \times T_C - 5.7$	— — —	30.4 — —	— — —	— 24.8 —	— — —	— — 19.3	ns ns ns
154	$\overline{\text{RD}}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	0.0	—	ns
155	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	7.2	—	ns
156	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56301.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 2-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
131	Page mode cycle time	t_{PC}	$4.5 \times T_C$	68.2	—	56.3	—	45.0	—	ns
132	$\overline{\text{CAS}}$ assertion to data valid (read)	t_{CAC}	**66 MHz**: $2.75 \times T_C - 7.5$ **80 MHz**: $2.75 \times T_C - 6.5$ **100 MHz**: $2.75 \times T_C - 5.7$	— — —	34.2 — —	— — —	— 27.9 —	— — —	— — 21.8	ns ns ns
133	Column address valid to data valid (read)	t_{AA}	**66 MHz**: $3.75 \times T_C - 7.5$ **80 MHz**: $3.75 \times T_C - 6.5$ **100 MHz**: $3.75 \times T_C - 5.7$	— — —	49.3 — —	— — —	— 40.4 —	— — —	— — 31.8	ns ns ns
134	$\overline{\text{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	0.0	—	ns
135	Last $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	$3.5 \times T_C - 4.0$	49.0	—	39.8	—	31.0	—	ns
136	Previous $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion	t_{RHCP}	$6 \times T_C - 4.0$	86.9	—	71.0	—	56.0	—	ns
137	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	21.0	—	ns
138	Last $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion[5] • BRW[1:0] = 00 • BRW[1:0] = 01 • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	 $2.75 \times T_C - 6.0$ $4.25 \times T_C - 6.0$ $5.25 \times T_C - 6.0$ $6.25 \times T_C - 6.0$	 35.8 58.6 73.8 89.0	 — — — —	 28.4 47.2 59.7 72.2	 — — — —	 21.5 36.5 46.5 56.5	 — — — —	 ns ns ns ns
139	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$2 \times T_C - 4.0$	26.3	—	21.0	—	16.0	—	ns
140	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$T_C - 4.0$	11.2	—	8.5	—	6.0	—	ns
141	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$3.5 \times T_C - 4.0$	49.0	—	39.8	—	31.0	—	ns
142	Last column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$5 \times T_C - 4.0$	71.8	—	58.5	—	46.0	—	ns
143	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	15.1	—	11.8	—	8.7	—	ns
144	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RCH}	$1.25 \times T_C - 3.7$	15.2	—	11.9	—	8.8	—	ns

Table 2-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3] (Continued)

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
145	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$3.25 \times T_C - 4.2$	45.0	—	36.4	—	28.3	—	ns
146	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	63.7	—	51.8	—	40.5	—	ns
147	Last $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	67.7	—	55.1	—	43.2	—	ns
148	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	$3.75 \times T_C - 4.3$	52.5	—	42.6	—	33.2	—	ns
149	Data valid to $\overline{\text{CAS}}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	3.6	—	2.3	—	1.0	—	ns
150	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$3.5 \times T_C - 4.0$	49.0	—	39.8	—	31.0	—	ns
151	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	14.6	—	11.3	—	8.2	—	ns
152	Last $\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	64.2	—	52.3	—	41.0	—	ns
153	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	**66 MHz**: $3.25 \times T_C - 7.5$ **80 MHz**: $3.25 \times T_C - 6.5$ **100 MHz**: $3.25 \times T_C - 5.7$	— — —	41.7 — —	— — —	— 34.1 —	— — —	— — 26.8	ns ns ns
154	$\overline{\text{RD}}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	0.0	—	ns
155	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	7.2	—	ns
156	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56301.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

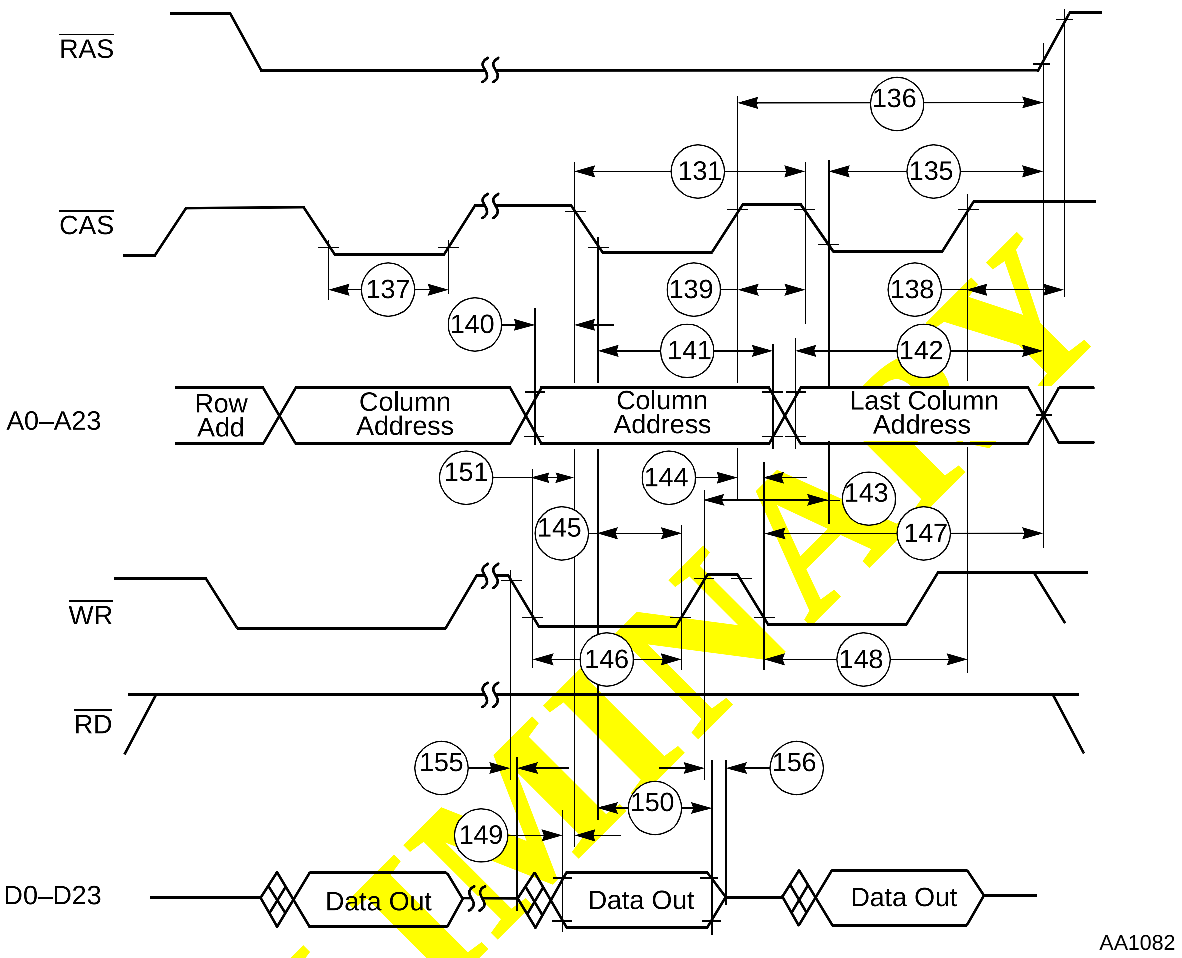


Figure 2-15 DRAM Page Mode Write Accesses

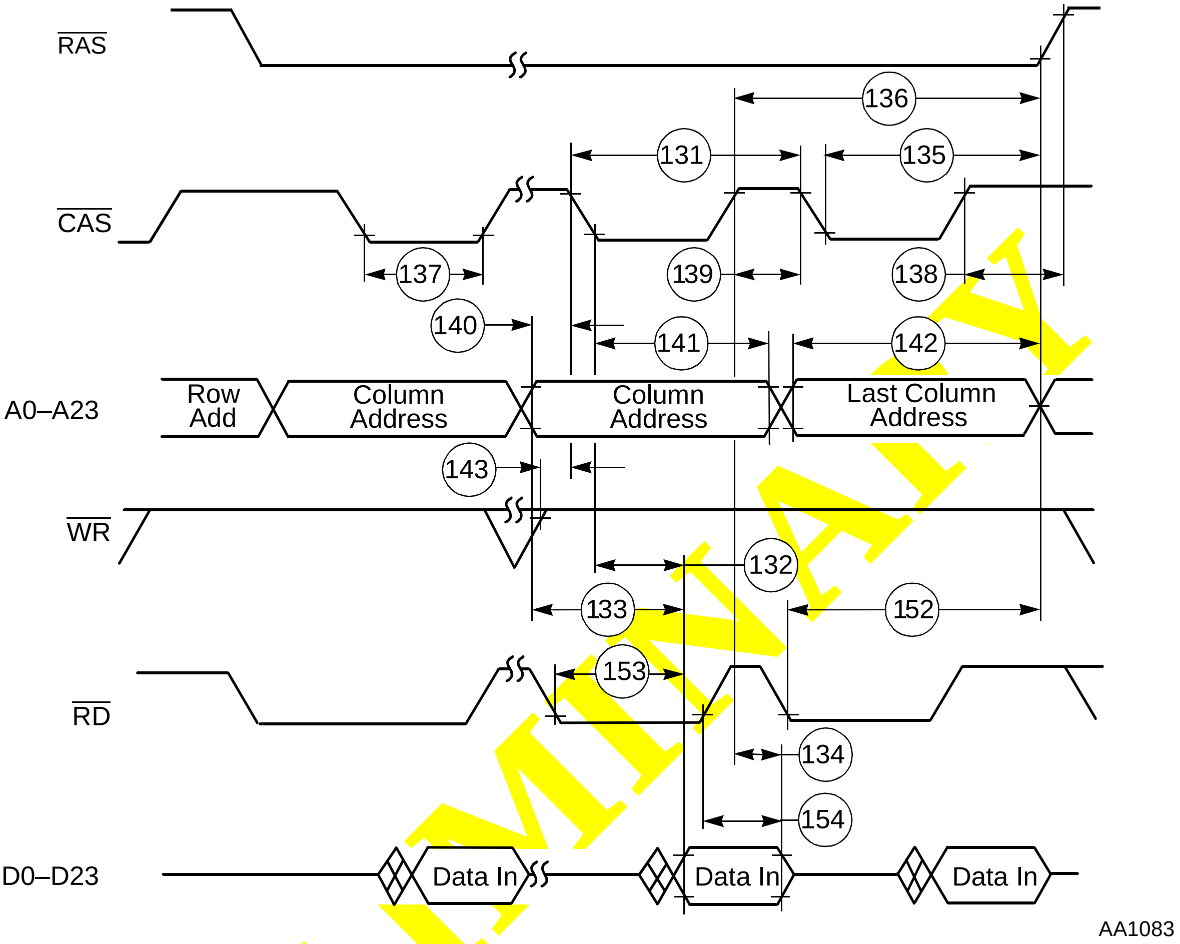
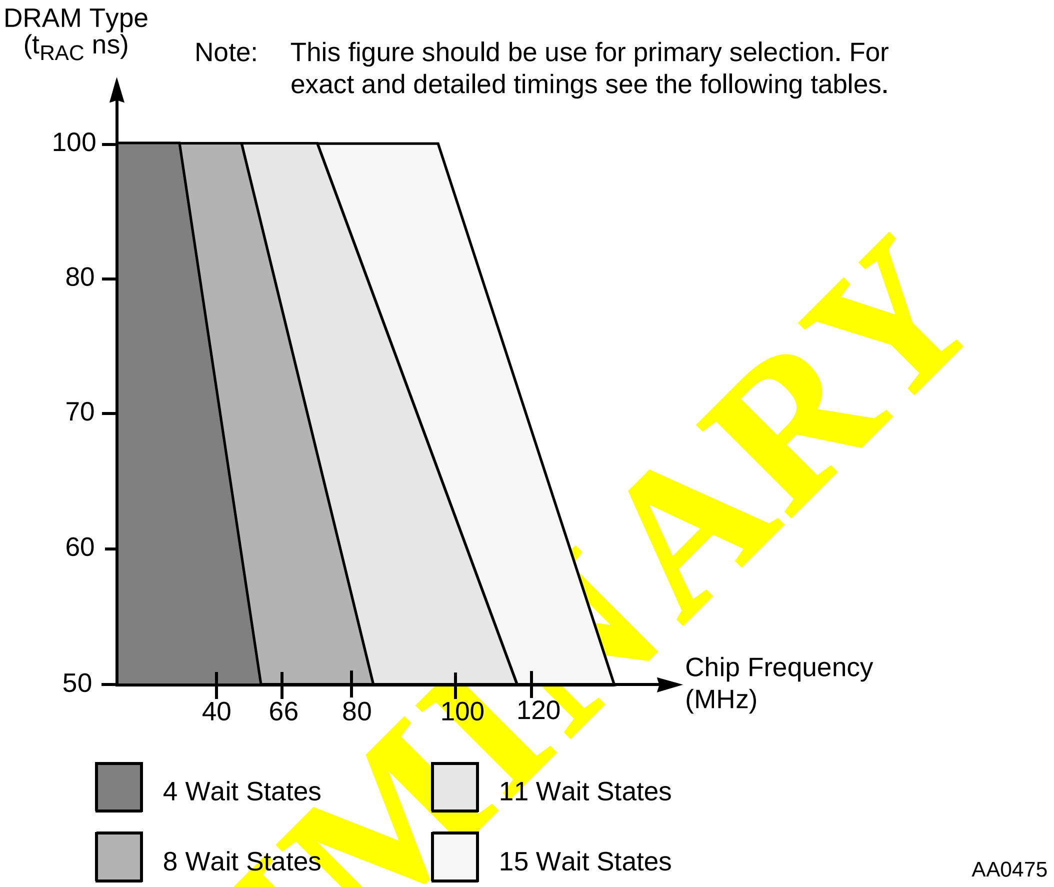


Figure 2-16 DRAM Page Mode Read Accesses



Note: This figure should be use for primary selection. For exact and detailed timings see the following tables.

Figure 2-17 DRAM Out-of-Page Wait States Selection Guide

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$5 \times T_C$	250.0	—	166.7	—	ns
158	$\overline{\text{RAS}}$ assertion to data valid (read)	t_{RAC}	$2.75 \times T_C - 7.5$	—	130.0	—	84.2	ns
159	$\overline{\text{CAS}}$ assertion to data valid (read)	t_{CAC}	$1.25 \times T_C - 7.5$	—	55.0	—	34.2	ns
160	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
161	$\overline{\text{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
162	$\overline{\text{RAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{RP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
163	$\overline{\text{RAS}}$ assertion pulse width	t_{RAS}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
164	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
165	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CSH}	$2.75 \times T_C - 4.0$	133.5	—	87.7	—	ns
166	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
167	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{RCD}	$1.5 \times T_C \pm 2$	73.0	77.0	48.0	52.0	ns
168	$\overline{\text{RAS}}$ assertion to column address valid	t_{RAD}	$1.25 \times T_C \pm 2$	60.5	64.5	39.7	43.7	ns
169	$\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{CRP}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
170	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
171	Row address valid to $\overline{\text{RAS}}$ assertion	t_{ASR}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
172	$\overline{\text{RAS}}$ assertion to row address not valid	t_{RAH}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
173	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
174	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
175	$\overline{\text{RAS}}$ assertion to column address not valid	t_{AR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
176	Column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
177	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$1.5 \times T_C - 3.8$	71.2	—	46.2	—	ns
178	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	33.8	—	21.3	—	ns
179	$\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RRH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
180	$\overline{\mathrm{CAS}}$ assertion to $\overline{\mathrm{WR}}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	70.8	—	45.8	—	ns
181	$\overline{\mathrm{RAS}}$ assertion to $\overline{\mathrm{WR}}$ deassertion	t_{WCR}	$3 \times T_C - 4.2$	145.8	—	95.8	—	ns
182	$\overline{\mathrm{WR}}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	220.5	—	145.5	—	ns
183	$\overline{\mathrm{WR}}$ assertion to $\overline{\mathrm{RAS}}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	233.2	—	154.0	—	ns
184	$\overline{\mathrm{WR}}$ assertion to $\overline{\mathrm{CAS}}$ deassertion	t_{CWL}	$4.25 \times T_C - 4.3$	208.2	—	137.4	—	ns
185	Data valid to $\overline{\mathrm{CAS}}$ assertion (write)	t_{DS}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
186	$\overline{\mathrm{CAS}}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
187	$\overline{\mathrm{RAS}}$ assertion to data not valid (write)	t_{DHR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
188	$\overline{\mathrm{WR}}$ assertion to $\overline{\mathrm{CAS}}$ assertion	t_{WCS}	$3 \times T_C - 4.3$	145.7	—	95.7	—	ns
189	$\overline{\mathrm{CAS}}$ assertion to $\overline{\mathrm{RAS}}$ assertion (refresh)	t_{CSR}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
190	$\overline{\mathrm{RAS}}$ deassertion to $\overline{\mathrm{CAS}}$ assertion (refresh)	t_{RPC}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
191	$\overline{\mathrm{RD}}$ assertion to $\overline{\mathrm{RAS}}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	221.0	—	146.0	—	ns
192	$\overline{\mathrm{RD}}$ assertion to data valid	t_{GA}	$4 \times T_C - 7.5$	—	192.5	—	125.8	ns
193	$\overline{\mathrm{RD}}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{\mathrm{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
195	$\overline{\mathrm{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	12.5	—	8.3	ns

Notes:
1. The number of wait states for out of page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{\mathrm{RD}}$ deassertion will always occur after $\overline{\mathrm{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Reduced DSP clock speed allows use of DRAM out-of-page access with four Wait states (See **Figure 2-17**.).

Table 2-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2]

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	9 × T_C	136.4	—	112.5	—	90.0	—	ns
158	$\overline{\mathrm{RAS}}$ assertion to data valid (read)	t_{RAC}	**66 MHz**: 4.75 × T_C − 7.5	—	64.5	—	—	—	—	ns
			80 MHz: 4.75 × T_C − 6.5	—	—	—	52.9	—	—	ns
			100 MHz: 4.75 × T_C − 5.7	—	—	—	—	—	41.8	ns
159	$\overline{\mathrm{CAS}}$ assertion to data valid (read)	t_{CAC}	**66 MHz**: 2.25 × T_C − 7.5	—	26.6	—	—	—	—	ns
			80 MHz: 2.25 × T_C − 6.5	—	—	—	21.6	—	—	ns
			100 MHz: 2.25 × T_C − 5.7	—	—	—	—	—	16.8	ns
160	Column address valid to data valid (read)	t_{AA}	**66 MHz**: 3 × T_C − 7.5	—	40.0	—	—	—	—	ns
			80 MHz: 3 × T_C − 6.5	—	—	—	31.0	—	—	ns
			100 MHz: 3 × T_C − 5.7	—	—	—	—	—	24.3	ns
161	$\overline{\mathrm{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	0.0	—	ns
162	$\overline{\mathrm{RAS}}$ deassertion to $\overline{\mathrm{RAS}}$ assertion	t_{RP}	3.25 × T_C − 4.0	45.2	—	36.6	—	28.5	—	ns
163	$\overline{\mathrm{RAS}}$ assertion pulse width	t_{RAS}	5.75 × T_C − 4.0	83.1	—	67.9	—	53.5	—	ns
164	$\overline{\mathrm{CAS}}$ assertion to $\overline{\mathrm{RAS}}$ deassertion	t_{RSH}	3.25 × T_C − 4.0	45.2	—	36.6	—	28.5	—	ns
165	$\overline{\mathrm{RAS}}$ assertion to $\overline{\mathrm{CAS}}$ deassertion	t_{CSH}	4.75 × T_C − 4.0	68.0	—	55.4	—	43.5	—	ns
166	$\overline{\mathrm{CAS}}$ assertion pulse width	t_{CAS}	2.25 × T_C − 4.0	30.1	—	24.1	—	18.5	—	ns
167	$\overline{\mathrm{RAS}}$ assertion to $\overline{\mathrm{CAS}}$ assertion	t_{RCD}	2.5 × T_C ± 2	35.9	39.9	29.3	33.3	23.0	27.0	ns
168	$\overline{\mathrm{RAS}}$ assertion to column address valid	t_{RAD}	1.75 × T_C ± 2	24.5	28.5	19.9	23.9	15.5	19.5	ns
169	$\overline{\mathrm{CAS}}$ deassertion to $\overline{\mathrm{RAS}}$ assertion	t_{CRP}	4.25 × T_C − 4.0	59.8	—	49.1	—	38.5	—	ns
170	$\overline{\mathrm{CAS}}$ deassertion pulse width	t_{CP}	2.75 × T_C − 4.0	37.7	—	30.4	—	23.5	—	ns

Table 2-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
171	Row address valid to $\overline{\text{RAS}}$ assertion	t_{ASR}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	28.5	—	ns
172	$\overline{\text{RAS}}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	13.5	—	ns
173	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	7.4	—	5.4	—	3.5	—	ns
174	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	28.5	—	ns
175	$\overline{\text{RAS}}$ assertion to column address not valid	t_{AR}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	53.5	—	ns
176	Column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	56.6	—	46.0	—	36.0	—	ns
177	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$2 \times T_C - 3.8$	26.5	—	21.2	—	16.2	—	ns
178	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$[5] assertion	t_{RCH}	$1.25 \times T_C - 3.7$	15.2	—	11.9	—	8.8	—	ns
179	$\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}$[5] assertion	t_{RRH}	**66 MHz**: $0.25 \times T_C - 3.7$ **80 MHz**: $0.25 \times T_C - 3.0$ **100 MHz**: $0.25 \times T_C - 2.4$	0.1 — —	— — —	— 0.1 —	— — —	— — 0.1	— — —	ns ns ns
180	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$3 \times T_C - 4.2$	41.3	—	33.3	—	25.8	—	ns
181	$\overline{\text{RAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCR}	$5.5 \times T_C - 4.2$	79.1	—	64.6	—	50.8	—	ns
182	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$8.5 \times T_C - 4.5$	124.3	—	101.8	—	80.5	—	ns
183	$\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$8.75 \times T_C - 4.3$	128.3	—	105.1	—	83.2	—	ns
184	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	$7.75 \times T_C - 4.3$	113.1	—	92.6	—	73.2	—	ns
185	Data valid to $\overline{\text{CAS}}$ assertion (write)	t_{DS}	$4.75 \times T_C - 4.0$	68.0	—	55.4	—	43.5	—	ns
186	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	28.5	—	ns
187	$\overline{\text{RAS}}$ assertion to data not valid (write)	t_{DHR}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	53.5	—	ns

Table 2-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
188	$\overline{\mathrm{WR}}$ assertion to $\overline{\mathrm{CAS}}$ assertion	t_{WCS}	$5.5 \times T_C - 4.3$	79.0	—	64.5	—	50.7	—	ns
189	$\overline{\mathrm{CAS}}$ assertion to $\overline{\mathrm{RAS}}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	11.0	—	ns
190	$\overline{\mathrm{RAS}}$ deassertion to $\overline{\mathrm{CAS}}$ assertion (refresh)	t_{RPC}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	13.5	—	ns
191	$\overline{\mathrm{RD}}$ assertion to $\overline{\mathrm{RAS}}$ deassertion	t_{ROH}	$8.5 \times T_C - 4.0$	124.8	—	102.3	—	81.0	—	ns
192	$\overline{\mathrm{RD}}$ assertion to data valid	t_{GA}	**66 MHz**: $7.5 \times T_C - 7.5$ **80 MHz**: $7.5 \times T_C - 6.5$ **100 MHz**: $7.5 \times T_C - 5.7$	— — —	106.1 — —	— — —	— 87.3 —	— — —	— — 69.3	ns ns ns
193	$\overline{\mathrm{RD}}$ deassertion to data not valid[4]	t_{GZ}	0.0	0.0	—	0.0	—	0.0	—	ns
194	$\overline{\mathrm{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	7.2	—	ns
195	$\overline{\mathrm{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56301.
4. $\overline{\mathrm{RD}}$ deassertion will always occur after $\overline{\mathrm{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
5. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 2-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2]

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$12 \times T_C$	181.8	—	150.0	—	120.0	—	ns
158	$\overline{\text{RAS}}$ assertion to data valid (read)	t_{RAC}	**66 MHz**: $6.25 \times T_C - 7.5$ **80 MHz**: $6.25 \times T_C - 6.5$ **100 MHz**: $6.25 \times T_C - 5.7$	— — —	87.2 — —	— — —	— 71.6 —	— — —	— — 56.8	ns ns ns
159	$\overline{\text{CAS}}$ assertion to data valid (read)	t_{CAC}	**66 MHz**: $3.75 \times T_C - 7.5$ **80 MHz**: $3.75 \times T_C - 6.5$ **100 MHz**: $3.75 \times T_C - 5.7$	— — —	49.3 — —	— — —	— 40.4 —	— — —	— — 31.8	ns ns ns
160	Column address valid to data valid (read)	t_{AA}	**66 MHz**: $4.5 \times T_C - 7.5$ **80 MHz**: $4.5 \times T_C - 6.5$ **100 MHz**: $4.5 \times T_C - 5.7$	— — —	60.7 — —	— — —	— 49.8 —	— — —	— — 39.3	ns ns ns
161	$\overline{\text{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	0.0	—	ns
162	$\overline{\text{RAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{RP}	$4.25 \times T_C - 4.0$	60.4	—	49.1	—	38.5	—	ns
163	$\overline{\text{RAS}}$ assertion pulse width	t_{RAS}	$7.75 \times T_C - 4.0$	113.4	—	92.9	—	73.5	—	ns
164	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	$5.25 \times T_C - 4.0$	75.5	—	61.6	—	48.5	—	ns
165	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CSH}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns
166	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$3.75 \times T_C - 4.0$	52.8	—	42.9	—	33.5	—	ns
167	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{RCD}	$2.5 \times T_C \pm 2$	35.9	39.9	29.3	33.3	23.0	27.0	ns
168	$\overline{\text{RAS}}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 2$	24.5	28.5	19.9	23.9	15.5	19.5	ns
169	$\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{CRP}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	53.5	—	ns
170	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$4.25 \times T_C - 4.0$	60.4	—	49.1	—	38.5	—	ns

Table 2-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$4.25 \times T_C - 4.0$	60.4	—	49.1	—	38.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	13.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	7.4	—	5.4	—	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$5.25 \times T_C - 4.0$	75.5	—	61.6	—	48.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$7.75 \times T_C - 4.0$	113.4	—	92.9	—	73.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$6 \times T_C - 4.0$	86.9	—	71.0	—	56.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$3.0 \times T_C - 3.8$	41.7	—	33.7	—	26.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	22.8	—	18.2	—	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	**66 MHz**: $0.25 \times T_C - 3.7$ **80 MHz**: $0.25 \times T_C - 3.0$ **100 MHz**: $0.25 \times T_C - 2.4$	0.1 — —	— — —	— 0.1 —	— — —	— — 0.1	— — —	ns ns ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$5 \times T_C - 4.2$	71.6	—	58.3	—	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$7.5 \times T_C - 4.2$	109.4	—	89.6	—	70.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$11.5 \times T_C - 4.5$	169.7	—	139.3	—	110.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$11.75 \times T_C - 4.3$	173.7	—	142.7	—	113.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$10.25 \times T_C - 4.3$	151.0	—	130.1	—	103.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	53.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$5.25 \times T_C - 4.0$	75.5	—	61.6	—	48.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$7.75 \times T_C - 4.0$	113.4	—	92.9	—	73.5	—	ns

Table 2-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
188	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$6.5 \times T_C - 4.3$	94.2	—	77.0	—	60.7	—	ns
189	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	11.0	—	ns
190	$\overline{\text{RAS}}$ deassertion to $\overline{\text{CAS}}$ assertion (refresh)	t_{RPC}	$2.75 \times T_C - 4.0$	37.7	—	30.4	—	23.5	—	ns
191	$\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	170.2	—	139.8	—	111.0	—	ns
192	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	**66 MHz**: $10 \times T_C - 7.5$ **80 MHz**: $10 \times T_C - 6.5$ **100 MHz**: $10 \times T_C - 5.7$	— — —	144.0 — —	— — —	— 118.5 —	— — —	— — 94.3	ns ns ns
193	$\overline{\text{RD}}$ deassertion to data not valid[4]	t_{GZ}		0.0	—	0.0	—	0.0	—	ns
194	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	7.2	—	ns
195	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56301.
4. $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
5. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 2-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$16 \times T_C$	242.4	—	200.0	—	160.0	—	ns
158	$\overline{\text{RAS}}$ assertion to data valid (read)	t_{RAC}	**66 MHz**: $8.25 \times T_C - 7.5$	—	117.5	—	—	—	—	ns
			80 MHz: $8.25 \times T_C - 6.5$	—	—	—	96.6	—	—	ns
			100 MHz: $8.25 \times T_C - 5.7$	—	—	—	—	—	76.8	ns
159	$\overline{\text{CAS}}$ assertion to data valid (read)	t_{CAC}	**66 MHz**: $4.75 \times T_C - 7.5$	—	64.5	—	—	—	—	ns
			80 MHz: $4.75 \times T_C - 6.5$	—	—	—	52.9	—	—	ns
			100 MHz: $4.75 \times T_C - 5.7$	—	—	—	—	—	41.8	ns
160	Column address valid to data valid (read)	t_{AA}	**66 MHz**: $5.5 \times T_C - 7.5$	—	75.8	—	—	—	—	ns
			80 MHz: $5.5 \times T_C - 6.5$	—	—	—	62.3	—	—	ns
			100 MHz: $5.5 \times T_C - 5.7$	—	—	—	—	—	49.3	ns
161	$\overline{\text{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}	0.0	0.0	—	0.0	—	0.0	—	ns
162	$\overline{\text{RAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{RP}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns
163	$\overline{\text{RAS}}$ assertion pulse width	t_{RAS}	$9.75 \times T_C - 4.0$	143.7	—	117.9	—	93.5	—	ns
164	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns
165	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CSH}	$8.25 \times T_C - 4.0$	121.0	—	99.1	—	78.5	—	ns
166	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$4.75 \times T_C - 4.0$	68.0	—	55.4	—	43.5	—	ns
167	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{RCD}	$3.5 \times T_C \pm 2$	51.0	55.0	41.8	45.8	33.0	37.0	ns
168	$\overline{\text{RAS}}$ assertion to column address valid	t_{RAD}	$2.75 \times T_C \pm 2$	39.7	43.7	32.4	36.4	25.5	29.5	ns
169	$\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{CRP}	$7.75 \times T_C - 4.0$	113.4	—	92.9	—	73.5	—	ns
170	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns

Table 2-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
171	Row address valid to $\overline{\text{RAS}}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns
172	$\overline{\text{RAS}}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	37.7	—	30.4	—	23.5	—	ns
173	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	7.4	—	5.4	—	3.5	—	ns
174	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns
175	$\overline{\text{RAS}}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C - 4.0$	143.7	—	117.9	—	93.5	—	ns
176	Column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$7 \times T_C - 4.0$	102.1	—	83.5	—	66.0	—	ns
177	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$5 \times T_C - 3.8$	72.0	—	58.7	—	46.2	—	ns
178	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	22.8	—	18.2	—	13.8	—	ns
179	$\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}$[4] assertion	t_{RRH}	**66 MHz**: $0.25 \times T_C - 3.7$ **80 MHz**: $0.25 \times T_C - 3.0$ **100 MHz**: $0.25 \times T_C - 2.4$	0.1 — —	— — —	— 0.1 —	— — —	— — 0.1	— — —	ns ns ns
180	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$6 \times T_C - 4.2$	86.7	—	70.8	—	55.8	—	ns
181	$\overline{\text{RAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCR}	$9.5 \times T_C - 4.2$	139.7	—	114.6	—	90.8	—	ns
182	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$15.5 \times T_C - 4.5$	230.3	—	189.3	—	150.5	—	ns
183	$\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$15.75 \times T_C - 4.3$	234.3	—	192.6	—	153.2	—	ns
184	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	**66–80 MHz:** $14.25 \times T_C - 4.3$ **100 MHz:** $14.75 \times T_C - 4.3$	211.6 —	— —	180.1 —	— —	— 143.2	— —	ns ns
185	Data valid to $\overline{\text{CAS}}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	128.6	—	105.4	—	83.5	—	ns
186	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns

Table 2-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
187	$\overline{\text{RAS}}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	143.7	—	117.9	—	93.5	—	ns
188	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	139.6	—	114.5	—	90.7	—	ns
189	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	11.0	—	ns
190	$\overline{\text{RAS}}$ deassertion to $\overline{\text{CAS}}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	68.0	—	55.4	—	43.5	—	ns
191	$\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	230.8	—	189.8	—	151.0	—	ns
192	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	**66 MHz**: $14 \times T_C - 7.5$ **80 MHz**: $14 \times T_C - 6.5$ **100 MHz**: $14 \times T_C - 5.7$	— — —	204.6 — —	— — —	— 168.5 —	— — —	— — 134.3	ns ns ns
193	$\overline{\text{RD}}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	0.0	—	ns
194	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	7.2	—	ns
195	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

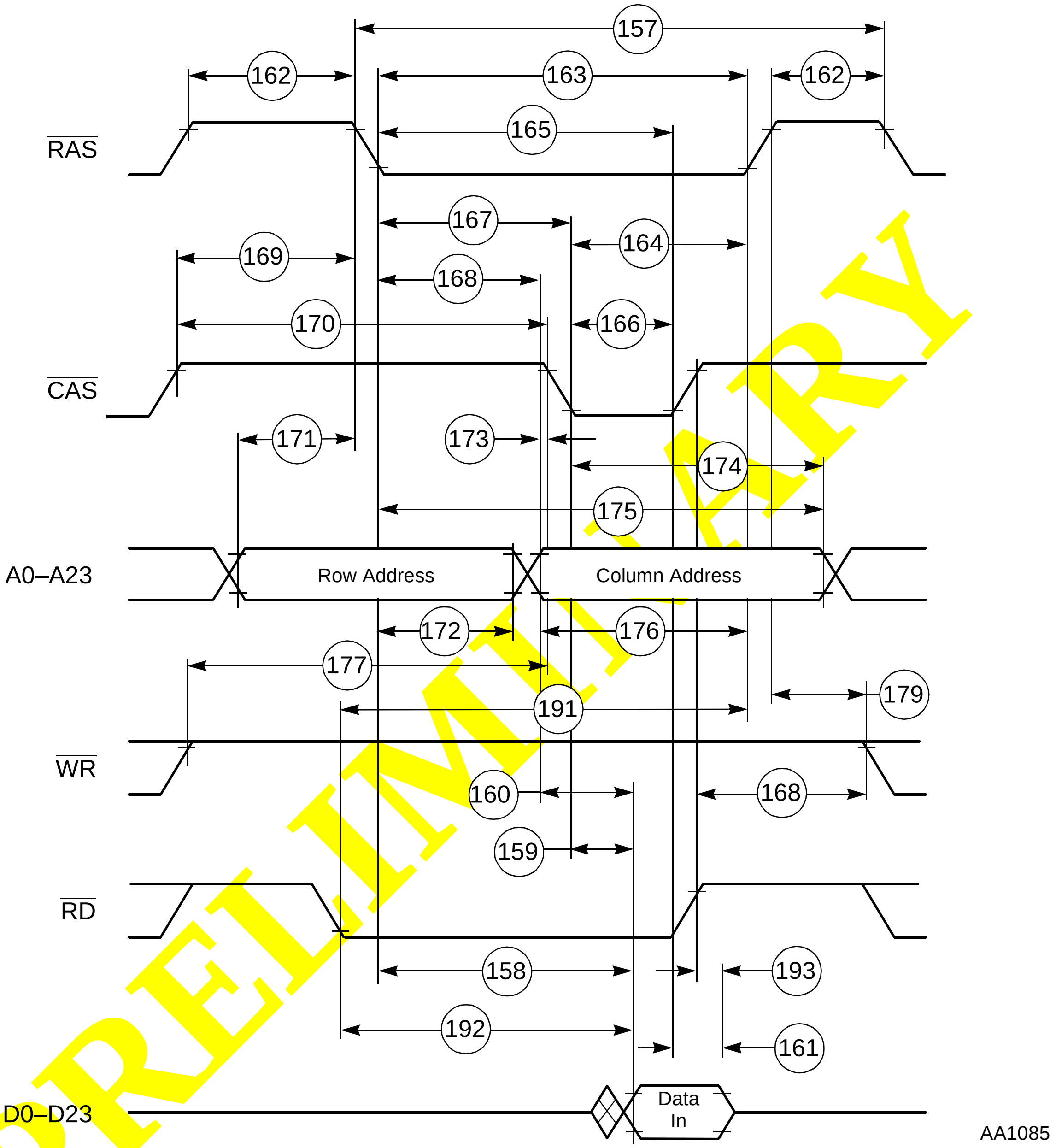


Figure 2-18 DRAM Out-of-Page Read Access

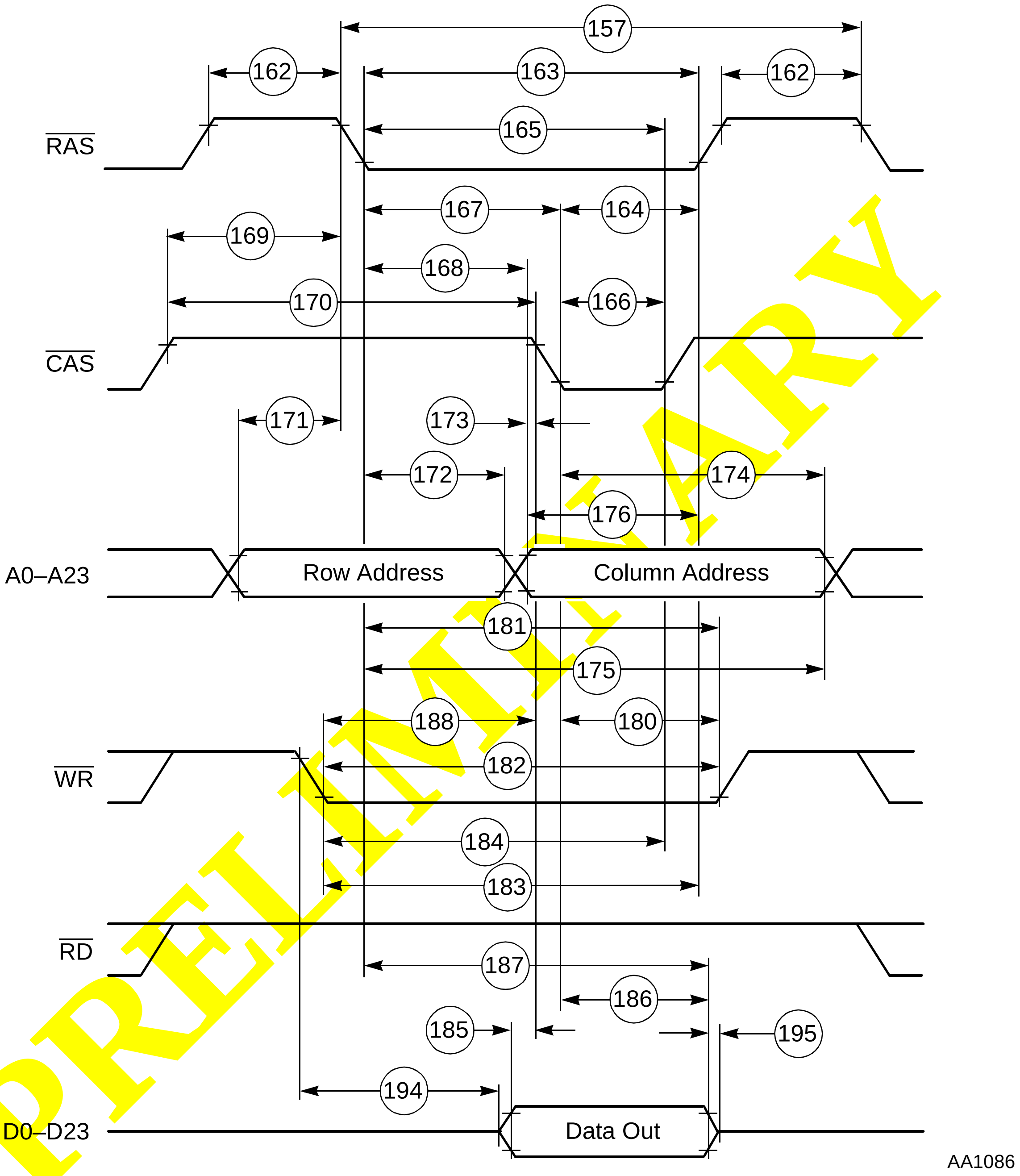


Figure 2-19 DRAM Out-of-Page Write Access

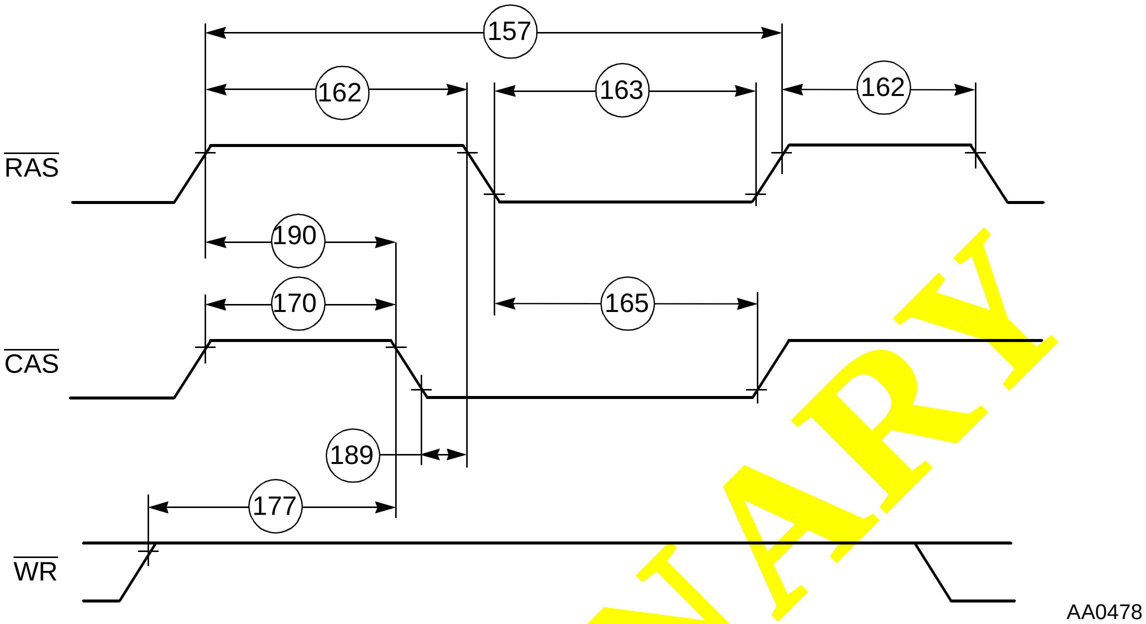


Figure 2-20 DRAM Refresh Access

Synchronous Timings (SRAM)

Table 2-17 External Bus Synchronous Timings (SRAM Access)[4]

No.	Characteristics	Expression[1, 2]	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
196	CLKOUT high to $\overline{\text{BS}}$ assertion	66 MHz: $0.25 \times T_C + 5.0$	4.8	8.8	—	—	—	—	ns
		80 MHz: $0.25 \times T_C + 4.5$	—	—	4.1	7.6	—	—	ns
		100 MHz: $0.25 \times T_C + 4.2$	—	—	—	—	3.5	6.7	ns
197	CLKOUT high to $\overline{\text{BS}}$ deassertion	**66 MHz**: $0.75 \times T_C + 5.0$	12.4	16.4	—	—	—	—	ns
		80 MHz: $0.75 \times T_C + 4.5$	—	—	10.4	13.9	—	—	ns
		100 MHz: $0.75 \times T_C + 4.2$	—	—	—	—	8.5	11.7	ns
198	CLKOUT high to address and AA valid[5]	**66 MHz**: $0.25 \times T_C + 5.0$	—	8.8	—	—	—	—	ns
		80 MHz: $0.25 \times T_C + 4.5$	—	—	—	7.6	—	—	ns
		100 MHz: $0.25 \times T_C + 4.0$	—	—	—	—	—	6.5	ns
	CLKOUT high to $\overline{\text{BL}}$ valid		—	5.0	—	5.0	—	5.0	ns
199	CLKOUT high to address and AA invalid[5]	$0.25 \times T_C$	3.8	—	3.1	—	2.5	—	ns
	CLKOUT high to $\overline{\text{BL}}$ invalid		0.0	—	0.0	—	0.0	—	ns
200	$\overline{\text{TA}}$ valid to CLKOUT high (setup time)		6.0	—	5.0	—	4.0	—	ns
201	CLKOUT high to $\overline{\text{TA}}$ invalid (hold time)		0.0	—	0.0	—	0.0	—	ns
202	CLKOUT high to data out active	$0.25 \times T_C$	3.8	—	3.1	—	2.5	—	ns
203	CLKOUT high to data out valid	**66 MHz**: $0.25 \times T_C + 5.0$	4.8	8.8	—	—	—	—	ns
		80 MHz: $0.25 \times T_C + 4.5$	—	—	4.1	7.6	—	—	ns
		100 MHz: $0.25 \times T_C + 4.0$	—	—	—	—	3.3	6.5	ns
204	CLKOUT high to data out invalid	$0.25 \times T_C$	3.8	—	3.1	—	2.5	—	ns
205	CLKOUT high to data out high impedance	**66 MHz**: $0.25 \times T_C + 1.0$	—	4.8	—	—	—	—	ns
		80 MHz: $0.25 \times T_C + 0.5$	—	—	—	3.6	—	—	ns
		100 MHz: $0.25 \times T_C$	—	—	—	—	—	2.5	ns

Table 2-17 External Bus Synchronous Timings (SRAM Access)[4] (Continued)

No.	Characteristics	Expression[1, 2]	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
206	Data in valid to CLKOUT high (setup)		6.0	—	5.0	—	4.0	—	ns
207	CLKOUT high to data in invalid (hold)		0.0	—	0.0	—	0.0	—	ns
208	CLKOUT high to $\overline{\text{RD}}$ assertion	**66 MHz**: $0.75 \times T_C + 5.0$	12.4	16.4	—	—	—	—	ns
		80 MHz: $0.75 \times T_C + 4.5$	—	—	10.4	13.9	—	—	ns
		100 MHz: $0.75 \times T_C + 4.0$	—	—	—	—	8.2	11.5	ns
209	CLKOUT high to $\overline{\text{RD}}$ deassertion		0.0	5.0	0.0	4.5	0.0	4.0	ns
210	CLKOUT high to $\overline{\text{WR}}$ assertion[3]	**66 MHz**: $0.5 \times T_C + 5.3$ [WS = 1 or WS $\geq$ 4]	8.9	12.9	—	—	—	—	ns
		80 MHz: $0.5 \times T_C + 4.8$ [WS = 1 or WS $\geq$ 4]	—	—	7.6	11.1	—	—	ns
		100 MHz: $0.5 \times T_C + 4.3$ [WS = 1 or WS $\geq$ 4]	—	—	—	—	6.3	9.3	ns
		All frequencies: [$2 \leq$ WS ≤ 3]	1.3	5.3	1.3	4.8	1.3	4.3	ns
211	CLKOUT high to $\overline{\text{WR}}$ deassertion		0.0	4.8	0.0	4.3	0.0	3.8	ns

Notes:
1. WS is the number of wait states specified in the BCR.
2. The asynchronous delays specified in the expressions are valid for DSP56301.
3. If WS > 1, $\overline{\text{WR}}$ assertion refers to the next rising edge of CLKOUT.
4. External bus synchronous timings should be used only for reference to the clock and *not* for relative timings.
5. T198 and T199 are valid for Address Trace mode if the ATE bit in the OMR is set. Use the status of $\overline{\text{BR}}$ (See T212) to determine whether the access referenced by A0–A23 is internal or external, when this mode is enabled.

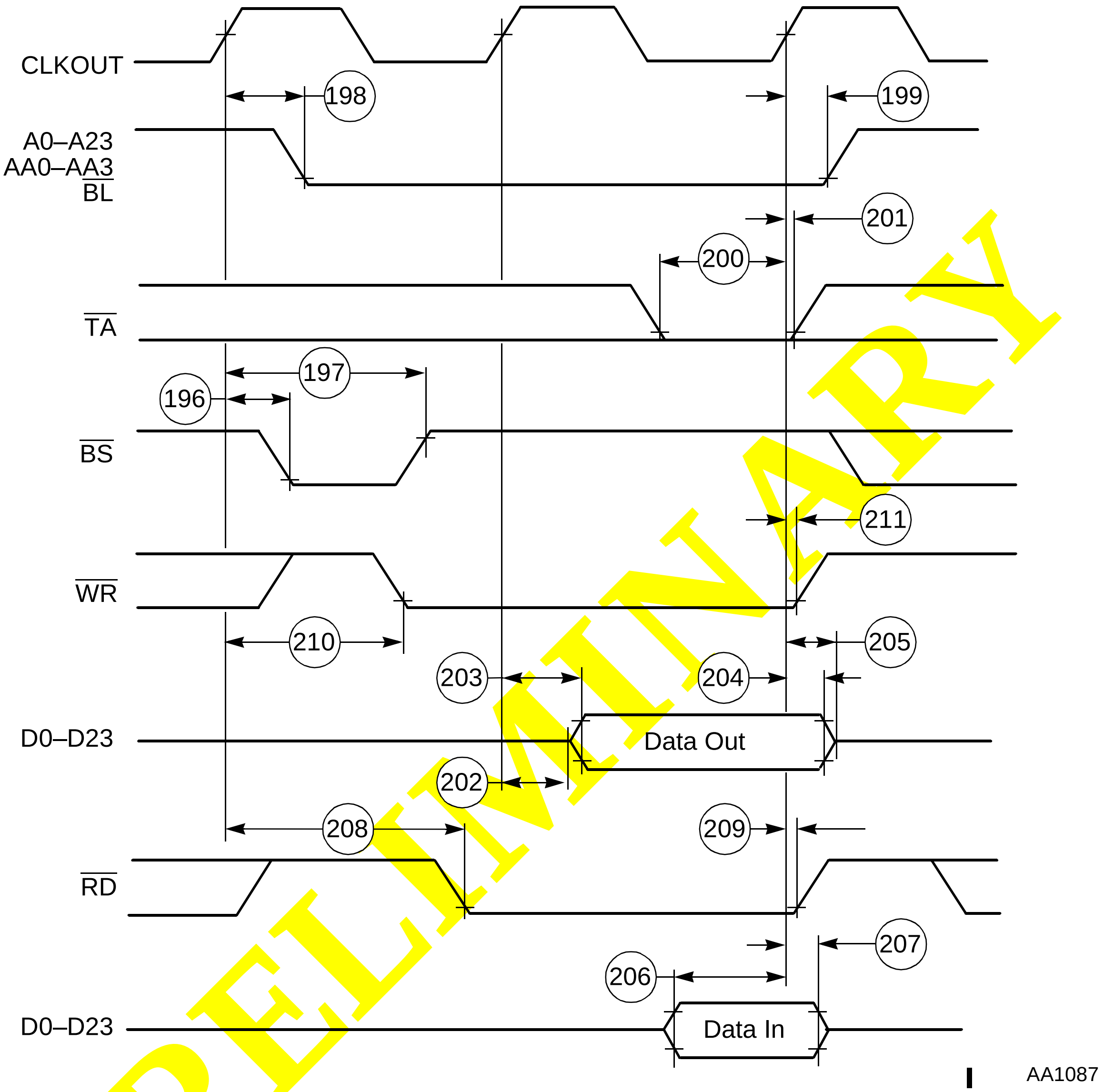


Figure 2-21 Synchronous Bus Timings SRAM 1 WS (BCR Controlled)

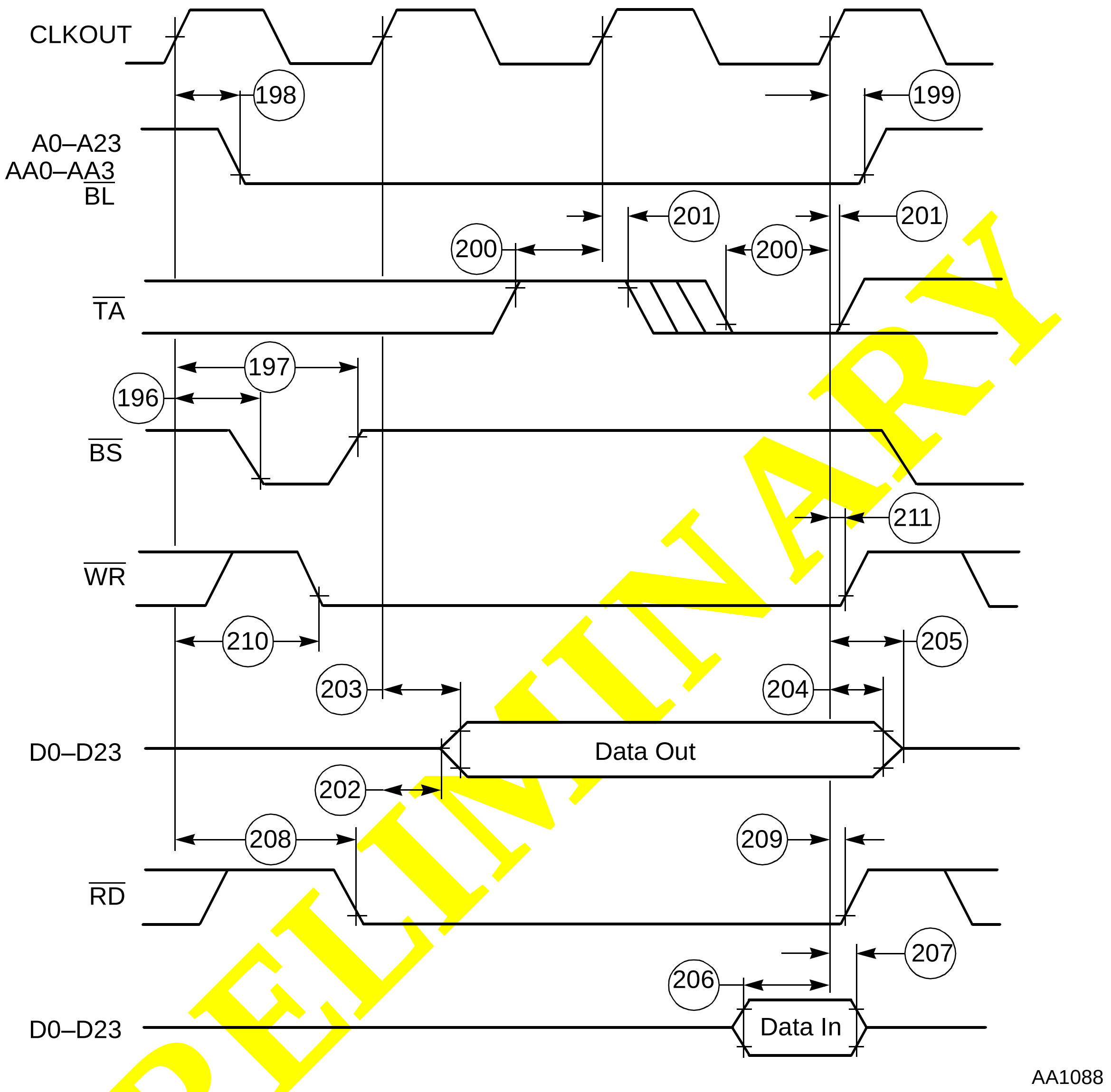


Figure 2-22 Synchronous Bus Timings SRAM 2 WS (TA Controlled)

Arbitration Timings

Table 2-18 Arbitration Bus Timings[1]

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
212	CLKOUT high to $\overline{BR}$ assertion / deassertion[2]		1.0	5.0	1.0	4.5	1.0	4.0	ns
213	$\overline{BG}$ asserted / deasserted to CLKOUT high (setup)		6.0	—	5.0	—	4.0	—	ns
214	CLKOUT high to $\overline{BG}$ deasserted / asserted (hold)		0.0	—	0.0	—	0.0	—	ns
215	$\overline{BB}$ deassertion to CLKOUT high (input setup)		6.0	—	5.0	—	4.0	—	ns
216	CLKOUT high to $\overline{BB}$ assertion (input hold)		0.0	—	0.0	—	0.0	—	ns
217	CLKOUT high to $\overline{BB}$ assertion (output)		1.0	5.0	1.0	4.5	1.0	4.0	ns
218	CLKOUT high to $\overline{BB}$ deassertion (output)		1.0	5.0	1.0	4.5	1.0	4.0	ns
219	$\overline{BB}$ high to $\overline{BB}$ high impedance (output)		—	6.8	—	5.6	—	4.5	ns
220	CLKOUT high to address and controls active	$0.25 \times T_C$	3.8	—	3.1	—	2.5	—	ns
221	CLKOUT high to address and controls high impedance	**66 MHz**: $0.25 \times T_C + 1.0$ **80 MHz**: $0.25 \times T_C + 0.5$ **100 MHz**: $0.25 \times T_C$	— — —	4.8 — —	— — —	— 3.6 —	— — —	— — 2.5	ns ns ns
222	CLKOUT high to AA active	$0.25 \times T_C$	3.8	—	3.1	—	2.5	—	ns
223	CLKOUT high to AA deassertion	**66 MHz**: $0.25 \times T_C + 5.0$ **80 MHz**: $0.25 \times T_C + 4.5$ **100 MHz**: $0.25 \times T_C + 4.0$	4.8 — —	8.8 — —	— 4.1 —	— 7.6 —	— — 3.2	— — 6.5	ns ns ns
224	CLKOUT high to AA high impedance	**66 MHz**: $0.75 \times T_C + 1.0$ **80 MHz**: $0.75 \times T_C + 0.5$ **100 MHz**: $0.75 \times T_C$	— — —	12.4 — —	— — —	— 9.9 —	— — —	— — 7.5	ns ns ns

Notes:
1. The asynchronous delays specified in the expressions are valid for DSP56301.
2. T212 is valid for Address Trace mode when the ATE bit in the OMR is set. $\overline{BR}$ is deasserted for internal accesses and asserted for external accesses.

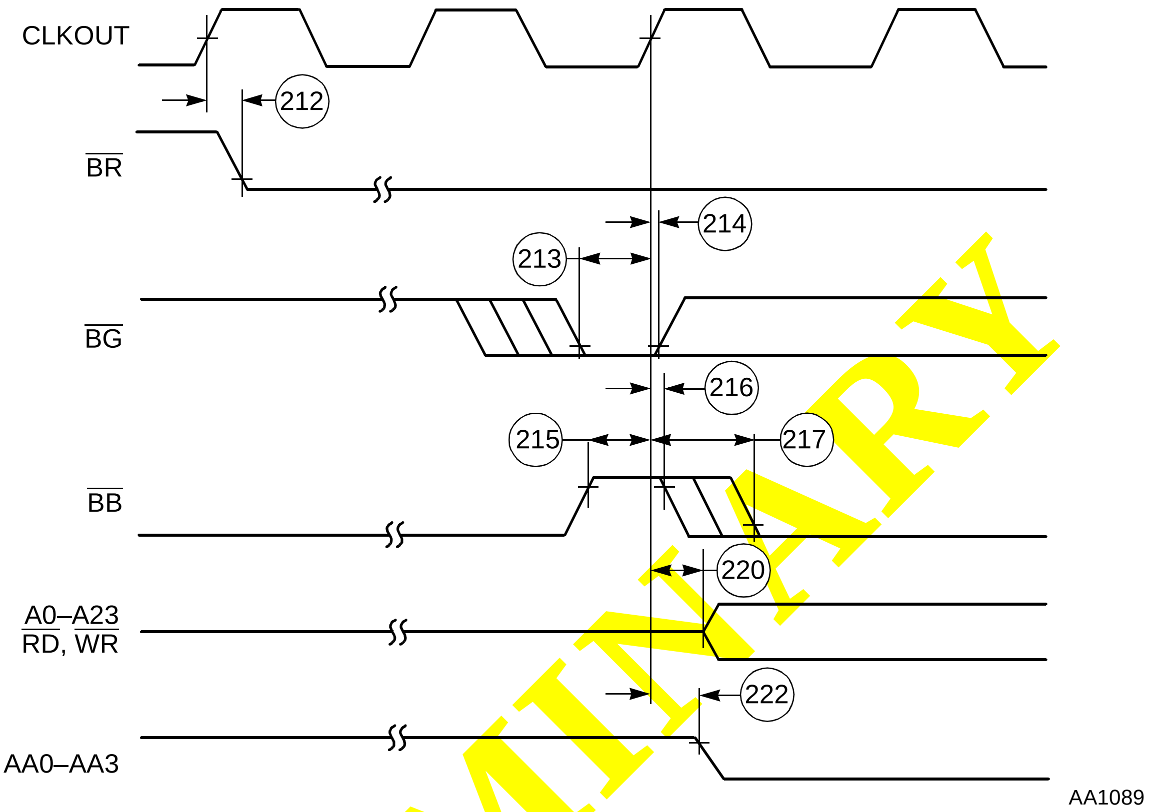


Figure 2-23 Bus Acquisition Timings

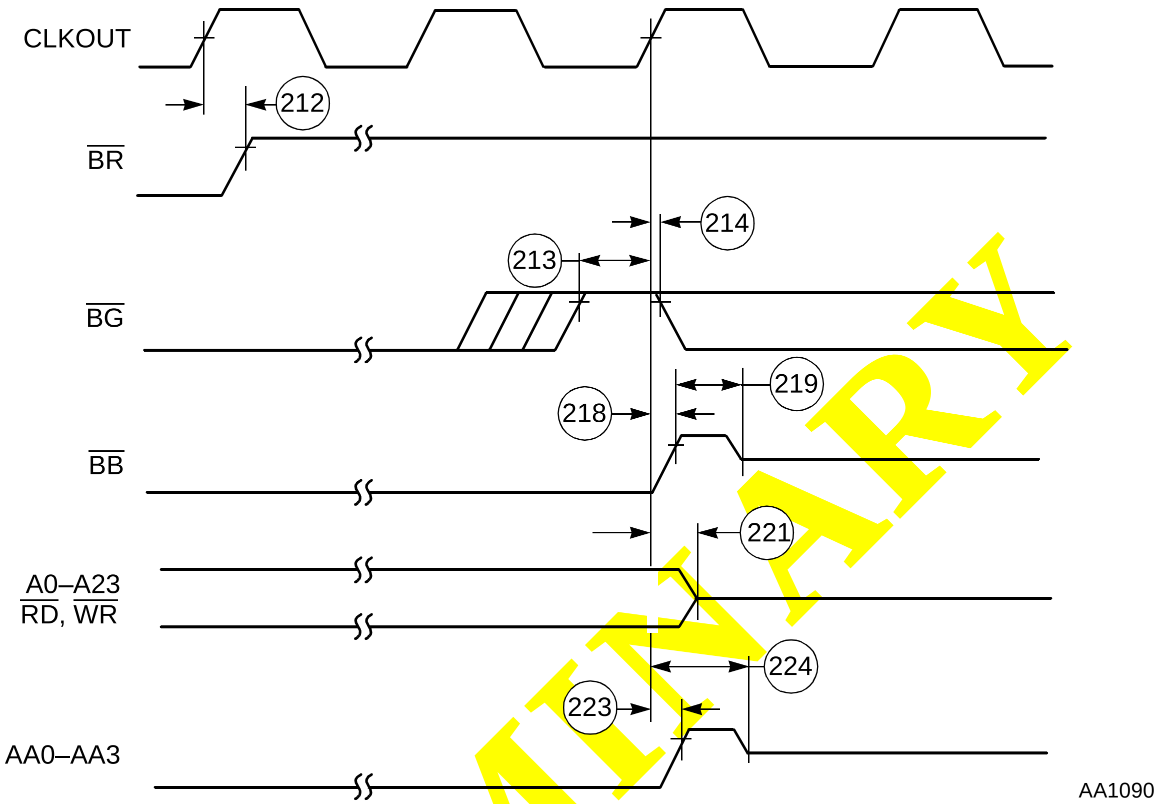


Figure 2-24 Bus Release Timings Case 1 (BRT Bit in OMR Cleared)

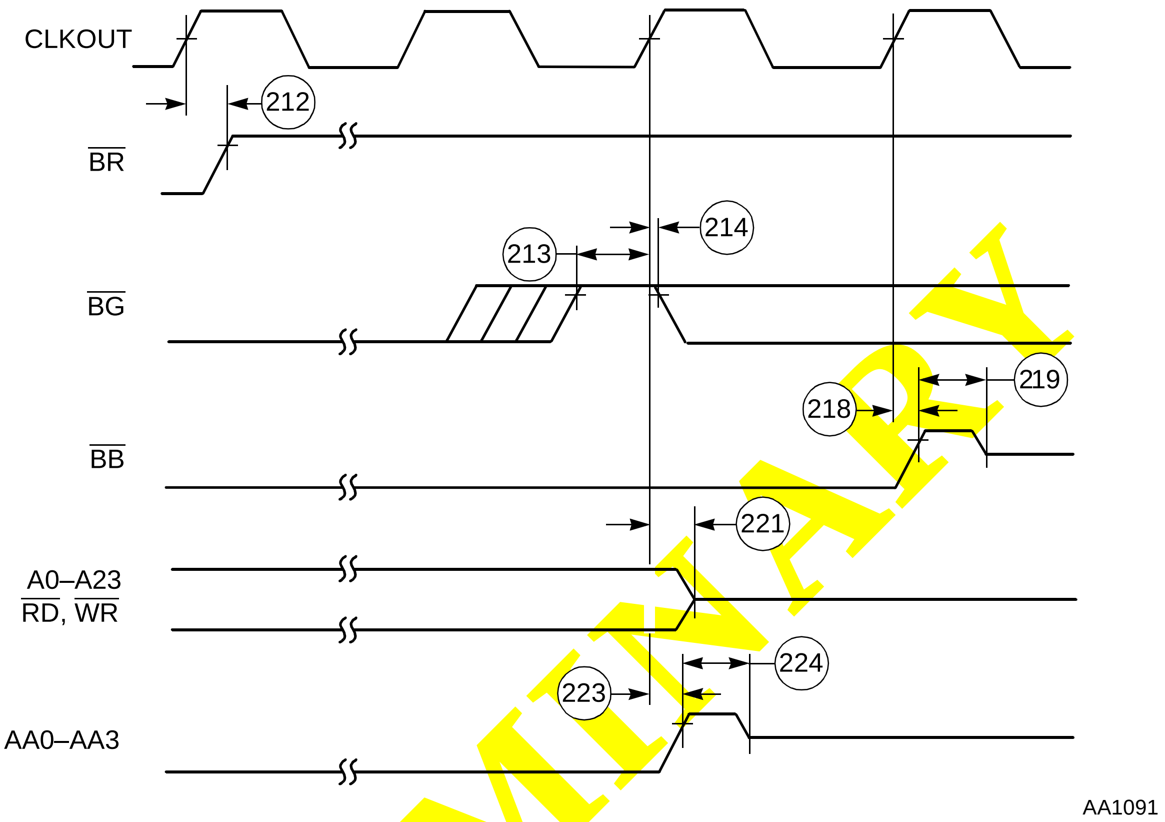


Figure 2-25 Bus Release Timings Case 2 (BRT Bit in OMR Set)

HOST INTERFACE TIMING

Table 2-19 Universal Bus Mode Timing Parameters

No.	Characteristic	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
300	Access Cycle Time	$3 \times T_C$	45.5	—	37.5	—	30.0	—	
301	HA[10:0], HAEN Setup to Data Strobe Assertion[1]		7.0	—	5.8	—	4.6	—	ns
302	HA[10:0], HAEN Valid Hold from Data Strobe Deassertion[1]		0.0	—	0.0	—	0.0	—	ns
303	HRW Setup to $\overline{\mathrm{HDS}}$ Assertion[2]		7.0	—	5.8	—	4.6	—	ns
304	HRW Valid Hold from $\overline{\mathrm{HDS}}$ Deassertion[2]		0.0	—	0.0	—	0.0	—	ns
305	Data Strobe Deasserted Width[1]		5.0	—	4.1	—	3.3	—	ns
306	Data Strobe Asserted Pulse Width[1]	$2.5 \times T_C + 2.0$ [9]	39.9	—	32.9	—	26.3	—	ns
307	$\overline{\mathrm{HBS}}$ Asserted Pulse Width		3.0	—	2.5	—	2.0	—	
308	$\overline{\mathrm{HBS}}$ Assertion to Data Strobe Assertion[1]	$T_C - 6.0$ [9]	—	9.2	—	7.6	—	6.0	ns
309	$\overline{\mathrm{HBS}}$ Assertion to Data Strobe Deassertion[1]	$2.5 \times T_C + 3.5$ [9]	41.4	—	34.1	—	27.3	—	
310	$\overline{\mathrm{HBS}}$ Deassertion to Data Strobe Deassertion[1]	$1.5 \times T_C + 4.0$ [9]	26.7	—	22.1	—	17.6	—	
311	Data Out Valid to $\overline{\mathrm{TA}}$ Assertion ($\overline{\mathrm{HBS}}$ Not Used—Tied to V_{CC})[2]	$2 \times T_C - 14.0$	16.3	—	11.0	—	6.0	—	ns
312	Data Out Active from Read Data Strobe Assertion[3]		2.0	—	1.7	—	1.3	—	ns
313	Data Out Valid from Read Data Strobe Assertion (No Wait States Inserted—HTA Asserted)[3]		—	21.0	—	18.9	—	16.9	ns
314	Data Out Valid Hold from Read Data Strobe Deassertion$_3$		2.0	—	1.7	—	1.3	—	ns
315	Data Out High Impedance from Read Data Strobe Deassertion[3]		—	14.5	—	12.0	—	9.6	ns
316	Data In Valid Setup to Write Data Strobe Deassertion[4]		10.0	—	8.3	—	6.6	—	ns
317	Data In Valid Hold from Write Data Strobe Deassertion[4]		0.0	—	0.0	—	0.0	—	ns

Table 2-19 Universal Bus Mode Timing Parameters (Continued)

No.	Characteristic	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
318	$\overline{\text{HSAK}}$ Assertion from Data Strobe Assertion[1]		—	25.0	—	22.2	—	19.6	ns
319	$\overline{\text{HSAK}}$ Asserted Hold from Data Strobe Deassertion[1]		2.0	—	1.7	—	1.3	—	ns
320	HTA Active from Data Strobe Assertion[1,2,5]		3.8	—	3.1	—	2.5	—	ns
321	HTA Assertion from Data Strobe Assertion ($\overline{\text{HBS}}$ Not Used—Tied to V_{CC})[1,2,5]	$2.0 \times T_C + 13.8$ [9]	44.1	—	37.8	—	31.8	—	
322	HTA Assertion from $\overline{\text{HBS}}$ Assertion[2,5]	$2.0 \times T_C + 13.8$ [9]	44.1	—	37.8	—	31.8	—	ns
323	HTA Deasserted from Data Strobe Assertion[1,2,5]		—	26.7	—	23.6	—	20.7	ns
324	HTA Assertion to Data Strobe Deassertion[1,2]		0.0	—	0.0	—	0.0	—	ns
325	HTA High Impedance from Data Strobe Deassertion[1,2]		—	18.5	—	15.3	—	12.2	ns
326	$\overline{\text{HIRQ}}$ Asserted Pulse Width (HIRH = 0, HIRD = 1)	$(LT + 1) \times T_C - 6.0$ [7]	9.2	—	6.5	—	4.0	—	ns
327	$\overline{\text{Data Strobe}}$ Deasserted Hold from $\overline{\text{HIRQ}}$ Deassertion (HIRH = 0)[1]		0.0	—	0.0	—	0.0	—	ns
328	$\overline{\text{HIRQ}}$ Asserted Hold from Data Strobe Assertion (HIRH = 1)[1]	$1.5 \times T_C$	22.7	—	18.8	—	15.0	—	ns
329	$\overline{\text{HIRQ}}$ Deassertion from Data Strobe Assertion (HIRH = 1, HIRD = 1)[1]	$2.5 \times T_C + 28.0$ [9]	—	65.9	—	55.9	—	46.5	ns
330	$\overline{\text{HIRQ}}$ High Impedance from Data Strobe Assertion (HIRH = 1, HIRD = 0)[1,6]	$2.5 \times T_C + 28.0$ [9]	—	65.9	—	55.9	—	46.5	ns
331	$\overline{\text{HIRQ}}$ Active from Data Strobe Deassertion (HIRH = 1, HIRD = 0)[1]	$2.5 \times T_C$	37.9	—	31.3	—	25.0	—	ns
332	$\overline{\text{HIRQ}}$ Deasserted Hold from Data Strobe Deassertion[1]	$2.5 \times T_C$	37.9	—	31.3	—	25.0	—	ns
333	HDRQ[2] Asserted Hold from Data Strobe Assertion[1]	$1.5 \times T_C$	22.7	—	18.8	—	15.0	—	ns
334	HDRQ[2] Deassertion from Data Strobe Assertion[1]	$2.5 \times T_C + 28.0$ [9]	—	65.9	—	55.9	—	46.5	ns

Table 2-19 Universal Bus Mode Timing Parameters (Continued)

No.	Characteristic	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
335	HDRQ[2] Deasserted Hold from Data Strobe Deassertion[1]	$2.5 \times T_C + 4.5$ [9]	42.4	—	35.0	—	28.0	—	ns
336	$\overline{\text{HDAK}}$ Assertion to Data Strobe Assertion[1]		7.0	—	5.8	—	4.6	—	ns
337	$\overline{\text{HDAK}}$ Asserted Hold from Data Strobe Deassertion[1]		0.0	—	0.0	—	0.0	—	ns
338	$\overline{\text{HDBEN}}$ Deasserted Hold from Data Strobe Assertion[1]		3.0	—	2.5	—	2.0	—	ns
339	$\overline{\text{HDBEN}}$ Assertion from Data Strobe Assertion[1]		—	25.0	—	22.2	—	19.6	ns
340	$\overline{\text{HDBEN}}$ Asserted Hold from Data Strobe Deassertion[1]		3.0	—	2.5	—	2.0	—	ns
341	$\overline{\text{HDBEN}}$ Deassertion from Data Strobe Deassertion[1]		—	25.0	—	22.2	—	19.6	ns
342	HDBDR High Hold from Read Data Strobe Assertion[3]		3.0	—	2.5	—	2.0	—	ns
343	HDBDR Low from Read Data Strobe Assertion[3]		—	25.0	—	22.2	—	19.6	ns
344	HDBDR Low Hold from Read Data Strobe Deassertion[3]		3.0	—	2.5	—	2.0	—	ns
345	HDBDR High from Read Data Strobe Deassertion[3]		—	25.0	—	22.2	—	19.6	ns
346	HRST Assertion to Host Port Pins High Impedance[2]		—	25.0	—	22.2	—	19.6	ns

Notes:
1. The Data Strobe is $\overline{\text{HRD}}$ or $\overline{\text{HWR}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
2. HTA, HDRQ, and HRST may be programmed as active-high or active-low. In the example timing diagrams, HDRQ and HRST are shown as active-high and HTA is shown as active low.
3. The Read Data Strobe is $\overline{\text{HRD}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
4. The Write Data Strobe is $\overline{\text{HWR}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
5. HTA requires an external pull-down resistor if programmed as active high (HTAP = 0); or an external pull-up resistor if programmed as active low (HTAP = 1). The resistor value should be consistent with the DC specifications.
6. $\overline{\text{HIRQ}}$ requires an external pull-up resistor if programmed as open drain (HIRD = 0). The resistor value should be consistent with the DC specifications.
7. “LT” is the value of the latency timer register (CLAT) as programmed by the user during self configuration.
8. Values are valid for $V_{CC} = 3.3 \pm 0.3V$
9. The Asynchronous delay in this expression is valid only for the 66MHz DSP56301/D (DSP56301PW66 or DSP56301GC66).

Table 2-20 Universal Bus Mode, Synchronous Port A Type Host Timing

No.	Characteristic	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
300	Access Cycle Time	$3 \times T_C$	45.5	—	37.5	—	30.0	—	
301	HA[10:0], HAEN Setup to Data Strobe Assertion[1]		7.0	—	5.8	—	4.6	—	ns
302	HA[10:0], HAEN Valid Hold from Data Strobe Deassertion[1]		0.0	—	0.0	—	0.0	—	ns
305	Data Strobe Deasserted Width[1]		5.0	—	4.1	—	3.3	—	ns
307	$\overline{\text{HBS}}$ Asserted Pulse Width		3.0	—	2.5	—	2.0	—	
308	$\overline{\text{HBS}}$ Assertion to Data Strobe Assertion[1]	$T_C - 6.0$ [9]	—	9.2	—	7.6	—	6.0	ns
309	$\overline{\text{HBS}}$ Assertion to Data Strobe Deassertion[1]	$2.5 \times T_C + 3.5$ [9]	41.4	—	34.1	—	27.3	—	
310	$\overline{\text{HBS}}$ Deassertion to Data Strobe Deassertion[1]	$1.5 \times T_C + 4.0$ [9]	26.7	—	22.1	—	17.6	—	
312	Data Out Active from Read Data Strobe Assertion[3]		2.0	—	1.7	—	1.3	—	ns
313	Data Out Valid from Read Data Strobe Assertion (No Wait States Inserted—HTA Asserted)[3]		—	21.0	—	18.9	—	16.9	ns
314	Data Out Valid Hold from Read Data Strobe Deassertion$_3$		2.0	—	1.7	—	1.3	—	ns
315	Data Out High Impedance from Read Data Strobe Deassertion[3]		—	14.5	—	12.0	—	9.6	ns
316	Data In Valid Setup to Write Data Strobe Deassertion[4]		10.0	—	8.3	—	6.6	—	ns
317	Data In Valid Hold from Write Data Strobe Deassertion[4]		0.0	—	0.0	—	0.0	—	ns
324	HTA Assertion to Data Strobe Deassertion[1,2]		0.0	—	0.0	—	0.0	—	ns
325	HTA High Impedance from Data Strobe Deassertion[1,2]		—	18.5	—	15.3	—	12.2	ns
326	$\overline{\text{HIRQ}}$ Asserted Pulse Width (HIRH = 0, HIRD = 1)	$(LT + 1) \times T_C - 6.0$[7]	9.2	—	6.5	—	4.0	—	ns
327	Data Strobe Deasserted Hold from $\overline{\text{HIRQ}}$ Deassertion (HIRH = 0)[1]		0.0	—	0.0	—	0.0	—	ns
328	$\overline{\text{HIRQ}}$ Asserted Hold from Data Strobe Assertion (HIRH = 1)[1]	$1.5 \times T_C$	22.7	—	18.8	—	15.0	—	ns

No.	Characteristic	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
329	$\overline{\text{HIRQ}}$ Deassertion from Data Strobe Assertion (HIRH = 1, HIRD = 1)[1]	$2.5 \times T_C + 28.0$ [9]	—	65.9	—	55.9	—	46.5	ns
330	$\overline{\text{HIRQ}}$ High Impedance from Data Strobe Assertion (HIRH = 1, HIRD = 0)[1,6]	$2.5 \times T_C + 28.0$ [9]	—	65.9	—	55.9	—	46.5	ns
331	$\overline{\text{HIRQ}}$ Active from Data Strobe Deassertion (HIRH = 1, HIRD = 0)[1]	$2.5 \times T_C$	37.9	—	31.3	—	25.0	—	ns
332	$\overline{\text{HIRQ}}$ Deasserted Hold from Data Strobe Deassertion[1]	$2.5 \times T_C$	37.9	—	31.3	—	25.0	—	ns
346	HRST Assertion to Host Port Pins High Impedance[2]		—	25.0	—	22.2	—	19.6	ns
347	$\overline{\text{HBS}}$ Assertion to CLKOUT Rising Edge		5.2	—	4.3	—	3.4	—	ns
348	Data Strobe Deassertion to CLKOUT Rising Edge[1]		9.0	—	7.4	—	5.9	—	ns

Notes:
1. The Data Strobe is $\overline{\text{HRD}}$ or $\overline{\text{HWR}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
2. HTA, HDRQ, and HRST may be programmed as active-high or active-low. In the example timing diagrams, HDRQ and HRST are shown as active-high and HTA is shown as active low.
3. The Read Data Strobe is $\overline{\text{HRD}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
4. The Write Data Strobe is $\overline{\text{HWR}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
5. HTA requires an external pull-down resistor if programmed as active high (HTAP = 0); or an external pull-up resistor if programmed as active low (HTAP = 1). The resistor value should be consistent with the DC specifications.
6. $\overline{\text{HIRQ}}$ requires an external pull-up resistor if programmed as open drain (HIRD = 0). The resistor value should be consistent with the DC specifications.
7. "LT" is the value of the latency timer register (CLAT) as programmed by the user during self configuration.
8. Values are valid for $V_{CC} = 3.3 \pm 0.3V$
9. The Asynchronous delay in this expression is valid only for the 66MHz DSP56301/D (DSP56301PW66 or DSP56301GC66).

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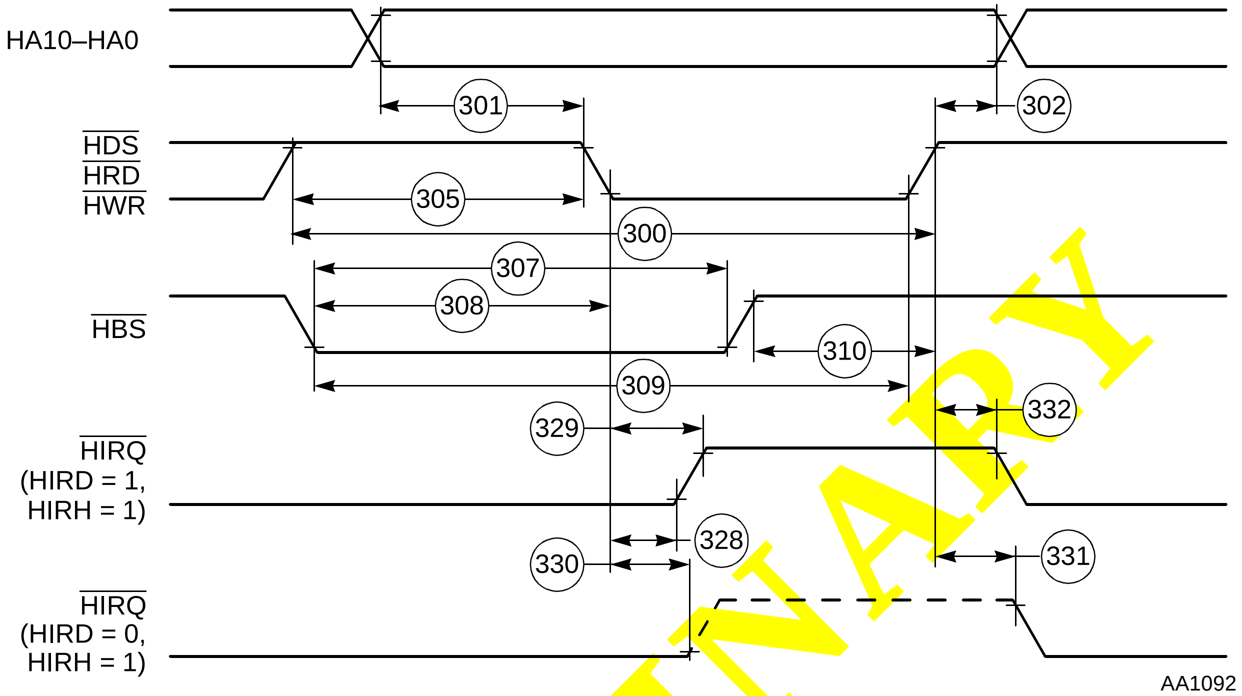


Figure 2-26 Universal Bus Mode I/O Access Timing

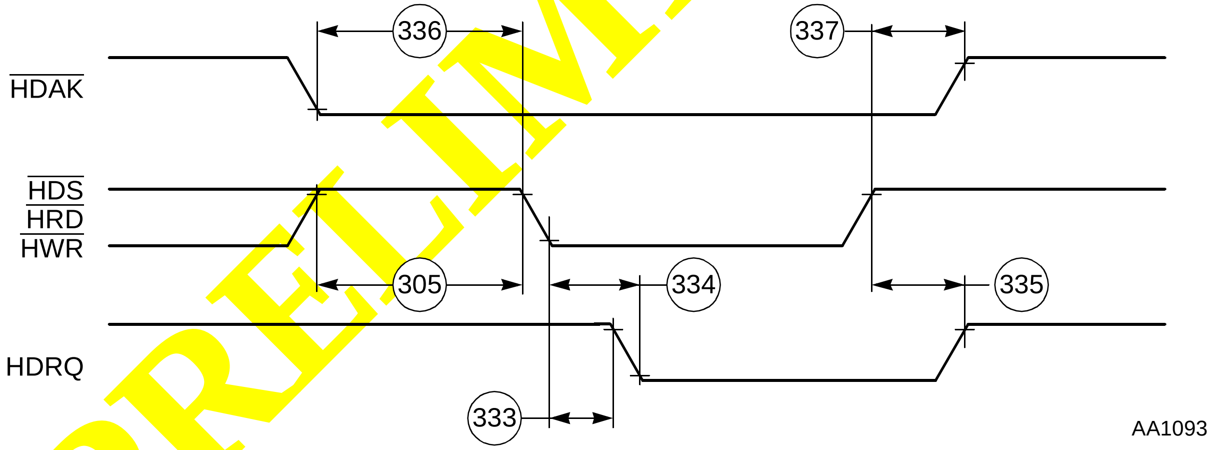


Figure 2-27 Universal Bus Mode DMA Access Timing

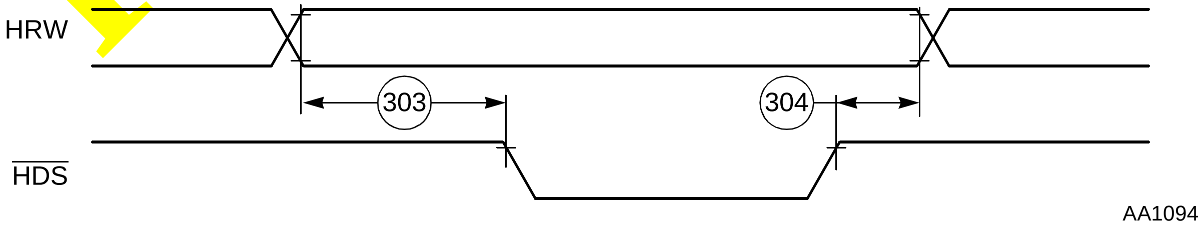


Figure 2-28 HRW to $\overline{HDS}$ Timing

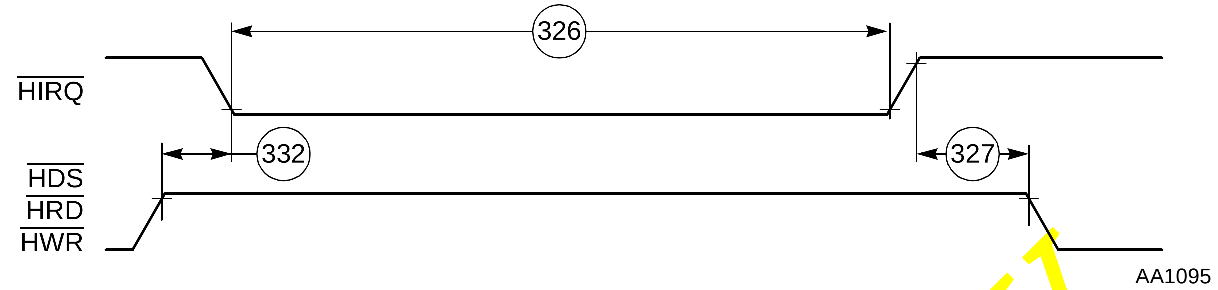


Figure 2-29 $\overline{\text{HIRQ}}$ Pulse Width (HIRH = 0)

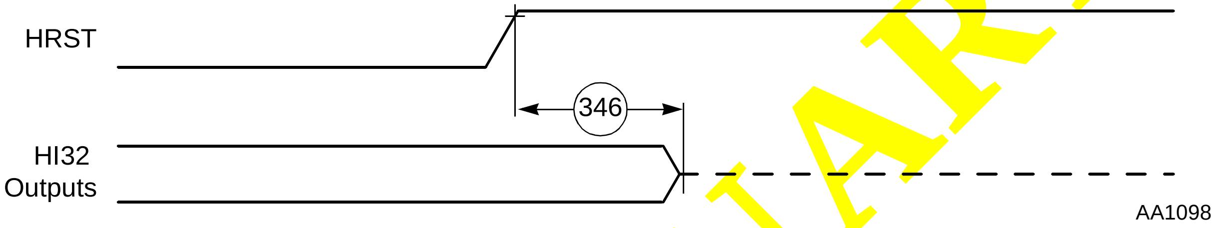


Figure 2-30 HRST Timing

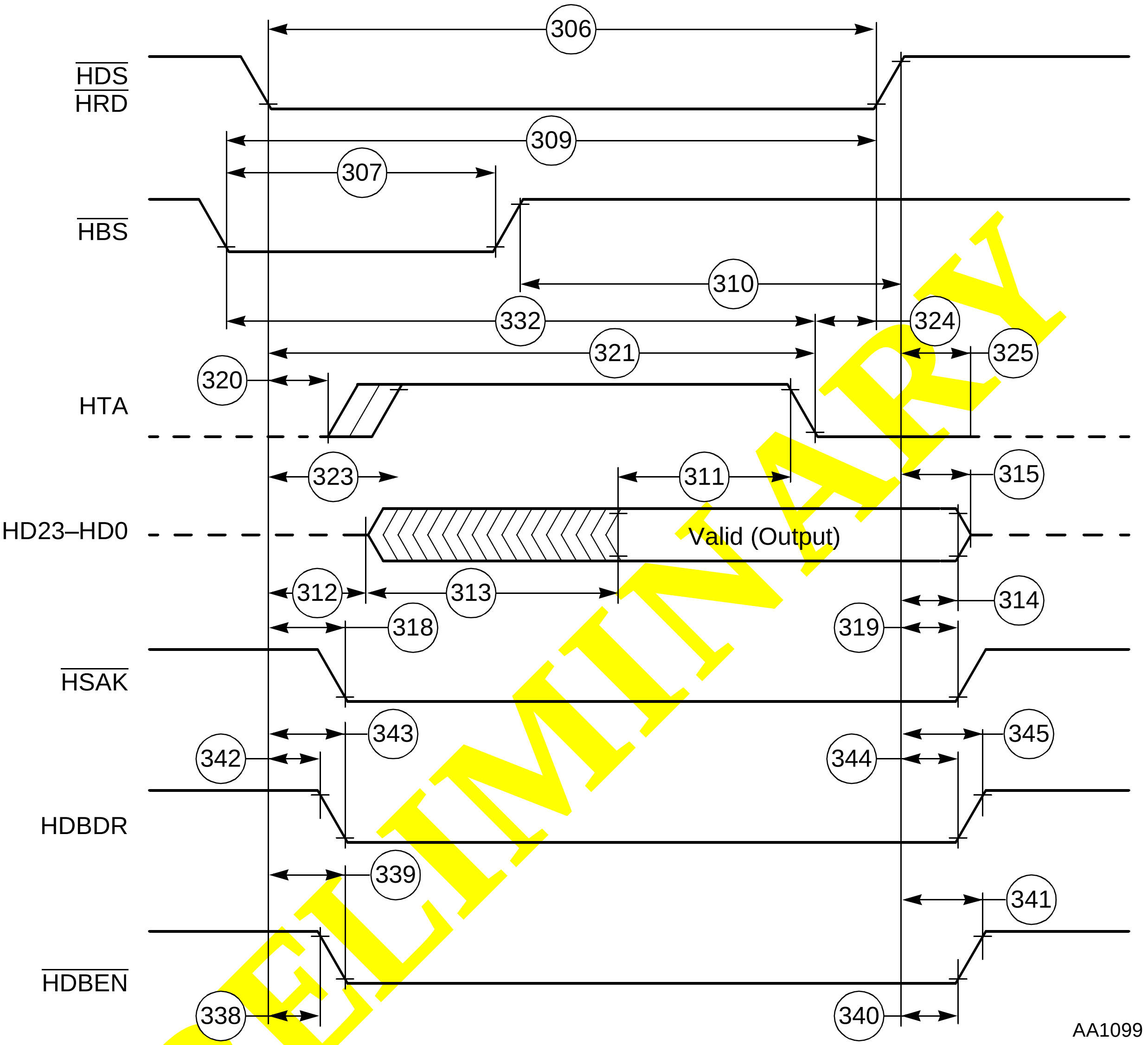


Figure 2-31 Read Timing

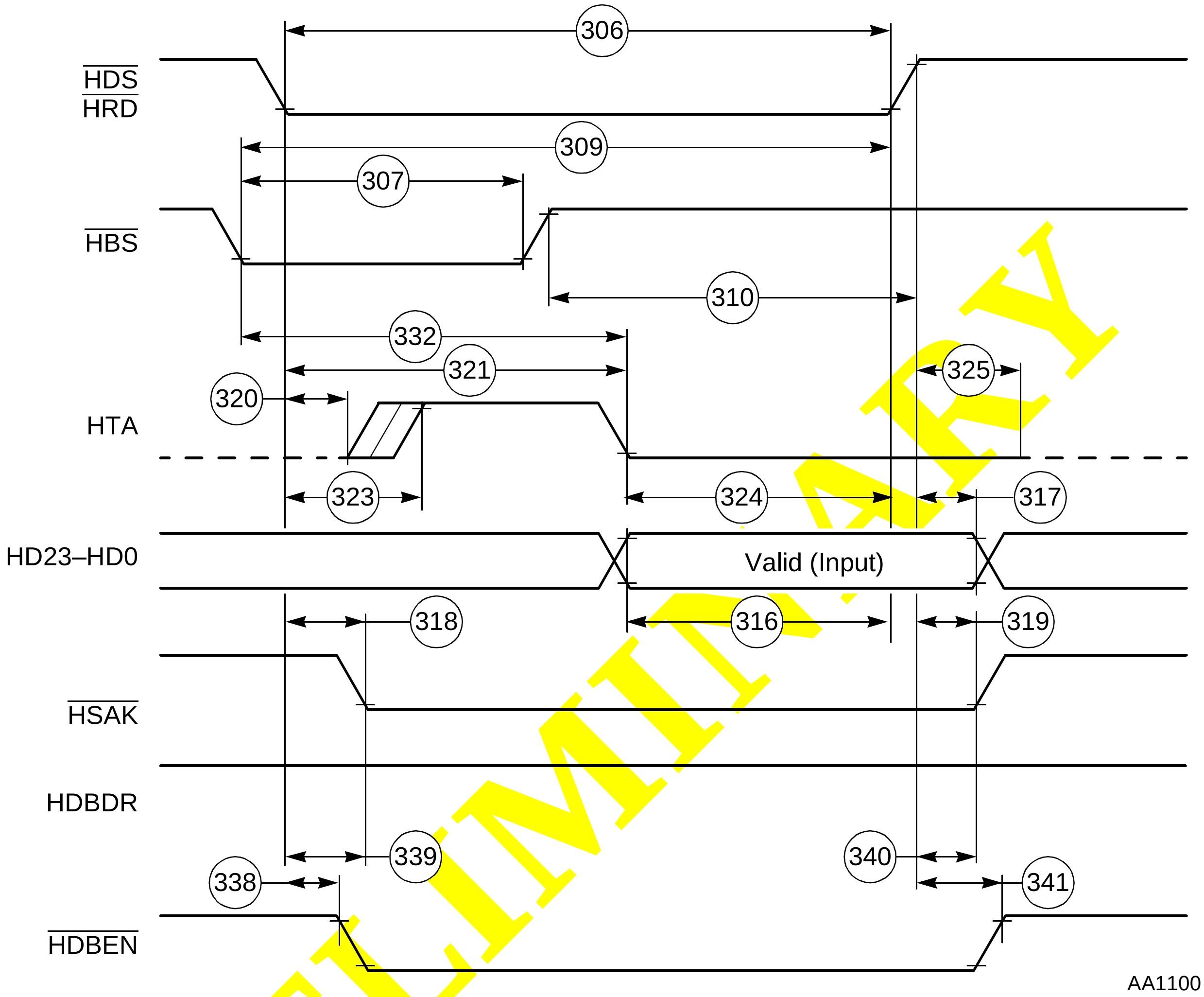


Figure 2-32 Write Timing

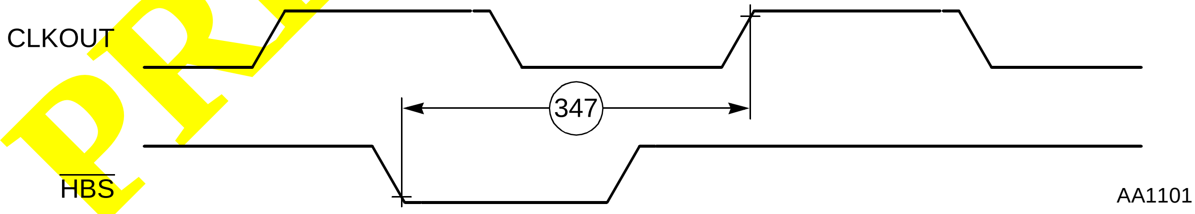


Figure 2-33 HBS Synchronous Timing

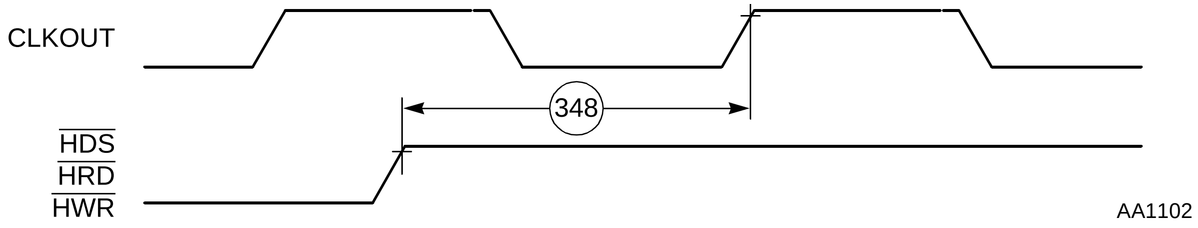


Figure 2-34 Data Strobe Synchronous Timing

Table 2-21 PCI Mode Timing Parameters[1]

No.	Characteristic[10]	Symbol	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
349	HCLK to Signal Valid Delay—Bussed Signals	t_{VAL}	2.0	11.0	2.0	11.0	2.0	11.0	ns
350	HCLK to Signal Valid Delay—Point to Point	$t_{VAL(ptp)}$	2.0	12.0	2.0	12.0	2.0	12.0	ns
351	Float to Active Delay	t_{ON}	2.0	—	2.0	—	2.0	—	ns
352	Active to Float Delay	t_{OFF}	—	28.0	—	28.0	—	28.0	ns
353	Input Set Up Time to HCLK—Bussed Signals	t_{SU}	7.0	—	7.0	—	7.0	—	ns
354	Input Set Up Time to HCLK—Point to Point	$t_{SU(ptp)}$	10.0, 12.0	—	10.0, 12.0	—	10.0, 12.0	—	ns
355	Input Hold Time from HCLK	t_H	0.0	—	0.0	—	0.0	—	ns
356	Reset Active Time After Power Stable	t_{RST}	1.0	—	1.0	—	1.0	—	ms
357	Reset Active Time After HCLK Stable	$t_{RST\text{-}CLK}$	100.0	—	100.0	—	100.0	—	µs
358	Reset Active to Output Float Delay	$t_{RST\text{-}OFF}$	—	40.0	—	40.0	—	40.0	ns
359	HCLK Cycle Time	t_{CYC}	30.0	—	30.0	—	30.0	—	ns
360	HCLK High Time	t_{HIGH}	12.0	—	11.0	—	11.0	—	ns
361	HCLK Low Time	t_{LOW}	12.0	—	11.0	—	11.0	—	ns

Notes:
1. For standard PCI timing, see the PCI Local Bus Specification, Rev. 2.0, especially Chapters 3 and 4.
2. The HI32 supports these timings for a PCI bus operating at 33 MHz for a DSP clock frequency of 56 MHz and above. The DSP core operating frequency should be greater than 5/3 of the PCI bus frequency to maintain proper PCI operation.
3. $\overline{\text{HGNT}}$ has a setup time of 10 ns. $\overline{\text{HREQ}}$ has a setup time of 12 ns.

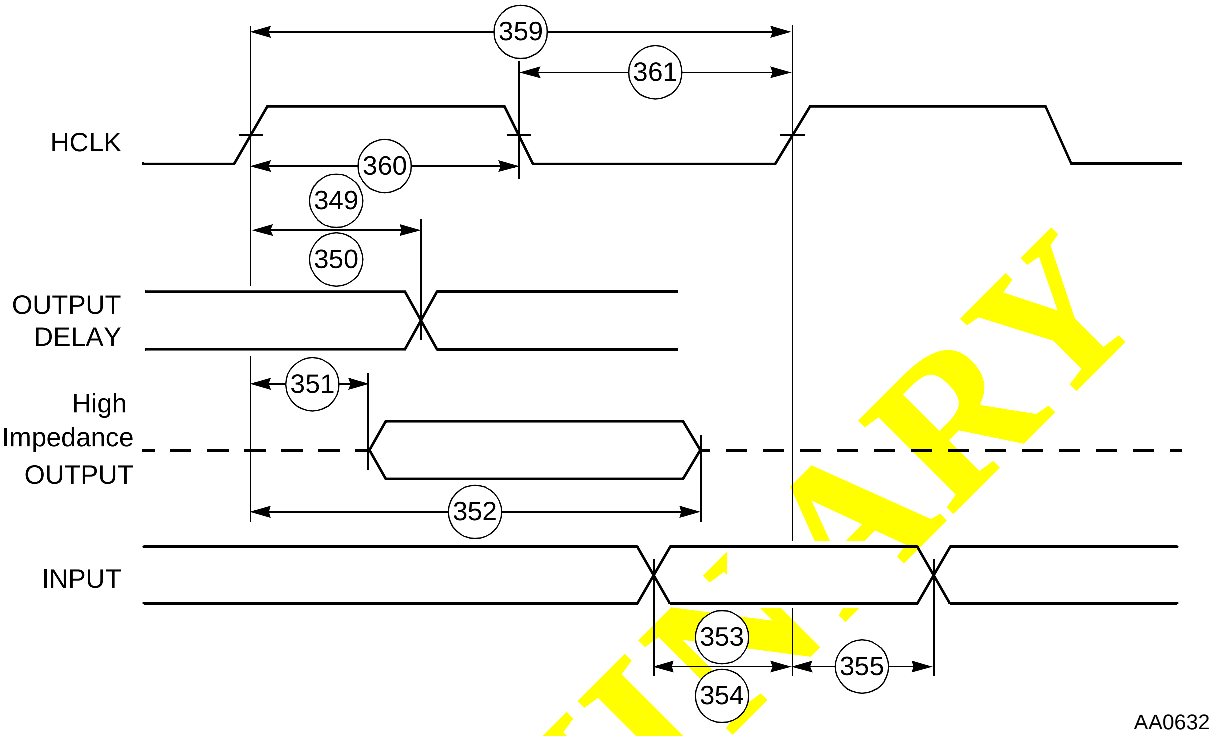


Figure 2-35 PCI Timing

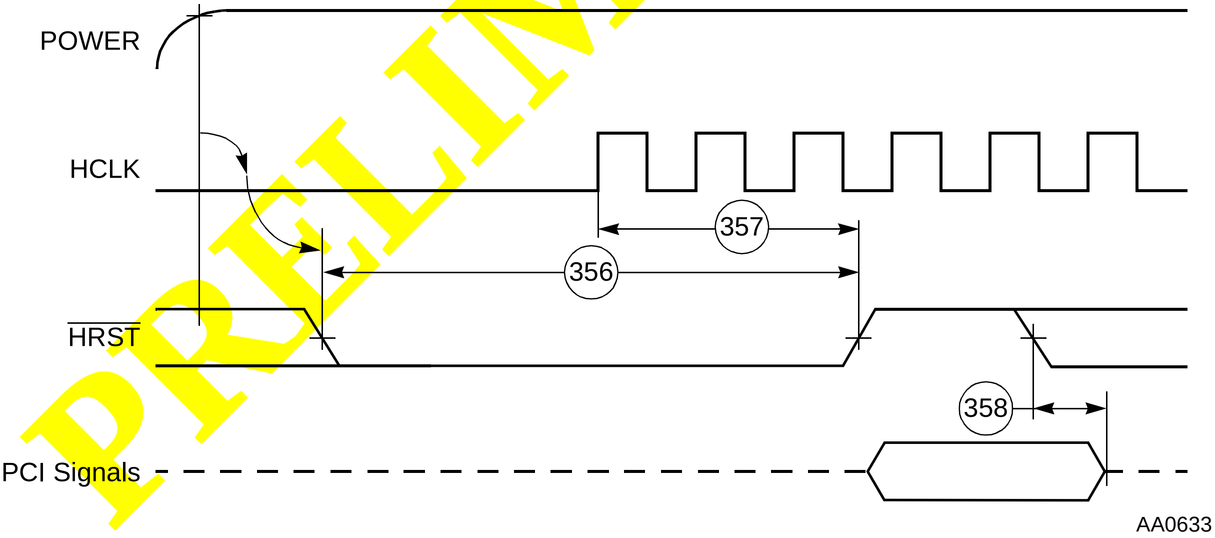


Figure 2-36 PCI Reset Timing

SCI TIMING

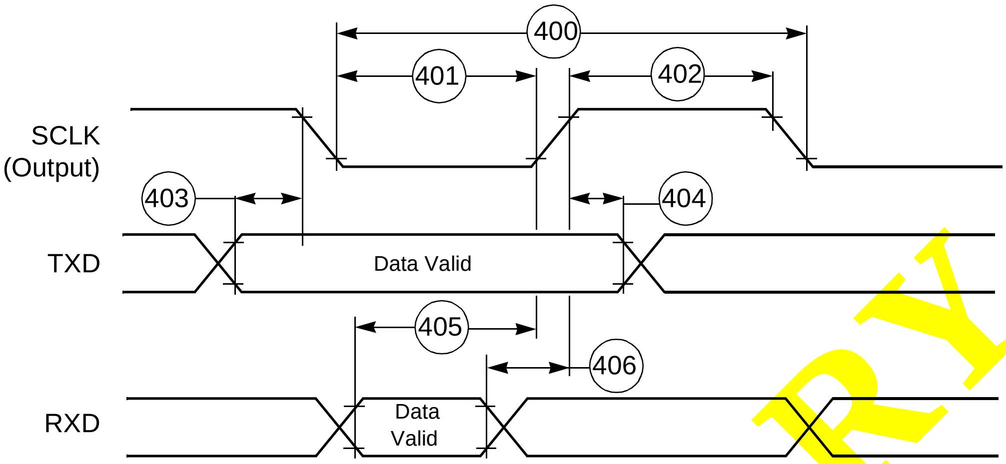
Table 2-22 SCI Timing

No.	Characteristics[1]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	**Max**	**Min**	**Max**	**Min**	**Max**	
400	Synchronous clock cycle	t_{SCC}[2]	$8 \times T_C$	121.0	—	100.0	—	80.0	—	ns
401	Clock low period		$t_{SCC}/2 - 10.0$	50.5	—	40.0	—	30.0	—	ns
402	Clock high period		$t_{SCC}/2 - 10.0$	50.5	—	40.0	—	30.0	—	ns
403	Output data setup to clock falling edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 17.0$	20.5	—	14.3	—	8.0	—	ns
404	Output data hold after clock rising edge (internal clock)		$t_{SCC}/4 - 0.5 \times T_C$	22.5	—	18.8	—	15.0	—	ns
405	Input data setup time before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C + 25.0$	63.0	—	56.3	—	50.0	—	ns
406	Input data not valid before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 5.5$	—	32.0	—	25.8	—	19.5	ns
407	Clock falling edge to output data valid (external clock)			—	32.0	—	32.0	—	32.0	ns
408	Output data hold after clock rising edge (external clock)		$T_C + 8.0$	23.0	—	20.5	—	18.0	—	ns
409	Input data setup time before clock rising edge (external clock)			0.0	—	0.0	—	0.0	—	ns
410	Input data hold time after clock rising edge (external clock)			9.0	—	9.0	—	9.0	—	ns
411	Asynchronous clock cycle	t_{ACC}[3]	$64 \times T_C$	969.7	—	800.0	—	640.0	—	ns
412	Clock low period		$t_{ACC}/2 - 10.0$	474.8	—	390.0	—	310.0	—	ns
413	Clock high period		$t_{ACC}/2 - 10.0$	474.8	—	390.0	—	310.0	—	ns

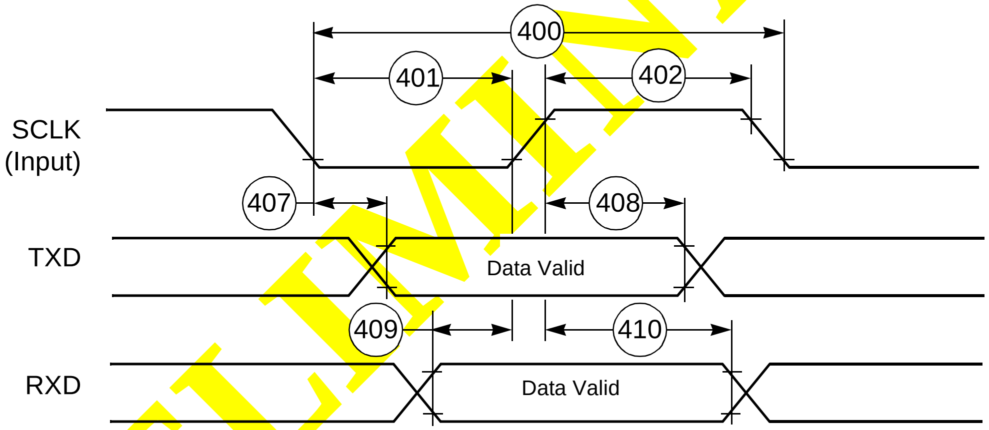
Table 2-22 SCI Timing (Continued)

No.	Characteristics[1]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
414	Output data setup to clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	458.8	—	370.0	—	290.0	—	ns
415	Output data hold afterclockrisingedge (internal clock)		$t_{ACC}/2 - 30.0$	458.8	—	370.0	—	290.0	—	ns

Notes:
1. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF + 2 TTL Loads
2. t_{SCC} = synchronous clock cycle time (For internal clock, t_{SCC} is determined by the SCI clock control register and $T_{C.}$)
3. t_{ACC} = asynchronous clock cycle time; value given for 1X Clock mode (For internal clock, t_{ACC} is determined by the SCI clock control register and $T_{C.}$)



a) Internal Clock



b) External Clock

Figure 2-37 SCI Synchronous Mode Timing

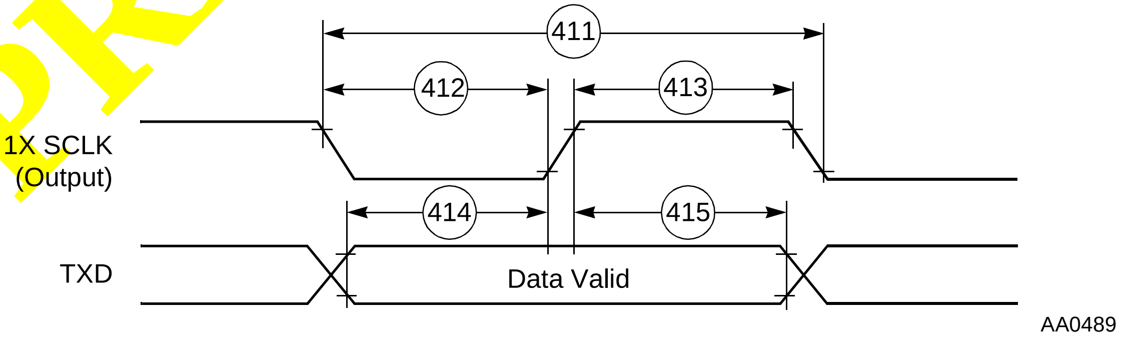


Figure 2-38 SCI Asynchronous Mode Timing

ESSI0/ESSI1 TIMING

Table 2-23 ESSI Timings

No.	Characteristics[4, 6, 7]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Cond-ition[5]	Unit
				Min	Max	Min	Max	Min	Max		
430	Clock cycle[1]	t_{SSICC}	$4 \times T_C$ $3 \times T_C$	60.6 45.5	— —	50.0 37.5	— —	40.0 30.0	— —	i ck x ck	ns
431	Clock high period • For internal clock • For external clock		 $2 \times T_C - 10.0$ $1.5 \times T_C$	 20.3 22.7	 — —	 15.0 18.8	 — —	 10.0 15.0	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $2 \times T_C - 10.0$ $1.5 \times T_C$	 20.3 22.7	 — —	 15.0 18.8	 — —	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bl) high			— —	37.0 22.0	— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bl) low			— —	37.0 22.0	— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (wr) high[2]			— —	39.0 24.0	— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
436	RXC rising edge to FSR out (wr) low[2]			— —	39.0 24.0	— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
437	RXC rising edge to FSR out (wl) high			— —	36.0 21.0	— —	36.0 21.0	— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (wl) low			— —	37.0 22.0	— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge			0.0 19.0	— —	0.0 19.0	— —	0.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	5.0 3.0	— —	5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[2]			23.0 1.0	— —	23.0 1.0	— —	23.0 1.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge			23.0 1.0	— —	23.0 1.0	— —	23.0 1.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	3.0 0.0	— —	3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge			0.0 19.0	— —	0.0 19.0	— —	0.0 19.0	— —	x ck i ck s	ns

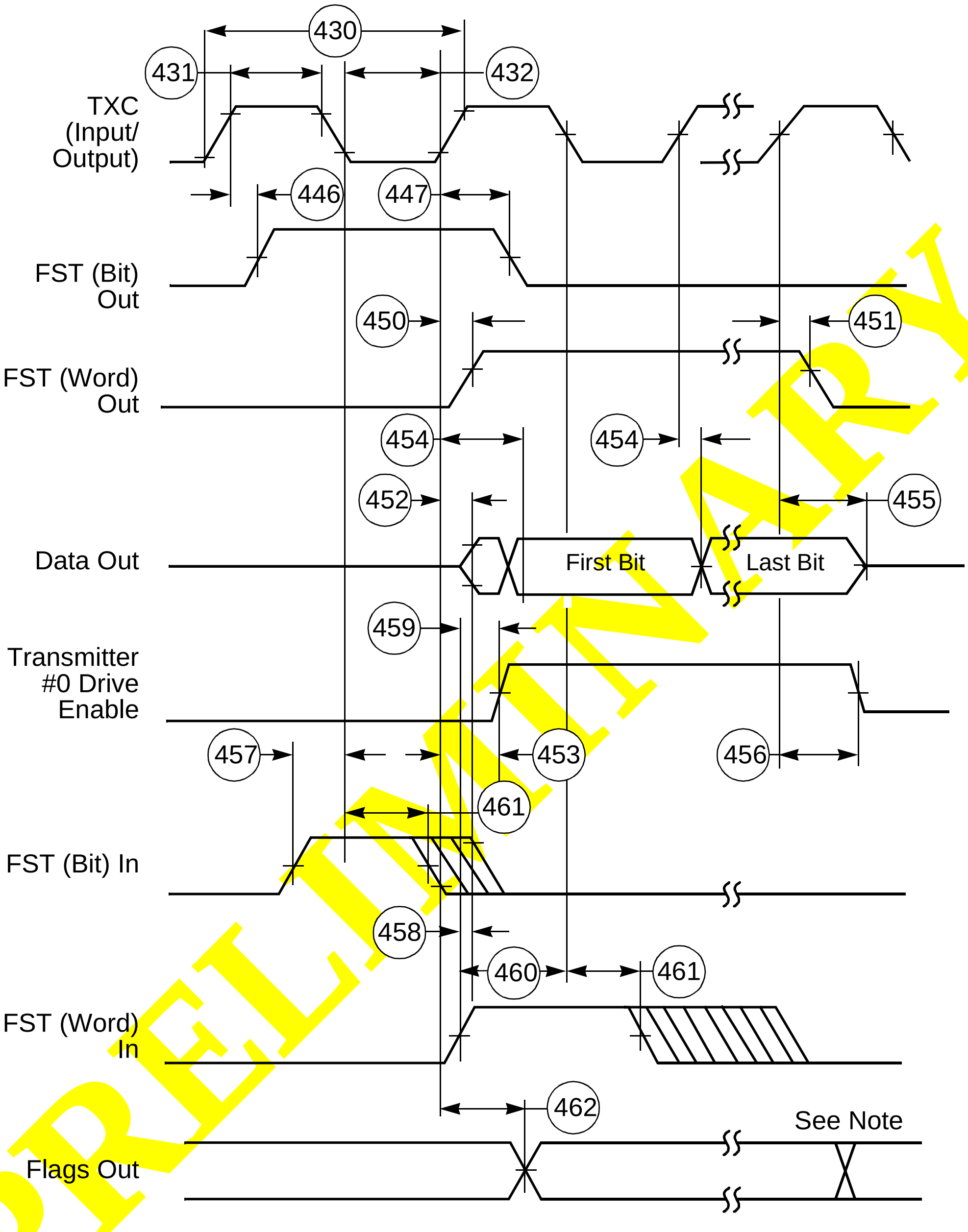
Table 2-23 ESSI Timings (Continued)

No.	Characteristics[4, 6, 7]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Condition[5]	Unit
				Min	Max	Min	Max	Min	Max		
445	Flags input hold time after RXC falling edge			6.0 0.0	— —	6.0 0.0	— —	6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bl) high			— —	29.0 15.0	— —	29.0 15.0	— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bl) low			— —	31.0 17.0	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (wr) high[2]			— —	31.0 17.0	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (wr) low[2]			— —	33.0 19.0	— —	33.0 19.0	— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (wl) high			— —	30.0 16.0	— —	30.0 16.0	— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (wl) low			— —	31.0 17.0	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance			— —	31.0 17.0	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
453	TXC rising edge to Transmitter #0 drive enable assertion			— —	34.0 20.0	— —	34.0 20.0	— —	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid		$35 + 0.5 \times T_C$ 21.0	— —	42.6 21.0	— —	41.3 21.0	— —	40.0 21.0	x ck i ck	ns
455	TXC rising edge to data out high impedance[3]			— —	31.0 16.0	— —	31.0 16.0	— —	31.0 16.0	x ck i ck	ns
456	TXC rising edge to Transmitter #0 drive enable deassertion[3]			— —	34.0 20.0	— —	34.0 20.0	— —	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr) setup time before TXC falling edge[2]			2.0 21.0	— —	2.0 21.0	— —	2.0 21.0	— —	x ck i ck	ns
458	FST input (wl) to data out enable from high impedance			—	27.0	—	27.0	—	27.0	—	ns
459	FST input (wl) to Transmitter #0 drive enable assertion			—	31.0	—	31.0	—	31.0	—	ns

Table 2-23 ESSI Timings (Continued)

No.	Characteristics[4, 6, 7]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Cond-ition[5]	Unit
				Min	Max	Min	Max	Min	Max		
460	FST input (wl) setup time before TXC falling edge			2.0 21.0	— —	2.0 21.0	— —	2.0 21.0	— —	x ck i ck	ns
461	FST input hold time after TXC falling edge			4.0 0.0	— —	4.0 0.0	— —	4.0 0.0	— —	x ck i ck	ns
462	Flag output valid after TXC rising edge			— —	32.0 18.0	— —	32.0 18.0	— —	32.0 18.0	x ck i ck	ns

Notes:
1. For the internal clock, the external clock cycle is defined by Icyc and the ESSI control register.
2. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as Bit Length Frame Sync signal), until the one before last bit clock of the first word in frame.
3. Periodically sampled and not 100% tested
4. $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$ + 2 TTL Loads
5. TXC (SCK Pin) = Transmit Clock
   RXC (SC0 or SCK Pin) = Receive Clock
   FST (SC2 Pin) = Transmit Frame Sync
   FSR (SC1 or SC2 Pin) Receive Frame Sync
6. i ck = Internal Clock
   x ck = External Clock
   i ck a = Internal Clock, Asynchronous mode
   (Asynchronous implies that TXC and RXC are two different clocks)
   i ck s = Internal Clock, Synchronous mode
   (Synchronous implies that TXC and RXC are the same clock)
7. bl = bit length
   wl = word length
   wr = word length relative



Note: 1. In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

AA0490

Figure 2-39 ESSI Transmitter Timing

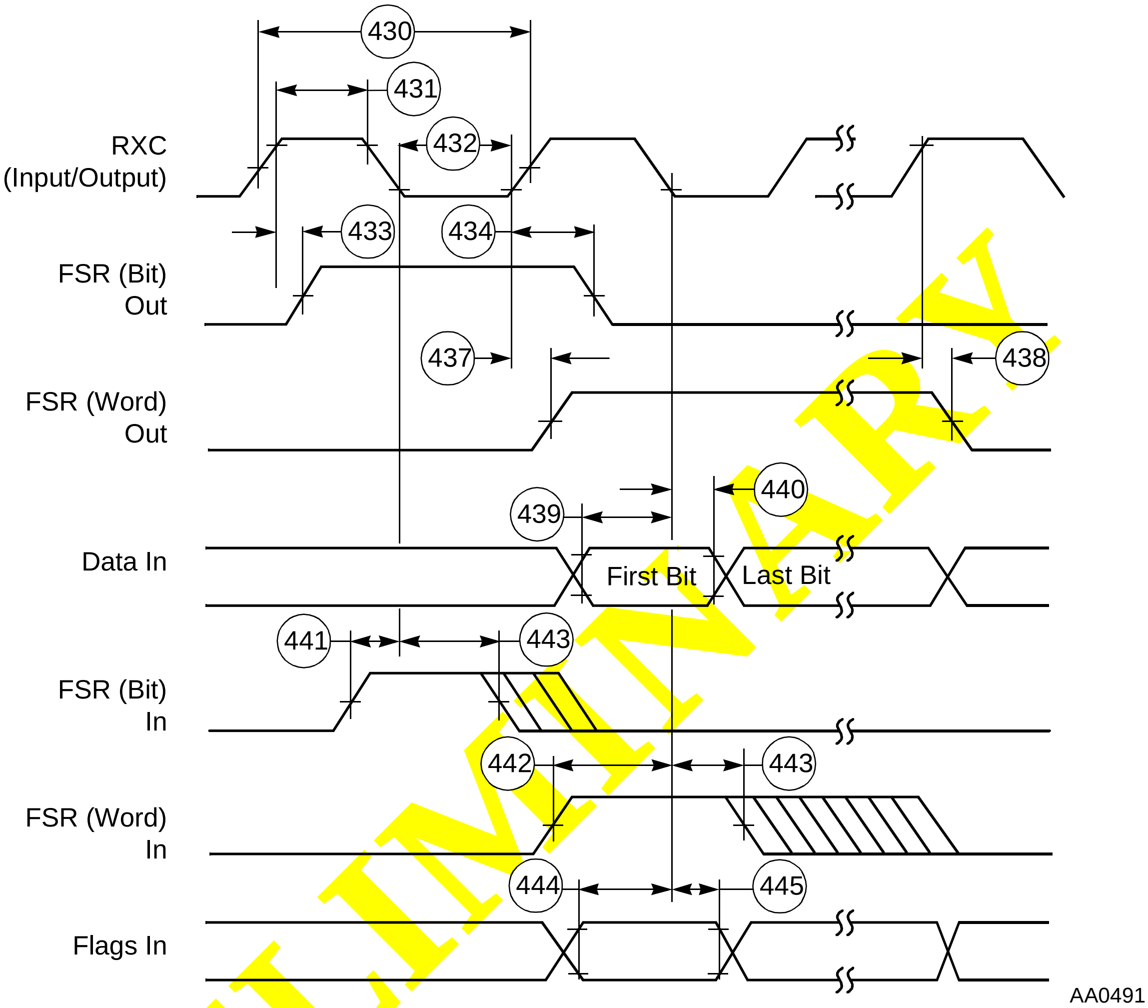


Figure 2-40 ESSI Receiver Timing

TIMER TIMING

Table 2-24 Timer Timing

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
480	TIO Low	2 × T_C + 2.0	32.5	—	27.0	—	22.0	—	ns
481	TIO High	2 × T_C + 2.0	32.5	—	27.0	—	22.0	—	ns
482	Timer setup time from TIO (Input) assertion to CLKOUT rising edge		9.0	15.15	9.0	12.5	9.0	10.0	ns
483	Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid caused by first interrupt instruction execution	10.25 × T_C + 1.0	156.0	—	129.1	—	103.5	—	ns
484	CLKOUT rising edge to TIO (Output) assertion • Minimum • Maximum	0.5 × T_C + 3.5 0.5 × T_C + 19.8	11.1 —	— 28.1	9.8 —	— 26.1	8.5 —	— 24.8	ns ns
485	CLKOUT rising edge to TIO (Output) deassertion • Minimum • Maximum	60.5 × T_C + 3.5 **66–80 MHz:** 0.5 × T_C + 19.8 **100 MHz**: 0.5 × T_C + 19.0	11.1 — —	— 28.1 —	9.8 — —	— 26.1 —	8.5 — —	— — 24.8	ns ns ns
Note: V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF + 2 TTL Loads									

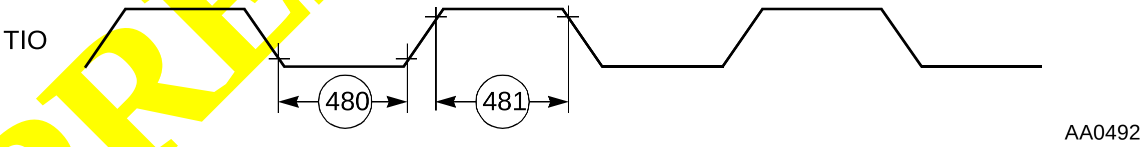


Figure 2-41 TIO Timer Event Input Restrictions

Preliminary Data

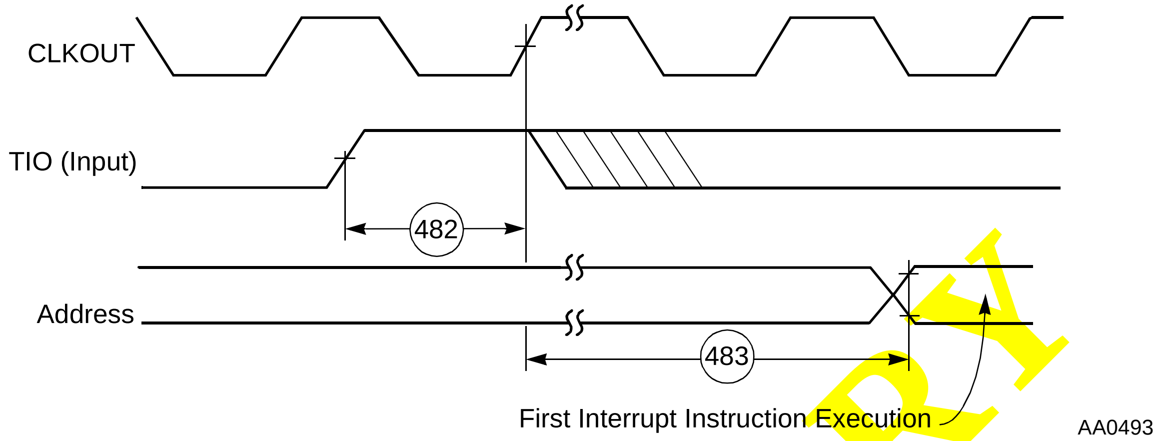


Figure 2-42 Timer Interrupt Generation

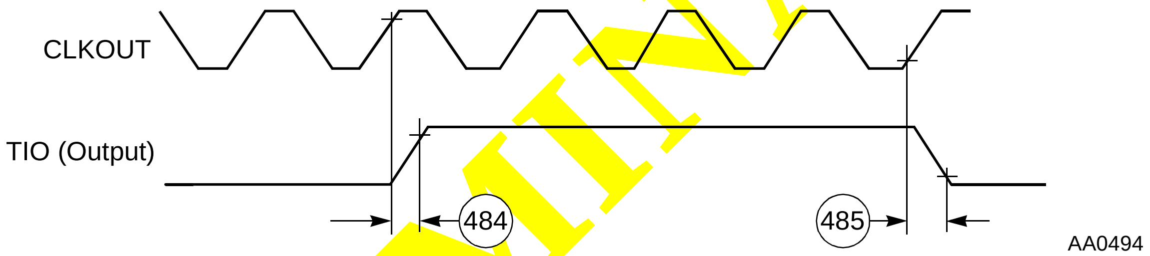


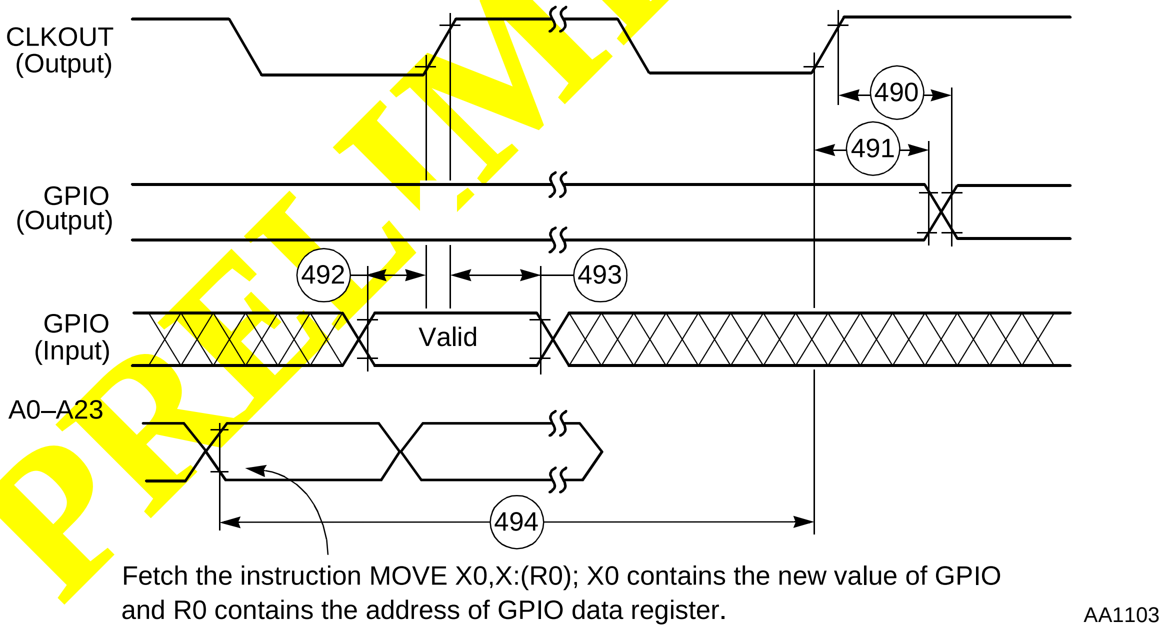
Figure 2-43 External Pulse Generation

GPIO TIMING

Table 2-25 GPIO Timing

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	31.0	—	31.0	—	31.0	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		3.0	—	3.0	—	3.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		12.0	—	12.0	—	12.0	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	0.0	—	0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	$6.75 \times T_C$	102.3	—	84.4	—	67.5	—	ns

Note: $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$ + 2 TTL Loads



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of GPIO data register.

Figure 2-44 GPIO Timing

JTAG TIMING

Table 2-26 JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	**Max**	
500	TCK frequency of operation = $1 / (T_C \times 3) \leq 22.0$ MHz	0.0	22.0	MHz
501	TCK cycle time in Crystal mode	45.0	—	ns
502	TCK clock pulse width measured at 1.5 V	20.0	—	ns
503	TCK rise and fall times	0.0	3.0	ns
504	Boundary scan input data setup time	5.0	—	ns
505	Boundary scan input data hold time	24.0	—	ns
506	TCK low to output data valid	0.0	40.0	ns
507	TCK low to output high impedance	0.0	40.0	ns
508	TMS, TDI data setup time	5.0	—	ns
509	TMS, TDI data hold time	25.0	—	ns
510	TCK low to TDO data valid	0.0	44.0	ns
511	TCK low to TDO high impedance	0.0	44.0	ns
512	$\overline{\text{TRST}}$ assert time	100.0	—	ns
513	$\overline{\text{TRST}}$ setup time to TCK low	40.0	—	ns

Notes:
1. $V_{CC} = 3.3$ V ± 0.3 V; $T_J = -40$°C to +100 °C, $C_L = 50$ pF + 2 TTL Loads
2. All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

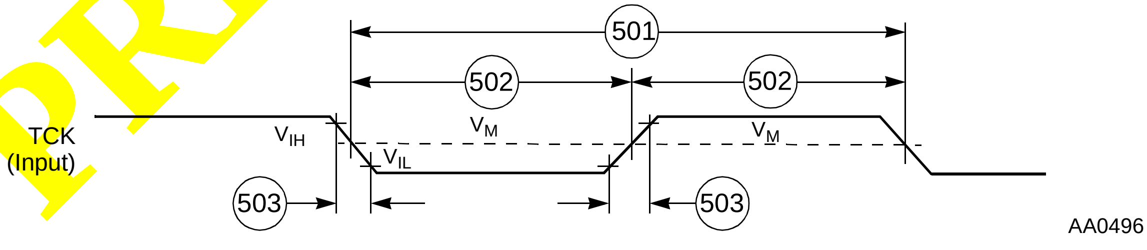


Figure 2-45 Test Clock Input Timing Diagram

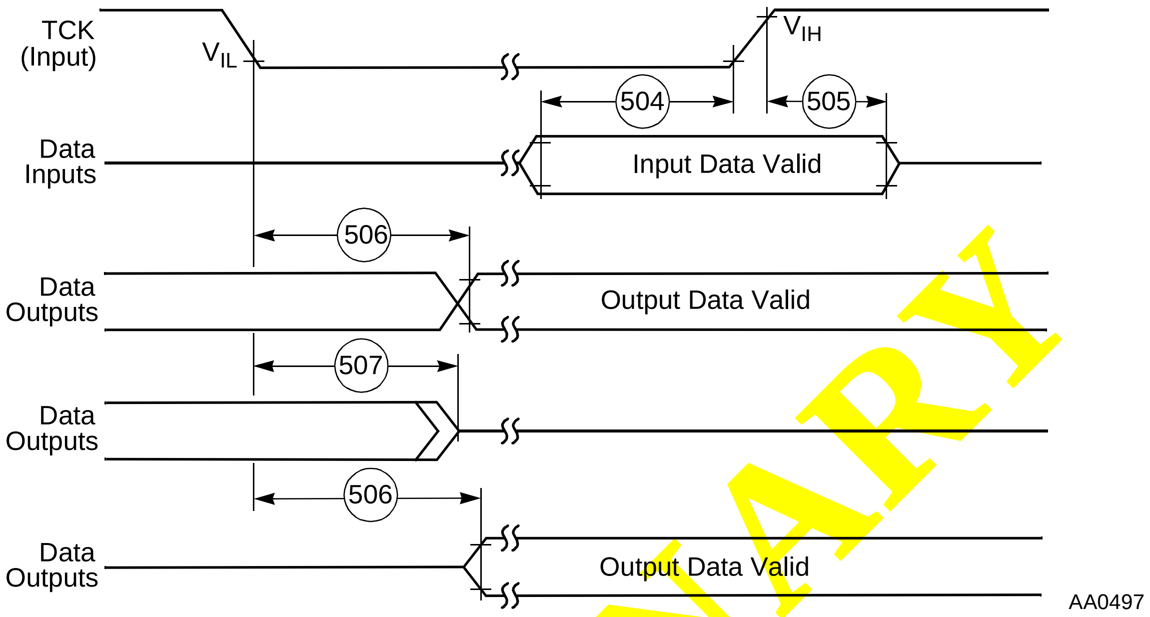


Figure 2-46 Boundary Scan (JTAG) Timing Diagram

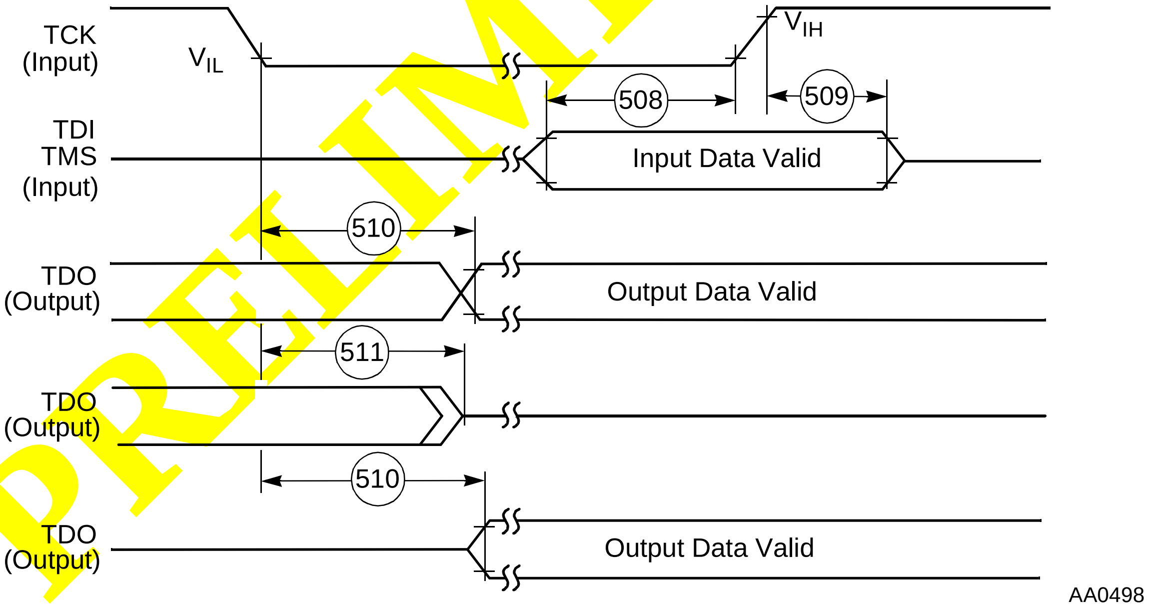


Figure 2-47 Test Access Port Timing Diagram

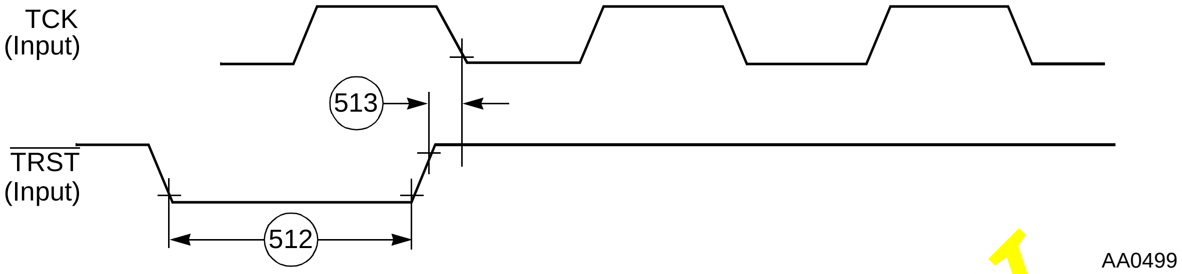


Figure 2-48 $\overline{\text{TRST}}$ Timing Diagram

OnCE MODULE TIMING

Table 2-27 OnCE Module Timing

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
500	TCK frequency of operation	$1 / (T_C \times 3)$, max 22.0 MHz	0.0	22.0	0.0	22.0	0.0	22.0	MHz
514	$\overline{\text{DE}}$ assertion time in order to enter Debug mode	$1.5 \times T_C + 10.0$	32.7	—	28.8	—	25.0	—	ns
515	Response time when DSP56301 is executing NOP instructions from internal memory	$5.5 \times T_C + 30.0$	—	113.3	—	98.8	—	85.0	ns
516	Debug acknowledge assertion time	$3 \times T_C + 10.0$	55.5	—	47.5	—	40.0	—	ns
Note: V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF + 2 TTL Loads									

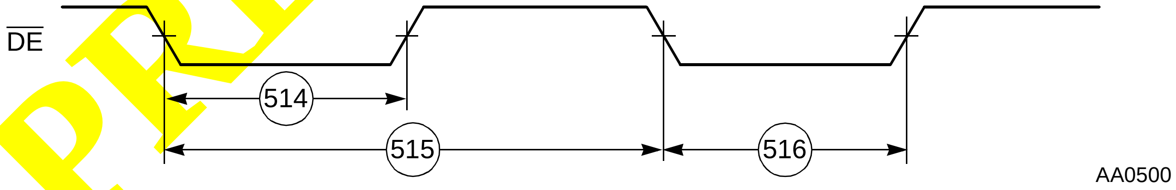


Figure 2-49 OnCE—Debug Request

SECTION 3

PACKAGING

PIN-OUT AND PACKAGE INFORMATION

This sections provides information about the available packages for this product, including diagrams of the package pinouts and tables describing how the signals described in **Section 1** are allocated for each package.

The DSP56301 is available in two package types:

- 208-pin Thin Quad Flat Pack (TQFP)
- 252-pin Plastic Ball Grid Array (PBGA)

TQFP Package Description

Top and bottom views of the TQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.

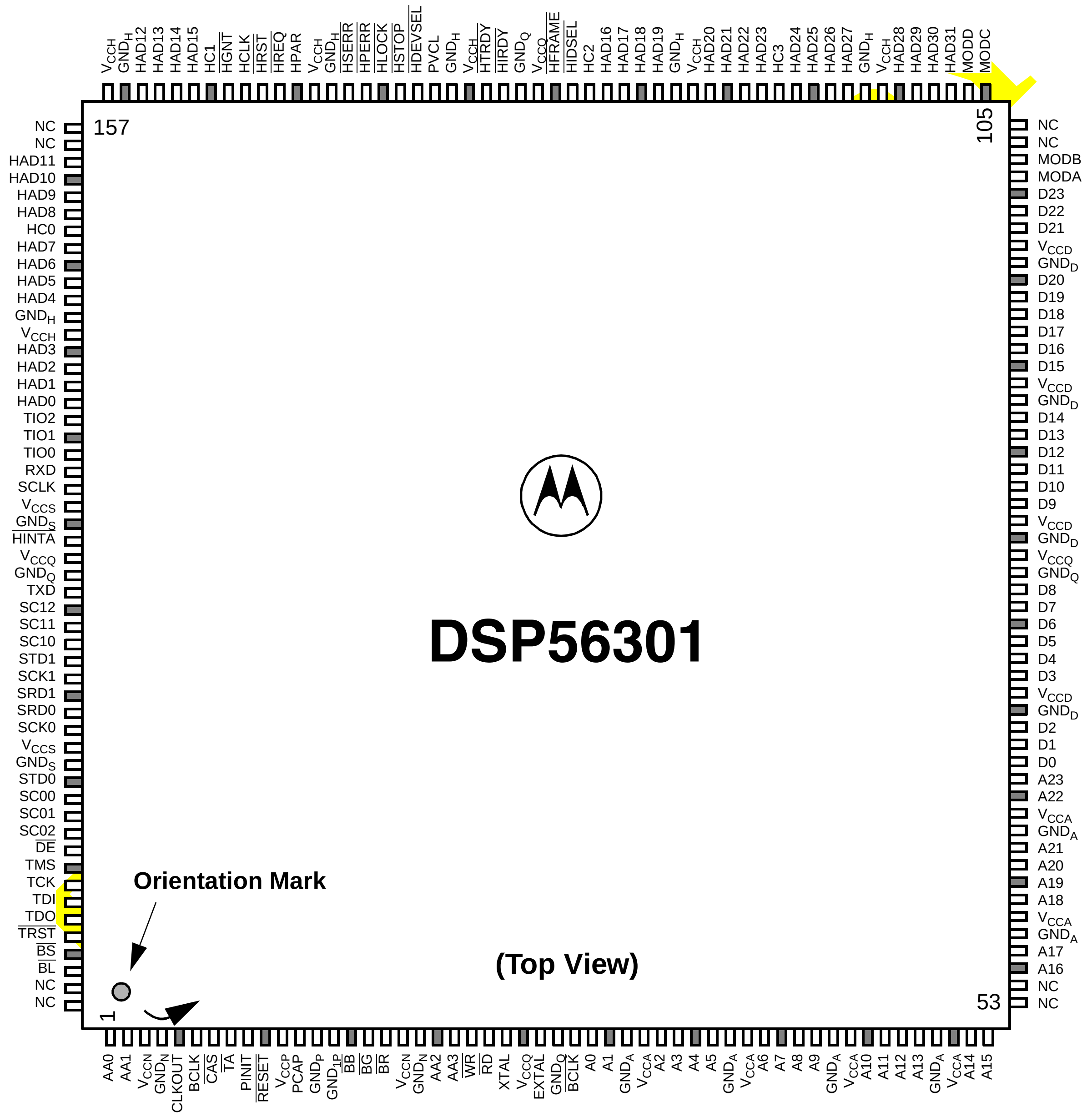


Figure 3-1 DSP56301 Thin Quad Flat Pack (TQFP), Top View

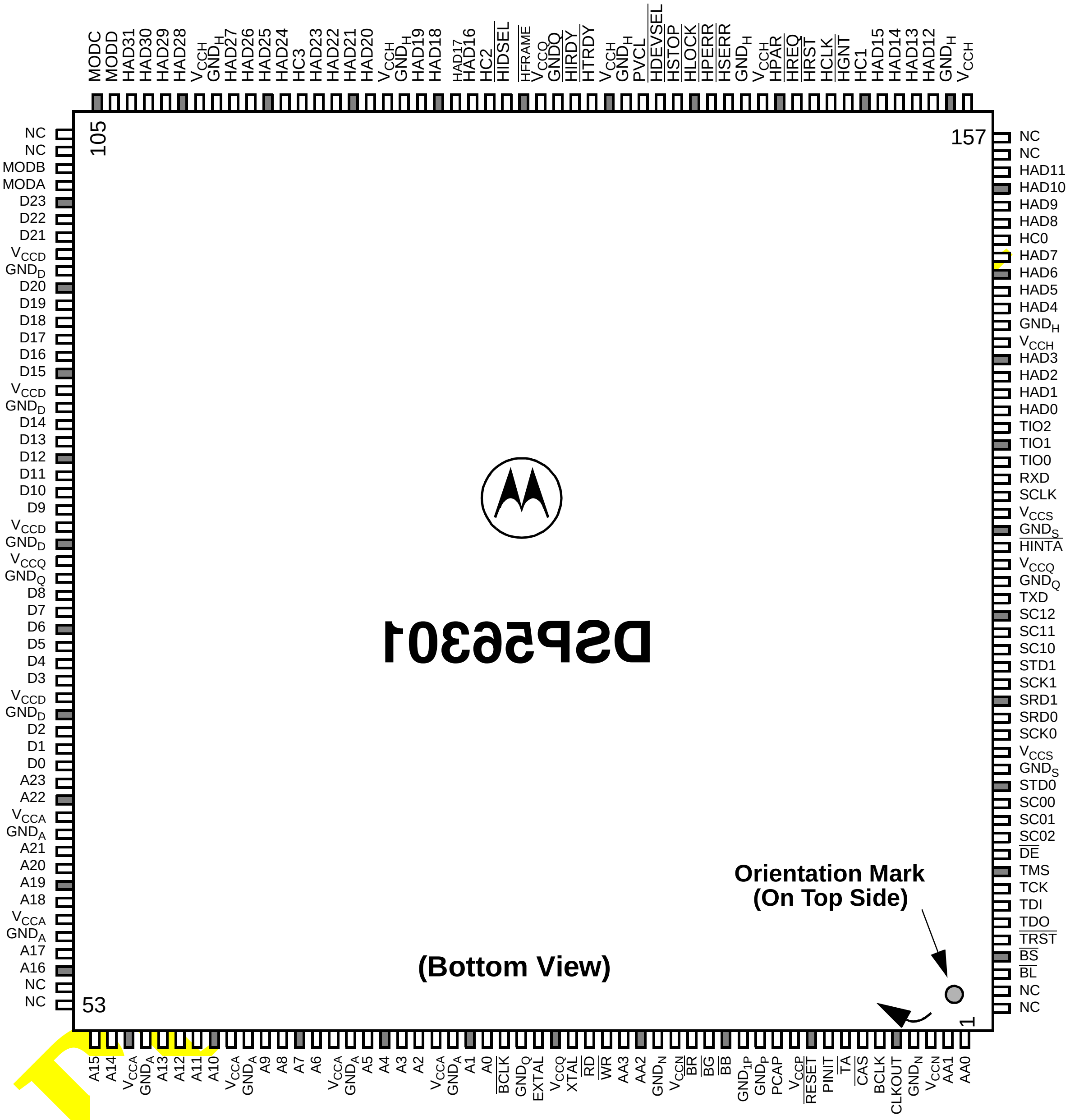


Figure 3-2 DSP56301 Thin Quad Flat Pack (TQFP), Bottom View

Table 3-1 DSP56301 TQFP Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	AA0/$\overline{\text{RAS0}}$	26	EXTAL	51	A14
2	AA1/$\overline{\text{RAS1}}$	27	GND_{Q}	52	A15
3	V_{CCN}	28	$\overline{\text{BCLK}}$	53	NC
4	GND_{N}	29	A0	54	NC
5	CLKOUT	30	A1	55	A16
6	BCLK	31	GND_{A}	56	A17
7	$\overline{\text{CAS}}$	32	V_{CCA}	57	GND_{A}
8	$\overline{\text{TA}}$	33	A2	58	V_{CCA}
9	PINIT/$\overline{\text{NMI}}$	34	A3	59	A18
10	$\overline{\text{RESET}}$	35	A4	60	A19
11	V_{CCP}	36	A5	61	A20
12	PCAP	37	GND_{A}	62	A21
13	GND_{P}	38	V_{CCA}	63	GND_{A}
14	GND_{1P}	39	A6	64	V_{CCA}
15	$\overline{\text{BB}}$	40	A7	65	A22
16	$\overline{\text{BG}}$	41	A8	66	A23
17	$\overline{\text{BR}}$	42	A9	67	D0
18	V_{CCN}	43	GND_{A}	68	D1
19	GND_{N}	44	V_{CCA}	69	D2
20	AA2/$\overline{\text{RAS2}}$	45	A10	70	GND_{D}
21	AA3/$\overline{\text{RAS3}}$	46	A11	71	V_{CCD}
22	$\overline{\text{WR}}$	47	A12	72	D3
23	$\overline{\text{RD}}$	48	A13	73	D4
24	XTAL	49	GND_{A}	74	D5
25	V_{CCQ}	50	V_{CCA}	75	D6

Table 3-1 DSP56301 TQFP Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
76	D7	101	MODA / $\overline{\text{IRQA}}$	126	HAD17 or HD9
77	D8	102	MODB / $\overline{\text{IRQB}}$	127	HAD16 or HD8
78	GND$_Q$	103	NC	128	HC2 / $\overline{\text{HBE2}}$, HA2, or PB18
79	V$_{CCQ}$	104	NC	129	$\overline{\text{HIDSEL}}$ or $\overline{\text{HRD}}$ / $\overline{\text{HDS}}$
80	GND$_D$	105	MODC / $\overline{\text{IRQC}}$	130	$\overline{\text{HFRAME}}$
81	V$_{CCD}$	106	MODD / $\overline{\text{IRQD}}$	131	V$_{CCQ}$
82	D9	107	HAD31 or HD23	132	GND$_Q$
83	D10	108	HAD30 or HD22	133	$\overline{\text{HIRDY}}$, $\overline{\text{HDBDR}}$, or PB21
84	D11	109	HAD29 or HD21	134	$\overline{\text{HTRDY}}$, $\overline{\text{HDBEN}}$, or PB20
85	D12	110	HAD28 or HD20	135	V$_{CCH}$
86	D13	111	V$_{CCH}$	136	GND$_H$
87	D14	112	GND$_H$	137	PVCL
88	GND$_D$	113	HAD27 or HD19	138	$\overline{\text{HDEVSEL}}$, $\overline{\text{HSAK}}$, or PB22
89	V$_{CCD}$	114	HAD26 or HD18	139	$\overline{\text{HSTOP}}$ or $\overline{\text{HWR}}$ / HRW
90	D15	115	HAD25 or HD17	140	$\overline{\text{HLOCK}}$, $\overline{\text{HBS}}$, or PB23
91	D16	116	HAD24 or HD16	141	$\overline{\text{HPERR}}$ or HDRQ
92	D17	117	HC3 / $\overline{\text{HBE3}}$ or PB19	142	$\overline{\text{HSERR}}$ or $\overline{\text{HIRQ}}$
93	D18	118	HAD23 or HD15	143	GND$_H$
94	D19	119	HAD22 or HD14	144	V$_{CCH}$
95	D20	120	HAD21 or HD13	145	HPAR or $\overline{\text{HDAK}}$
96	GND$_D$	121	HAD20 or HD12	146	$\overline{\text{HREQ}}$ or HTA
97	V$_{CCD}$	122	V$_{CCH}$	147	$\overline{\text{HRST}}$ or HRST
98	D21	123	GND$_H$	148	HCLK
99	D22	124	HAD19 or HD11	149	$\overline{\text{HGNT}}$ or HAEN
100	D23	125	HAD18 or HD10	150	HC1 / $\overline{\text{HBE1}}$, HA1, or PB17

Table 3-1 DSP56301 TQFP Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
151	HAD15, HD7, or PB15	171	HAD2, HA5, or PB2	191	SRD0 or PC4
152	HAD14, HD6, or PB14	172	HAD1, HA4, or PB1	192	SCK0 or PC3
153	HAD13, HD5, or PB13	173	HAD0, HA3, or PB0	193	V_{CCS}
154	HAD12, HD4, or PB12	174	TIO2	194	GND_S
155	GND_H	175	TIO1	195	STD0 or PC5
156	V_{CCH}	176	TIO0	196	SC00 or PC0
157	NC	177	RXD or PE0	197	SC01 or PC1
158	NC	178	SCLK or PE2	198	SC02 or PC2
159	HAD11, HD3, or PB11	179	V_{CCS}	199	$\overline{\text{DE}}$
160	HAD10, HD2, or PB10	180	GND_S	200	TMS
161	HAD9, HD1, or PB9	181	$\overline{\text{HINTA}}$	201	TCK
162	HAD8, HD0, or PB8	182	V_{CCQ}	202	TDI
163	HC0/$\overline{\text{HBE0}}$, HA0, or PB16	183	GND_Q	203	TDO
164	HAD7, HA10, or PB7	184	TXD or PE1	204	$\overline{\text{TRST}}$
165	HAD6, HA9, or PB6	185	SC12 or PD2	205	$\overline{\text{BS}}$
166	HAD5, HA8, or PB5	186	SC11 or PD1	206	$\overline{\text{BL}}$
167	HAD4, HA7, or PB4	187	SC10 or PD0	207	NC
168	GND_H	188	STD1 or PD5	208	NC
169	V_{CCH}	189	SCK1 or PD3		
170	HAD3, HA6, or PB3	190	SRD1 or PD4		

Note:

1. Signal names are based on configured functionality. Most pins supply a single signal. Some pins provide a signal with dual functionality, such as the MODx/$\overline{\text{IRQx}}$ pins that select an operating mode after $\overline{\text{RESET}}$ is deasserted, but act as interrupt lines during operation. Some pins have two or more configurable functions; names assigned to these pins indicate the function for a specific configuration. For example, Pin 165 is address/data line HAD6 in PCI bus mode, address line HA9 in non-PCI bus mode, or GPIO line PB6 when the GPIO function is enabled for this pin.
2. NC stands for Not Connected. These pins are reserved for future development. Do not connect and line, component, trace, or via to these pins.

Table 3-2 DSP56301 TQFP Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	29	AA1	2	D21	98
A1	30	AA2	20	D22	99
A10	45	AA3	21	D23	100
A11	46	$\overline{BB}$	15	D3	72
A12	47	BCLK	6	D4	73
A13	48	$\overline{BCLK}$	28	D5	74
A14	51	$\overline{BG}$	16	D6	75
A15	52	$\overline{BL}$	206	D7	76
A16	55	$\overline{BR}$	17	D8	77
A17	56	$\overline{BS}$	205	D9	82
A18	59	$\overline{CAS}$	7	$\overline{DE}$	199
A19	60	CLKOUT	5	EXTAL	26
A2	33	D0	67	GND_{1P}	14
A20	61	D1	68	GND_A	31
A21	62	D10	83	GND_A	37
A22	65	D11	84	GND_A	43
A23	66	D12	85	GND_A	49
A3	34	D13	86	GND_A	57
A4	35	D14	87	GND_A	63
A5	36	D15	90	GND_D	70
A6	39	D16	91	GND_D	80
A7	40	D17	92	GND_D	88
A8	41	D18	93	GND_D	96
A9	42	D19	94	GND_H	112
		D2	69		
AA0	1	D20	95	GND_H	123

Table 3-2 DSP56301 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND$_H$	136	HAD0	173	HAD31	107
GND$_H$	143	HAD1	172	HAD4	167
GND$_H$	155	HAD10	160	HAD5	166
GND$_H$	168	HAD11	159	HAD6	165
GND$_N$	4	HAD12	154	HAD7	164
GND$_N$	19	HAD13	153	HAD8	162
GND$_P$	13	HAD14	152	HAD9	161
GND$_Q$	27	HAD15	151	HAEN	149
GND$_Q$	78	HAD16	127	$\overline{HBE0}$	163
GND$_Q$	132	HAD17	126	$\overline{HBE1}$	150
GND$_Q$	183	HAD18	125	$\overline{HBE2}$	128
GND$_Q$	183	HAD19	124	$\overline{HBE3}$	117
GND$_S$	180	HAD2	171	$\overline{HBS}$	140
GND$_S$	194	HAD20	121	HC0	163
HA0	163	HAD21	120	HC1	150
HA1	150	HAD22	119	HC2	128
HA10	164	HAD23	118	HC3	117
HA2	128	HAD24	116	HCLK	148
HA3	173	HAD25	115	HD0	162
HA4	172	HAD26	114	HD1	161
HA5	171	HAD27	113	HD10	125
HA6	170	HAD28	110	HD11	124
HA7	167	HAD29	109	HD12	121
HA8	166	HAD3	170	HD13	120
HA9	165	HAD30	108	HD14	119

Table 3-2 DSP56301 TQFP Signal Identification by Name (Continued)

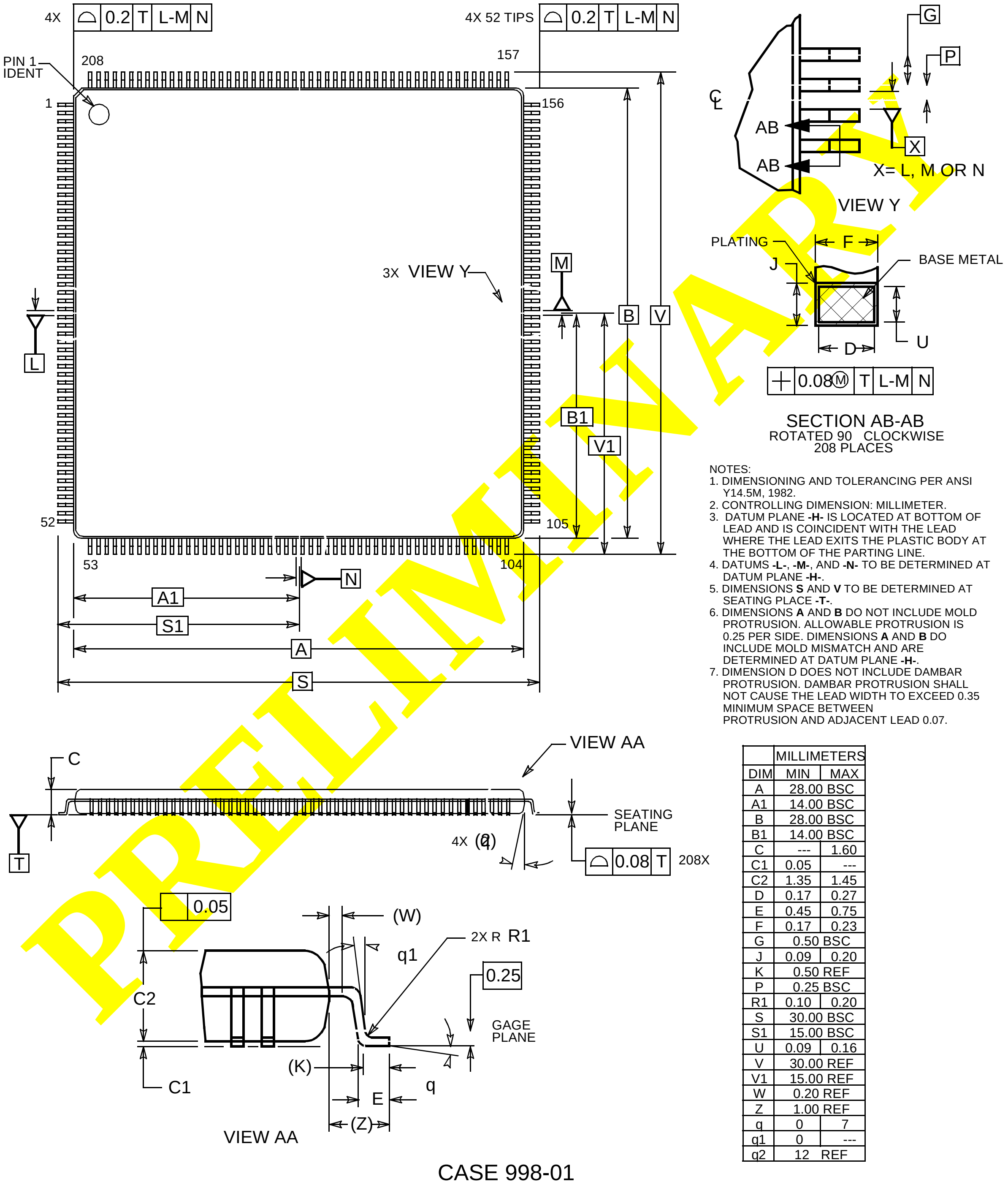
Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
HD15	118	HIDSEL	129	NC	28
HD16	116	$\overline{\mathrm{HINTA}}$	181	NC	53
HD17	115	$\overline{\mathrm{HIRDY}}$	133	NC	54
HD18	114	$\overline{\mathrm{HIRQ}}$	142	NC	103
HD19	113	$\overline{\mathrm{HLOCK}}$	140	NC	104
HD2	160	HPAR	145	NC	157
HD20	110	$\overline{\mathrm{HPERR}}$	141	NC	158
HD21	109	$\overline{\mathrm{HRD}}$	129	NC	207
HD22	108	$\overline{\mathrm{HREQ}}$	146	NC	208
HD23	107	$\overline{\mathrm{HRST}}$ / HRST	147	$\overline{\mathrm{NMI}}$	9
HD3	159	HRW	139	PB0	173
HD4	154	$\overline{\mathrm{HSAK}}$	138	PB1	172
HD5	153	$\overline{\mathrm{HSERR}}$	142	PB10	160
HD6	152	$\overline{\mathrm{HSTOP}}$	139	PB11	159
HD7	151	HTA	146	PB12	154
HD8	127	$\overline{\mathrm{HTRDY}}$	134	PB13	153
HD9	126	$\overline{\mathrm{HWR}}$	139	PB14	152
$\overline{\mathrm{HDAK}}$	145	$\overline{\mathrm{IRQA}}$	101	PB15	151
$\overline{\mathrm{HDBDR}}$	133	$\overline{\mathrm{IRQB}}$	102	PB16	163
$\overline{\mathrm{HDBEN}}$	134	$\overline{\mathrm{IRQC}}$	105	PB17	150
$\overline{\mathrm{HDEVSEL}}$	138	$\overline{\mathrm{IRQD}}$	106	PB18	128
HDRQ	141	MODA	101	PB19	117
$\overline{\mathrm{HDS}}$	129	MODB	102	PB2	171
$\overline{\mathrm{HFRAME}}$	130	MODC	105	PB20	134
$\overline{\mathrm{HGNT}}$	149	MODD	106	PB21	133

Table 3-2 DSP56301 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
PB22	138	PINIT	9	TDO	203
PB23	140	PVCL	137	TIO0	176
PB3	170	$\overline{\text{RAS0}}$	1	TIO1	175
PB4	167	$\overline{\text{RAS1}}$	2	TIO2	174
PB5	166	$\overline{\text{RAS2}}$	20	TMS	200
PB6	165	$\overline{\text{RAS3}}$	21	$\overline{\text{TRST}}$	204
PB7	164	$\overline{\text{RD}}$	23	TXD	184
PB8	162	$\overline{\text{RESET}}$	10	V_{CCA}	32
PB9	161	RXD	177	V_{CCA}	38
PC0	196	SC00	196	V_{CCA}	44
PC1	197	SC01	197	V_{CCA}	50
PC2	198	SC02	198	V_{CCA}	58
PC3	192	SC10	187	V_{CCA}	64
PC4	191	SC11	186	V_{CCD}	71
PC5	195	SC12	185	V_{CCD}	81
PCAP	12	SCK0	192	V_{CCD}	89
PD0	187	SCK1	189	V_{CCD}	97
PD1	186	SCLK	178	V_{CCH}	111
PD2	185	SRD0	191	V_{CCH}	122
PD3	189	SRD1	190	V_{CCH}	135
PD4	190	STD0	195	V_{CCH}	144
PD5	188	STD1	188	V_{CCH}	156
PE0	177	$\overline{\text{TA}}$	8	V_{CCH}	169
PE1	184	TCK	201	V_{CCN}	3
PE2	178	TDI	202	V_{CCN}	18
V_{CCP}	11	V_{CCQ}	131	V_{CCS}	193
V_{CCQ}	25	V_{CCQ}	182	$\overline{\text{WR}}$	22
V_{CCQ}	79	V_{CCS}	179	XTAL	24

Note: NC stands for Not Connected. These pins are reserved for future development. Do not connect and line, component, trace, or via to these pins.

TQFP Package Mechanical Drawing



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE **-H-** IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS **-L-**, **-M-**, AND **-N-** TO BE DETERMINED AT DATUM PLANE **-H-**.
5. DIMENSIONS **S** AND **V** TO BE DETERMINED AT SEATING PLACE **-T-**.
6. DIMENSIONS **A** AND **B** DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS **A** AND **B** DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE **-H-**.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35 MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	28.00 BSC	
A1	14.00 BSC	
B	28.00 BSC	
B1	14.00 BSC	
C	---	1.60
C1	0.05	---
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.10	0.20
S	30.00 BSC	
S1	15.00 BSC	
U	0.09	0.16
V	30.00 REF	
V1	15.00 REF	
W	0.20 REF	
Z	1.00 REF	
q	0	7
q1	0	---
q2	12 REF	

CASE 998-01

Figure 3-3 DSP56301 Mechanical Information, 208-pin TQFP Package

PBGA Package Description

Top and bottom views of the PBGA package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.

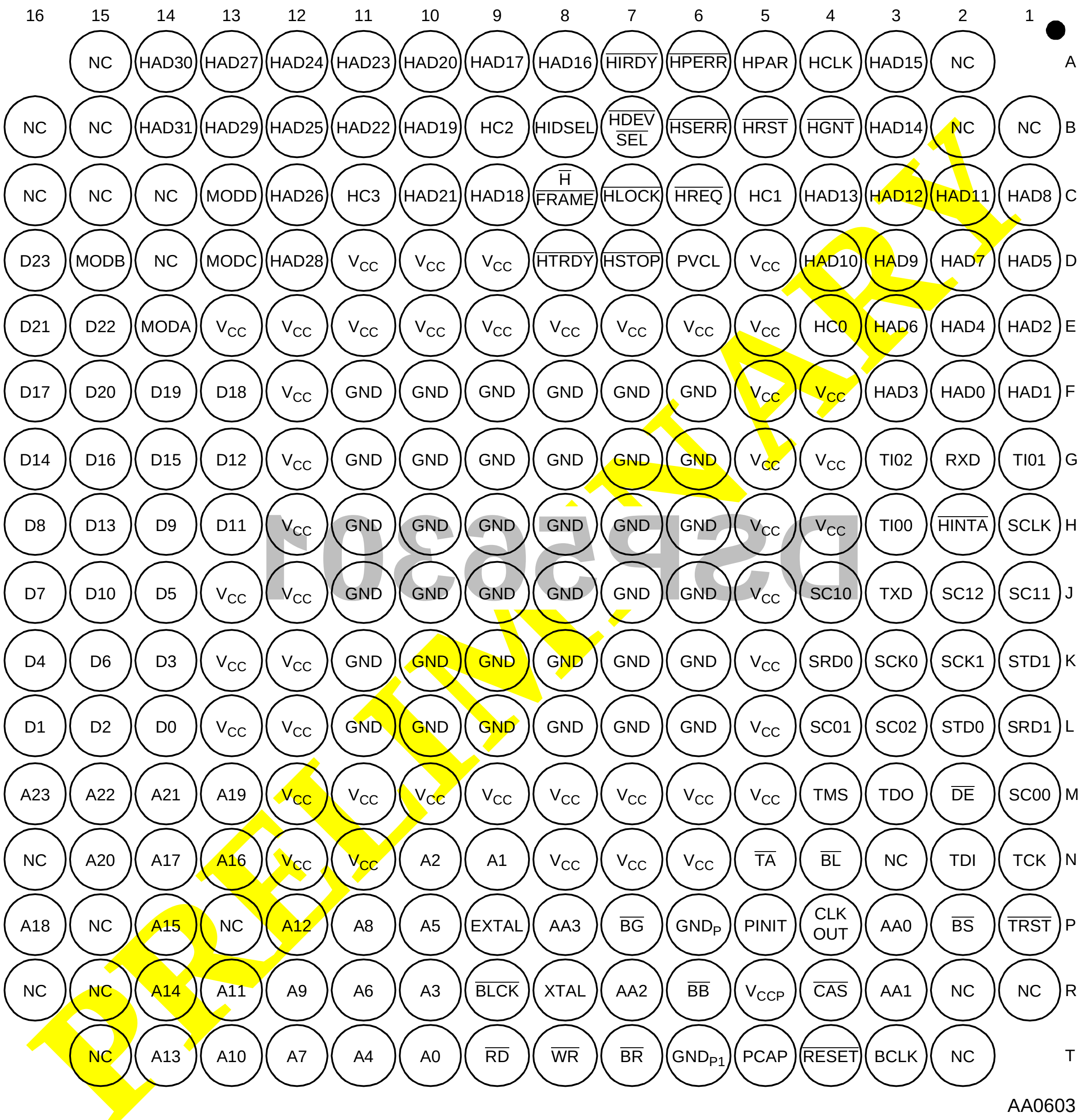
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A		NC	HAD15	HCLK	HPAR	$\overline{\text{HPERR}}$	$\overline{\text{HIRDY}}$	HAD16	HAD17	HAD20	HAD23	HAD24	HAD27	HAD30	NC	
B	NC	NC	HAD14	$\overline{\text{HGNT}}$	$\overline{\text{HRST}}$	$\overline{\text{HSERR}}$	$\overline{\text{HDEV}}$ SEL	HIDSEL	HC2	HAD19	HAD22	HAD25	HAD29	HAD31	NC	NC
C	HAD8	HAD11	HAD12	HAD13	HC1	$\overline{\text{HREQ}}$	$\overline{\text{HLOCK}}$	H $\overline{\text{FRAME}}$	HAD18	HAD21	HC3	HAD26	MODD	NC	NC	NC
D	HAD5	HAD7	HAD9	HAD10	V_{CC}	PVCL	$\overline{\text{HSTOP}}$	$\overline{\text{HTRDY}}$	V_{CC}	V_{CC}	V_{CC}	HAD28	MODC	NC	MODB	D23
E	HAD2	HAD4	HAD6	HC0	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	MODA	D22	D21
F	HAD1	HAD0	HAD3	V_{CC}	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	D18	D19	D20	D17
G	TI01	RXD	TI02	V_{CC}	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	D12	D15	D16	D14
H	SCLK	$\overline{\text{HINTA}}$	TI00	V_{CC}	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	D11	D9	D13	D8
J	SC11	SC12	TXD	SC10	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	V_{CC}	D5	D10	D7
K	STD1	SCK1	SCK0	SRD0	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	V_{CC}	D3	D6	D4
L	SRD1	STD0	SC02	SC01	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	V_{CC}	D0	D2	D1
M	SC00	$\overline{\text{DE}}$	TDO	TMS	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	A19	A21	A22	A23
N	TCK	TDI	NC	$\overline{\text{BL}}$	$\overline{\text{TA}}$	V_{CC}	V_{CC}	V_{CC}	A1	A2	V_{CC}	V_{CC}	A16	A17	A20	NC
P	$\overline{\text{TRST}}$	$\overline{\text{BS}}$	AA0	CLK OUT	PINIT	GND_P	$\overline{\text{BG}}$	AA3	EXTAL	A5	A8	A12	NC	A15	NC	A18
R	NC	NC	AA1	$\overline{\text{CAS}}$	V_{CCP}	$\overline{\text{BB}}$	AA2	XTAL	$\overline{\text{BCLK}}$	A3	A6	A9	A11	A14	NC	NC
T		NC	BCLK	$\overline{\text{RESET}}$	PCAP	GND_{P1}	$\overline{\text{BR}}$	$\overline{\text{WR}}$	$\overline{\text{RD}}$	A0	A4	A7	A10	A13	NC	

AA0602

Figure 3-4 DSP56301 Plastic Ball Grid Array (PBGA), Top View

Bottom View



	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A		NC	HAD30	HAD27	HAD24	HAD23	HAD20	HAD17	HAD16	$\overline{\text{HIRDY}}$	$\overline{\text{HPERR}}$	HPAR	HCLK	HAD15	NC	●
B	NC	NC	HAD31	HAD29	HAD25	HAD22	HAD19	HC2	HIDSEL	$\overline{\text{HDEV}}$ $\overline{\text{SEL}}$	$\overline{\text{HSERR}}$	$\overline{\text{HRST}}$	$\overline{\text{HGNT}}$	HAD14	NC	NC
C	NC	NC	NC	MODD	HAD26	HC3	HAD21	HAD18	$\overline{\text{H}}$ $\overline{\text{FRAME}}$	$\overline{\text{HLOCK}}$	$\overline{\text{HREQ}}$	HC1	HAD13	HAD12	HAD11	HAD8
D	D23	MODB	NC	MODC	HAD28	V_{CC}	V_{CC}	V_{CC}	$\overline{\text{HTRDY}}$	$\overline{\text{HSTOP}}$	PVCL	V_{CC}	HAD10	HAD9	HAD7	HAD5
E	D21	D22	MODA	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	HC0	HAD6	HAD4	HAD2
F	D17	D20	D19	D18	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	V_{CC}	HAD3	HAD0	HAD1
G	D14	D16	D15	D12	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	V_{CC}	TI02	RXD	TI01
H	D8	D13	D9	D11	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	V_{CC}	TI00	$\overline{\text{HINTA}}$	SCLK
J	D7	D10	D5	V_{CC}	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	SC10	TXD	SC12	SC11
K	D4	D6	D3	V_{CC}	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	SRD0	SCK0	SCK1	STD1
L	D1	D2	D0	V_{CC}	V_{CC}	GND	GND	GND	GND	GND	GND	V_{CC}	SC01	SC02	STD0	SRD1
M	A23	A22	A21	A19	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	TMS	TDO	$\overline{\text{DE}}$	SC00
N	NC	A20	A17	A16	V_{CC}	V_{CC}	A2	A1	V_{CC}	V_{CC}	V_{CC}	$\overline{\text{TA}}$	$\overline{\text{BL}}$	NC	TDI	TCK
P	A18	NC	A15	NC	A12	A8	A5	EXTAL	AA3	$\overline{\text{BG}}$	GND_P	PINIT	CLK OUT	AA0	$\overline{\text{BS}}$	$\overline{\text{TRST}}$
R	NC	NC	A14	A11	A9	A6	A3	$\overline{\text{BLCK}}$	XTAL	AA2	$\overline{\text{BB}}$	V_{CCP}	$\overline{\text{CAS}}$	AA1	NC	NC
T		NC	A13	A10	A7	A4	A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{BR}}$	GND_{P1}	PCAP	$\overline{\text{RESET}}$	BCLK	NC	

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Figure 3-5 DSP56301 Plastic Ball Grid Array (PBGA), Bottom View

Table 3-3 DSP56301 PBGA Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A2	NC	B12	HAD25 or HD17	D5	V_{CC}
A3	HAD15, HD7, or PB15	B13	HAD29 or HD21	D6	PVCL
A4	HCLK	B14	HAD31 or HD23	D7	$\overline{\text{HSTOP}}$ or $\overline{\text{HWR}}$ / HRW
A5	HPAR or $\overline{\text{HDAK}}$	B15	NC	D8	$\overline{\text{HTRDY}}$, $\overline{\text{HDBEN}}$, or PB20
A6	$\overline{\text{HPERR}}$ or HDRQ	B16	NC	D9	V_{CC}
A7	$\overline{\text{HIRDY}}$, $\overline{\text{HDBDR}}$, or PB21	C1	HAD8, HD0, or PB8	D10	V_{CC}
A8	HAD16 or HD8	C2	HAD11, HD3, or PB11	D11	V_{CC}
A9	HAD17 or HD9	C3	HAD12, HD4, or PB12	D12	HAD28 or HD20
A10	HAD20 or HD12	C4	HAD13, HD5, or PB13	D13	MODC / $\overline{\text{IRQC}}$
A11	HAD23 or HD15	C5	HC1 / $\overline{\text{HBE1}}$, HA1, or PB17	D14	NC
A12	HAD24 or HD16	C6	$\overline{\text{HREQ}}$ or HTA	D15	MODB / $\overline{\text{IRQB}}$
A13	HAD27 or HD19	C7	$\overline{\text{HLOCK}}$, $\overline{\text{HBS}}$, or PB23	D16	D23
A14	HAD30 or HD22	C8	$\overline{\text{HFRAME}}$	E1	HAD2, HA5, or PB2
A15	NC	C9	HAD18 or HD10	E2	HAD4, HA7, or PB4
B1	NC	C10	HAD21 or HD13	E3	HAD6, HA9, or PB6
B2	NC	C11	HC3 / $\overline{\text{HBE3}}$ or PB19	E4	HC0 / $\overline{\text{HBE0}}$, HA0, or PB16
B3	HAD14, HD6, or PB14	C12	HAD26 or HD18	E5	V_{CC}
B4	$\overline{\text{HGNT}}$ or HAEN	C13	MODD / $\overline{\text{IRQD}}$	E6	V_{CC}
B5	$\overline{\text{HRST}}$ / HRST	C14	NC	E7	V_{CC}
B6	$\overline{\text{HSERR}}$ or $\overline{\text{HIRQ}}$	C15	NC	E8	V_{CC}
B7	$\overline{\text{HDEVSEL}}$, $\overline{\text{HSAK}}$, or PB22	C16	NC	E9	V_{CC}
B8	HIDSEL or $\overline{\text{HRD}}$ / $\overline{\text{HDS}}$	D1	HAD5, HA8, or PB5	E10	V_{CC}
B9	HC2 / $\overline{\text{HBE2}}$, HA2, or PB18	D2	HAD7, HA10, or PB7	E11	V_{CC}
B10	HAD19 or HD11	D3	HAD9, HD1, or PB9	E12	V_{CC}
B11	HAD22 or HD14	D4	HAD10, HD2, or PB10	E13	V_{CC}

Table 3-3 DSP56301 PBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
E14	MODA/$\overline{\text{IRQA}}$	G7	GND	H16	D8
E15	D22	G8	GND	J1	SC11 or PD1
E16	D21	G9	GND	J2	SC12 or PD2
F1	HAD1, HA4, or PB1	G10	GND	J3	TXD or PE1
F2	HAD0, HA3, or PB0	G11	GND	J4	SC10 or PD0
F3	HAD3, HA6, or PB3	G12	V_{CC}	J5	V_{CC}
F4	V_{CC}	G13	D12	J6	GND
F5	V_{CC}	G14	D15	J7	GND
F6	GND	G15	D16	J8	GND
F7	GND	G16	D14	J9	GND
F8	GND	H1	SCLK or PE2	J10	GND
F9	GND	H2	$\overline{\text{HINTA}}$	J11	GND
F10	GND	H3	TIO0	J12	V_{CC}
F11	GND	H4	V_{CC}	J13	V_{CC}
F12	V_{CC}	H5	V_{CC}	J14	D5
F13	D18	H6	GND	J15	D10
F14	D19	H7	GND	J16	D7
F15	D20	H8	GND	K1	STD1 or PD5
F16	D17	H9	GND	K2	SCK1 or PD3
G1	TIO1	H10	GND	K3	SCK0 or PC3
G2	RXD or PE0	H11	GND	K4	SRD0 or PC4
G3	TIO2	H12	V_{CC}	K5	V_{CC}
G4	V_{CC}	H13	D11	K6	GND
G5	V_{CC}	H14	D9	K7	GND
G6	GND	H15	D13	K8	GND

Table 3-3 DSP56301 PBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
K9	GND	M2	$\overline{\text{DE}}$	N11	V_{CC}
K10	GND	M3	TDO	N12	V_{CC}
K11	GND	M4	TMS	N13	A16
K12	V_{CC}	M5	V_{CC}	N14	A17
K13	V_{CC}	M6	V_{CC}	N15	A20
K14	D3	M7	V_{CC}	N16	NC
K15	D6	M8	V_{CC}	P1	$\overline{\text{TRST}}$
K16	D4	M9	V_{CC}	P2	$\overline{\text{BS}}$
L1	SRD1 or PD4	M10	V_{CC}	P3	AA0/$\overline{\text{RAS0}}$
L2	STD0 or PC5	M11	V_{CC}	P4	CLKOUT
L3	SC02 or PC2	M12	V_{CC}	P5	PINIT/$\overline{\text{NMI}}$
L4	SC01 or PC1	M13	A19	P6	GND_P
L5	V_{CC}	M14	A21	P7	$\overline{\text{BG}}$
L6	GND	M15	A22	P8	AA3/$\overline{\text{RAS3}}$
L7	GND	M16	A23	P9	EXTAL
L8	GND	N1	TCK	P10	A5
L9	GND	N2	TDI	P11	A8
L10	GND	N3	NC	P12	A12
L11	GND	N4	$\overline{\text{BL}}$	P13	NC
L12	V_{CC}	N5	$\overline{\text{TA}}$	P14	A15
L13	V_{CC}	N6	V_{CC}	P15	NC
L14	D0	N7	V_{CC}	P16	A18
L15	D2	N8	V_{CC}	R1	NC
L16	D1	N9	A1	R2	NC
M1	SC00 or PC0	N10	A2	R3	AA1/$\overline{\text{RAS1}}$

Table 3-3 DSP56301 PBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
R4	$\overline{\text{CAS}}$	R13	A11	T7	$\overline{\text{BR}}$
R5	V_{CCP}	R14	A14	T8	$\overline{\text{WR}}$
R6	$\overline{\text{BB}}$	R15	NC	T9	$\overline{\text{RD}}$
R7	AA2 / $\overline{\text{RAS2}}$	R16	NC	T10	A0
R8	XTAL	T2	NC	T11	A4
R9	$\overline{\text{BCLK}}$	T3	BCLK	T12	A7
R10	A3	T4	$\overline{\text{RESET}}$	T13	A10
R11	A6	T5	PCAP	T14	A13
R12	A9	T6	GND_{1P}	T15	NC

Note:

1. Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx / $\overline{\text{IRQx}}$ pins that select an operating mode after $\overline{\text{RESET}}$ is deasserted, but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{\text{HAS}}$ / HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data / address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for GND_P and GND_{P1} that support the PLL, other GND signals do not support individual subsystems in the chip.
2. NC stands for Not Connected. These pins are reserved for future development. Do not connect and line, component, trace, or via to these pins.

Table 3-4 DSP56301 PBGA Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	T10	AA2	R7	D22	E15
A1	N9	AA3	P8	D23	D16
A10	T13	$\overline{BB}$	R6	D3	K14
A11	R13	BCLK	T3	D4	K16
A12	P12	$\overline{BCLK}$	R9	D5	J14
A13	T14	$\overline{BG}$	P7	D6	K15
A14	R14	$\overline{BL}$	N4	D7	J16
A15	P14	$\overline{BR}$	T7	D8	H16
A16	N13	$\overline{BS}$	P2	D9	H14
A17	N14	$\overline{CAS}$	R4	$\overline{DE}$	M2
A18	P16	CLKOUT	P4	EXTAL	P9
A19	M13	D0	L14	GND	F10
A2	N10	D1	L16	GND	F11
A20	N15	D10	J15	GND	F6
A21	M14	D11	H13	GND	F7
A22	M15	D12	G13	GND	F8
A23	M16	D13	H15	GND	F9
A3	R10	D14	G16	GND	G10
A4	T11	D15	G14	GND	G11
A5	P10	D16	G15	GND	G6
A6	R11	D17	F16	GND	G7
A7	T12	D18	F13	GND	G8
A8	P11	D19	F14	GND	G9
A9	R12	D2	L15	GND	H10
AA0	P3	D20	F15	GND	H11
AA1	R3	D21	E16		

Table 3-4 DSP56301 PBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	H6	HA0	E4	HAD21	C10
GND	H7	HA1	C5	HAD22	B11
GND	H8	HA10	D2	HAD23	A11
GND	H9	HA2	B9	HAD24	A12
GND	J10	HA3	F2	HAD25	B12
GND	J11	HA4	F1	HAD26	C12
GND	J6	HA5	E1	HAD27	A13
GND	J7	HA6	F3	HAD28	D12
GND	J8	HA7	E2	HAD29	B13
GND	J9	HA8	D1	HAD3	F3
GND	K10	HA9	E3	HAD30	A14
GND	K11	HAD0	F2	HAD31	B14
GND	K6	HAD1	F1	HAD4	E2
GND	K7	HAD10	D4	HAD5	D1
GND	K8	HAD11	C2	HAD6	E3
GND	K9	HAD12	C3	HAD7	D2
GND	L10	HAD13	C4	HAD8	C1
GND	L11	HAD14	B3	HAD9	D3
GND	L6	HAD15	A3	HAEN	B4
GND	L7	HAD16	A8	$\overline{\text{HBE0}}$	E4
GND	L8	HAD17	A9	$\overline{\text{HBE1}}$	C5
GND	L9	HAD18	C9	$\overline{\text{HBE2}}$	B9
GND$_{1P}$	T6	HAD19	B10	$\overline{\text{HBE3}}$	C11
GND$_{P}$	P6	HAD2	E1	$\overline{\text{HBS}}$	C7
		HAD20	A10	HC0	E4

Table 3-4 DSP56301 PBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
HC1	C5	HD7	A3	HTA	C6
HC2	B9	HD8	A8	$\overline{\text{HTRDY}}$	D8
HC3	C11	HD9	A9	$\overline{\text{HWR}}$	D7
HCLK	A4	$\overline{\text{HDAK}}$	A5	$\overline{\text{IRQA}}$	E14
HD0	C1	$\overline{\text{HDBDR}}$	A7	$\overline{\text{IRQB}}$	D15
HD1	D3	$\overline{\text{HDBEN}}$	D8	$\overline{\text{IRQC}}$	D13
HD10	C9	$\overline{\text{HDEVSEL}}$	B7	$\overline{\text{IRQD}}$	C13
HD11	B10	HDRQ	A6	MODA	E14
HD12	A10	$\overline{\text{HDS}}$	B8	MODB	D15
HD13	C10	$\overline{\text{HFRAME}}$	C8	MODC	D13
HD14	B11	$\overline{\text{HGNT}}$	B4	MODD	C13
HD15	A11	$\overline{\text{HIDSEL}}$	B8	NC	A15
HD16	A12	$\overline{\text{HINTA}}$	H2	NC	A2
HD17	B12	$\overline{\text{HIRDY}}$	A7	NC	B1
HD18	C12	$\overline{\text{HIRQ}}$	B6	NC	B15
HD19	A13	$\overline{\text{HLOCK}}$	C7	NC	B16
HD2	D4	HPAR	A5	NC	B2
HD20	D12	$\overline{\text{HPERR}}$	A6	NC	C14
HD21	B13	$\overline{\text{HRD}}$	B8	NC	C15
HD22	A14	$\overline{\text{HREQ}}$	C6	NC	C16
HD23	B14	$\overline{\text{HRST}}$ / HRST	B5	NC	D14
HD3	C2	HRW	D7	NC	N16
HD4	C3	$\overline{\text{HSAK}}$	B7	NC	N3
HD5	C4	$\overline{\text{HSERR}}$	B6	NC	P13
HD6	B3	$\overline{\text{HSTOP}}$	D7	NC	P15

Table 3-4 DSP56301 PBGA Signal Identification by Name (Continued)

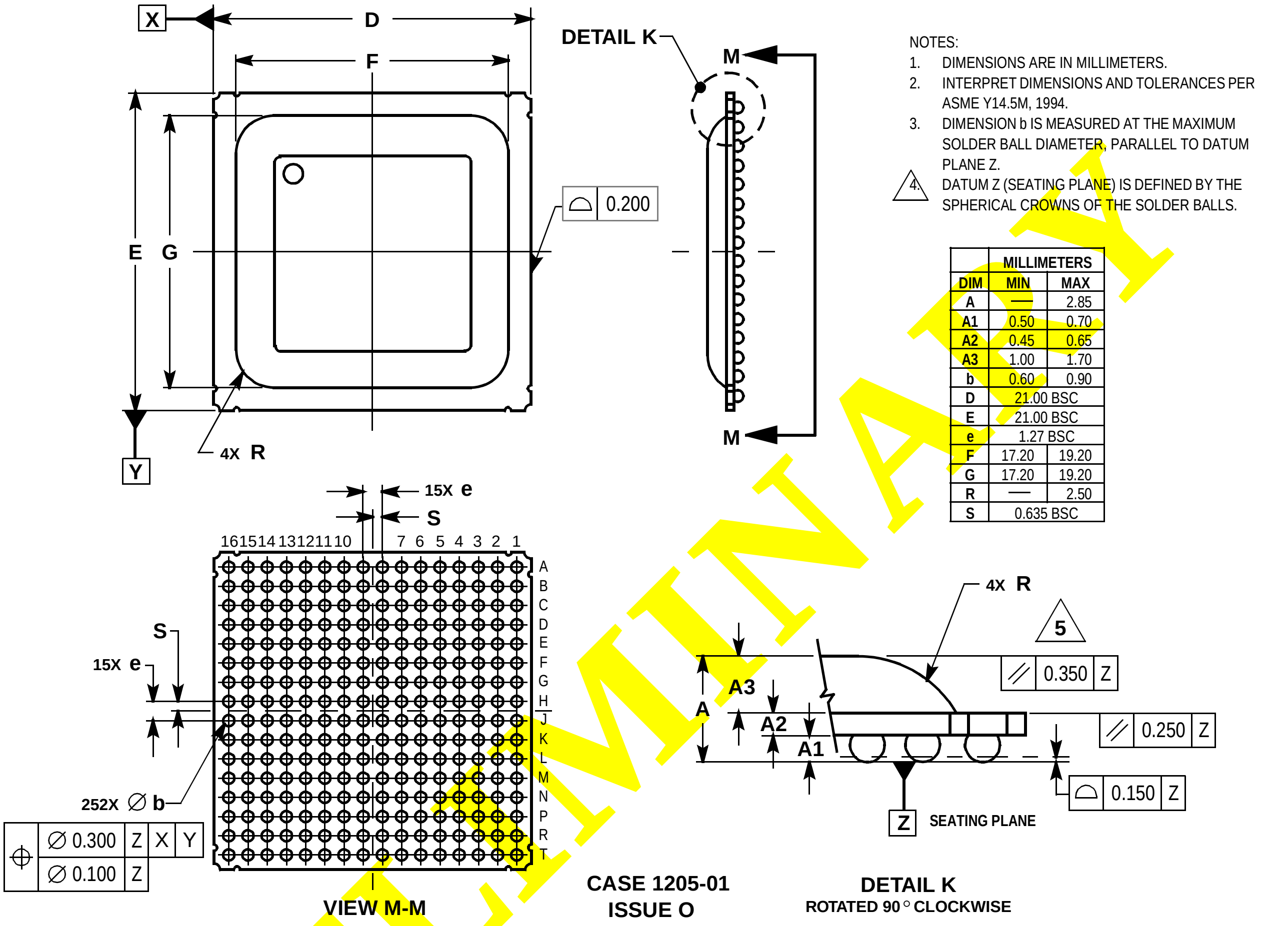
Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
NC	R1	PB3	F3	$\overline{RAS0}$	P3
NC	R2	PB4	E2	$\overline{RAS1}$	R3
NC	R15	PB5	D1	$\overline{RAS2}$	R7
NC	R16	PB6	E3	$\overline{RAS3}$	P8
NC	T2	PB7	D2	$\overline{RD}$	T9
NC	T15	PB8	C1	$\overline{RESET}$	T4
$\overline{NMI}$	P5	PB9	D3	RXD	G2
PB0	F2	PC0	M1	SC00	M1
PB1	F1	PC1	L4	SC01	L4
PB10	D4	PC2	L3	SC02	L3
PB11	C2	PC3	K3	SC10	J4
PB12	C3	PC4	K4	SC11	J1
PB13	C4	PC5	L2	SC12	J2
PB14	B3	PCAP	T5	SCK0	K3
PB15	A3	PD0	J4	SCK1	K2
PB16	E4	PD1	J1	SCLK	H1
PB17	C5	PD2	J2	SRD0	K4
PB18	B9	PD3	K2	SRD1	L1
PB19	C11	PD4	L1	STD0	L2
PB2	E1	PD5	K1	STD1	K1
PB20	D8	PE0	G2	$\overline{TA}$	N5
PB21	A7	PE1	J3	TCK	N1
PB22	B7	PE2	H1	TDI	N2
PB23	C7	PINIT	P5	TDO	M3
		PVCL	D6	TIO0	H3

Table 3-4 DSP56301 PBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
TIO1	G1	V_{CC}	F12	V_{CC}	M10
TIO2	G3	V_{CC}	F4	V_{CC}	M11
TMS	M4	V_{CC}	F5	V_{CC}	M12
$\overline{\text{TRST}}$	P1	V_{CC}	G12	V_{CC}	M5
TXD	J3	V_{CC}	G4	V_{CC}	M6
V_{CC}	D10	V_{CC}	G5	V_{CC}	M7
V_{CC}	D11	V_{CC}	H12	V_{CC}	M8
V_{CC}	D5	V_{CC}	H4	V_{CC}	M9
V_{CC}	D9	V_{CC}	H5	V_{CC}	N11
V_{CC}	E10	V_{CC}	J12	V_{CC}	N12
V_{CC}	E11	V_{CC}	J13	V_{CC}	N6
V_{CC}	E12	V_{CC}	J5	V_{CC}	N7
V_{CC}	E13	V_{CC}	K12	V_{CC}	N8
V_{CC}	E5	V_{CC}	K13	V_{CCP}	R5
V_{CC}	E6	V_{CC}	K5	$\overline{\text{WR}}$	T8
V_{CC}	E7	V_{CC}	L12	XTAL	R8
V_{CC}	E8	V_{CC}	L13		
V_{CC}	E9	V_{CC}	L5		

Note: NC stands for Not Connected. These pins are reserved for future development. Do not connect and line, component, trace, or via to these pins.

PBGA Package Mechanical Drawing



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	—	2.85
A1	0.50	0.70
A2	0.45	0.65
A3	1.00	1.70
b	0.60	0.90
D	21.00 BSC	
E	21.00 BSC	
e	1.27 BSC	
F	17.20	19.20
G	17.20	19.20
R	—	2.50
S	0.635 BSC	

Figure 3-6 DSP56301 Mechanical Information, 252-pin PBGA Package

ORDERING DRAWINGS

Complete mechanical information regarding DSP56301 packaging is available by facsimile through Motorola's Mfax™ system. Call the following number to obtain information by facsimile:

(602) 244-6609

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller’s Personal Identification Number (PIN)

Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The DSP56301 208-pin TQFP package mechanical drawing is referenced as 998-01. The reference number for the 252-pin PBGA package is 1205-01.

SECTION 4

DESIGN CONSIDERATIONS

THERMAL DESIGN CONSIDERATIONS

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C / W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C / W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C / W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C / W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T) / P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, Thermal Characterization Parameter or Ψ_{JT}, has been defined to be $(T_J - T_T) / P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

ELECTRICAL DESIGN CONSIDERATIONS

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP, and from the board ground to each GND pin.
- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 in per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{TA}}$, and $\overline{\text{BG}}$ pins. Maximum PCB trace lengths on the order of 6 inches are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels, except for the three pins with internal pull-up resistors ($\overline{\text{TRST}}$, TMS, $\overline{\text{DE}}$).
- Take special care to minimize noise levels on the V_{CCP}, GND_P, and GND_{P1} pins.
- The following pins must be asserted after power-up: $\overline{\text{RESET}}$, $\overline{\text{HRST}}$ (default after reset is active low), and $\overline{\text{TRST}}$.

- At power-up, the voltage difference between 5 V tolerant pins and the chip V_{CC} should not exceed 3.5 V.
- If multiple DSP56301 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.

POWER CONSUMPTION CONSIDERATIONS

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is Alternating Current (AC), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the formula:

Equation 3: $I = C \times V \times f$

where:
C = node / pin capacitance
V = voltage swing
f = frequency of node / pin toggle

Example 4-1 Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is:

Equation 4: $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48 \text{ mA}$

The Maximum Internal Current (I_{CCI}max) value reflects the typical possible switching of the internal buses on worst-case operation conditions, which is not necessarily a real application case. The Typical Internal Current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption:

- Set the EBD bit when not accessing external memory.
- Minimize external memory accesses, and use internal memory accesses.
- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.
- Connect the unused inputs to pull-up or pull-down resistors.
- Disable unused peripherals.

- Disable unused pin activity (e.g., CLKOUT, XTAL).

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (i.e., to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value:

Equation 5: $$I/MIPS = I/MHz = (I_{typF2} - I_{typF1})/(F2 - F1)$$

where: I_{typF2} = current at F2
I_{typF1} = current at F1
F2 = high frequency (any specified operating frequency)
F1 = low frequency (any specified operating frequency lower than F2)

Note: F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

PLL PERFORMANCE ISSUES

The following explanations should be considered as general observations on expected PLL behavior. There is no testing that verifies these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature and voltage ranges. As defined in **Table 2-5** on page 2-7, for input frequencies greater than 15 MHz and the Multiplication Factor (MF) ≤ 4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between –1.4 ns and +3.2 ns.

Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤ 4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5%. For mid-range MF (10 < MF < 500) this jitter is between 0.5% and ~2%. For large MF (MF > 500), the frequency jitter is 2–3%.

Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5%. If the rate of change of the frequency of EXTAL is slow (i.e., it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time), then the allowed jitter can be 2%. The phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed values.

SECTION 5

ORDERING INFORMATION

ORDERING PRODUCT

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and to place an order.

Table 5-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56301	3 V	Thin Quad Flat Pack (TQFP)	208	66	XC56301PW66
				80	XC56301PW80
				100	XC56301PW100
		Plastic Ball Grid Array (PBGA)	252	66	XC56301GC66
				80	XC56301GC80
				100	XC56301GC100

APPENDIX A

POWER CONSUMPTION BENCHMARK

The following benchmark program permits evaluation of DSP power usage in a test situation. It enables the PLL, disables the external clock, and uses repeated Multiply-Accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;***********************************************************************
***
;***********************************************************************
***
;*                                                                     *
;* CHECKS   Typical Power Consumption                                *
;*                                                                     *
;***********************************************************************
***

          page      200,55,0,0,0
          nolist

I_VEC EQU $000000   ; Interrupt vectors for program debug only
START EQU $8000     ; MAIN (external) program starting address
INT_PROG EQU$100    ; INTERNAL program memory starting address
INT_XDAT EQU$0      ; INTERNAL X-data memory starting address
INT_YDAT EQU$0      ; INTERNAL Y-data memory starting address

          INCLUDE "ioequ.asm"
          INCLUDE "intequ.asm"

          list

          org       P:START
;
          movep #$0123FF,x:M_BCR; BCR: Area 3 : 1 w.s (SRAM)
; Area 2 : 0 w.s (SSRAM)
; Default: 1 w.s (SRAM)
;
          movep     #$0d0000,x:M_PCTL; XTAL disable
; PLL enable
; CLKOUT disable
;
;Load the program
;
          move      #INT_PROG,r0
          move      #PROG_START,r1
          do        #(PROG_END-PROG_START),PLOAD_LOOP
          move      p:(r1)+,x0
          move      x0,p:(r0)+
```

```
          nop
PLOAD_LOOP
;
; Load the X-data
;
          move     #INT_XDAT,r0
          move     #XDAT_START,r1
          do       #(XDAT_END-XDAT_START),XLOAD_LOOP
          move     p:(r1)+,x0
          move     x0,x:(r0)+
XLOAD_LOOP
;
;Load the Y-data
;
          move     #INT_YDAT,r0
          move     #YDAT_START,r1
          do       #(YDAT_END-YDAT_START),YLOAD_LOOP
          move     p:(r1)+,x0
          move     x0,y:(r0)+
YLOAD_LOOP
;

          jmp      INT_PROG

PROG_START
          move     #$0,r0
          move     #$0,r4
          move     #$3f,m0
          move     #$3f,m4
;
          clr      a
          clr      b
          move     #$0,x0
          move     #$0,x1
          move     #$0,y0
          move     #$0,y1
          bset     #4,omr              ; ebd
;
sbr       dor      #60,_end
          mac      x0,y0,a  x:(r0)+,x1         y:(r4)+,y1
          mac      x1,y1,a  x:(r0)+,x0         y:(r4)+,y0
          add      a,b
          mac      x0,y0,a  x:(r0)+,x1
          mac      x1,y1,a                     y:(r4)+,y0
          move     b1,x:$ff
_end
          bra      sbr
          nop
          nop
          nop
          nop
PROG_END
          nop
```

```
          nop


XDAT_START
;         org       x:0
          dc        $262EB9
          dc        $86F2FE
          dc        $E56A5F
          dc        $616CAC
          dc        $8FFD75
          dc        $9210A
          dc        $A06D7B
          dc        $CEA798
          dc        $8DFBF1
          dc        $A063D6
          dc        $6C6657
          dc        $C2A544
          dc        $A3662D
          dc        $A4E762
          dc        $84F0F3
          dc        $E6F1B0
          dc        $B3829
          dc        $8BF7AE
          dc        $63A94F
          dc        $EF78DC
          dc        $242DE5
          dc        $A3E0BA
          dc        $EBAB6B
          dc        $8726C8
          dc        $CA361
          dc        $2F6E86
          dc        $A57347
          dc        $4BE774
          dc        $8F349D
          dc        $A1ED12
          dc        $4BFCE3
          dc        $EA26E0
          dc        $CD7D99
          dc        $4BA85E
          dc        $27A43F
          dc        $A8B10C
          dc        $D3A55
          dc        $25EC6A
          dc        $2A255B
          dc        $A5F1F8
          dc        $2426D1
          dc        $AE6536
          dc        $CBBC37
          dc        $6235A4
          dc        $37F0D
          dc        $63BEC2
          dc        $A5E4D3
          dc        $8CE810
```

```
          dc       $3FF09
          dc       $60E50E
          dc       $CFFB2F
          dc       $40753C
          dc       $8262C5
          dc       $CA641A
          dc       $EB3B4B
          dc       $2DA928
          dc       $AB6641
          dc       $28A7E6
          dc       $4E2127
          dc       $482FD4
          dc       $7257D
          dc       $E53C72
          dc       $1A8C3
          dc       $E27540
XDAT_END

YDAT_START
;         org      y:0
          dc       $5B6DA
          dc       $C3F70B
          dc       $6A39E8
          dc       $81E801
          dc       $C666A6
          dc       $46F8E7
          dc       $AAEC94
          dc       $24233D
          dc       $802732
          dc       $2E3C83
          dc       $A43E00
          dc       $C2B639
          dc       $85A47E
          dc       $ABFDDF
          dc       $F3A2C
          dc       $2D7CF5
          dc       $E16A8A
          dc       $ECB8FB
          dc       $4BED18
          dc       $43F371
          dc       $83A556
          dc       $E1E9D7
          dc       $ACA2C4
          dc       $8135AD
          dc       $2CE0E2
          dc       $8F2C73
          dc       $432730
          dc       $A87FA9
          dc       $4A292E
          dc       $A63CCF
          dc       $6BA65C
          dc       $E06D65
          dc       $1AA3A
```

```
         dc       $A1B6EB
         dc       $48AC48
         dc       $EF7AE1
         dc       $6E3006
         dc       $62F6C7
         dc       $6064F4
         dc       $87E41D
         dc       $CB2692
         dc       $2C3863
         dc       $C6BC60
         dc       $43A519
         dc       $6139DE
         dc       $ADF7BF
         dc       $4B3E8C
         dc       $6079D5
         dc       $E0F5EA
         dc       $8230DB
         dc       $A3B778
         dc       $2BFE51
         dc       $E0A6B6
         dc       $68FFB7
         dc       $28F324
         dc       $8F2E8D
         dc       $667842
         dc       $83E053
         dc       $A1FD90
         dc       $6B2689
         dc       $85B68E
         dc       $622EAF
         dc       $6162BC
         dc       $E4A245
YDAT_END
;***********************************************************************
***
;
;        EQUATES for DSP56301 I/O registers and ports
;        Reference: DSP56301 Specifications Revision 3.00
;
;        Last update:       November 15 1993
;         Changes:          GPIO for ports C,D and E,
;                           HI32
;                           DMA status reg
;                            PLL control reg
;                           AAR
;                           SCI registers address
;                           SSI registers addr. + split TSR from SSISR
;
         December 19 1993 (cosmetic - page and opt directives)
;        August    9 1994 ESSI and SCI control registers bit update
;
;***********************************************************************
***
```

```
          page      132,55,0,0,0
          opt       mex

ioequ   ident   1,0

;------------------------------------------------------------------------
-
;
;       EQUATES for I/O Port Programming
;
;------------------------------------------------------------------------
-

;       Register Addresses

M_DATH EQU $FFFFCF ; Host port GPIO data Register
M_DIRH EQU $FFFFCE ; Host port GPIO direction Register
M_PCRC EQU $FFFFBF ; Port C Control Register
M_PRRC EQU $FFFFBE ; Port C Direction Register
M_PDRC EQU $FFFFBD ; Port C GPIO Data Register
M_PCRD EQU $FFFFAF ; Port D Control register
M_PRRD EQU $FFFFAE ; Port D Direction Data Register
M_PDRD EQU $FFFFAD ; Port D GPIO Data Register
M_PCRE EQU $FFFF9F ; Port E Control register
M_PRRE EQU $FFFF9E ; Port E Direction Register
M_PDRE EQU $FFFF9D ; Port E Data Register
M_OGDB EQU $FFFFFC ; OnCE GDB Register

;------------------------------------------------------------------------
-
;
;     EQUATES for Host Interface
;
;------------------------------------------------------------------------
-

;    Register Addresses

M_DTXS EQU $FFFFCD ; DSP SLAVE TRANSMIT DATA FIFO (DTXS)
M_DTXM EQU $FFFFCC ; DSP MASTER TRANSMIT DATA FIFO (DTXM)
M_DRXR EQU $FFFFCB ; DSP RECEIVE DATA FIFO (DRXR)
M_DPSR EQU $FFFFCA ; DSP PCI STATUS REGISTER (DPSR)
M_DSR EQU $FFFFC9  ; DSP STATUS REGISTER (DSR)
M_DPAR EQU $FFFFC8 ; DSP PCI ADDRESS REGISTER (DPAR)
M_DPMC EQU $FFFFC7 ; DSP PCI MASTER CONTROL REGISTER (DPMC)
M_DPCR EQU $FFFFC6 ; DSP PCI CONTROL REGISTER (DPCR)
M_DCTR EQU $FFFFC5 ; DSP CONTROL REGISTER (DCTR)

;       Host Control Register Bit Flags

M_HCIE EQU 0       ; Host Command Interrupt Enable
M_STIE EQU 1       ; Slave Transmit Interrupt Enable
M_SRIE EQU 2       ; Slave Receive Interrupt Enable
```

```
M_HF35 EQU $38     ; Host Flags 5-3 Mask
M_HF3 EQU 3        ; Host Flag 3
M_HF4 EQU 4        ; Host Flag 4
M_HF5 EQU 5        ; Host Flag 5
M_HINT EQU 6       ; Host Interrupt A
M_HDSM EQU 13      ; Host Data Strobe Mode
M_HRWP EQU 14      ; Host RD/WR Polarity
M_HTAP EQU 15      ; Host Transfer Acknowledge Polarity
M_HDRP EQU 16      ; Host Dma Request Polarity
M_HRSP EQU 17      ; Host Reset Polarity
M_HIRP EQU 18      ; Host Interrupt  Request Polarity
M_HIRC EQU 19      ; Host Interupt Request Control
M_HM0 EQU 20       ; Host Interface Mode
M_HM1 EQU 21       ; Host Interface Mode
M_HM2 EQU 22       ; Host Interface Mode
M_HM EQU $700000   ; Host Interface Mode Mask

;       Host PCI Control Register Bit Flags

M_PMTIE EQU 1      ; PCI Master Transmit Interrupt Enable
M_PMRIE EQU 2      ; PCI Master Receive Interrupt Enable
M_PMAIE EQU 4      ; PCI Master Address Interrupt Enable
M_PPEIE EQU 5      ; PCI Parity Error Interrupt Enable
M_PTAIE EQU 7      ; PCI Transaction Abort Interrupt Enable
M_PTTIE EQU 9      ; PCI Transaction Termination Interrupt Enable
M_PTCIE EQU 12     ; PCI Transfer Complete Interrupt Enable
M_CLRT EQU 14      ; Clear Transmitter
M_MTT EQU 15       ; Master Transfer Terminate
M_SERF EQU 16      ; HSERR~ Force
M_MACE EQU 18      ; Master Access Counter Enable
M_MWSD EQU 19      ; Master Wait States Disable
M_RBLE EQU 20      ; Receive Buffer Lock Enable
M_IAE EQU 21       ; Insert Address Enable

;       Host PCI Master Control Register Bit Flags

M_ARH EQU $00ffff  ; DSP PCI Transaction Address (High)
M_BL EQU $3f0000   ; PCI Data Burst Length
M_FC EQU $c00000   ; Data Transfer Format Control

;       Host PCI Address Register Bit Flags

M_ARL EQU $00ffff  ; DSP PCI Transaction Address (Low)
M_C EQU $0f0000    ; PCI Bus Command
M_BE EQU $f00000   ; PCI Byte Enables

;       DSP Status Register Bit Flags

M_HCP EQU 0        ; Host Command pending
M_STRQ EQU 1       ; Slave Transmit Data Request
M_SRRQ EQU 2       ; Slave Receive Data Request
M_HF02 EQU $38     ; Host Flag 0-2 Mask
M_HF0 EQU 3        ; Host Flag 0
```

```
M_HF1 EQU 4        ; Host Flag 1
M_HF2 EQU 5        ; Host Flag 2

;       DSP PCI Status Register Bit Flags

M_MWS EQU 0        ; PCI Master Wait States
M_MTRQ EQU 1       ; PCI Master Transmit Data Request
M_MRRQ EQU 2       ; PCI Master Receive Data Request
M_MARQ EQU 4       ; PCI Master Address Request
M_APER EQU 5       ; PCI Address Parity Error
M_DPER EQU 6       ; PCI Data Parity Error
M_MAB EQU 7        ; PCI Master Abort
M_TAB EQU 8        ; PCI Target Abort
M_TDIS EQU 9       ; PCI Target Disconnect
M_TRTY EQU 10      ; PCI Target Retry
M_TO EQU 11        ; PCI Time Out Termination
M_RDC EQU $3F0000  ; Remaining Data Count Mask (RDC5-RDC0)
M_RDC0 EQU 16      ; Remaining Data Count  0
M_RDC1 EQU 17      ; Remaining Data Count  1
M_RDC2 EQU 18      ; Remaining Data Count  2
M_RDC3 EQU 19      ; Remaining Data Count  3
M_RDC4 EQU 20      ; Remaining Data Count  4
M_RDC5 EQU 21      ; Remaining Data Count  5
M_HACT EQU 23      ; Hi32 Active


;-----------------------------------------------------------------------
-
;
;       EQUATES for Serial Communications Interface (SCI)
;
;-----------------------------------------------------------------------
-

;       Register Addresses

M_STXH EQU $FFFF97 ; SCI Transmit Data Register (high)
M_STXM EQU $FFFF96 ; SCI Transmit Data Register (middle)
M_STXL EQU $FFFF95 ; SCI Transmit Data Register (low)
M_SRXH EQU $FFFF9A ; SCI Receive Data Register (high)
M_SRXM EQU $FFFF99 ; SCI Receive Data Register (middle)
M_SRXL EQU $FFFF98 ; SCI Receive Data Register (low)
M_STXA EQU $FFFF94 ; SCI Transmit Address Register
M_SCR EQU $FFFF9C  ; SCI Control Register
M_SSR EQU $FFFF93  ; SCI Status Register
M_SCCR EQU $FFFF9B ; SCI Clock Control Register

;       SCI Control Register Bit Flags

M_WDS EQU $7       ; Word Select Mask (WDS0-WDS3)
M_WDS0 EQU 0       ; Word Select 0
M_WDS1 EQU 1       ; Word Select 1
M_WDS2 EQU 2       ; Word Select 2
```

```
M_SSFTD EQU 3      ; SCI Shift Direction
M_SBK EQU 4        ; Send Break
M_WAKE EQU 5       ; Wakeup Mode Select
M_RWU EQU 6        ; Receiver Wakeup Enable
M_WOMS EQU 7       ; Wired-OR Mode Select
M_SCRE EQU 8       ; SCI Receiver Enable
M_SCTE EQU 9       ; SCI Transmitter Enable
M_ILIE EQU 10      ; Idle Line Interrupt Enable
M_SCRIE EQU 11     ; SCI Receive Interrupt Enable
M_SCTIE EQU 12     ; SCI Transmit Interrupt Enable
M_TMIE EQU 13      ; Timer Interrupt Enable
M_TIR EQU 14       ; Timer Interrupt Rate
M_SCKP EQU 15      ; SCI Clock Polarity
M_REIE EQU 16      ; SCI Error Interrupt Enable (REIE)

;       SCI Status Register Bit Flags

M_TRNE EQU 0       ; Transmitter Empty
M_TDRE EQU 1       ; Transmit Data Register Empty
M_RDRF EQU 2       ; Receive Data Register Full
M_IDLE EQU 3       ; Idle Line Flag
M_OR EQU 4         ; Overrun Error Flag
M_PE EQU 5         ; Parity Error
M_FE EQU 6         ; Framing Error Flag
M_R8 EQU 7         ; Received Bit 8 (R8) Address

;       SCI Clock Control Register

M_CD EQU $FFF      ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12       ; Clock Out Divider
M_SCP EQU 13       ; Clock Prescaler
M_RCM EQU 14       ; Receive Clock Mode Source Bit
M_TCM EQU 15       ; Transmit Clock Source Bit

;-----------------------------------------------------------------------
-
;
;      EQUATES for Synchronous Serial Interface (SSI)
;
;-----------------------------------------------------------------------
-

;
;       Register Addresses Of SSI0
M_TX00 EQU $FFFFBC ; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB ; SSIO Transmit Data Register 1
M_TX02 EQU $FFFFBA ; SSIO Transmit Data Register 2
M_TSR0 EQU $FFFFB9 ; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8  ; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7; SSI0 Status Register
M_CRB0 EQU $FFFFB6 ; SSI0 Control Register B
M_CRA0 EQU $FFFFB5 ; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4; SSI0 Transmit Slot Mask Register A
```

```
M_TSMB0 EQU $FFFFB3; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1; SSI0 Receive Slot Mask Register B

;       Register Addresses Of SSI1
M_TX10 EQU $FFFFAC ; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB ; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA ; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9 ; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8  ; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7; SSI1 Status Register
M_CRB1 EQU $FFFFA6 ; SSI1 Control Register B
M_CRA1 EQU $FFFFA5 ; SSI1 Control Register A
M_TSMA1 EQU $FFFFA4; SSI1 Transmit Slot Mask Register A
M_TSMB1 EQU $FFFFA3; SSI1 Transmit Slot Mask Register B
M_RSMA1 EQU $FFFFA2; SSI1 Receive Slot Mask Register A
M_RSMB1 EQU $FFFFA1; SSI1 Receive Slot Mask Register B

;       SSI Control Register A Bit Flags

M_PM EQU $FF       ; Prescale Modulus Select Mask (PM0-PM7)
M_PSR EQU 11       ; Prescaler Range
M_DC EQU $1F000    ; Frame Rate Divider Control Mask (DC0-DC7)
M_ALC EQU 18       ; Alignment Control (ALC)
M_WL EQU $380000   ; Word Length Control Mask (WL0-WL7)
M_SSC1 EQU 22      ; Select SC1 as TR #0 drive enable (SSC1)

;       SSI Control Register B Bit Flags

M_OF EQU $3        ; Serial Output Flag Mask
M_OF0 EQU 0        ; Serial Output Flag 0
M_OF1 EQU 1        ; Serial Output Flag 1
M_SCD EQU $1C      ; Serial Control Direction Mask
M_SCD0 EQU 2       ; Serial Control 0 Direction
M_SCD1 EQU 3       ; Serial Control 1 Direction
M_SCD2 EQU 4       ; Serial Control 2 Direction
M_SCKD EQU 5       ; Clock Source Direction
M_SHFD EQU 6       ; Shift Direction
M_FSL EQU $180     ; Frame Sync Length Mask (FSL0-FSL1)
M_FSL0 EQU 7       ; Frame Sync Length 0
M_FSL1 EQU 8       ; Frame Sync Length 1
M_FSR EQU 9        ; Frame Sync Relative Timing
M_FSP EQU 10       ; Frame Sync Polarity
M_CKP EQU 11       ; Clock Polarity
M_SYN EQU 12       ; Sync/Async Control
M_MOD EQU 13       ; SSI Mode Select
M_SSTE EQU $1C000  ; SSI Transmit enable Mask
M_SSTE2 EQU 14     ; SSI Transmit #2 Enable
M_SSTE1 EQU 15     ; SSI Transmit #1 Enable
M_SSTE0 EQU 16     ; SSI Transmit #0 Enable
M_SSRE EQU 17      ; SSI Receive Enable
M_SSTIE EQU 18     ; SSI Transmit Interrupt Enable
M_SSRIE EQU 19     ; SSI Receive Interrupt Enable
```

```
M_STLIE EQU 20     ; SSI Transmit Last Slot Interrupt Enable
M_SRLIE EQU 21     ; SSI Receive Last Slot Interrupt Enable
M_STEIE EQU 22     ; SSI Transmit Error Interrupt Enable
M_SREIE EQU 23     ; SSI Receive Error Interrupt Enable


;       SSI Status Register Bit Flags

M_IF EQU $3        ; Serial Input Flag Mask
M_IF0 EQU 0        ; Serial Input Flag 0
M_IF1 EQU 1        ; Serial Input Flag 1
M_TFS EQU 2        ; Transmit Frame Sync Flag
M_RFS EQU 3        ; Receive Frame Sync Flag
M_TUE EQU 4        ; Transmitter Underrun Error FLag
M_ROE EQU 5        ; Receiver Overrun Error Flag
M_TDE EQU 6        ; Transmit Data Register Empty
M_RDF EQU 7        ; Receive Data Register Full

;       SSI Transmit Slot Mask Register A

M_SSTSA EQU $FFFF  ; SSI Transmit Slot Bits Mask A (TS0-TS15)

;       SSI Transmit Slot Mask Register B

M_SSTSB EQU $FFFF  ; SSI Transmit Slot Bits Mask B (TS16-TS31)

;       SSI Receive Slot Mask Register A

M_SSRSA EQU $FFFF  ; SSI Receive Slot Bits Mask A (RS0-RS15)

;       SSI Receive Slot Mask Register B

M_SSRSB EQU $FFFF  ; SSI Receive Slot Bits Mask B (RS16-RS31)



;------------------------------------------------------------------------
-
;
;       EQUATES for Exception Processing
;
;------------------------------------------------------------------------
-


;       Register Addresses

M_IPRC EQU $FFFFFF ; Interrupt Priority Register Core
M_IPRP EQU $FFFFFE ; Interrupt Priority Register Peripheral

;       Interrupt Priority Register Core (IPRC)

M_IAL EQU $7       ; IRQA Mode Mask
```

```
M_IAL0 EQU 0       ; IRQA Mode Interrupt Priority Level (low)
M_IAL1 EQU 1       ; IRQA Mode Interrupt Priority Level (high)
M_IAL2 EQU 2       ; IRQA Mode Trigger Mode
M_IBL EQU $38      ; IRQB Mode Mask
M_IBL0 EQU 3       ; IRQB Mode Interrupt Priority Level (low)
M_IBL1 EQU 4       ; IRQB Mode Interrupt Priority Level (high)
M_IBL2 EQU 5       ; IRQB Mode Trigger Mode
M_ICL EQU $1C0     ; IRQC Mode Mask
M_ICL0 EQU 6       ; IRQC Mode Interrupt Priority Level (low)
M_ICL1 EQU 7       ; IRQC Mode Interrupt Priority Level (high)
M_ICL2 EQU 8       ; IRQC Mode Trigger Mode
M_IDL EQU $E00     ; IRQD Mode Mask
M_IDL0 EQU 9       ; IRQD Mode Interrupt Priority Level (low)
M_IDL1 EQU 10      ; IRQD Mode Interrupt Priority Level (high)
M_IDL2 EQU 11      ; IRQD Mode Trigger Mode
M_D0L EQU $3000    ; DMA0 Interrupt priority Level Mask
M_D0L0 EQU 12      ; DMA0 Interrupt Priority Level (low)
M_D0L1 EQU 13      ; DMA0 Interrupt Priority Level (high)
M_D1L EQU $C000    ; DMA1 Interrupt Priority Level Mask
M_D1L0 EQU 14      ; DMA1 Interrupt Priority Level (low)
M_D1L1 EQU 15      ; DMA1 Interrupt Priority Level (high)
M_D2L EQU $30000   ; DMA2 Interrupt priority Level Mask
M_D2L0 EQU 16      ; DMA2 Interrupt Priority Level (low)
M_D2L1 EQU 17      ; DMA2 Interrupt Priority Level (high)
M_D3L EQU $C0000   ; DMA3 Interrupt Priority Level Mask
M_D3L0 EQU 18      ; DMA3 Interrupt Priority Level (low)
M_D3L1 EQU 19      ; DMA3 Interrupt Priority Level (high)
M_D4L EQU $300000  ; DMA4 Interrupt priority Level Mask
M_D4L0 EQU 20      ; DMA4 Interrupt Priority Level (low)
M_D4L1 EQU 21      ; DMA4 Interrupt Priority Level (high)
M_D5L EQU $C00000  ; DMA5 Interrupt priority Level Mask
M_D5L0 EQU 22      ; DMA5 Interrupt Priority Level (low)
M_D5L1 EQU 23      ; DMA5 Interrupt Priority Level (high)


;       Interrupt Priority Register Peripheral (IPRP)

M_HPL EQU $3       ; Host Interrupt Priority Level Mask
M_HPL0 EQU 0       ; Host Interrupt Priority Level (low)
M_HPL1 EQU 1       ; Host Interrupt Priority Level (high)
M_S0L EQU $C       ; SSI0 Interrupt Priority Level Mask
M_S0L0 EQU 2       ; SSI0 Interrupt Priority Level (low)
M_S0L1 EQU 3       ; SSI0 Interrupt Priority Level (high)
M_S1L EQU $30      ; SSI1 Interrupt Priority Level Mask
M_S1L0 EQU 4       ; SSI1 Interrupt Priority Level (low)
M_S1L1 EQU 5       ; SSI1 Interrupt Priority Level (high)
M_SCL EQU $C0      ; SCI  Interrupt Priority Level  Mask
M_SCL0 EQU 6       ; SCI  Interrupt Priority Level  (low)
M_SCL1 EQU 7       ; SCI  Interrupt Priority Level  (high)
M_T0L EQU $300     ; TIMER Interrupt Priority Level Mask
M_T0L0 EQU 8       ; TIMER Interrupt Priority Level (low)
M_T0L1 EQU 9       ; TIMER Interrupt Priority Level (high)
```

```
;-----------------------------------------------------------------------
-
;
;       EQUATES for TIMER
;
;-----------------------------------------------------------------------
-

;       Register Addresses Of TIMER0

M_TCSR0 EQU $FFFF8F; TIMER0 Control/Status Register
M_TLR0 EQU $FFFF8E ; TIMER0 Load Reg
M_TCPR0 EQU $FFFF8D; TIMER0 Compare Register
M_TCR0 EQU $FFFF8C ; TIMER0 Count Register

;       Register Addresses Of TIMER1

M_TCSR1 EQU $FFFF8B; TIMER1 Control/Status Register
M_TLR1 EQU $FFFF8A ; TIMER1 Load Reg
M_TCPR1 EQU $FFFF89; TIMER1 Compare Register
M_TCR1 EQU $FFFF88 ; TIMER1 Count Register


;       Register Addresses Of TIMER2

M_TCSR2 EQU $FFFF87; TIMER2 Control/Status Register
M_TLR2 EQU $FFFF8  ; TIMER2 Load Reg
M_TCPR2 EQU $FFFF85; TIMER2 Compare Register
M_TCR2 EQU $FFFF84 ; TIMER2 Count Register
M_TPLR EQU $FFFF83 ; TIMER Prescaler Load Register
M_TPCR EQU $FFFF82 ; TIMER Prescalar Count Register


;     Timer Control/Status Register Bit Flags

M_TE EQU 0         ; Timer Enable
M_TOIE EQU 1       ; Timer Overflow Interrupt Enable
M_TCIE EQU 2       ; Timer Compare Interrupt Enable
M_TC EQU $F0       ; Timer Control Mask (TC0-TC3)
M_INV EQU 8        ; Inverter Bit
M_TRM EQU 9        ; Timer Restart Mode
M_DIR EQU 11       ; Direction Bit
M_DI EQU 12        ; Data Input
M_DO EQU 13        ; Data Output
M_PCE EQU 15       ; Prescaled Clock Enable
M_TOF EQU 20       ; Timer Overflow Flag
M_TCF EQU 21       ; Timer Compare Flag

;      Timer Prescaler Register Bit Flags

M_PS EQU $600000   ; Prescaler Source Mask
M_PS0 EQU 21
```

```
M_PS1 EQU 22

;         Timer Control Bits
M_TC0 EQU 4        ; Timer Control 0
M_TC1 EQU 5        ; Timer Control 1
M_TC2 EQU 6        ; Timer Control 2
M_TC3 EQU 7        ; Timer Control 3


;-----------------------------------------------------------------------
-
;
;       EQUATES for Direct Memory Access (DMA)
;
;-----------------------------------------------------------------------
-

;       Register Addresses Of DMA
M_DSTR EQU $FFFFF4 ; DMA Status Register
M_DOR0 EQU $FFFFF3 ; DMA Offset Register 0
M_DOR1 EQU $FFFFF2 ; DMA Offset Register 1
M_DOR2 EQU $FFFFF1 ; DMA Offset Register 2
M_DOR3 EQU $FFFFF0 ; DMA Offset Register 3


;       Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF ; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE ; DMA0 Destination Address Register
M_DCO0 EQU $FFFFED ; DMA0 Counter
M_DCR0 EQU $FFFFEC ; DMA0 Control Register

;       Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB ; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA ; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9 ; DMA1 Counter
M_DCR1 EQU $FFFFE8 ; DMA1 Control Register

;       Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7 ; DMA2 Source Address Register
M_DDR2 EQU $FFFFE6 ; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5 ; DMA2 Counter
M_DCR2 EQU $FFFFE4 ; DMA2 Control Register

;       Register Addresses Of DMA4

M_DSR3 EQU $FFFFE3 ; DMA3 Source Address Register
M_DDR3 EQU $FFFFE2 ; DMA3 Destination Address Register
M_DCO3 EQU $FFFFE1 ; DMA3 Counter
M_DCR3 EQU $FFFFE0 ; DMA3 Control Register
```

```
;       Register Addresses Of DMA4


M_DSR4 EQU $FFFFDF ; DMA4 Source Address Register
M_DDR4 EQU $FFFFDE ; DMA4 Destination Address Register
M_DCO4 EQU $FFFFDD ; DMA4 Counter
M_DCR4 EQU $FFFFDC ; DMA4 Control Register

;       Register Addresses Of DMA5

M_DSR5 EQU $FFFFDB ; DMA5 Source Address Register
M_DDR5 EQU $FFFFDA ; DMA5 Destination Address Register
M_DCO5 EQU $FFFFD9 ; DMA5 Counter
M_DCR5 EQU $FFFFD8 ; DMA5 Control Register

;         DMA Control Register

M_DSS EQU $3       ; DMA Source Space Mask (DSS0-Dss1)
M_DSS0 EQU 0       ; DMA Source Memory space 0
M_DSS1 EQU 1       ; DMA Source Memory space 1
M_DDS EQU $C       ; DMA Destination Space Mask (DDS-DDS1)
M_DDS0 EQU 2       ; DMA Destination Memory Space 0
M_DDS1 EQU 3       ; DMA Destination Memory Space 1
M_DAM EQU $3F0     ; DMA Address Mode Mask (DAM5-DAM0)
M_DAM0 EQU 4       ; DMA Address Mode 0
M_DAM1 EQU 5       ; DMA Address Mode 1
M_DAM2 EQU 6       ; DMA Address Mode 2
M_DAM3 EQU 7       ; DMA Address Mode 3
M_DAM4 EQU 8       ; DMA Address Mode 4
M_DAM5 EQU 9       ; DMA Address Mode 5
M_D3D EQU 10       ; DMA Three Dimensional Mode
M_DRS EQU $F800    ; DMA Request Source Mask (DRS0-DRS4)
M_DCON EQU 16      ; DMA Continuous Mode
M_DPR EQU $60000   ; DMA Channel Priority
M_DPR0 EQU 17      ; DMA Channel Priority Level (low)
M_DPR1 EQU 18      ; DMA Channel Priority Level (high)
M_DTM EQU $380000  ; DMA Transfer Mode Mask (DTM2-DTM0)
M_DTM0 EQU 19      ; DMA Transfer Mode 0
M_DTM1 EQU 20      ; DMA Transfer Mode 1
M_DTM2 EQU 21      ; DMA Transfer Mode 2
M_DIE EQU 22       ; DMA Interrupt Enable bit
M_DE EQU 23        ; DMA Channel Enable bit

;       DMA Status Register

M_DTD EQU $3F      ; Channel Transfer Done Status MASK (DTD0-DTD5)
M_DTD0 EQU 0       ; DMA Channel Transfer Done Status 0
M_DTD1 EQU 1       ; DMA Channel Transfer Done Status 1
M_DTD2 EQU 2       ; DMA Channel Transfer Done Status 2
M_DTD3 EQU 3       ; DMA Channel Transfer Done Status 3
M_DTD4 EQU 4       ; DMA Channel Transfer Done Status 4
M_DTD5 EQU 5       ; DMA Channel Transfer Done Status 5
M_DACT EQU 8       ; DMA Active State
```

```
M_DCH EQU $E00     ; DMA Active Channel Mask (DCH0-DCH2)
M_DCH0 EQU 9       ; DMA Active Channel 0
M_DCH1 EQU 10      ; DMA Active Channel 1
M_DCH2 EQU 11      ; DMA Active Channel 2


;-----------------------------------------------------------------------
-
;
;       EQUATES for Phase Lock Loop (PLL)
;
;-----------------------------------------------------------------------
-

;       Register Addresses Of PLL

M_PCTL EQU $FFFFFD ; PLL Control Register

;       PLL Control Register

M_MF EQU $FFF      ; Multiplication Factor Bits Mask (MF0-MF11)
M_DF EQU $7000     ; Division Factor Bits Mask (DF0-DF2)
M_XTLR EQU 15      ; XTAL Range select bit
M_XTLD EQU 16      ; XTAL Disable Bit
M_PSTP EQU 17      ; STOP Processing State Bit
M_PEN EQU 18       ; PLL Enable Bit
M_PCOD EQU 19      ; PLL Clock Output Disable Bit
M_PD EQU $F00000   ; PreDivider Factor Bits Mask (PD0-PD3)


;-----------------------------------------------------------------------
-
;
;       EQUATES for BIU
;
;-----------------------------------------------------------------------
-

;       Register Addresses Of BIU


M_BCR EQU $FFFFFB  ; Bus Control Register
M_DCR EQU $FFFFFA  ; DRAM Control Register
M_AAR0 EQU $FFFFF9 ; Address Attribute Register 0
M_AAR1 EQU $FFFFF8 ; Address Attribute Register 1
M_AAR2 EQU $FFFFF7 ; Address Attribute Register 2
M_AAR3 EQU $FFFFF6 ; Address Attribute Register 3
M_IDR EQU $FFFFF5  ; ID Register

;       Bus Control Register

M_BA0W EQU $1F     ; Area 0 Wait Control Mask (BA0W0-BA0W4)
M_BA1W EQU $3E0    ; Area 1 Wait Control Mask (BA1W0-BA14)
```

```
M_BA2W EQU $1C00   ; Area 2 Wait Control Mask (BA2W0-BA2W2)
M_BA3W EQU $E000   ; Area 3 Wait Control Mask (BA3W0-BA3W3)
M_BDFW EQU $1F0000 ; Default Area Wait Control Mask (BDFW0-BDFW4)
M_BBS EQU 21       ; Bus State
M_BLH EQU 22       ; Bus Lock Hold
M_BRH EQU 23       ; Bus Request Hold

;       DRAM Control Register

M_BCW EQU $3       ; In Page Wait States Bits Mask (BCW0-BCW1)
M_BRW EQU $C       ; Out Of Page Wait States Bits Mask (BRW0-BRW1)
M_BPS EQU $300     ; DRAM Page Size Bits Mask (BPS0-BPS1)
M_BPLE EQU 11      ; Page Logic Enable
M_BME EQU 12       ; Mastership Enable
M_BRE EQU 13       ; Refresh Enable
M_BSTR EQU 14      ; Software Triggered Refresh
M_BRF EQU $7F8000  ; Refresh Rate Bits Mask (BRF0-BRF7)
M_BRP EQU 23       ; Refresh prescaler

;       Address Attribute Registers

M_BAT EQU $3       ; External Access Type and Pin Definition Bits Mask
(BAT0-BAT1)
M_BAAP EQU 2       ; Address Attribute Pin Polarity
M_BPEN EQU 3       ; Program Space Enable
M_BXEN EQU 4       ; X Data Space Enable
M_BYEN EQU 5       ; Y Data Space Enable
M_BAM EQU 6        ; Address Muxing
M_BPAC EQU 7       ; Packing Enable
M_BNC EQU $F00     ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M_BAC EQU $FFF000  ; Address to Compare Bits Mask (BAC0-BAC11)

;       control and status bits in SR

M_CP EQU $c00000   ; mask for CORE-DMA priority bits in SR
M_CA EQU 0         ; Carry
M_V EQU 1          ; Overflow
M_Z EQU 2          ; Zero
M_N EQU 3          ; Negative
M_U EQU 4          ; Unnormalized
M_E EQU 5          ; Extension
M_L EQU 6          ; Limit
M_S EQU 7          ; Scaling Bit
M_I0 EQU 8         ; Interupt Mask Bit 0
M_I1 EQU 9         ; Interupt Mask Bit 1
M_S0 EQU 10        ; Scaling Mode Bit 0
M_S1 EQU 11        ; Scaling Mode Bit 1
M_SC EQU 13        ; Sixteen_Bit Compatibility
M_DM EQU 14        ; Double Precision Multiply
M_LF EQU 15        ; DO-Loop Flag
M_FV EQU 16        ; DO-Forever Flag
M_SA EQU 17        ; Sixteen-Bit Arithmetic
M_CE EQU 19        ; Instruction Cache Enable
```

```
M_SM EQU 20        ; Arithmetic Saturation
M_RM EQU 21        ; Rounding Mode
M_CP0 EQU 22       ; bit 0 of priority bits in SR
M_CP1 EQU 23       ; bit 1 of priority bits in SR

;       control and status bits in OMR
M_CDP EQU $300     ; mask for CORE-DMA priority bits in OMR
M_MA EQU 0         ; Operating Mode A
M_MB EQU 1         ; Operating Mode B
M_MC EQU 2         ; Operating Mode C
M_MD EQU 3         ; Operating Mode D
M_EBD EQU 4        ; External Bus Disable bit in OMR
M_SD EQU 6         ; Stop Delay
M_CDP0 EQU 8       ; bit 0 of priority bits in OMR
M_CDP1 EQU 9       ; bit 1 of priority bits in OMR
M_BEN EQU 10       ; Burst Enable
M_TAS EQU 11       ; TA Synchronize Select
M_BRT EQU 12       ; Bus Release Timing
M_XYS EQU 16       ; Stack Extension space select bit in OMR.
M_EUN EQU 17       ; Extensed stack UNderflow flag in OMR.
M_EOV EQU 18       ; Extended stack OVerflow flag in OMR.
M_WRP EQU 19       ; Extended WRaP flag in OMR.
M_SEN EQU 20       ; Stack Extension Enable bit in OMR.
;***********************************************************************
**
;
;     EQUATES for DSP56301 interrupts
;     Reference: DSP56301 Specifications Revision 3.00
;
;     Last update: November 15 1993 (Debug request & HI32 interrupts)
;                  December 19 1993 (cosmetic - page and opt directives)
;                  August 16 1994 (change interrupt addresses to be
;                           relative to I_VEC)
;
;***********************************************************************
**

         page      132,55,0,0,0
         opt       mex

intequ  ident   1,0

         if        @DEF(I_VEC)
         ;leave user definition as is.
         else
I_VEC    equ       $0
         endif

;-----------------------------------------------------------------------
-
; Non-Maskable interrupts
;-----------------------------------------------------------------------
-
```

```
I_RESET  EQU  I_VEC+$00   ; Hardware RESET
I_STACK  EQU  I_VEC+$02   ; Stack Error
I_ILL    EQU  I_VEC+$04   ; Illegal Instruction
I_DBG    EQU  I_VEC+$06   ; Debug Request
I_TRAP   EQU  I_VEC+$08   ; Trap
I_NMI    EQU  I_VEC+$0A   ; Non Maskable Interrupt

;-----------------------------------------------------------------------
-
; Interrupt Request Pins
;-----------------------------------------------------------------------
-
I_IRQA   EQU  I_VEC+$10   ; IRQA
I_IRQB   EQU  I_VEC+$12   ; IRQB
I_IRQC   EQU  I_VEC+$14   ; IRQC
I_IRQD   EQU  I_VEC+$16   ; IRQD

;-----------------------------------------------------------------------
-
; DMA Interrupts
;-----------------------------------------------------------------------
-
I_DMA0   EQU  I_VEC+$18   ; DMA Channel 0
I_DMA1   EQU  I_VEC+$1A   ; DMA Channel 1
I_DMA2   EQU  I_VEC+$1C   ; DMA Channel 2
I_DMA3   EQU  I_VEC+$1E   ; DMA Channel 3
I_DMA4   EQU  I_VEC+$20   ; DMA Channel 4
I_DMA5   EQU  I_VEC+$22   ; DMA Channel 5



;-----------------------------------------------------------------------
-
; Timer Interrupts
;-----------------------------------------------------------------------
-
I_TIM0C  EQU  I_VEC+$24   ; TIMER 0 compare
I_TIM0OF EQU  I_VEC+$26   ; TIMER 0 overflow
I_TIM1C  EQU  I_VEC+$28   ; TIMER 1 compare
I_TIM1OF EQU  I_VEC+$2A   ; TIMER 1 overflow
I_TIM2C  EQU  I_VEC+$2C   ; TIMER 2 compare
I_TIM2OF EQU  I_VEC+$2E   ; TIMER 2 overflow

;-----------------------------------------------------------------------
-
; ESSI Interrupts
;-----------------------------------------------------------------------
-
I_SI0RD  EQU  I_VEC+$30   ; ESSI0 Receive Data
I_SI0RDE EQU  I_VEC+$32   ; ESSI0 Receive Data With Exception Status
I_SI0RLS EQU  I_VEC+$34   ; ESSI0 Receive last slot
I_SI0TD  EQU  I_VEC+$36   ; ESSI0 Transmit data
I_SI0TDE EQU  I_VEC+$38   ; ESSI0 Transmit Data With Exception Status
```

```
I_SI0TLS EQU  I_VEC+$3A   ; ESSI0 Transmit last slot
I_SI1RD  EQU  I_VEC+$40   ; ESSI1 Receive Data
I_SI1RDE EQU  I_VEC+$42   ; ESSI1 Receive Data With Exception Status
I_SI1RLS EQU  I_VEC+$44   ; ESSI1 Receive last slot
I_SI1TD  EQU  I_VEC+$46   ; ESSI1 Transmit data
I_SI1TDE EQU  I_VEC+$48   ; ESSI1 Transmit Data With Exception Status
I_SI1TLS EQU  I_VEC+$4A   ; ESSI1 Transmit last slot

;------------------------------------------------------------------------
-
; SCI Interrupts
;------------------------------------------------------------------------
-
I_SCIRD  EQU  I_VEC+$50   ; SCI Receive Data
I_SCIRDE EQU  I_VEC+$52   ; SCI Receive Data With Exception Status
I_SCITD  EQU  I_VEC+$54   ; SCI Transmit Data
I_SCIIL  EQU  I_VEC+$56   ; SCI Idle Line
I_SCITM  EQU  I_VEC+$58   ; SCI Timer

;------------------------------------------------------------------------
-
; HOST Interrupts
;------------------------------------------------------------------------
-
I_HPTT   EQU  I_VEC+$60   ; Host PCI Transaction Termination
I_HPTA   EQU  I_VEC+$62   ; Host PCI Transaction Abort
I_HPPE   EQU  I_VEC+$64   ; Host PCI Parity Error
I_HPTC   EQU  I_VEC+$66   ; Host PCI Transfer Complete
I_HPMR   EQU  I_VEC+$68   ; Host PCI Master Receive
I_HSR    EQU  I_VEC+$6A   ; Host Slave Receive
I_HPMT   EQU  I_VEC+$6C   ; Host PCI Master Transmit
I_HST    EQU  I_VEC+$6E   ; Host Slave Transmit
I_HPMA   EQU  I_VEC+$70   ; Host PCI Master Address
I_HCNMI  EQU  I_VEC+$72   ; Host Command/Host NMI (Default)

;------------------------------------------------------------------------
-
; INTERRUPT ENDING ADDRESS
;------------------------------------------------------------------------
-
I_INTEND EQU  I_VEC+$FF   ; last address of interrupt vector space
```

APPENDIX B

DSP56301 BOOSTRAP CODE LISTING

```
; BOOTSTRAP CODE FOR DSP56301 - (C) Copyright 1996 Motorola Inc.
; Revised June 18, 1996.
;
; Bootstrap through the Host Interface, External EPROM or SCI.
;
; This  is the Bootstrap  program  contained  in the DSP56301 192-word  Boot
; ROM.  This  program  can  load  any program  RAM segment  from an external
; EPROM, from the Host Interface or from the SCI serial interface.
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; If MD:MC:MB:MA=x000,  then  the  Boot  ROM is bypassed  and the DSP56301
; will start fetching instructions  beginning  with address $C00000 (MD=0)
; or $008000  (MD=1)  assuming  that  an external  memory  of SRAM type is
; used.  The accesses  will  be performed  using  31 wait  states with no address
; attributes selected (default area).
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; If  MD:MC:MB:MA=x001,   then   it  loads   a  program   RAM segment   from
; consecutive  byte-wide  P memory  locations,  starting  at P:$D00000  (bits
; 7-0).  The  memory  is  selected  by  the  Address  Attribute AA1  and  is
; accessed with 31 wait states.
;
; The EPROM  bootstrap  code expects  first  to read 3 bytes specifying  the
; number  of program  words,  afterwards  3 bytes specifying  the address  to
; start  loading  the program  words  and then 3 bytes for each program  word
; to be loaded.  The number of words,  the starting  address  and the program
; words  are  read  least  significant  byte  first  followed  by the mid and
; then by the most significant byte.
;
; The program  words  will  be condensed  into  24-bit  words  and stored  in
; contiguous  PRAM  memory  locations  starting  at  the  specified starting
; address.  After  reading  the  program  words,  program  execution starts
; from the same address where loading started.
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; If MD:MC:MB:MA=x010, then it loads the program RAM from the SCI interface.
;
```

```
; The SCI bootstrap  code expects  first  to receive  3 bytes specifying  the
; number  of program  words,  afterwards  3 bytes specifying  the address  to
; start  loading  the program  words  and then 3 bytes for each program  word
; to be loaded.  The number of words,  the starting  address  and the program
; words  are received  least significant  byte first followed  by the mid and
; then by the most significant byte.
;
; The program  words  will  be condensed  into  24-bit  words  and stored  in
; contiguous  PRAM  memory  locations  starting  at  the  specified  starting
; address.  After  reading  the  program  words,  program  execution  starts
; from the same address where loading started.
;
; The SCI is programmed  to work  in asynchronous  mode  with 8 data bits,  1
; stop  bit  and  no parity.  The  clock  source  is external  and  the clock
; frequency  must  be 16x the baud  rate.  After  each  byte is received,  it
; is echoed back through the SCI transmitter.
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; If MD:MC:MB:MA=x011,  then it loads the program RAM from the Host Interface
; programmed to operate in the Universal Bus mode supporting 56301-to-56301
; glue less connection.
;
; The HI32  bootstrap  code expects  first  to read a 24-bit  word specifying
; the number  of program  words,  afterwards  a 24-bit  word  specifying  the
; address  to start  loading  the program  words  and then  24-bit  word  for
; each  program  word  to be loaded.
;
; The   program   words   will   be   stored   in  contiguous   PRAM   memory
; locations    starting    at    the    specified    starting    address.   After
; reading  the  program  words,  program  execution  starts  from  the  same
; address where loading started.
;
; The Host Interface  bootstrap  load program  may be stopped  by setting the
; Host  Flag  0 (HF0)  in HCTR  register.  This will start  execution  of the
; loaded program from the specified starting address.
;
; During  the access,  the HAEN and HA10-HA3  pins must be driven  low;  pins
; HA2-HA0 select the HI32 registers.
; Before  booting  through  the Host  Interface  it is recommended  that  the
; Host  boot  program  will verify  that the HI32 is operational,  by reading
; the status register (HSTR) and confirm that its value is $3.
;
; Suggested 56301-to-56301 connection:
;
;   slave   master
;   56301/HI32     56301/PortA
```

```
;
;   HA[10:3]   <-  A[10:3]        ; selects HI32 (base address 00000000)
;   HA[2:0]    <-  A[2:0]         ; selects HTXR registers
;   HD[24:0]   <-> D[24:0]        ; Data bus
;   HBS_       <-  BS_            ; Bus Strobe (optional, see Note1)
;   HAEN       <-  AAx            ; DMA cycle disable (AAx is active low)
;   HTA        ->  TA_            ; Transfer Acknowledge (optional, see Note2)
;   HIRQ_      ->  IRQx_         ; Interrupt Request (active low, open drain)
;   HWR_       <-  WR_            ; Write strobe
;   HRD_       <-  RD_            ; Read strobe
;   HRST       <-  system reset   ; Reset (active low)
;
; Pins  HP31,  HP32  and HDAK_  must  be tied to Vcc.  Pins HP[22:20]  may be
; used  as GPIO pins.  Pin HINTA_  may be used as software  driven  interrupt
; request pin.
;
; Note1:  If HBS_ to BS_  connection is used,  the synchronous  connection of
; the  HI32  is  used  and  therefore  the  56301/master  should  access  the
; 56301/slave  as  SRAM  with  2 wait  states.  In  addition  the  CLKOUT  of
; 56301/master  should  be  connected  to  EXTAL  of  56301/slave,  and  both
; master  and  slave  should  enable  the  PLL  while  in the  case  of slave
; multiplication,   division  and  pre-division   factors  should  be  one  to
; guarantee synchronization between master and slave.
; In the case of asynchronous connection, HBS_ must be tied to Vcc.
;
; Note2:  If HTA  to HTA_  connection  is not  used,  it is recommended  that
; the HOST  Processor’s  boot  program  will  verify  that the Host Interface
; is ready,  by reading  the status register  (HSTR)  and confirm that TRDY=1
; or HTRQ=1.
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; If MD:MC:MB:MA=x100, then it loads the program RAM from the Host
; Interface programmed to operate in the PCI target (slave) mode.
;
; The HI32  bootstrap  code expects  first  to read a 24-bit  word specifying
; the number  of program  words,  afterwards  a 24-bit  word  specifying  the
; address  to start  loading  the program  words  and then  24-bit  word  for
; each  program  word  to be loaded.
;
; The   program   words   will   be   stored   in contiguous   PRAM   memory
; locations    starting    at    the    specified    starting    address.   After
; reading  the  program  words,  program  execution  starts  from  the  same
; address where loading started.
;
; The Host Interface  bootstrap  load program  may be stopped  by setting the
; Host  Flag  0 (HF0)  in HCTR  register.  This will start  execution  of the
```

```
; loaded program from the specified starting address.
;
; The HOST Processor  must first  configure  the Host Interface  as PCI slave
; and then  start  writing  data  to the Host  Interface.  The HOST Processor
; must  program  the  HCTR  HTF1-HTF0   bits  as  01,   10  or  11  and  then
; correspondingly drive the 24-bit data mapped into 32-bit PCI bus word.
;
; Note  that  for the synchronization  purposes,  the DSP to PCI clock  ratio
; should be more then 5/3.
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; If MD:MC:MB:MA=x101, then it loads the program RAM from the Host
; Interface programmed to operate in the Universal Bus mode supporting
; ISA (slave) glue less connection.
;
; Using  self  configuration  mode,  the base  address  in CBMA  is initially
; written  with  $2f  which  corresponds  to  an  ISA  HTXR  address  of $2fe
; (Serial Port 2 Modem Status read only register).
;
; The HI32 bootstrap code expects to read 32 consecutive times the “magic
; number” $0037. Subsequently the bootstrap code expects to read a 16-bit word
; which is the designated ISA Port Address; this address is written into the
; CBMA. The HOST Processor must poll for the Host Interface to be re-configured.
; This must be done by reading the HSTR and verifying that the value $0013 is
; read. From this moment the HOST Processor may start writing data to the
; Host Interface.
;
; The  HI32  bootstrap  code  expects  first  to  read  a  24-bit  word  (see
; Note  below)  specifying  the  number  of  program  words,  afterwards  a
; 24-bit  word  specifying  the  address  to  start  loading  the  program
; words and then 24-bit word for each program word to be loaded.
;
; The   program   words   will   be   stored   in  contiguous   PRAM   memory
; locations   starting   at   the   specified   starting   address.   After
; reading  the  program  words,  program  execution  starts  from  the  same
; address where loading started.
;
; The Host Interface  bootstrap  load program  may be stopped  by setting the
; Host  Flag  0 (HF0)  in HCTR  register.  This will start  execution  of the
; loaded program from the specified starting address.
;
; Note:  This  ISA connection  implies  16 bit data  width  access  only  and
; that  the  number  of 16-bit  wide  words  that  are  transferred  must  be
; even.
;
; The 24-bit  words  has to be packed  into  16-bit  ISA words  and then sent
```

```
; by the HOST Processor in the following sequence:
;
;   |  M0  |  L0  |
;   |  L1  |  H0  |
;   |  H1  |  M1  |
;
; The boot program  will convert  every  three 16-bit  wide host words to two
; 24-bit wide 56301 opcodes in the following format:
;
;   |  H0  |  M0  |  L0  |
;   |  H1  |  M1  |  L1  |
;
; The Host  Processor  must  program  the Host  Interface  to operate  in the
; zero fill mode (HTF1-HTF0 = 01 in HCTR).
;
; Suggested 56301 to ISA connection:
;
;   HA[10]  <- SBHE_            ; selects HI32 (base address 10011111)
;   HA[9]   <- SA[0]            ; selects HI32 (base address 10011111)
;   HA[8:3] <- SA[9:4]          ; selects HI32 (base address 10011111)
;   HA[2:0] <- SA[3:1]          ; selects HTXR registers
;   HD[15:0] - SD[15:0]         ; Data bus
;   HD[23:16] - Not connected   ; High Data Bus - Should be pulled up or down
;   HDBEN_  -> OE_              ; Output enable of transceivers
;   HDBDR   -> DIR              ; Direction of transceivers
;   HSAK_   -> IO16_            ; 16 bit data word
;   HBS_    <- Vcc              ; Bus Strobe disabled
;   HAEN    <- AEN              ; DMA cycle enable
;   HTA     -> CHRDY            ; Channel ready
;   HWR_    <- IOWC_            ; IO/DMA write strobe
;   HRD_    <- IORC_            ; IO/DMA read strobe
;   HRST    <- inverted RSTDRV  ; invert ISA reset
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; If  MD:MC:MB:MA=x110,  then  it  loads  the  program  RAM  from  the  Host
; Interface  programmed  to  operate  in the  Universal  Bus  (UB)  mode,  in
; double-strobe pin configuration.
;
; The HI32 bootstrap  code expects first  to receive  3 bytes specifying  the
; number  of program  words,  afterwards  3 bytes specifying  the address  to
; start  loading  the program  words  and then 3 bytes for each program  word
; to be loaded.  The number of words,  the starting  address  and the program
; words  are received  least significant  byte first followed  by the mid and
; then by the most significant byte.
;
; The program  words  will  be condensed  into  24-bit  words  and stored  in
```

```
; contiguous  PRAM  memory  locations  starting  at  the  specified  starting
; address.   After  reading  the  program  words,  program  execution  starts
; from the same address where loading started.
;
; The Host Interface  bootstrap  load program  may be stopped  by setting the
; Host  Flag  0 (HF0)  in HCTR  register.  This will start  execution  of the
; loaded program from the specified starting address.
;
; The user must externally decode the port address with active  low logic and
; connect the select line to HAEN; all the address lines shall be pulled down
; except for HA3, HA2 and HA1 that select the HOST Interface registers.
;
; When booting through the Host Interface it is recommended that the Host
; boot program will verify that the Host Interface is operational, by
; reading the status register (HSTR) and confirm that TRDY=1.
;
; When  booting  through  the  Host  Interface,  it is recommended  that  the
; HOST  Processor's  boot  program  will  verify  that the Host Interface  is
; ready,  by reading  the status  register  (HSTR)  and confirm  that  TRDY=1
; or HTRQ=1.
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; If  MD:MC:MB:MA=x111,   then  it  loads  the  program  RAM  from  the  Host
; Interface  programmed  to  operate  in the  Universal  Bus  (UB)  mode,  in
; single-strobe pin configuration.
;
; Other than the single-strobe pin configuration, this mode is identical to
; the double-strobe pin configuration UB mode (MD:MC:MB:MA=x110).
;
;

BOOT    equ     $D00000         ; this is the location in P memory
                                ; on the external memory bus
                                ; where the external byte-wide
                                ; EPROM would be located
AARV    equ     $D00409         ; AAR1 selects the EPROM as CE~
                                ; mapped as P from $D00000 to
                                ; $DFFFFF, active low

M_SSR   EQU     $FFFF93         ; SCI Status Register
M_STXL  EQU     $FFFF95         ; SCI Transmit Data Register (low)
M_SRXL  EQU     $FFFF98         ; SCI Receive Data Register (low)
M_SCCR  EQU     $FFFF9B         ; SCI Clock Control Register
M_SCR   EQU     $FFFF9C         ; SCI Control Register
M_PCRE  EQU     $FFFF9F         ; Port E Control register
M_DCTR  EQU     $FFFFC5         ; DSP Control Register (DCTR)
```

```
M_DPMC  EQU     $FFFFC7         ; DSP PCI Master Control Register (DPMC)
M_DPAR  EQU     $FFFFC8         ; DSP PCI Address Register (DPAR)
M_DSR   EQU     $FFFFC9         ; DSP Status Register (DSR)
M_DRXR  EQU     $FFFFCB         ; DSP Receive Data FIFO (DRXR)
M_AAR1  EQU     $FFFFF8         ; Address Attribute Register 1


        ORG PL:$ff0000,PL:$ff0000    ; bootstrap code starts at $ff0000

START
        jclr #3,omr,CONT        ; If MD:MC:MB:MA=xxxx continue boot
CONT    clr a #$0a,X0           ; clear a and load X0 with constant $0a0000
        move #$3e,x1             ;  X1=$3E0000  prepare  for  UB  mode  host
programming
                                ; HM=$3 (UB)
                                ; HIRD=1 (HIRQ_ pin - drive high enabled)
                                ; HIRH=1 (HIRQ_ pin - handshake enabled)
                                ; HRSP=1 (HRST pin - active low)
                                ; HTAP=0 (HTA  pin - active high)
                                ; HDSM=0 (Double-strobe pin mode enabled)
        jclr #2,omr,EPRSCILD    ; If MD:MC:MB:MA=x0xx,
                                 ; go load from EPROM/SCI/56301-56301
        jclr #1,omr,IHOSTLD     ; If MD:MC:MB:MA=x10x, go load from PCI/ISA HOST
        jclr #0,omr,UB2HOSTLD   ; If MD:MC:MB:MA=x110, go load from
                                 ; double-strobe UB Host
                                ; If MD:MC:MB:MA=x111, go load from
                                 ;single-strobe UB Host

;============================================================================
; This is the routine that loads from the Host Interface in UB (UNIVERSAL) mode,
; with single-strobe pin configuration (RD/WR,DS).
; MD:MC:MB:MA=x111 - Host UB

UB1HOSTLD
   bset #13,x1             ; HDSM=1 (Double-strobe pin mode disabled)

;============================================================================
; This is the routine that loads from the Host Interface in UB (UNIVERSAL) mode,
; with double-strobe pin configuration (RD,WR).
; MD:MC:MB:MA=x110 - Host UB

UB2HOSTLD
         movep x1,X:M_DCTR ; Configure HI32 in UB mode Single or Double strobe
        do #6,_LOOP0            ; read # of words and start address
        jclr #2,X:M_DSR,*       ; Wait for SRRQ to go high (i.e. data ready)
        movep X:M_DRXR,a2       ;
        asr #8,a,a              ; Shift 8 bit data into A1
_LOOP0                          ;
```

```
        move a1,r0              ; starting address for load
        move a1,r1              ; save it in r1
                                ; a0 holds the number of words
; Download P memory through UB


        do a0,_LOOP1            ; Load instruction words
        do #3,_LOOP2            ; for each byte
_LBLA
        jset #2,X:M_DSR,_LBLB   ; Wait for SRRQ to go high (i.e. data ready)
        jclr #3,X:M_DSR,_LBLA   ; If HF0=1, stop loading new data.
        enddo                   ; Must terminate the do loop
        bra <TERMINATE          ; Terminate loop (enddo) and finish
_LBLB
        movep X:M_DRXR,a2       ; Store 16-bit data in accumulator
        asr #8,a,a              ; Shift 8 bit data into A1
_LOOP2                          ; and go get another 24-bit word.
        movem a1,p:(r0)+        ; Store 24-bit data in P mem
         nop                     ; movem cannot be at LA.
_LOOP1                          ; and go get another 24-bit word.
        bra <FINISH             ; finish bootstrap

;========================================================================
IHOSTLD
        jclr #0,omr,PCIHOSTLD   ; If MD:MC:MB:MA=x100, go load from PCI HOST

;========================================================================
; This routine loads from the Host Interface in ISA (UNIVERSAL) mode.
; MD:MC:MB:MA=x101 - Host ISA

; Using self configuration mode, the base address in CBMA is written with
; $2f which corresponds to an ISA HTXR address of $2fe (Serial Port 2 Modem
; Status read only register).

ISAHOSTLD
        move #$5a,b             ; b1=$5a0000
        movep b1,X:M_DCTR       ; Configure HI32 as Self-Config
        movep #$00002f,X:M_DPMC ; write to DPMC
        rep #4
       movep X0,X:M_DPAR       ; write to DPAR (CSTR+CCMR,CCCR+CRID,CLAT,CBMA)
                                ; completing 32 bit write
; Switch to ISA mode
        movep X0,X:M_DCTR       ; Software personal reset
        move #$010020,y1        ; width 16, offset 32
                               ; (also used as replacement to needed NOP after
                                 ;sw reset!)
        movep #$3a0000,X:M_DCTR ; HM=$3 (UB)
```

```
                                ; HIRD=1 (HIRQ_ pin - drive high enabled)
                                ; HIRH=0 (HIRQ_ pin - handshake disabled)
                                ; HRSP=1 (HRST pin - active low)
                                ; HDRP=0 (HDRQ pin - active high)
                                ; HTAP=0 (HTA  pin - active high)
                                ; HDSM=0 (Data-strobe pin mode enabled)

; read the “magic sequence” 32 consecutive words with value $37
_LBLC
        do #32,_LOOP3           ;
        jclr #2,X:M_DSR,*       ; Wait for SRRQ to go high (i.e. data ready)
        movep X:M_DRXR,A1       ; Store 24-bit data into A1
        and #$00ffff,A          ; Mask upper byte
        cmp #$37,A              ; Compare the 24-bit dat to $000037
        beq <_LBLD              ; If data = $37 then go back to loop
        enddo                   ; else break the loop and retry
        bra <_LBLC
_LBLD
        nop
_LOOP3

; read new CBMA value (“ISA base address”)
        jclr #2,X:M_DSR,*       ; Wait for SRRQ to go high (i.e. data ready)
        movep X:M_DRXR,A1       ; Store 24-bit data into A1

; Switch to Self Configuration mode
        movep X0,X:M_DCTR       ; Software personal reset
        movep A1,X:M_DPMC       ; write to DPMC
                     ; (also used as replacement to needed NOP after sw reset!)
        movep b1,X:M_DCTR       ; Configure HI32 as Self-Config
        rep #4
       movep X0,X:M_DPAR       ; write to DPAR (CSTR+CCMR,CCCR+CRID,CLAT,CBMA)

; Switch to ISA mode
        movep X0,X:M_DCTR       ; Software personal reset
        move #$010010,x1        ; width 16, offset 16
                     ; (also used as replacement to needed NOP after sw reset!)
        movep #$3a0010,x:M_DCTR ; HM=$3 (UB)
                                ; HIRD=1 (HIRQ_ pin - drive high enabled)
                                ; HIRH=0 (HIRQ_ pin - handshake disabled)
                                ; HRSP=1 (HRST pin - active low)
                                ; HDRP=0 (HDRQ pin - active high)
                                ; HTAP=0 (HTA  pin - active high)
                                ; HDSM=0 (Double-strobe pin mode enabled)
                                ; HF4 =1 (turn on flag 4 for handshake)

        jclr #2,X:M_DSR,*       ; Wait for SRRQ to go high (i.e. data ready)
```

```
        movep X:M_DRXR,a0       ; Store number of words
        jclr #2,X:M_DSR,*       ; Wait for SRRQ to go high (i.e. data ready)
        movep X:M_DRXR,x0       ; Store starting address
        jclr #2,X:M_DSR,*       ; Wait for SRRQ to go high (i.e. data ready)
        movep X:M_DRXR,y0       ; Store starting address
        insert x1,x0,a          ; concatenate next 16-bit word
        insert y1,y0,a          ; concatenate next 16-bit word
        move a1,r0              ; start to p-mem
        move a0,a1              ; number of words to transfer

; Download P memory through UB
        lsr a   r0,r1           ; divide loop count by 2 and save r0

        do a1,_LOOP4            ; Load instruction words
_LBLE
        jset #2,X:M_DSR,_LBLF   ; Wait for SRRQ to go high (i.e. data ready)
        jclr #3,X:M_DSR,_LBLE   ; If HF0=1, stop loading new data.
        bra <TERMINATE          ; Terminate loop (enddo) and finish
_LBLF
        movep X:M_DRXR,a0       ; Store 16-bit data in accumulator
_LBLG
        jset #2,X:M_DSR,_LBLH   ; Wait for SRRQ to go high (i.e. data ready)
        jclr #3,X:M_DSR,_LBLG   ; If HF0=1, stop loading new data.
        bra <TERMINATE          ; Terminate loop (enddo) and finish
_LBLH
        movep X:M_DRXR,x0       ; Store 16-bit data in register
_LBLI
        jset #2,X:M_DSR,_LBLJ   ; Wait for SRRQ to go high (i.e. data ready)
        jclr #3,X:M_DSR,_LBLI   ; If HF0=1, stop loading new data.
        bra <TERMINATE          ; Terminate loop (enddo) and finish
_LBLJ
        movep X:M_DRXR,y0       ; Store 16-bit data in register
        insert x1,x0,a          ; concatenate next 16-bit word
        insert y1,y0,a          ; concatenate next 16-bit word
        movem a0,p:(r0)+        ; Store 24-bit data in P mem.
        movem a1,p:(r0)+        ; Store 24-bit data in P mem.
        nop                     ; movem cannot be at LA.
_LOOP4                          ; and go get another 24-bit word.
        bra <FINISH             ; finish bootstrap

;=========================================================================
; This is the routine that loads from the Host Interface in PCI mode.
; MD:MC:MB:MA=x100 - Host PCI

PCIHOSTLD
        bset #20,X:M_DCTR       ; Configure HI32 as PCI
UB3_CONT
```

```
        jclr #2,X:M_DSR,*       ; Wait for SRRQ to go high (i.e. data ready)
        movep X:M_DRXR,a0       ; Store number of words
        jclr #2,X:M_DSR,*       ; Wait for SRRQ to go high (i.e. data ready)
        movep X:M_DRXR,r0       ; Store starting address
        move r0,r1              ; save r0

        do a0,_LOOP5            ; Load instruction words
_LBLK
        jset #2,X:M_DSR,_LBLL   ; Wait for SRRQ to go high (i.e. data ready)
       jclr #3,X:M_DSR,_LBLK   ; If HF0=1, stop loading data. Else check SRRQ.
        bra <TERMINATE          ; Terminate loop (enddo) and finish
_LBLL
        movep X:M_DRXR,P:(R0)+  ; Store 24-bit data in P mem.
        nop                     ; movem cannot be at LA.
_LOOP5                          ; and go get another 24-bit word.
                                ; finish bootstrap
        bra <FINISH             ;

;=========================================================================
EPRSCILD
        jclr #1,omr,EPROMLD     ; If MD:MC:MB:MA=x001, go load from EPROM
        jclr #0,omr,SCILD       ; If MD:MC:MB:MA=x010, go load from SCI
                                ; If MD:MC:MB:MA=x011, 56301-to-56301 boot

;=========================================================================
; This is the routine for 56301-to-56301 boot.
; MD:MC:MB:MA=x011 - HI32 in UB mode, double strobe, HTA pin active low

UB3HOSTLD
        movep #$268000,x:M_DCTR ; HM=$2 (UB)
                     ; HIRD=0 (HIRQ_ pin - drive high disabled, open drain)
                                ; HIRH=1 (HIRQ_ pin - handshake enabled)
                                ; HRSP=1 (HRST pin - active low)
                                ; HDRP=0 (HDRQ pin - active high)
                                ; HTAP=1 (HTA  pin - active low)
                                ; HDSM=0 (Double-strobe pin mode enabled)

        bra <UB3_CONT           ; continue


;=========================================================================
; This is the routine that loads from the SCI.
; MD:MC:MB:MA=x010 - external SCI clock

SCILD
        movep #$0302,X:M_SCR    ; Configure SCI Control Reg
        movep #$C000,X:M_SCCR   ; Configure SCI Clock Control Reg
```

```
        movep #7,X:M_PCRE       ; Configure SCLK, TXD and RXD

        do #6,_LOOP6            ; get 3 bytes for number of
                                ; program words and 3 bytes
                                ; for the starting address
        jclr #2,X:M_SSR,*       ; Wait for RDRF to go high
        movep X:M_SRXL,A2       ; Put 8 bits in A2
        jclr #1,X:M_SSR,*       ; Wait for TDRE to go high
        movep A2,X:M_STXL       ; echo the received byte
        asr #8,a,a
_LOOP6
        move a1,r0              ; starting address for load
        move a1,r1              ; save starting address

        do a0,_LOOP7            ; Receive program words
        do #3,_LOOP8
        jclr #2,X:M_SSR,*       ; Wait for RDRF to go high
        movep X:M_SRXL,A2       ; Put 8 bits in A2
        jclr #1,X:M_SSR,*       ; Wait for TDRE to go high
        movep a2,X:M_STXL       ; echo the received byte
        asr #8,a,a
_LOOP8
        movem a1,p:(r0)+        ; Store 24-bit result in P mem.
        nop                     ; movem cannot be at LA.
_LOOP7
        bra <FINISH             ; Boot from SCI done

;=======================================================================
; This is the routine that loads from external EPROM.
; MD:MC:MB:MA=x001

EPROMLD
        move #BOOT,r2           ; r2 = address of external EPROM
        movep #AARV,X:M_AAR1    ; aar1 configured for SRAM types of access


        do #6,_LOOP9            ; read number of words and starting address
        movem p:(r2)+,a2        ; Get the 8 LSB from ext. P mem.
        asr #8,a,a              ; Shift 8 bit data into A1
_LOOP9                          ;
        move a1,r0              ; starting address for load
        move a1,r1              ; save it in r1
                                ; a0 holds the number of words

        do a0,_LOOP10           ; read program words
        do #3,_LOOP11           ; Each instruction has 3 bytes
        movem p:(r2)+,a2        ; Get the 8 LSB from ext. P mem.
```

```
        asr #8,a,a              ; Shift 8 bit data into A1
_LOOP11                         ; Go get another byte.
        movem a1,p:(r0)+        ; Store 24-bit result in P mem.
        nop                     ; movem cannot be at LA.
_LOOP10                         ; and go get another 24-bit word.
        bra <FINISH             ; Boot from EPROM done

;========================================================================
TERMINATE
        enddo                   ; End the loop before exit.
FINISH

; This is the exit handler that returns execution to normal
; expanded mode and jumps to the RESET vector.

        andi #$0,ccr            ; Clear CCR as if RESET to 0.
        jmp (r1)                ; Then go to starting Prog addr.

; End of bootstrap code. Number of program words: 191.
```

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Preliminary Data

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How to reach us:

USA/Europe/Locations Not Listed:
Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
303-675-2140
1 (800) 441-2447

Mfax™:
RMFAX0@email.sps.mot.com
TOUCHTONE (602) 244-6609
US & Canada ONLY (800) 774-1848

Asia/Pacific:
Motorola Semiconductors H.K. Ltd.
8B Tai Ping Industrial Park
51 Ting Kok Road
Tai Po, N.T., Hong Kong
852-26629298

Technical Resource Center:
1 (800) 521-6274

DSP Helpline
dsphelp@dsp.sps.mot.com

Japan:
Nippon Motorola Ltd.
SPD, Strategic Planning Office
4-32-1, Nishi-Gotanda
Sinagawa-ku, Tokyo 141, Japan
81-3-5487-8488

Internet:
http://www.motorola-dsp.com

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