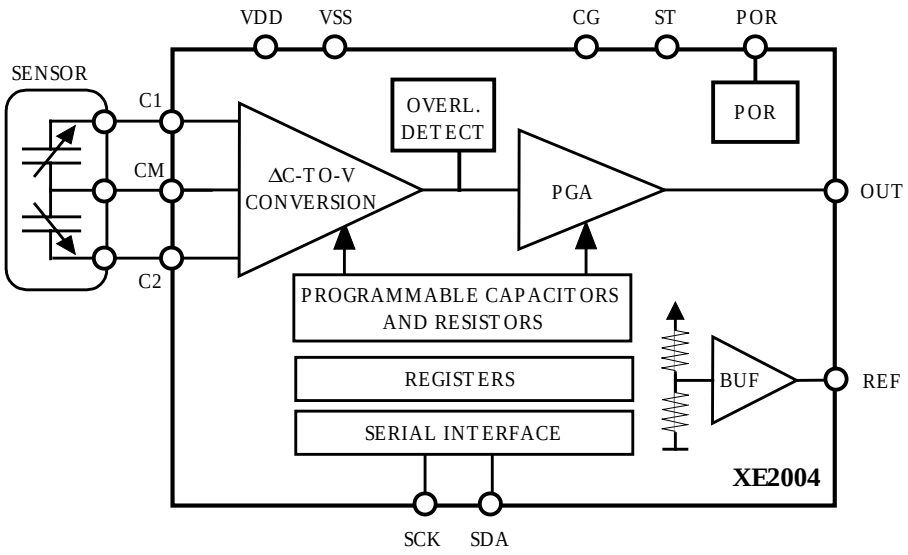
XEMICS

XE2004
Data Sheet



XE2004

Programmable Low-Power Capacitive Sensor Conditioning IC

General Description

XE2004 is a high precision capacitance-to-voltage converter, based on an analog signal path with digital programmable gain, offset and non-linearity. A low-power, low-voltage device, XE2004 provides power-on-reset and sensor overload detection.

The XE2004 is available as dice and in 16 pin SOIC.

Applications

- Micro-machined sensors and MEMS
- Single and differential capacitive sensors
- Pressure sensors
- Touch sensors
- Flow sensors and fluid control
- Gas and humidity sensors
- Portable, battery operated sensors

Key product features

- high precision capacitance-to-voltage conversion
- digital programming of analog signal path
- read-out of electrically floating capacitances
- output voltage proportional to supply voltage
- power-on reset sensor overload detection
- bandwidth up to 10 kHz
- resolves down to 0.25e-18 F/sqrt(Hz) at 5 V
- wide voltage supply range 2.4 – 5.5 V
- low-power operation: 180 uA at 2.4 V
- industrial and extended temperature operating range

Device Options

- 16 pin SOIC WB
- dice
- temperature range –40 – 85 °C (I-grade)
- temperature range –55 – 125 °C (E-grade)

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XE2004

Programmable Low-Power Capacitive Sensor Conditioning IC

Functional Description

The XE2004 implements a capacitance-to-voltage conversion. The output voltage is proportional to the supply voltage, and to a linearized expression including the sensor capacitances and supply voltage.

Analog signal path:
The XE2004 is composed of two stages. The first stage is a capacitance-to-voltage converter. It is based on a floating charge amplifier architecture. This allows the IC to operate only with capacitive sensors that have electrically floating electrodes.The second stage is a programmable gain amplifier.

Digital calibration:
Offset, span and linearity of the analog output signal can be digitally adjusted. The calibration settings are stored in on-chip registers. The power-on-reset sequence of XE2004 allows to upload calibration data from an external non-volatile memory or host control equipment into the registers.

Sensor overload detection:
The XE2004 provides three programmable thresholds that allow the detection of sensory overload. Upon overload, the output voltage of XE2004 will not saturate to the supply rail but give a pre-defined output voltage.

Low sensitivity to sensor's parasitic resistances:
XE2004 accepts relatively low parasitic resistors in parallel with the sensor's capacitances. For example, a parallel resistance as low as 100 kOhm in parallel with the sensor's capacitors will lead to an output error below 0.1 %.

Low power operation:
Several characteristics make XE2004 particularly suited for battery operated applications:

- Low-power, low-voltage operation (2.4 V, 180 uA)
- The power-on-reset function allows automatic uploading of calibration data and user settings from an external non-volatile memory.

Pin Configuration

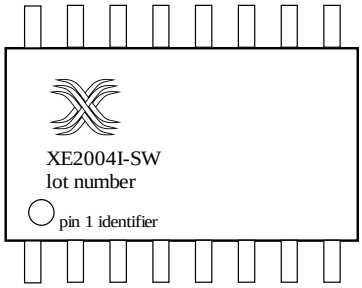


Figure 1 XE2004I-SW in 16 pin SOIC WB (not to scale)

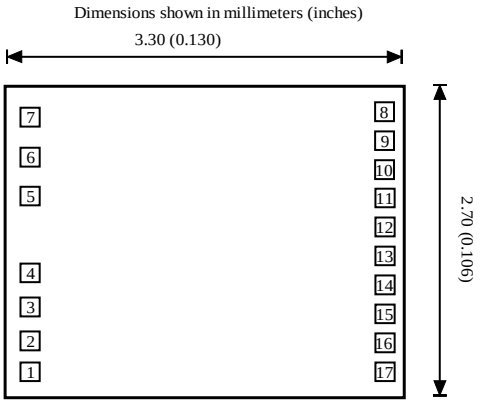


Figure 2 Pad location on XE2004I-000 (not to scale)

XE2004

Programmable Low-Power Capacitive Sensor Conditioning IC

Pin Description

Pin				Description
Position in 16 pin SOIC	Position on die	Name	Type	
-	1	NC	Not connected	-
-	2	NC	Not connected	-
-	3	NC	Not connected	-
1	4	POR	Analog	Power-on-reset signal
16	5	ST	Analog	Test output for oscillator frequency
15	6	SCK	Logic Input	Clock line for data transfer
14	7	SDA	Logic Input/Output	Data line for data transfer
-	8	NC	Not connected	-
12	9	C1	Analog	Upper electrode of capacitive sensor
11	10	CM	Analog	Middle electrode of capacitive sensor
10	11	C2	Analog	Lower electrode of capacitive sensor
-	12	NC	Not connected	-
9	13	VDD	Power	Positive power supply
8	14	REF	Analog Input or Output	Reference voltage (selectable as input or output)
7	15	VSS	Power	Negative power supply
6	16	CG	Analog	Connect optional filter capacitor
5	17	OUT	Analog	Output signal

Absolute Maximum Ratings

Condition	Minimum	Typical	Maximum	Unit
Voltage on any point with respect to VSS	-0.3		5.5	V
Storage temperature	-55		150	°C

Electrical Characteristics

Power supply 2.4 V, operating temperature 27 °C, unless indicated otherwise.

Symbol	description	min	typ	max	Unit	comment
VDD	power supply	2.4		5.5	V	
IVDD	current consumption		180	250	µA	1
start-up time	t_start		20	40	ms	2

Note 1: The current consumption Ivdd varies with temperature and supply voltage, according to the following expression (T is temperature in °C; Vdd is supply voltage in V):

$$Ivdd(T,Vdd) = [Ivdd(27°C,2.4V) + 20\mu A/V \bullet (Vdd - 2.4V)] \bullet (1 + 0.005 \cdot (T - 27°C))$$

Note 2: At 3.0 V, 27 °C. Start-up time of XE2004 only. This duration may be different when combined with a non-volatile memory. Refer to Application Note AN2004.01.

Analog Signal Processing Chain

Transfer function

XE2004 is based on a digitally-controlled, analog signal processing chain. It provides an amplified output voltage that is a function of sensor capacitors CS1 and CS2, of various passive on-chip elements, and of the supply voltage. The passive on-chip elements can be trimmed digitally, thus allowing for the compensation of sensor imperfections such as offset and non-linearity.

IMPORTANT: the C-to-V converter architecture does only read out electrically floating capacitors CS1 and CS2. The connection of pins C1, CM or C2 to any another external element than a electrically floating electrode will adversely affect its operation.

The conversion of the sensor capacitances CS1 and CS2 to the output voltage OUT is realized by two amplifier stages in cascade. The first stage, called C-to-V conversion stage, provides 9 bits of programmable (coarse) offset compensation through registers COFF, COFFP. It also allows for 12 bits non-linearity compensation through registers CNOM, CDEN.

The second stage is a programmable gain amplifier with 8 bits of fine offset tuning register ROFF. Gain is programmable over 10 bits (registers GAINH, GAINL).

The sensor capacitors CS1 and CS2 form a capacitive half-bridge. If CS1 = CS2, XE2004 provides an output signal OUT that equals the value of internal reference voltage REF (suppose Voff is zero). Therefore, by expressing the output signal as OUT – REF, one obtains an output signal of 0 V for CS1 = CS2.

At DC, the overall transfer of XE2004 is given by:

$$VOUT - VREF = -K \cdot \left[\frac{C1 - C2}{C1 + C2 - Ccomp} \bullet VREF + Voff \right] \quad [Volt]$$

Note that the output voltage of the C-to-V conversion stage is equal to:

$$Vm = \frac{C1 - C2}{C1 + C2 - Ccomp} \bullet VREF \quad [Volt]$$

with

$$Ccomp = 22 \bullet \frac{CNOM}{CDEN} \quad [pF]$$

where :

K : gain of the (inverting) programmable gain amplifier

VREF : reference voltage on pin REF, either equal to (VDD – VSS)/2 (if register bit SET.1 to reset to zero, the default setting), or provided externally (if bit SET.1 to set to one).

C1 : = CS1+(1-λ).COFF; CS1 includes all capacitances between pins C1 and CM. λ = 0 if register bit COFFP.0 is reset (zero, default value), λ = 1 if register bit COFFP.0 is set (one).

C2 : = CS2+λ.COFF; CS2 includes all capacitances between pins C2 and CM. λ = 0 if register bit COFFP.0 is reset (zero, default value), λ = 1 if register bit COFFP.0 is set (one).

Ccomp : non-linearity compensation capacitor, determined by two on-chip capacitors CNOM, CDEN, programmable through registers CNOM and CDEN, respectively.

Voff : offset voltage, referred to the input of gain stage. Voff is the sum of offsets contributed by non-ideal amplifiers, and offset introduced through registers COFF, COFFP and ROFF.

Resolution

The output referred noise is 7 uV/sqrt(Hz) at 3 V, while the input referred resolution is 0.25e-18 F/sqrt(Hz) at 5 V (0.42e-18 F/ sqrt(Hz) at V).

Frequency response

The frequency response of the analog signal processing chain is the combination of the C-to-V stage and the programmable gain stage. The gain stage determines the overall bandwidth. The –3 dB cut-off frequency is given by this expression:

$$Bandwidth\ (-3\ dB) = \frac{1}{2\pi \cdot K \cdot Rgain \cdot (Cgain + CGext)} \quad [Hz]$$

where:

K : is gain of programmable gain amplifier

Rgain : equals 460 kOhm at 27 C. Variation over temperature may add –25 % at –55 °C and + 40 % at +125 °C, with respect to the cut-off frequency at 27 °C.

Cgain : equals 20 pF. The product Rgain*Cgain may vary +/- 50 % with respect to the nominal (designed) value.

CGext : value in pF of an optional external capacitor connected between pins CG and OUT

The nominal value for Bandwidth is 17.3 kHz for K = 1 and CGext = 0.

The electrical specifications of the analog signal path are given in Table 1 below.

Table 1 Electrical characteristics of the analog signal path

VDD-VSS = 3.0 V. –40 to 85 °C. CS1 = CS2 = 20 pF unless specified otherwise.

Symbol	Description	min	typ	max	Unit	comment
Sensor requirements						
Ctot	Total value sensor capacitances			220	pF	Note 5
Creldif	Relative difference of sensor capacitances	-50		50	%	Note 6
Rpar	Resistance parallel to sensor capacitor	7.2			MΩ	Note 10
Output voltage VOUT						
Vfs	VOUT dynamic range	VSS + 0.5		VDD – 0.5	V	
TCvout	Temperature variation of VOUT	-40		40	µV/°C	Note 1
Svout	White noise spectral density of VOUT		-100	-95	dBV/√Hz	
Voffres	Output referred residual offset	-1.1		1.1	mV	Note 1, 4
Gain						
K	Gain	1.0		8.0	-	Note 2, 9
Kstep	Gain trim step		0.007			Note 2, 9
Ktol	Nominal gain spread	- 10 %		+ 10 %		Note 3
TCgain	Temperature variation of gain	-150		150	ppm/°C	
External elements						
Rout	External resistive load on VOUT	10			kΩ	
Cout	External capacitive load on VOUT	0		10	nF	Note 7
CGext	External filter capacitor			1000	nF	Note 8

Note 1: Measured as VOUT – VGND. From 85 to 125 °C, the drift of VOUT increases to maximum +/- 200 ppm/°C.

Note 2: Gain is defined as the ratio between the output signal VOUT and the input signal VM of the gain amplifier.

Note 3 Spread of nominal value, before calibration.

Note 4: After offset trimming of output stage. Voffres is determined from VOUT – AGND.

Note 5: External sensor. CS1 + CS2. CS1 and CS2 include potential wiring and other paracitic capacitances.

Note 6: External sensor. The relative difference is defined as (CS1 – CS2) / (CS1 + CS2).

Note 7: the maximum capacitive load on VOUT is defined as the load at which the second harmonic distortion reaches –40 dB of the fundamental signal of 50 mV pp at the –3 dB cut-off frequency.

Note 8: CGext is in parallel to an on-chip filter capacitor CG of 20 pF typ.

Note 9: The gain of the output stage is programmable with 1023 equal steps of 0.007 between 1 and 8.

Note 10: For 1 % precision on VOUT. Rpar is typically a paracitic resistor related to sensor construction. Rpar is often not specified by other manufacturers, and typically more than 50 MΩ is required to assure 1 % precision. For XE2004, however, due to a special circuit technique, the minimim value for Rpar is relatively low. For 0.1 % precision, Rpar must be 51.2 MΩ at least.
The programmable gain amplifier drives loads of up to 10 kOhm or 10 nF.

Reference buffer amplifier

XE2004 converts the difference of capacitances CS1 and CS2 into a single-ended voltage VOUT. Positive and negative output signals are obtained by referencing the output signal VOUT to GND. GND equals half the supply voltage. The characteristics of the reference buffer amplifier are listed in Table 2.

VDD-VSS = 3.0 V.

Symbol	description	min	typ	max	Unit	comment
Vgnd	Buffered reference voltage		(VDD – VSS)/2			Note 1
Rgnd	External resitive load	10			kΩ	
Cgnd	External capacitive load	0		100	μF	

Note 1: Since VOUT – VGND can be trimmed for minimum offset, only the typical value for Vgnd is specified. For min and max specifications, refer to the specification of Voffres in Table 1.

Table 2 Reference buffer amplifier characteristics

Sensor Overload Detection

XE2004 has a sensor overload detection function. Sensor overload needs to be detected in order to avoid a situation in which the output voltage OUT saturates and gets stuck to VDD or VSS. This might lead to unwanted condition in closed loop control systems including XE2004. If an overload condition occurs, the output signal OUT will be clipped to the predefined threshold level, instead of VDD or VSS. OVTH register is used to program the upper and lower threshold levels, which are symmetrical around AGND. Upon removing the overload situation, the OUT will return to its normal reading.

The overload condition is met if one or more of the following cases is true:
- (CS1-CS2)/(CS1+CS2) > +/- 50%
- input signal of gain stage goes outside the lower limit of 40 % of VDD-VSS (2 V under 5 V supply)
- input signal of gain stage goes outside the upper limit of 60 % of VDD-VSS (3 V under 5 V supply)

The upper and lower threshold limits are programmable to 4 different values. See the description of OLTH register for more details.

Serial interface

XE2004 has a 2-wire serial interface to read from and writing to its internal registers. This interface is used, for instance, to configure XE2004 during factory calibration of the sensor. The serial interface may also be used upon power-up of XE2004 in combination with an external non-volatile memory (refer to application note AN2004.1).

A bi-directional bus oriented protocol is implemented. The XE2004 is always the slave.

The SCK pin is used to clock data. SDA is a bidirectional pin used to transfer data in and out of the registers.

Read and write commands are preceeded by a start condition which is a high-to-low transition of SDA when SCK is high, see Figure 3. Because of the push/pull output, a start cannot be generated while XE2004 is outputting data.

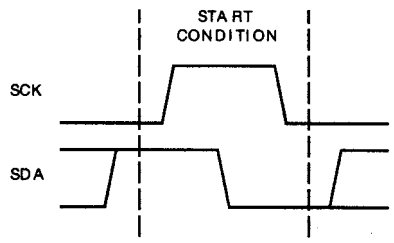


Figure 3 Definition of start condition.

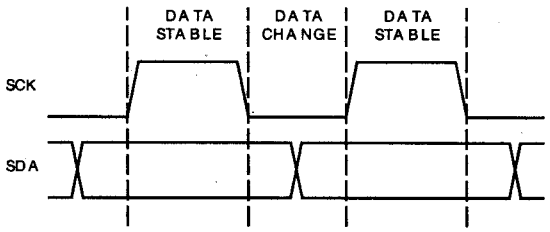


Figure 4 Definition of data validity.

The write operation is initiated with a start condition, see Figure 5. The start condition is followed by an eight-bit control byte which consists of six address bits and a two-bits command 01. After receipt of the control byte, XE2004 will enter the write mode and wait for the data to be written into its registers. The data is shifted into the device on the next eight SCK clock cycles.

The read operation is initiated with a start condition, see also Figure 5. The start condition is followed by an eight-bit control byte which consists of six address bits and a two-bits command 10. After receipt of the control byte, XE2004 will enter the read mode and prepare the data to be read. The data is shifted out of the device on the next eight SCK clock cycles. While clocking data out, a new start condition cannot be generated.

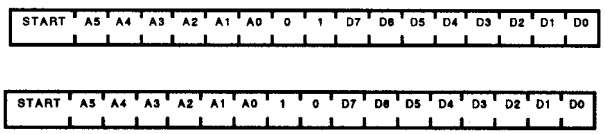


Figure 5 Write sequence (top) and read sequence (bottom).

The master must free the bus prior to the end of SCK pulse number 8 to allow XE2004 to send data, see figure below.

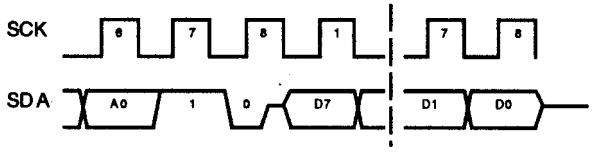


Figure 6 Read cycle timing.

Use of external non-volatile memory

An external non-volatile memory may be used to store 12 bytes of sensor-related data and other settings that were obtained during sensor manufacturing. Upon power-up (POR high-to-low transition), XE2004 is ready to receive data via SCK and SDA lines.

An application based on Microchip PIC12LC50x has been developed. Program code is available from XEMICS. For a detailed description, refer to Application Note AN2004.1 and DK2004 Development Kit User Guide.

Registers

XE2004 contains 23 8-bit registers that relate to various programmable elements and user settings. 14 registers are documented, 9 registers are reserved. From the 14 documented registers, 12 registers are related to sensor calibration and user settings, the 2 remaining ones are related to application debugging.

A summary of registers is given in Table 3. A detailed description of all registers is given further below.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00 0000	Reserved	-							
00 0001	SET	-	-	-	-	-	-	EXTREF	EXTCK
00 0010	CF	-	-	-	CF4	CF3	CF2	CF1	CF0
00 0011	CDEN	-	-	-	-	-	CDEN2	CDEN1	CDEN0
00 0100	CNOML	CNOML7	CNOML6	CNOML5	CNOML4	CNOML3	CNOML2	CNOML1	CNOML0
00 0101	CNOMH	-	-	-	-	-	-	-	CNOMH0
00 0110	COFF	-	-	-	-	COFF3	COFF2	COFF1	COFF0
00 0111	COFFP	-	-	-	-	-	-	-	POL
00 1000	Reserved	-							
00 1001	ROFF	ROFF7	ROFF6	ROFF5	ROFF4	ROFF3	ROFF2	ROFF1	ROFF0
00 1010	GAINL	GAINL7	GAINL6	GAINL5	GAINL4	GAINL3	GAINL2	GAINL1	GAINL0
00 1011	GAINH	-	-	-	-	-	-	GAINH1	GAINH0
00 1100	Reserved	-							
00 1101	Reserved	-							
00 1110	FOSC	-	-	-	-	FOSC3	FOSC2	FOSC1	FOSC0
00 1111	OVTH	-	-	-	-	-	-	OVTH1	OVTH0
01 0000	MON	-	-	-	MOSC	-	-	-	-
01 0001	Reserved	-							
01 0010	Reserved	-							
01 0011	Reserved	-							
01 0100	Reserved	-							
01 0101	PWR	-	-	-	-	-	-	-	PORF
01 1111	Reserved	-							

Table 3 Summary of registers

Configuration Register - SET

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	EXTREF	EXTCK
Default value	1	1	1	0	1	0	0	0

- **Bit 7..2 – Res: Reserved bits**

These bits are reserved and should always contain the default setting.

- **Bit 1 – EXTREF: External voltage reference**

The bit is to be set (one) in case an external voltage reference is connected to pin REF. The bit is to be reset (zero) in case the internal reference voltage source is used.

- **Bit 0 – EXTCK: External CLock**

The bit is to be set (one) in case an external cLock is connected to pin SCK. The internal cLock is then disabled. The bit is to be reset (zero) if the internal cLock is used.

Integration Capacitor (CF) Register - CF

Bit	7	6	5	4	3	2	1	0
	-	-	-	CF4	CF3	CF2	CF1	CF0
Default value	x	x	x	1	1	1	1	1

- **Bit 7..5 –DC: Don't care bits**

These bits are not reserved.

- **Bit 4..0 – CF: Integration Capacitor Value**

The value of the capacitor CF is programmable between 0 pF (all bits reset) and 31 pF (all bits set) in steps of 1 pF. Bit CF0 is LSB, bit CF4 is MSB.

Compensation Capacitor (CDEN) Register - CDEN

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	CDEN2	CDEN1	CDEN0
Default value	x	x	x	x	x	0	0	1

- **Bit 7..3 – DC: Don't care bits**

These bits are not reserved.

- **Bit 2..0 – CDEN: Stability Capacitor Value**

The value of the capacitor CDEN is programmable between 0 pF (all bits reset) and 42 pF (all bits set) in steps of 6 pF. Bit CDEN0 is LSB, bit CDEN2 is MSB.
Note: code CDEN = 0000 0000 is a forbidden value.

Compensation Capacitor (CNOM) Lower Register - CNOML

Bit	7	6	5	4	3	2	1	0
	CNOML7	CNOML6	CNOML5	CNOML4	CNOML3	CNOML2	CNOML1	CNOML0
Default value	0	0	0	0	0	0	0	0

- **Bit 7..0 – CNOML: Linearity Capacitor Value, Lower Register**

The value of the capacitor CNOM is determined by 9 bits contained in two registers, CNOML and CNOMH. CNOM is programmable between 0 pF (all bits reset) and 51.1 pF (all bits set) in steps of 0.1 pF. Bit CNOML0 is LSB, bit CNOMH0 is MSB.

Compensation Capacitor (CNOM) Higher Register - CNOMH

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CNOMH0
Default value	x	x	x	x	x	x	x	0

- **Bit 7..1 – DC: Don't care bits**

These bits are not reserved.

- **Bit 0 – CNOMH: Linearity Capacitor Value, Higher Register**

The value of the capacitor CNOM is determined by 9 bits contained in two registers, CNOML and CNOMH. CNOM is programmable between 0 pF (all bits reset) and 51.1 pF (all bits set) in steps of 0.1 pF. Bit CNOML0 is LSB, bit CNOMH0 is MSB.

Offset Capacitor Register - COFF

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	COFF3	COFF2	COFF1	COFF0
Default value	0	0	0	0	0	0	0	0

- **Bit 7..4 – Res: Reserved bits**

These bits are reserved and should always contain the default setting.

- **Bit 3..0 – COFF: Offset Capacitor Value**

The value of the capacitor COFF is determined by 8 bits. COFF is programmable between 0 pF (all bits reset) and 1.5 pF (all bits set) in steps of 0.1 pF. Bit COFF0 is LSB, bit COFF3 is MSB.

Polarity of Offset Capacitor Register - COFFP

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	POL
Default value	x	x	x	x	x	x	x	0

- **Bit 7..1 – DC: Don't care bits**

These bits are not reserved.

- **Bit 0 – POL: Polarity of Offset Capacitor**

If the polarity POL is reset (zero), COFF is connected in parallel with sensor capacitor CS1. If the polarity POL is set (one), COFF is connected in parallel with sensor capacitor CS2.

Offset Resistor Register - ROFF

Bit	7	6	5	4	3	2	1	0
	ROFF7	ROFF6	ROFF5	ROFF4	ROFF3	ROFF2	ROFF1	ROFF0
Default value	1	0	0	0	0	0	0	0

- **Bit 7..0 – Offset Resistor ROFF**

The value of the resistor ROFF is determined by 8 bits. ROFF is programmable between 0 Ohm (all bits reset) and 1.89 MOhm (all bits set) in steps of 7.4 kOhm. Bit ROFF0 is LSB, bit ROFF7 is MSB.

Gain, Lower Register - GAINL

Bit	7	6	5	4	3	2	1	0
	GAINL7	GAINL6	GAINL5	GAINL4	GAINL3	GAINL2	GAINL1	GAINL0
Default value	1	1	1	1	1	1	1	1

- **Bit 7..0 – GAINL: Gain Setting, Lower Register**

The value of the gain of the programmable gain amplifier, GAIN, is determined by 10 bits contained in two registers, GAINL and GAINH. GAIN is programmable between 1 (all bits reset) and 8 (all bits set) in steps of 6.84e-3. Bit GAINL0 is LSB, bit GAINH1 is MSB.

Gain, Higher Register - GAINH

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	GAINH1	GAINH0
Default value	x	x	x	x	x	x	1	1

- **Bit 7..2 – DC: Don't care bits**

These bits are not reserved.

- **Bit 1..0– GAINH: Gain Setting, Higher Register**

The value of the gain of the programmable gain amplifier, GAIN, is determined by 10 bits contained in two registers, GAINL and GAINH. GAIN is programmable between 1 (all bits reset) and 8 (all bits set) in steps of 6.84e-3. Bit GAINL0 is LSB, bit GAINH1 is MSB.

Oscillator Frequency Register - FOSC

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	FOSC3	FOSC2	FOSC1	FOSC0
Default value	x	x	x	x	1	0	1	0

- **Bit 7..4 – DC: Don't care bits**

These bits are not reserved.

- **Bit 3..0– FOSC: Oscillator Frequency Setting**

The value of the internal oscillator can be trimmed around its nominal value over 4 bits. The default nominal oscillator frequency is 320 kHz, programmable between 222 kHz (all bits reset) and 590 kHz (all bits set) in a non-linear fashion. Bit FOSC0 is LSB, bit FOSC3 is MSB.

Overload Threshold Register - OVTH

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	OVTH1	OVTH0
Default value	x	x	x	x	x	x	0	0

- **Bit 7..2 – DC: Don't care bits**

These bits are not reserved.

- **Bit 1..0– OVTH: Overload Threshold Setting**

The value of the overload threshold can be programmed to four values, according to the following Table. Code 11 disables the overload protection. If overload should happen for code 11, XE2004 will enter into a lock situation and the output signal OUT will stuck to VDD or VSS. This situation can only be resolved through resetting XE2004.

OVTH1	OVTH0	Lower threshold limit (% of VDD-VSS)	Upper threshold limit (% of VDD-VSS)
0	0	40 %	60 %
0	1	33 %	67 %
1	0	25 %	75 %
1	1	0 %	100 %

Monitor Register - MON

Bit	7	6	5	4	3	2	1	0
	-	-	-	MOSC	-	-	-	-
Default value	x	x	0	0	0	0	0	0

- **Bit 7..6 – DC: Don't care bits**

These bits are not reserved.

- **Bit 5 – Res: Reserved bits**

These bits are reserved and should always contain the default setting.

- **Bit 4– MOSC: Monitor Internal Oscillator Frequency**

The value of the internal RC oscillator can be monitored on pin ST when bit MEAS.4 is set (one). The frequency can programmed through register FOSC.

- **Bit 3..0 – Res: Reserved bits**

These bits are reserved and should always contain the default setting.

Power-on Register - PWR

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	PORF
Default value	x	x	1	1	1	1	1	0

- **Bit 7..6 – DC: Don't care bits**

These bits are not reserved.

- **Bit 5..1 – Res: Reserved bits**

These bits are reserved and should always contain the default setting.

- **Bit 0– PORF: Power-on Force**

This bit contains the status of the power-on-reset signal on pin POR. When PORF is set (one), POR pin is logical high, when PORF is reset (zero), POR pin is logical low.

XE2004

Programmable Low-Power Capacitive Sensor Conditioning IC

Application Notes and Development Tools

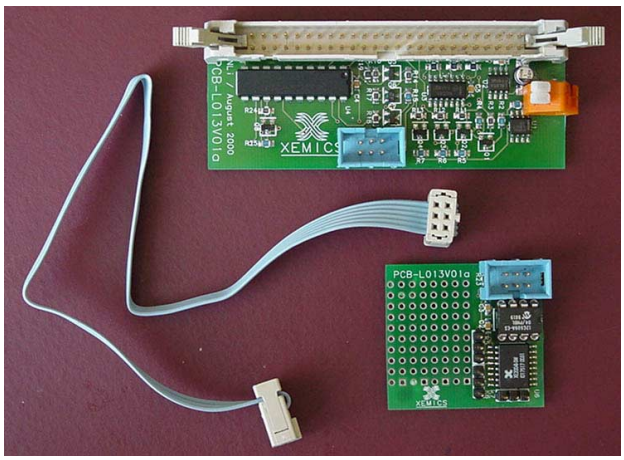
The following application notes and development tools are available from XEMICS:

AN2004.01	Using PIC12LC50x microcontroller with OTP memory to store register values of XE2004
AN2004.02	Getting to a calibrated sensor in 5 steps
DK2004	Development Kit for XE2004

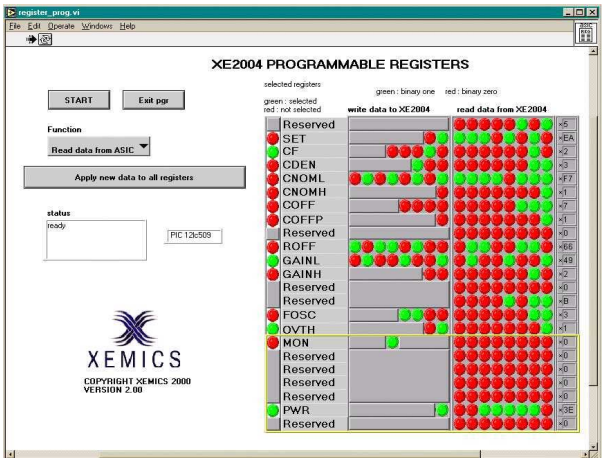
DK2004 is the XE2004 Development Kit. DK2004 is suited for evaluation of XE2004 in the application, as well as for use in manufatcuring environment. DK2004 contains:

- Evaluation board sockets for XE2004I-SW and a PIC12LC509A OTP microcontroller
- PC interface board
- 3 XE2004I-SW ICs
- 3 PIC12LC509A-04I/P ICs
- Labview™-based graphical user interface

DK2004 requires National Instruments' PCI-6503 card (DIO-24).



DK2004: evaluation board and PC interface board



DK2004: Graphical user interface

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