PRELIMINARY
QuikPAC Module Data

XM120-24A/F
120W, 1930-1990MHz
CDMA Power Module

General description:

The **XM120-24A/F QuikPAC™** 120W power module is a single-stage Class AB amplifier module for use in the output stages of CDMA RF power amplifiers. The power transistors are fabricated using Xemod's latest, high performance LDMOS process. This unit is available with either pre-set internal gate bias circuits including temperature compensation or external analog bias (user controlled).

Features:
- Multiple Bias Options
- High Gain
- High Efficiency
- Advanced, XeMOS II LDMOS FETS
- Stable Performance
- 50 Ω RF impedance
- QuikPAC System Compatible

Standard Operating Conditions

Parameter	Symbol	Min	Nom	Max	Units
Frequency Range	F	1930		1990	MHz
Supply (Drain) Voltage	V_D	26.0	28.0	32.0	VDC
Bias (Gate) Voltage – A Bias Option	V_G	3.0	3.5	5.0	VDC
Bias (Gate) Voltage – F Bias Option	V_G	11.0	12.0	13.0	VDC
Bias (Gate) Current, Average – A Bias Option	I_G			2.0	mA
Bias (Gate) Current, Average – F Bias Option	I_G			40.0	mA
Input and Output Impedance	Ω		50		Ohms
Load Impedance for Stable Operation (All Phases)	VSWR			10:1	
Baseplate Temperature	T_{OP}	-20		+90	ºC
Output Device Thermal Resistance, Channel to Baseplate	Θjc		0.37		ºC/W

Maximum Ratings

Parameter	Symbol	Value	Units
Supply (Drain) Voltage	V_{DD}	35	VDC
Input RF Power	P_{IN}	10	W
Load Impedance for continuous operation without damage	VSWR	5/1	
Output Device Channel Temperature		200	ºC
Lead Temperature during reflow soldering		+210	ºC
Storage Temperature	T_{STG}	-40 to +100	ºC

Performance at 25ºC

Parameter	Symbol	Min	Nom	Max	Units
Supply Voltage	$V_{D1,2}$	27.8	28.0	28.2	VDC
Power Output at 1 dB Compression (single tone)	P_{-1}		120		W
Gain at 24W CDMA Power Output	G	12.5	13.5		dB
Gain Flatness over frequency at 24W CDMA Output	ΔG		0.3	0.5	dB
Input Return Loss at 24W Output (CW) (50 Ω Ref)	iRL	11	13		dB
Quiescent Current (total)	I_{DQ}	1,080	1,200	1,320	mA
Drain Efficiency at 24W CDMA output (Single Carrier IS-95B)	η_D	19	20		%
ACPR at 24W CDMA Power Output (±885KHz; 30KHz BW)		45	47		dB
ALT-1 at 24W CDMA Power Output (±1.25MHz, Integrated)		50	54		dB
3rd order IMD – Two IS-95 Carriers at 2.5MHz Separation 24W Total CDMA Power Output			-35.5		dBc

Performance Over Temperature (F bias option only)

Parameter	Symbol	Min	Nom	Max	Units
Gain at 24W CDMA Power Output	G		12.5		dB
Gain Flatness over frequency at 24W CDMA Output	ΔG		0.3	0.7	dB
Input Return Loss at 24W Output (CW) (50 Ω Ref)	iRL		13.0		dB
Drain Efficiency at 24W CDMA output	η_D		19		%

Bias Options

This QuikPAC module is available with the following gate bias circuit options:

A Analog gate bias; provides a direct gate connection This option requires an externally supplied gate voltage (V_{GS}) on each gate lead (pins 1 and 5) to set the operating point (quiescent current- I_{DQ}) of the power transistors. V_{GS} may be safely set to any voltage in the range listed in the table. This permits a wide range of quiescent current to be used. Since the operating characteristics of the module will vary as I_{DQ} changes, the bias setting will depend on the application. The data provided in the Performance section of this data sheet was obtained with I_{DQ} set to a value within the range listed (a nominal value ±10%). This particular value was chosen to optimize gain, ACPR performance, and efficiency simultaneously.

F Pre-set bias, with temp comp; This option provides an internally regulated gate voltage that is preset at the factory. A voltage of +12VDC (±1V) should be applied to each gate lead (pins 1 and 5). No further adjustment is required. Although the module will operate with lower voltages applied, the internal regulator is not functioning and the specified performance may not be achieved.
The gate voltage is thermally compensated to maintain constant quiescent current over the temperature range listed in the data sheet. No compensation is provided for gain changes with temperature. This can only be provided with AGC external to the module
The quiescent current set during manufacture will be within the range specified in the Performance section (nominal ±10%) and is selected to balance ACPR, input return loss, and efficiency. This setting is suitable for most applications. Modules with different optimization profiles are available by special order.

Notes:

The "Preliminary" designation on this data sheet indicates this product has not yet entered production. The data supplied here is derived from engineering development and pilot production testing and may change.

Gate voltage must be applied coincident with or after application of the drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to a module unless it is terminated on both input and output.

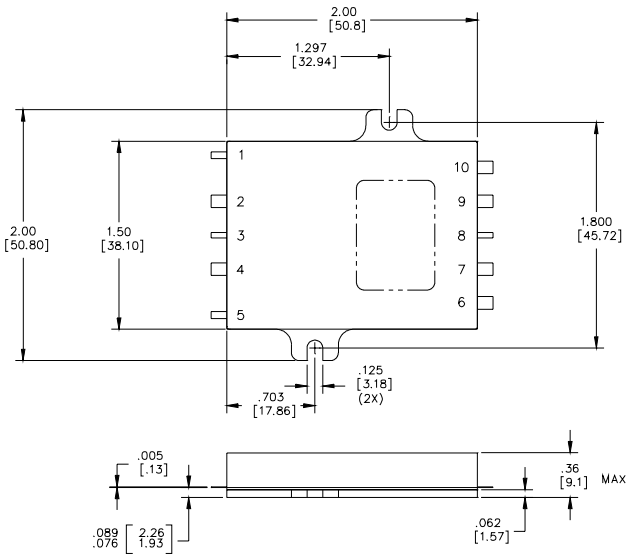
The V_{GS} corresponding to a specific I_{DQ} will vary from module to module and may vary between the two sides of a dual RF module by as much as ±0.10 volts. This is due to the normal die-to-die variation in threshold voltage of LDMOS transistors.

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

The RF leads are internally protected against DC voltages up to 100V. Care should be taken to avoid video transients that may damage the active devices.

Package Styles

B2F



LEAD IDENTIFICATION	
Lead No.	Function
1	Bias 1
2	Ground
3	Input
4	Ground
5	Bias 2
6	V_{DD2}
7	Ground
8	Output
9	Ground
10	V_{DD1}

DIMENSIONS ARE IN[MM].

This model is available in the B2F (H10894) package style. Please see the applicable outline drawing for detailed dimensions.

Ordering Information

With bias option A – order model XM120-24A-B2F
With bias option F – order model XM120-24F-B2F