XRT75L00D

E3/DS3/STS-1 LINE INTERFACE UNIT WITH SONET DESYNCHRONIZER

MARCH 2002 REV. P1.0.0

GENERAL DESCRIPTION

The XRT75L00D is a single-channel fully integrated Line Interface Unit (LIU) with Jitter Attenuator for E3/DS3/STS-1 applications. It incorporates an independent Receiver, Transmitter and Jitter Attenuator in a single 52 pin TQFP package.

The XRT75L00D can be configured to operate in either E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz) modes. The transmitter can be turned off or tri-stated for redundancy support and for conserving power.

The XRT75L00's differential receiver provides high noise interference margin and is able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75L00D incorporates an advanced crystal-less jitter attenuator that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications. Also the jitter attenuator can be used for clock smoothing in SONET STS-1 to DS3 de-mapping.

The XRT75L00D provides both Serial Microprocessor Interface as well as Hardware mode for programming and control.

The XRT75L00D supports local, remote and digital loop-backs. The XRT75L00D also contains an on-board Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error.

FEATURES

Receiver:

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip Clock Synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock.
- Provides low jitter output clock
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications

Transmitter:

- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications

Transmitter can be turned on or off.

Jitter Attenuator:

- On chip advanced crystal-less Jitter Attenuator.
- Jitter Attenuator can be selected in Receive or Transmit paths
- Jitter Attenuator can be disabled
- 16, 32 or 128 bits selectable FIFO size
- De-Synchronizer for SONET STS-1 to DS3 de-mapping
- Meets the Jitter requirements specified in the ETSI TBR-24, Bellcore GR-499-CORE 1995 and GR-253-CORE standards
- Meets the Jitter and Wander specifications described in the ANSI T1.105.03b
- Compliant with Jitter Transfer Template outlined in ITU G.751, G.752, G.755

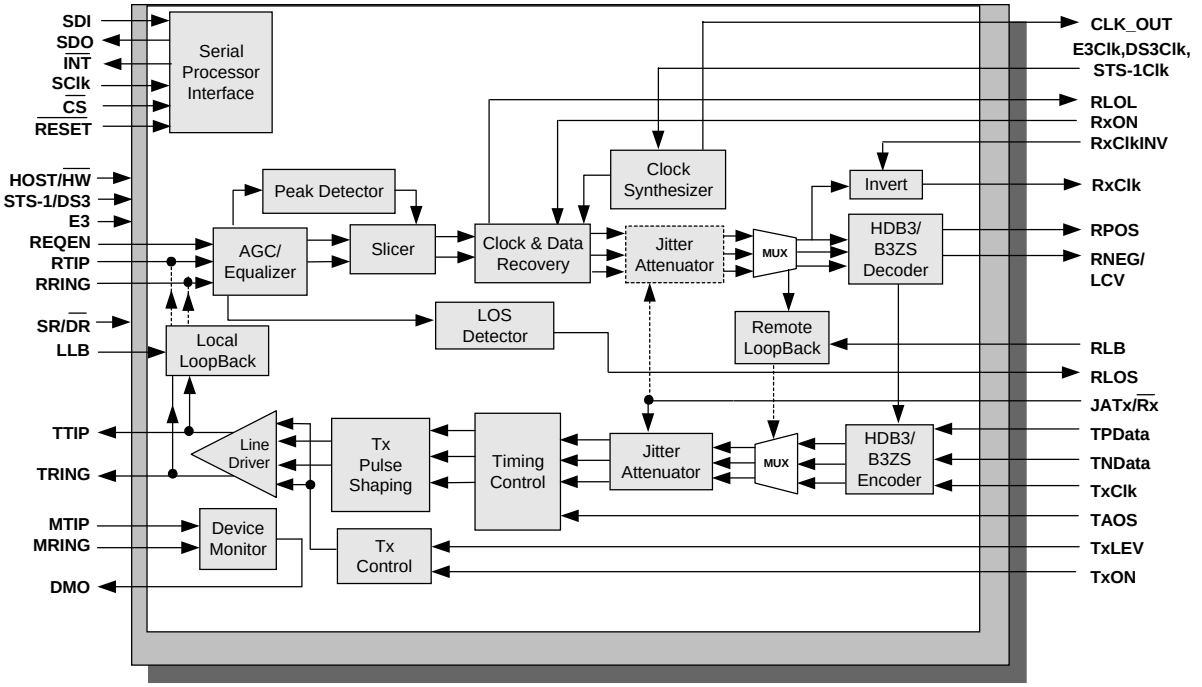
Control and Diagmostic:

- 5 wire Serial Microprocessor Interface for control and configuration
- Supports optional internal Transmit Driver Monitoring
- PRBS Error Counter Register to accumulate errors
- Hardware Mode for control and configuration
- Supports Local, Remote and Digital Loop-backs
- Single 3.3 V ± 5% power supply
- 5 V Tolerant I/O
- Available in 52 pin TQFP
- -40°C to 85°C Industrial Temperature Range

APPLICATIONS

- E3/DS3 Access Equipment
- STS1-SPE to DS3 Mapper
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

FIGURE 1. BLOCK DIAGRAM OF THE XRT75L00D



Note: Serial Processor Interface input pins are shared by in "Host" Mode and redefined in the "Hardware" Mode.

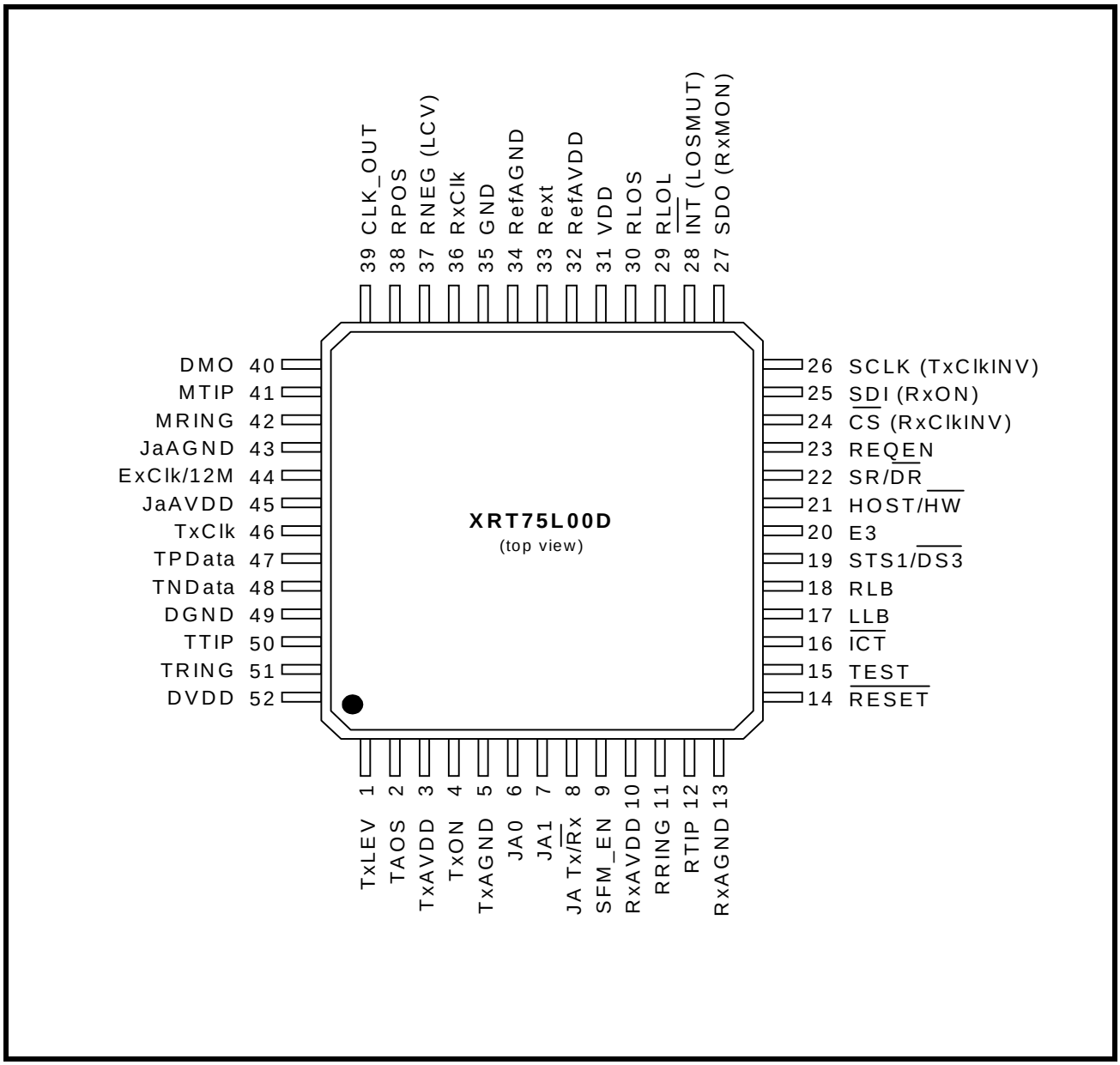
Transmit Interface Characteristics

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

Receive Interface Characteristics

- Integrated Adaptive Receive Equalization for optimal Clock and Data Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment

FIGURE 2. PIN OUT OF THE XRT75L00



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L00DIV	52 Pin TQFP	-40°C to +85°C

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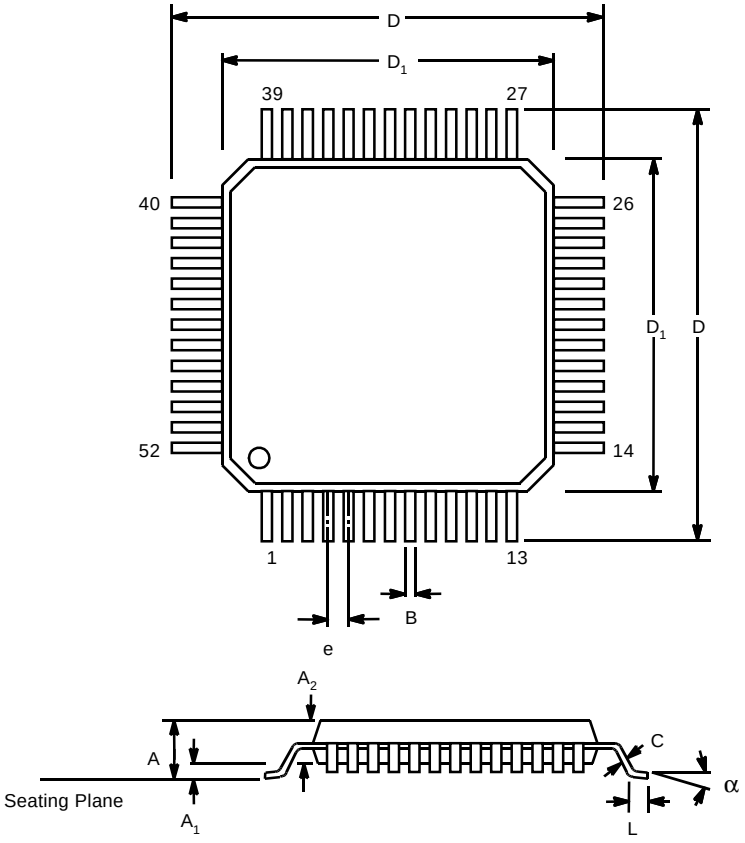
PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L00DIV	52 Pin TQFP (10mm x 10mm)	-40°C to +85°C

PACKAGE DIMENSIONS



Note: The control dimension is the millimeter column

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.009	0.015	0.22	0.38
C	0.004	0.008	0.09	0.20
D	0.465	0.480	11.80	12.20
D1	0.390	0.398	9.90	10.10
e	0.0256 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°
β	7° typ		7° typ	
aaa	-	0.003	-	0.08

REVISIONS:

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