SINGLE-CHANNEL T1/E1/J1 LH/SH TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

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GENERAL DESCRIPTION

The XRT83L30 is a fully integrated single-channel long-haul and short-haul line interface unit for T1(1.544Mbps) 100Ω, E1(2.048Mbps) 75Ω or 120Ω and J1 110Ω applications.

In long-haul applications the XRT83L30 accepts signals that have passed through cables from 0 feet to over 6000 feet in length and have been attenuated by 0 to 45dB at 772kHz in T1 mode or 0 to 43dB at 1024kHz in E1 mode. In T1 applications, the device generates five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements as well as for Channel Service Units (CSU) Line Build Out (LBO) filters of 0dB, -7.5dB, -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit pulse generator that can be used for arbitrary output pulse shaping allowing performance improvement over a wide variety of conditions.

The XRT83L30 provides both Serial Host microprocessor interface and Hardware mode for programming and control. Both B8ZS and HDB3 encoding and decoding functions are included and can be disabled as required. On-chip crystal-less jitter attenuator (with a 32 or 64 bit FIFO) can be placed either in the receive or the transmit path with loop bandwidths of less than 3Hz. The XRT83L30 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω for both transmitter and receiver. For the receiver this is accomplished by internal resistors or through the combination of one single fixed value external resistor and programmable internal resistors. In the absence of the power supply, the transmit output and receive input are tri-stated allowing for redundancy applications. The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master clocks from a variety of external clock sources.

APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

FEATURES

(See Page 2)

FIGURE 1. BLOCK DIAGRAM OF THE XRT83L30 T1/E1/J1 LIU (HOST MODE)

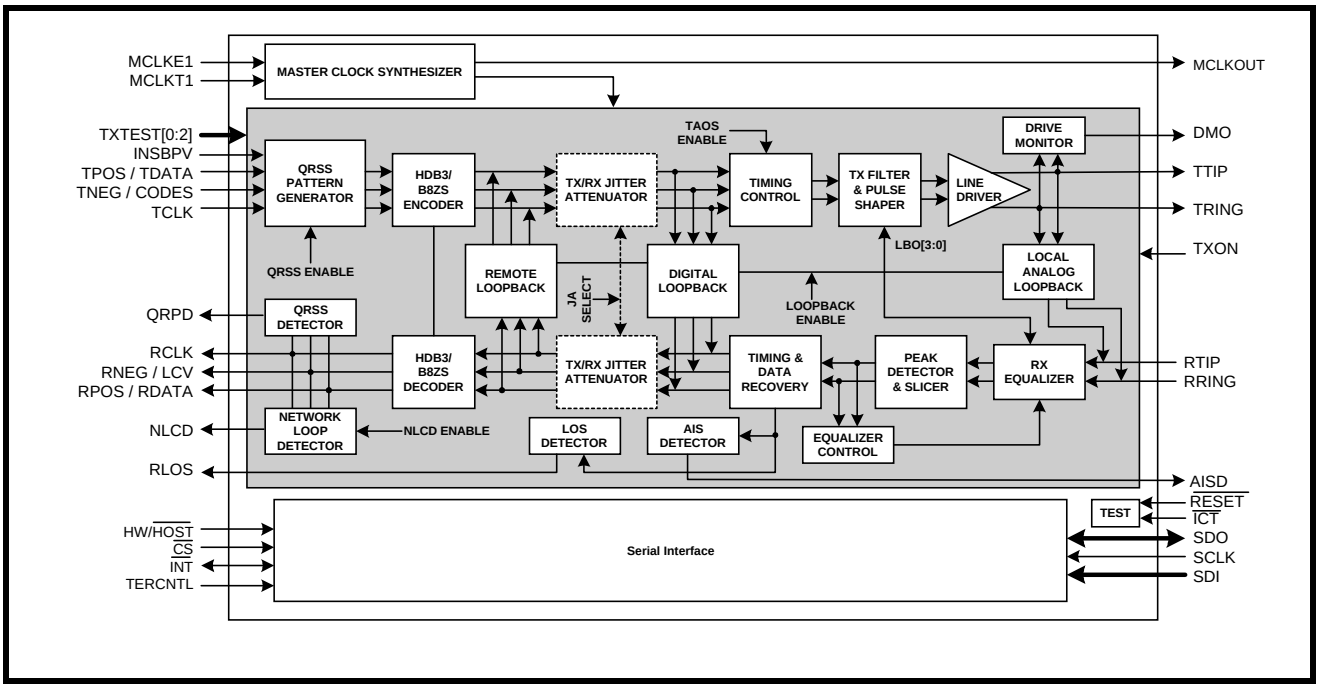
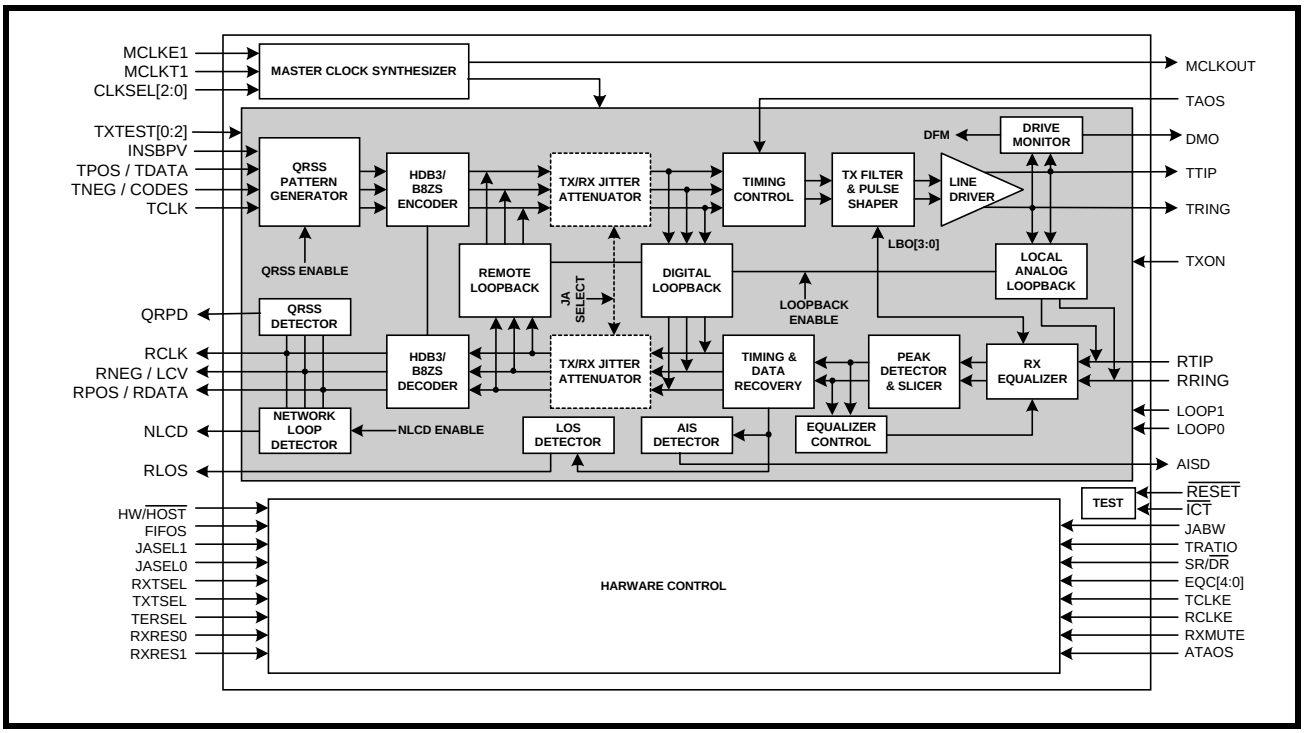


FIGURE 2. BLOCK DIAGRAM OF THE XRT83L30 T1/E1/J1 LIU (HARDWARE MODE)



FEATURES

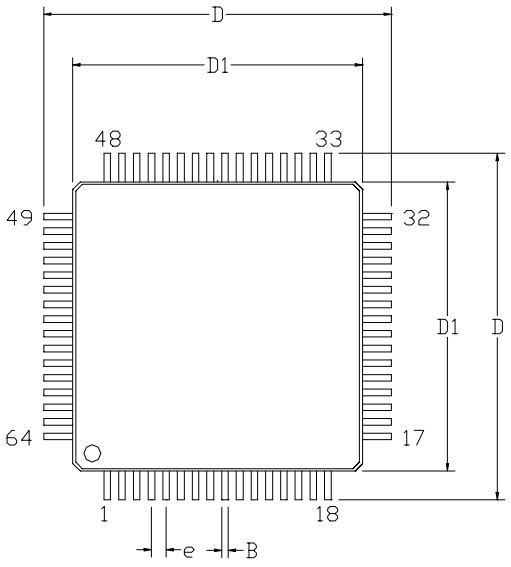
- Fully integrated single-channel long-haul or short-haul transceivers for E1,T1 or J1 applications.
- Adaptive Receive Equalizer for cable attenuation of up to 45dB for T1 and 43dB for E1.
- Programmable Transmit Pulse Shaper for E1,T1 or J1 long-haul and short-haul interfaces.
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping.
- Programmable Transmit Line Build-Outs (LBO) for T1 long-haul application from 0dB to -22.5dB in three 7.5dB steps.
- Tri-State transmit output and receive input capability for redundancy applications
- Selectable receiver sensitivity from 0 to 36dB or 0 to 45dB cable loss for T1 @772kHz and 0 to 43dB for E1 @1024kHz.
- High receiver interference immunity
- Receive monitor mode handles 0 to 29dB resistive attenuation along with 0 to 6dB of cable attenuation for both T1 and E1 modes.
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications.
- Internal and external impedance matching for 75Ω,100Ω, 110Ω and 120Ω.
- Transmit return loss meets or exceeds ETSI 300 166 standard
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO Selectable either in transmit or receive path
- On-chip frequency multiplier generates T1 or E1 Master clocks from variety of external clock sources
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)
- Receive loss of signal (RLOS) output
- On-chip HDB3/B8ZS/AMI encoder/decoder
- QRSS pattern generation and detection for testing and monitoring
- Error and Bipolar Violation Insertion and Detection
- Receiver Line Attenuation Indication Output in 1dB steps
- Network Loop-Code Detection for automatic Loop-Back Activation/Deactivation
- Transmit All Ones (TAOS) and In-Band Network Loop Up and Down code generators
- Supports Analog, Remote, Digital and Dual Loop-Back Modes
- Meets or exceeds T1 and E1 short-haul and long-haul network access specifications in ITU G.703,

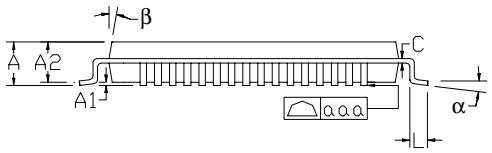
ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83L30	64 Pin TQFP	-40°C to +85°C
THERMAL INFORMATION	Theta - J_A = 38° C/W	Theta J_C = 7° C/W

PACKAGE DIMENSIONS

64 Lead Thin Quad Flat Pack
(10 x 10 x 1.4 mm LQFP)





	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.465	0.480	11.80	12.20
D1	0.390	0.398	9.90	10.10
e	0.0020 BSC		0.05 BSC	
L	0.018	0.050	0.45	0.75
α	0°	7°	0°	7°
β	7° typ		7° typ	
aaa	-	0.003	-	0.08

Note: Control Dimensions are the Millimeter Column

REVISION HISTORY

Rev. A1.0.0 Advanced version.

Rev. P1.1.0 Preliminary release.

NOTICE